A Digitally Controlled PLL for SoC Applications

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***Abstract*—A fully integrated digitally controlled phase-locked loop (PLL) used as a clock multiplying circuit is designed and fabricated. The PLL has no off-chip components and it is made from standard cells found in most digital standard cell libraries. The design is, therefore, portable between technologies as an IP block. Using a 0.35-μm standard CMOS process and a 3.0-V supply voltage, the PLL has a frequency range of 152 to 366 MHz and occupies an on-chip area of 0.07 mm^2. In addition, the next version of this all-digital PLL is described in synthesizable VHDL code, which simplifies digital system simulation and change of process. A new time-to-digital converter with higher resolution is designed for the improved PLL. An improved digitally controlled oscillator is also suggested.**

***Index Terms*—Oscillator, phase-locked loop (PLL), time-to-digital, VHDL.**

I. Introduction

THE phase-locked loop (PLL) is a widely used circuit for clocking digital IP blocks. Traditionally, a PLL is made as an analog building block. However, integrating an analog PLL in a digital noisy system-on-chip (SoC) environment is difficult. In addition, the analog PLL is sensitive to process parameters and must, therefore, be redesigned for each new technology. Digitally controlled clock generators will not have the same performance but are much easier to implement without targeting a specific technology. Assuming that the digitally controlled PLL is made with only active components such as transistors, it will scale nicely with technology. Capacitors and resistors, which are used in analog circuits, will not scale with technology changes to the same extent. Also, using digital components gives benefits such as robustness against supply voltage impurities due to high control voltages compared to deviations, and also the ability to design higher order filters without much extra power consumption or area penalty.

Robust and easily implemented fully digital clock multipliers without phase locking are proposed in [1] and [2]. These clock multipliers produce a fixed number of cycles for each period of an external reference clock signal followed by an idle margin. For many digital applications, such simpler clock generators is a feasible solution. However, for various applications, a phase-locked clock generated by a PLL is necessary to ensure correct functionality. Examples of digitally controlled PLLs are described in [3]–[6].

A PLL designed with standardized digital CMOS components (standard cells), is easy to implement using any CMOS technology, and can, therefore, radically decrease time-to-market for a design. Moreover, if the entire PLL is described in a HDL language, system simulations including the PLL can be performed in a digital HDL simulator.

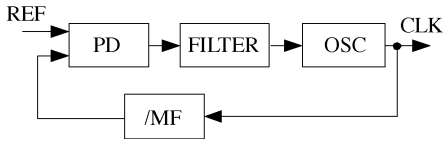

Fig. 1. General PLL block structure.

The critical component for a PLL made with standard cells is the oscillator, which has to be simulated as an analog component to get reliable estimates of its behavior. Simulating an oscillator is, however, much less troublesome than simulating a PLL due to lack of nonlinear feedback loops. The aim for this project is mainly to reduce the complexity in digital PLL design to the complexity of designing the oscillator.

The block structure of a general PLL, shown in Fig. 1, is divided into a phase detector, a loop filter, an oscillator, and a frequency divider. The design methodology used for this digitally controlled PLL is to transform the components used in the analog PLL into the digital domain. This results in a simple, area-effective low-power solution, which can be analyzed with z-domain theory.

For the all-digital PLL, the phase detector is a slightly modified standard type-IV detector [7] and the loop filter consists of a time-to-digital converter and an integrating digital recursive filter, which replaces the charge pump and the analog loop filter. The oscillator is a digitally controlled oscillator (DCO).

This paper consists of two major parts. First, the silicon prototype of the digitally controlled PLL is described together with measurement results. In this design, the fundamental methods for designing the PLL are tested. Mainly due to course phase error measurement, the first implementation is best suited for purely digital applications where a relatively high amount of jitter can be tolerated. The second part contains a z-domain stability analysis of the feedback loop and some fundamental improvements, such as describing the PLL in synthesizable VHDL code, improved phase error detection, and suggestions for alternative digitally controlled oscillators. To simplify comparison, the improved PLL is mapped to the same technology as the prototype PLL.

II. Design Overview

Fig. 2 shows the block structure of the all-digital PLL. The phase detector (PD) produces a pulse with length equal to the phase error. The phase error is then translated into a digital signal in a time-to-digital converter, which uses the buffered high-frequency output from the DCO "HF_CLK" as

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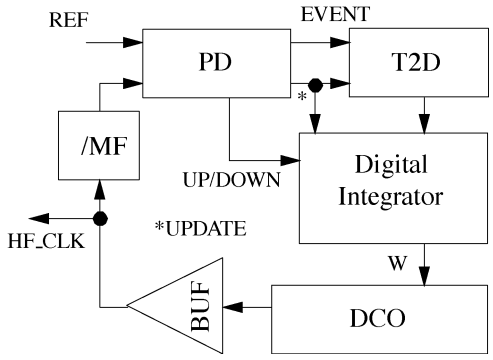

Fig. 2. Block structure of all-digital PLL.

the reference clock. The digitalized time measurement is fed into an integrating filter, which is controlling the DCO. After frequency division by the multiplication factor (MF), the output of the DCO is compared to the reference in the phase detector. The signal "UPDATE" from the phase detector is used to clock the registers and to reset the time-to-digital converter between measurements.

A. Digitally Controlled Oscillator

A difficulty when making an all standard-cell PLL is implementing an oscillator with high resolution. A variable number of inverters may be used for implementing a variable delay. In [4] and [8], this technique is used for coarse acquisition. Using only a variable number of inverters results in delay steps of several hundred picoseconds, which gives an inaccurate and unstable phase lock for high-frequency applications. Also, when using a variable number of inverters, great care must be taken not to induce glitches into the ring oscillator when switching delay.

The oscillator implemented for this digital PLL is a seven-stage ring oscillator with one inverter replaced by a NAND gate for shutting down the ring oscillator during idle mode. To change the frequency of the ring oscillator, a set of 21 tri-state inverters are connected parallel to each inverter (see Fig. 3). The idea for the oscillator was presented in [9]. A similar implementation is also found in [8].

When the tri-state inverters are enabled, additional current drive is added to each inverter stage. The 126 tri-state inverters are controlled by a 126-bit vector (C), which is decoded from a 7-bit control word (W). The 126-bit vector is all ones for $W = 0$, all zeros for $W = 126$ and 127, and for $W < 126$ and 127, the number of zeros in C is equal to W.

Measured period time versus digital control word for the DCO at 3.0-V supply voltage is shown in Fig. 4. The plot in Fig. 4 has a slope between 10 ps/bit and 150 ps/bit. It is important to keep the slope low since the slope sets the resolution of the DCO and, thereby, controls the jitter performance of the PLL. The jitter will, therefore, be higher at lower DCO frequencies. Since the resolution sets the jitter, it should be considerably higher than the required jitter performance.

A negative slope must also be avoided, since this might cause the PLL to be unstable. Since adding current drive by enabling a tri-state gate cannot slow down the oscillator, negative slope will not occur. The curve of Fig. 4 is, therefore, always monotonic.

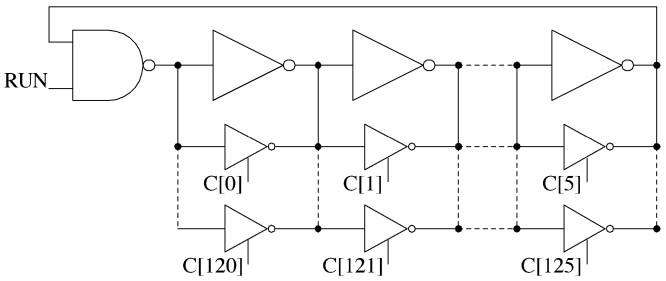

Fig. 3. DCO using parallel tri-state inverters to adjust frequency.

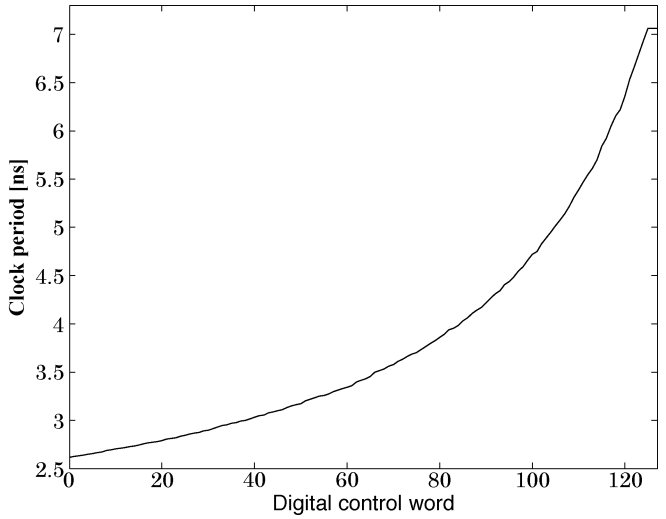

Fig. 4. Measured period time versus digital control word W for the DCO of Fig. 3.

If a larger frequency range is desired for the DCO, this can be accomplished using frequency division by powers of two or by using gate delays as in [8].

Although the DCO of Fig. 3 has the advantage of being made from all-standard cells, it has disadvantages such as relatively high power consumption and low maximum frequency from high capacitive load in the ring oscillator. Simulations indicate that over 50% of the power consumption for the PLL comes from the DCO. The nonlinear behavior also makes it harder to find a proper loop gain for the PLL. For applications demanding high resolution and less power consumption, a full-custom design of the DCO is preferable. For high-frequency operation, a digital-to-analog (D/A) converter followed by a voltage-controlled oscillator (VCO) is a good alternative.

B. Phase Detector

The type-IV phase detector has in its original configuration two outputs controlling the oscillator frequency for the duration of the phase error: one for signaling "UP" and one for signaling "DOWN." A slight modification is done to produce one signal "DIRECTION" and one signal "EVENT" showing the sign and length of the phase error. The modified phase detector is shown in Fig. 5.

Due to internal delay of the phase detector, the pulses at node UP and DOWN are longer than the actual phase error. There is, therefore, always a pulse at both nodes UP and DOWN. For the EVENT signal found in Fig. 2 and Fig. 5, the internal delay

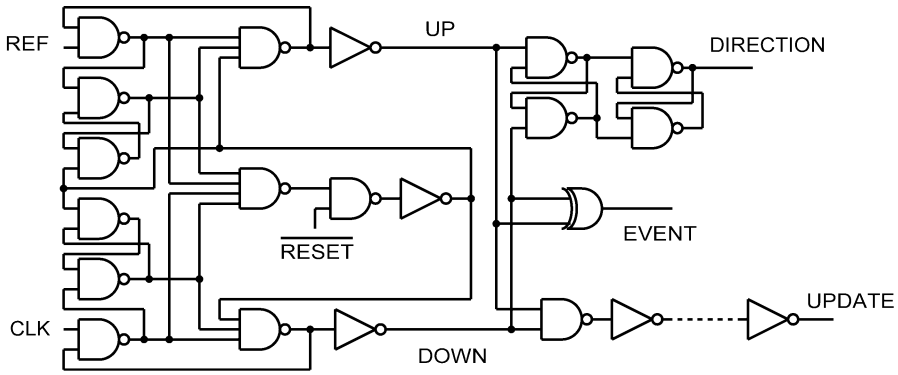

Fig. 5. Modified type-IV phase detector.

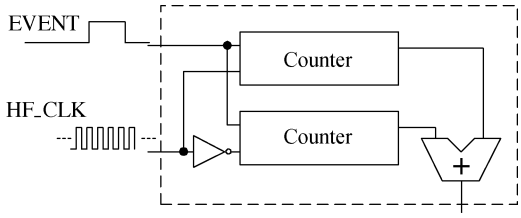

Fig. 6. Time-to-digital converter using both positive and negative edge of HF_CLK.

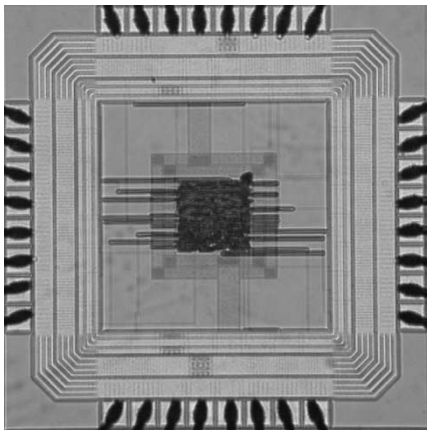

Fig. 7. Chip microphotograph of the prototype PLL (core area $= 0.07$ mm^2).

is cancelled out using an EXOR gate. Thereby, a more accurate measurement of the phase error is achieved.

The all-digital PLL works as a synchronous digital circuit, which, thus, needs a clock pulse for updating all registers. At the end of each phase error a short pulse is produced at the node UPDATE. This pulse, which is as long as the internal delay of the phase detector, is further delayed and used to clock registers in the integrating filter and to reset the time-to-digital converter between measurements.

C. Loop Filter

The loop filter consists of a time-to-digital converter and a digital recursive filter. The time-to-digital converter consists of a counter which measures the phase error using the DCO output as a reference. To double the precision, the counter uses both positive and negative edge from the DCO output (see Fig. 6).

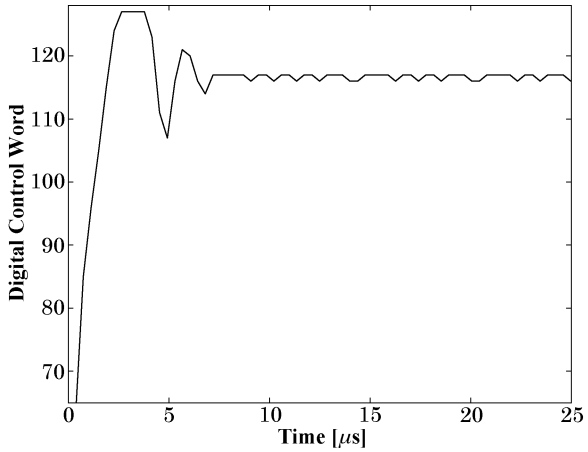

Fig. 8. Measured step response for the prototype PLL.

The result from the counter is used as input to the filter, a second-order integrator with the transfer function

$$F(z) = \frac{1}{1 - 0.5z^{-1} - 0.5z^{-2}}. \tag{1}$$

III. Fabrication and Test Results

The PLL is fabricated in a 0.35-μm triple-metal-layer CMOS process. Fig. 7 shows a chip photo of a prototype chip containing the digital PLL. The core area for the digital PLL is 0.07 mm^2 (260×260 μm).

A. Step Response

To study the capture and lock process of the PLL, the step response is tested. Fig. 8 shows step response for the control word W. The measurement is made using a reference period of 400 ns and a multiplication factor of 64. Phase lock is achieved after approximately 18 reference periods. Since the DCO frequency is changed stepwise, the control word will oscillate one bit during phase lock. This oscillation will cause a jitter equal to the resolution of the DCO on the output clock signal.

B. Power Consumption and Lock Range

Fig. 9 shows the power consumption in milliwatts per megahertz for the PLL. During this measurement, the power consumption is measured for phase lock at maximum and

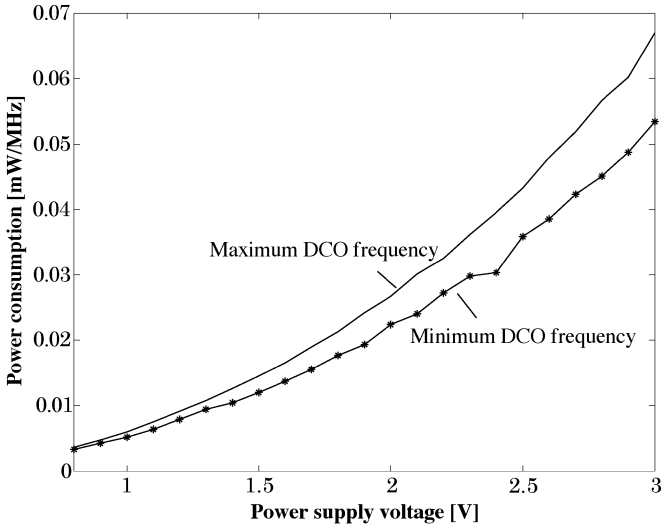

Fig. 9. Power consumption for the prototype PLL at maximum and minimum DCO frequency using supply voltages from 0.8 to 3.0 V.

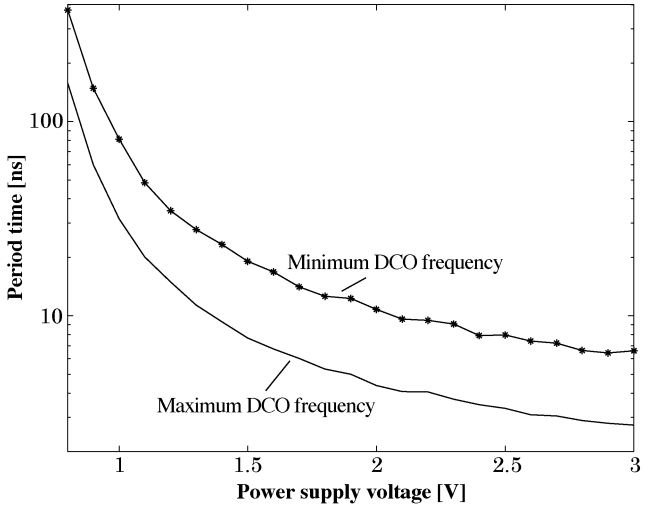

Fig. 10. Lock range for the prototype PLL using supply voltages from 0.8 to 3.0 V.

minimum possible DCO frequency, thereby the two curves of Fig. 9. Fig. 10 is extracted from the same measurement as shown in Fig. 9. It shows maximum and minimum DCO period time where phase lock is achieved. The lock range for the PLL is equal to the frequency range of the DCO. The measurements are made for a voltage range of 0.8–3.0 V. The all-digital PLL has, at 3.0-V supply voltage, a frequency range of 152–366 MHz while consuming 8.1–24 mW. At 2.0 V, the frequency range is 90–230 MHz while consuming 2.1–6.1 mW.

C. Jitter Measurements

The jitter measurement is performed on a Tektronix TDS7404 digital oscilloscope. Due to pad limitations and that the uncertainty of the jitter measurement is about 50 ps, jitter measurement is performed on the frequency divided output clock which is compared to the reference (Figs. 11 and 12). The measurements are made using a multiplication factor of 64 and an input reference clock of approximately 5 MHz. Supply voltage variations during the measurement is about 200 mVpp.

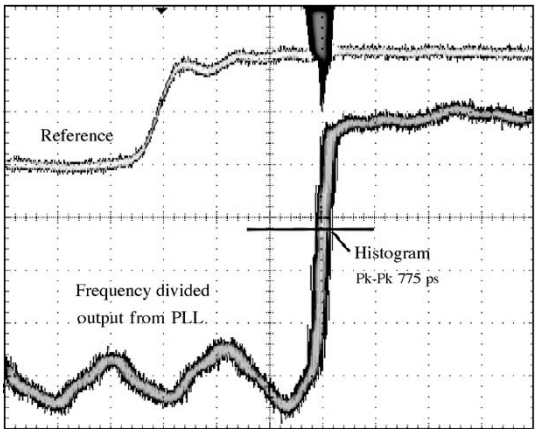

Fig. 11. Measured jitter of the prototype PLL when the control word jitters one LSB.

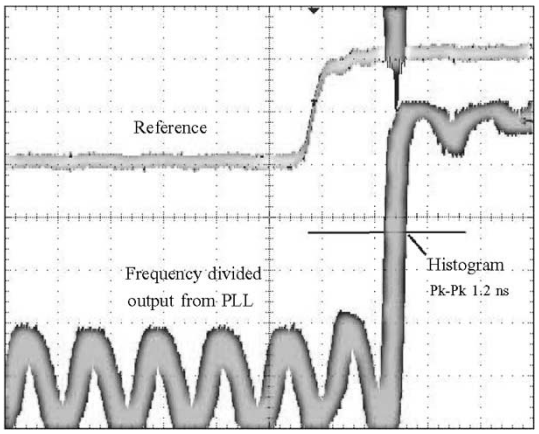

Fig. 12. Measured jitter of the prototype PLL when the control word jitters two LSB.

Assuming that jitter due to supply voltage and other interference is low, the jitter of the feedback clock is set by either the resolution of the time-to-digital converter ($T/2$) or the resolution of the generated feedback clock ($\mathrm{MF} \times \Delta T$). Here, T is the period time of the DCO output, ΔT is the resolution of the DCO, and MF is the frequency multiplication factor. At best possible phase lock, the control word to the DCO jitters one least significant bit (LSB), which gives an output jitter of ΔT from the DCO. In Fig. 11, a stable phase lock with a jitter of one LSB is found. In this measurement, ΔT is approximately 10 ps, $\mathrm{MF} = 64$, and the measured jitter is 775 ps ($\mathrm{MF} \times \Delta T = 640$ ps). Since the time-to-digital converter has a limited resolution of $T/2$, it is sometimes impossible to get a jitter of only one LSB in the control word to the DCO. In Fig. 12, the control word jitters two LSB and hence the jitter is approximately ($2 \times \mathrm{MF} \times \Delta T = 1280$ ps). The measured jitter in Fig. 12 is 1.2 ns. This might happen whenever $\mathrm{MF} \times \Delta T < (T/2)$.

Since the amount of jitter could be predicted from knowing the DCO resolution and the number of jittering LSBs in the feedback loop, it is concluded that this is the major source of jitter. The peak-to-peak jitter for the actual clock signal is, therefore, in the same order of magnitude as the DCO resolution, which is between 10 and 150 ps depending on output frequency. To enable minimum peak-to-peak jitter for the output clock at lower

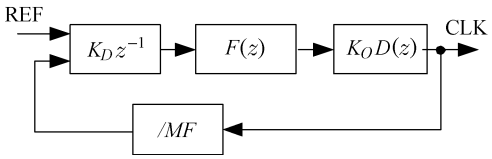

Fig. 13. Transfer function components of the digital PLL block structure.

multiplication factors, a better time-to-digital converter is necessary.

IV. Stability Analysis

In this section, a stability analysis is performed for the PLL. As an integrating filter, a few simple easy implemented first and second-order filters are evaluated. For the stability analysis, the z-domain transfer function is identified for each component (see Fig. 13).

A. Phase Detector

The phase detector gives the phase error of the previous reference period. The transfer function for the phase detector is given by (2), where K_D is the gain factor for the phase detector

$$K_D \times z^{-1}. \tag{2}$$

Since the phase error is measured with the resolution of half the period time of the DCO (T), K_D is given by

$$K_D = \frac{2}{T}. \tag{3}$$

B. DCO

For the analysis, the present phase of the frequency-divided output is labeled as $p(n)$. The present phase is the sum of the previous phase and added phase due to the control word $[w(n)]$ from the digital filter.

$$p(n) = p(n-1) + K_O \times w(n) \tag{4}$$

$$K_O = \Delta T, \tag{5}$$

where K_O is the gain factor for the DCO and ΔT is the resolution of the DCO.

The transfer function for the oscillator is, thus, given by

$$K_O \times D(z) = \frac{\Delta T}{1 - z^{-1}}. \tag{6}$$

C. Loop Equations

The open-loop transfer function $[O(z)]$ is given by

$$K = K_O \times K_D \times \mathrm{MF} = \frac{2 \times \mathrm{MF} \times \Delta T}{T} \tag{7}$$

$$O(z) = K z^{-1} F(z) D(z), \tag{8}$$

where $F(z)$ is the transfer function for the digital integrating filter.

This gives the closed-loop expression

$$C(z) = \frac{K z^{-1} F(z) D(z)}{1 + K z^{-1} F(z) D(z)}. \tag{9}$$

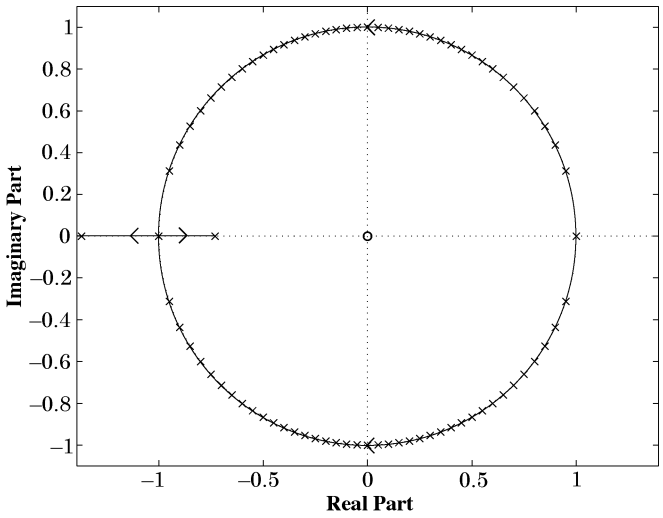

Fig. 14. Pole and zero position of $C(z)$ for varying K when filter $F(z) = (1)/(1 - z^{-1})$ is used.

The fact that the loop gain K varies with $\Delta T/T$, helps equalizing the loop gain over the DCO range. While ΔT varies 20 times over the DCO range, $\Delta T/T$ only varies 7 times.

D. Digital Filter

One goal for the design of the integrating filter is to find a simple filter which does not consume much power or chip area. This means that trivial multiplications such as 1 or 0.5 are preferred. For all filters, poles are given for the entire closed loop $[C(z)]$. The digital filter must be an integrator to avoid an offset phase error in the PLL. This is because a zero phase error should result in no changes of $w(n)$. The simplest possible integrator is the first-order filter given in (10). Using this filter yields a second-order PLL. Fig. 14 shows how the poles and zeroes for the PLL move with varying K. The arrows are pointing toward increasing K. From Fig. 14, it is obvious that the PLL tends to be unstable since the poles will, at best, be placed on the unit circle. In fact, any amount of extra delay in the loop will cause instability.

$$F(z) = \frac{1}{1 - z^{-1}}. \tag{10}$$

For the implemented prototype, the second-order integrator of (11) is used. Fig. 15 shows how the poles and zeroes for the resulting third-order PLL move with varying K. For small K, this gives a narrow-band PLL. The bandwidth of the PLL then increases for increasing K. The PLL will be stable when $K < 2.2$.

$$F(z) = \frac{1}{1 - 0.5z^{-1} - 0.5z^{-2}}. \tag{11}$$

A zero at $z = 0.5$ is added to the filter of (10). The new filter is given in (12). Poles and zeroes for the resulting second-order PLL using the filter of (12) is given in Fig. 16. This filter gives properties similar to the the filter of (11). Stability for this filter occurs for $K < 2.8$. Due to its simpler architecture and its slightly larger stability range, this filter is chosen for the

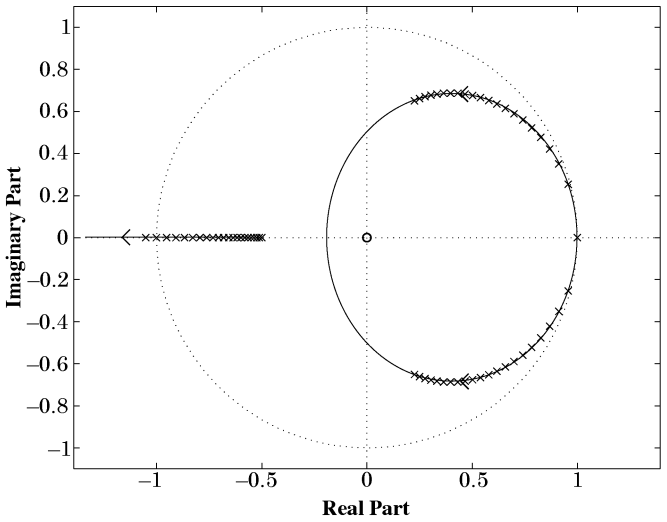

Fig. 15. Pole and zero position of $C(z)$ for varying K when filter $F(z) = (1)/(1 - 0.5z^{-1} - 0.5z^{-2})$ is used.

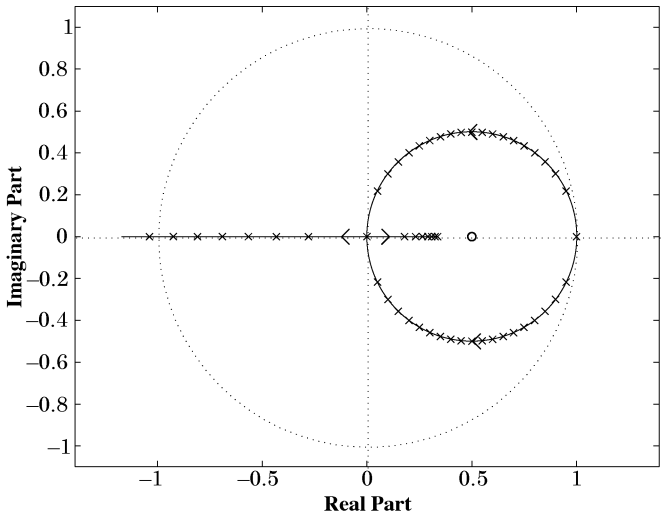

Fig. 16. Pole and zero position of $C(z)$ for varying K when filter $F(z) = (1 - 0.5z^{-1})/(1 - z^{-1})$ is used.

following HDL implementation. Changing the filter is, however, trivial.

$$F(z) = \frac{1 - 0.5z^{-1}}{1 - z^{-1}}. \tag{12}$$

If a zero is added to the second-order integrator of (11), the filter given by (13) with poles and zeroes for the resulting third-order PLL given by Fig. 17 is implemented. This filter gives a stable PLL for $K < 1.4$. This filter is discarded, since it has less stability range and is more complex then the filters of (11) and (12).

$$F(z) = \frac{1 - 0.5z^{-1}}{1 - 0.5z^{-1} - 0.5z^{-2}}. \tag{13}$$

V. Improved Design

Although the first prototype of the PLL is fully functional, some major improvements are found to be possible in order to enhance stability and jitter performance, and to shorten the acquisition time. This part describes an implementation of the all-digital PLL which use techniques similar to the first prototype but with some improved components.

The first prototype is made as a digital design in a schematic netlist editor. A more convenient method is to have a synthesizable VHDL description of the PLL. This makes system simulation including the PLL possible in a digital VHDL simulator. It also helps make the design independent of technology. Other improvements are improved time-to-digital conversion and DCO performance.

A. Time-to-Digital Converter

To increase the resolution of the phase error measurement to decrease the jitter, a new time-to-digital converter is implemented.

The previous time-to-digital converter is implemented as a counter where the DCO output frequency (and its inverse) is used as timing reference. The resolution in the time measurement is then limited to half of the period time for the high-frequency clock. However, a ring oscillator which is used for producing the high frequency clock contains many clock phases. A ring oscillator of length N, where N is an odd number, actually produces N clock phases ($ph1$ to phN). All N clock phases can easily be used to extract information about the phase

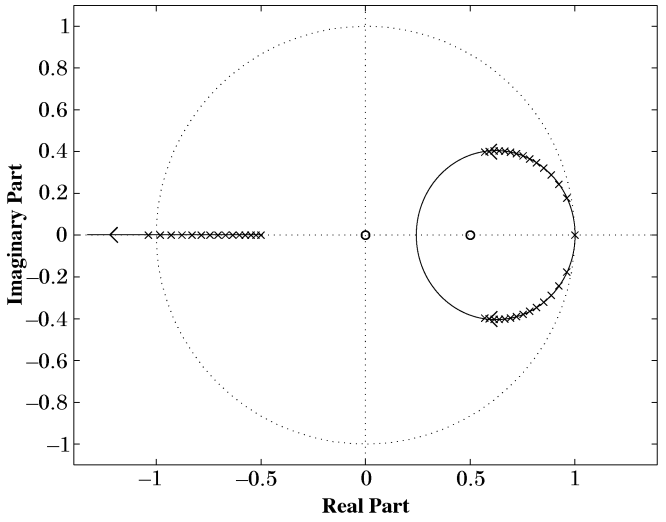

Fig. 17. Pole and zero position of $C(z)$ for varying K when filter $F(z) = (1 - 0.5z^{-1})/(1 - 0.5z^{-1} - 0.5z^{-2})$ is used.

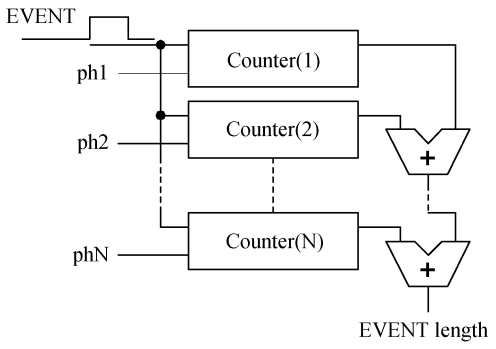

Fig. 18. Time-to-digital converter using multiple clock phases to enhance precision.

error using a counter for each of the N clocks. Fig. 18 shows a time-to-digital converter consisting of a set of N counters clocked with N clock phases. The EVENT signal is for each counter used as an enable signal. Note that to get maximum resolution, each counter must increment on both positive and negative edge. This implementation works fine on any ring oscillator where the delay in each stage is equal or almost equal, as in most VCOs with current-starved inverters.

If one counter (for instance, counter N) is observed, all the other counters will have the value of counter N or counter $N\pm1$. This means that for all counters but one, one of -1, 0, 1 is sufficient information. Thus all counters except for counter N can be replaced by a two-bit counter. A comparison between each two-bit counter and the two LSBs of counter N yields the result -1, 0, or 1. Hence, the set of N large counters can be replaced by one large counter and $N-1$ two-bit counters as in Fig. 19. As seen in Fig. 19, the result from the large counter is multiplied by two times the number of phases $(2N)$ before adding to the sum of the small counters. If the counters only increment on positive or negative edge, the result of the large counter is instead multiplied by N.

Assuming that all N clock phases in the DCO is used in the time-to-digital converter, the loop gain in (7) is instead given by

$$K = \frac{2 \times N \times \mathrm{MF} \times \Delta T}{T}. \tag{14}$$

For maximum resolution, an extra ring oscillator can be used together with the new time-to-digital converter. The resolution will then be equal to the delay of one inverter. A similar arrangement for time measurement can be found in [10]. If an extra ring oscillator is used as reference, the loop gain in (14) is instead given by

$$K = \frac{2 \times N \times \mathrm{MF} \times \Delta T}{T_{\mathrm{fix}}}, \tag{15}$$

where T_{fix} is the period time of the extra ring oscillator.

In the extra ring oscillator, the period time T_{fix} is decided by the number of inverters N and the propagation delay through an inverter t_p as follows:

$$T_{\mathrm{fix}} = 2 \times N \times t_p. \tag{16}$$

Equation (15) can, therefore, be rewritten as

$$K = \frac{\mathrm{MF} \times \Delta T}{t_p}. \tag{17}$$

It can be noted that the resolution of the phase detector is at least an order of magnitude better than for the time-to-digital converter, which is the bottleneck in the phase error measurement. However, this is not a problem unless the multiplication factor is small. Given a large enough multiplication factor, the phase steps of the oscillator times the multiplication factor will exceed the smallest phase error that can be converted to digital. The proposed PLL is, therefore, primarily intended for multiplication factors above eight.

B. Digitally Controlled Oscillator

The performance of the time-to-digital converter of Fig. 19 is dependent on the clock phases being evenly distributed over the clock period. To achieve this, the DCO of Fig. 3 is slightly modified. For the modified DCO (see Fig. 20), the tri-state inverters are distributed over all stages of the ring oscillator including the NAND gate. Distributing the tri-state inverters over seven stages instead of over six stages leads to 18 tri-state inverters per stage instead of 21. For the control of the new DCO, care must be taken not to cause a short circuit in the stage containing the NAND gate. To ensure that no short circuit can occur, the tri-state inverters parallel to the NAND gate are always disabled when the signal "RUN" is low.

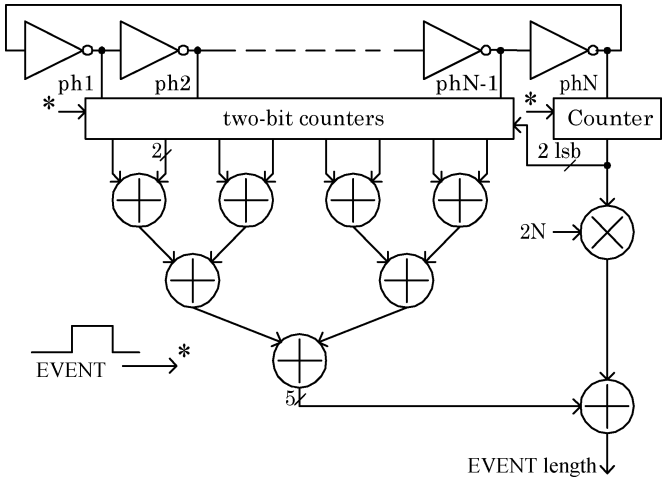

Fig. 19. Improved architecture for the time-to-digital converter using multiple clock phases.

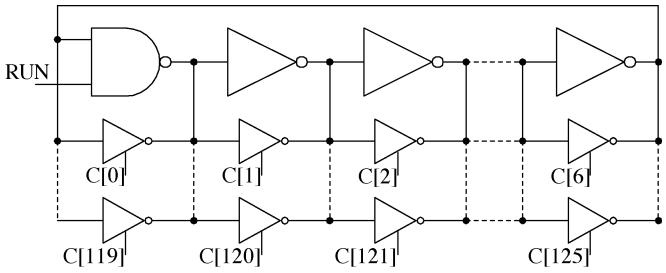

Fig. 20. DCO with evenly distributed clock phases.

The behavior of the new DCO is simulated in an analog simulation environment. The results are shown in Fig. 21. Actually, the new DCO, aside from having evenly distributed clock phases, also performs better both in terms of linearity and maximum clock rate. This is due to fewer parallel tri-state inverters per stage in the ring oscillator.

C. New DCO Made From a VCO and a Set of D/A Converters

This part describes a possible full-custom implementation of the DCO. A common solution for designing the DCO is to make it as a combination of a D/A converter and VCO. For instance, this is the approach in [3]. Chosen for the implementation of the new DCO is a seven-stage ring oscillator made from current-starved inverters (Fig. 22). To control the frequency of the VCO, each voltage at node $Vn(0)-Vn(6)$ and $Vp(0)-Vp(6)$ is separately controlled using 14 small D/A converters. The control voltages for the current-starved inverters are changed gradually to keep the clock phases evenly spread over the clock period.

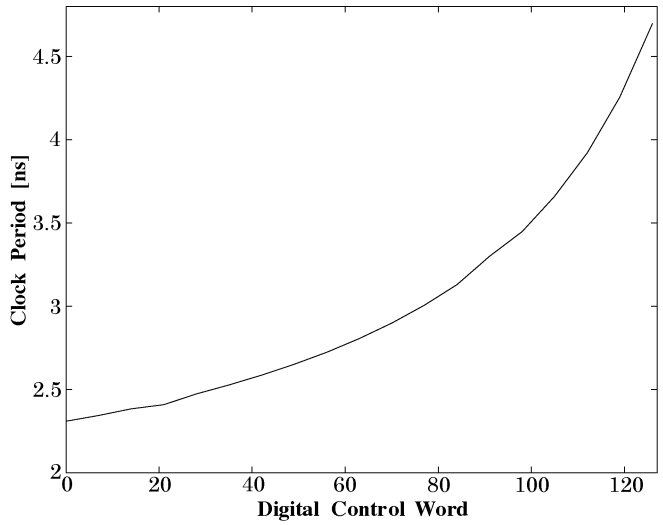

Fig. 21. Simulated period time versus digital control word W for the DCO of Fig. 20.

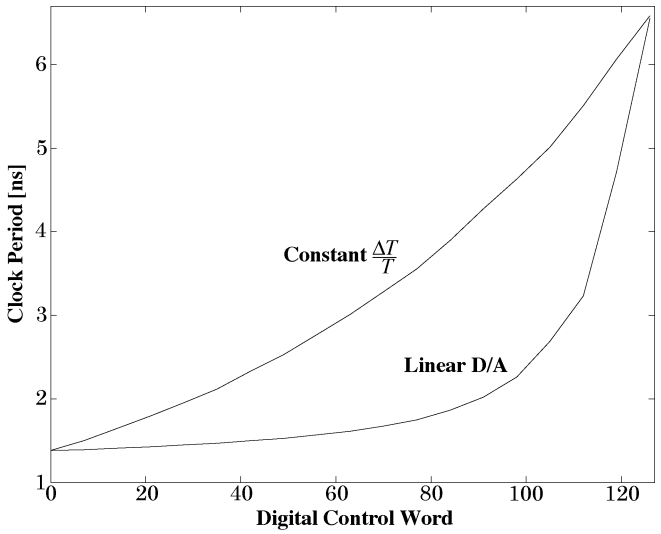

Fig. 23. Simulated period time versus digital control word W for the DCO of Fig. 22

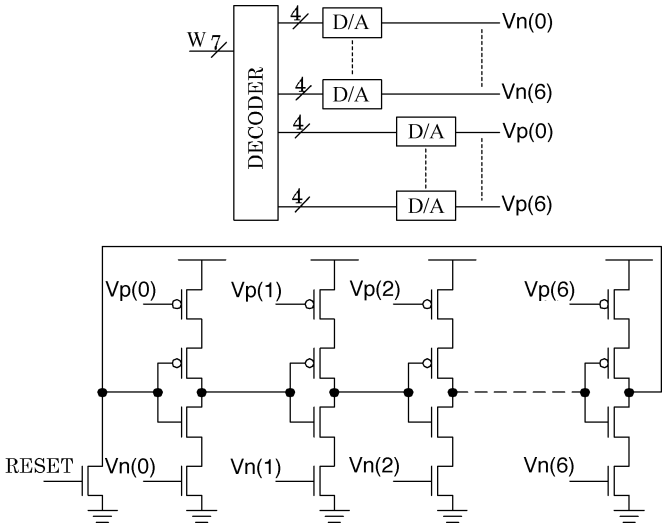

Fig. 22. DCO consisting of 14 D/A converters and a current-starved inverter VCO.

Using custom-made D/A converters gives the opportunity to linearize the oscillator by using nonlinear D/A converters. Since the loop gain of the PLL is proportional to $\Delta T/T$ [see (7)], a completely linear DCO is not the best solution. Instead, effort is made to keep the ratio $\Delta T/T$ constant. To achieve this, a set of control voltages is preliminary calculated. The calculated voltage levels are then refined using analog simulations. To start the VCO at a known state, a pull-down transistor controlled by the signal "RESET" is added. When RESET is high, the voltage $Vp(6)$ is set high to prevent a short circuit from occuring.

Fig. 23 shows the corresponding simulated period time versus digital control word for the D/A–VCO combination. Simulated period time versus digital control word for the D/A–VCO combination using linear D/A converters is also given as comparison.

The frequency range for the D/A–VCO combination is simulated to between 150 and 720 MHz. Simulations indicate that the power consumption for the VCO is much less than for the DCO of Fig. 3. A resistor chain with transistor switches [11] is used to implement the D/A converters. The main source of power consumption for the D/A–VCO is from the static current through the 14 resistor chains. The 14 transistor chains are designed with a resistance between power and ground of 30 $\mathrm{k}\Omega$ and thus consumes $14 \times (3^2/30\,\mathrm{k}) = 4.2$ mW of static power. This is to be compared with the DCO of Fig. 20, which according to simulations, consumes approximately 20 mW of dynamic power running at 400 MHz.

D. Phase Detector

Using the new time-to-digital converter gives a longer critical path and, therefore, the delay of the signal UPDATE in Fig. 5 needs to be longer. Instead of adding more inverters to the delay, a simple state machine triggered by a nondelayed version of UPDATE produces an appropriate delay. The simple state machine, which is clocked by the high-frequency output from the DCO produces a two-period pulse delayed by one period. The pulse is then further delayed two clock periods, which, aside from giving the time-to-digital converter enough computing time, also helps avoid metastability. Avoiding metastability for the pulse is extremely important since it is used for clocking the registers in the digital filter. To avoid timing violations between the time-to-digital converter and the digital filter, the reset signal to the time-to-digital converter is further delayed.

E. Integrating Filter

As an integrating filter, the filter given in (12) is chosen due to its simpler architecture and larger stability range. Since the optimum loop gain will differ with parameters such as multiplication factor and DCO resolution, a shifter is also implemented to scale the result. Instead of simply throwing all the LSBs, the number of bits in the digital filter is increased by one. The extra bit, which is not used to control the DCO then represents 2^{-1}. This reduces the impact of rounding errors for the digital filter.

F. HDL Description

All parts of the PLL except the DCO are described in synthesizable VHDL code, which can be found in [12]. All parts except for the time-to-digital converter are possible to synthesize to the highest frequency of the D/A–VCO oscillator, 720 MHz, using the 0.35-μm CMOS technology. It is, however, possible to reduce the time-to-digital converter to consist only of two-bit counters and then synthesize to 720 Mhz. The cost for this is a longer acquisition time, since the time-to-digital converter then will not be able to measure long phase errors. The core area will increase slightly for the improved PLL compared to the first prototype. This is mainly due to the time-to-digital converter, which is larger than the previous one.

The use of an HDL description makes digital system simulation, including the PLL, possible.

Since the DCO is either dependent on parallel tri-state gates for functionality or made full custom to improve performance, it is not included in the HDL description. To incorporate the DCO in the VHDL simulation, the DCO is simulated in an analog simulator once and the result is stored in a file. This makes the simulation of the PLL extremely fast compared to a mixed-mode simulation with the DCO as an analog component.

G. Metastability

Also considered in the new implementation is metastability. Metastability, which usually is ignored in these kinds of designs, can occur whenever an input to a flip-flop is not synchronized with the clock and the setup, or hold times for the flip-flop are violated. For the PLL, metastability can, therefore, occur in the time-to-digital converter, which has the unsynchronized phase error as input. It is, however, not possible to completely remove the risk of metastability [13]. What can be done is minimizing the probability of metastability occurring by synchronizing the phase error to each counter by inserting flip-flops in each counter. The flip-flops are used to synchronize the EVENT pulse to the clock phase of each counter.

VI. Comparison to Other Digital PLLs

Many digitally controlled PLLs divide the acquisition into frequency and phase acquisition as in [3]–[5]. Although separating the acquisition processes makes it easier to design the PLL without deeper analysis of the feedback circuit, it results in long acquisition time and high complexity. In a traditional PLL, both phase and frequency are found simultaneously instead, which is also the method for the proposed architecture. Aside from fast acquisition assuming that the feedback filter is correctly chosen, this also gives a simple architecture which results in a small core area. As an example, the PLL in [4], which is implemented in a similar technology, is ten times larger. The proposed PLL is possible to implement using digital standard cells in contrary to many other digital PLL designs, for instance, [3], [5], and [6]. Regarding power consumption, it is found to be comparable to the power consumption in [5] and [6] and lower than the power consumption in [3] and [4]. However, it should be noted that comparing power consumption is difficult since the different designs are implemented with different technology, supply voltage, and frequency range.

VII. Conclusion

A prototype of a standard-cell all-digital PLL clock multiplier is designed and fabricated using 0.35-μm CMOS technology. The all-digital PLL has, at 3.0-V supply voltage, a frequency range of 152–366 MHz while consuming 8.1–24 mW. At 2.0 V, the frequency range is 90–230 MHz while consuming 2.1–6.1 mW. The PLL occupies 0.07 mm^2 of on-chip area. Instead of a charge pump and an analog filter, a counter and a recursive digital filter is used as a loop filter. A DCO is made from a ring oscillator with additional tri-state gates. The digital PLL is implemented using cells found in an ordinary standard-cell library, which makes it portable between technologies. In the first prototype, the methods for implementing the digital PLL are tested. The digital PLL is then improved in the next version which is described in VHDL. For the improved all-digital PLL, a new time-to-digital converter with resolution down to one gate delay, is proposed. Also, a DCO implemented with a VCO and 14 nonlinear D/A converters is proposed. The nonlinear D/A converters help linearize the DCO to equalize the loop gain for the PLL. The VHDL description of the PLL makes it easy to include in digital simulations and then to synthesize to any technology assuming a DCO is available. The VHDL description of the PLL can be downloaded from [12]. The VHDL description is synthesizable except for the DCO, which is represented as simulation data.

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