A Digitally Programmable Delay Element: Design and Analysis

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***Abstract*—Variable delay elements are often used to manipulate the rising or falling edges of the clock or any other signal in integrated circuits (ICs). Delay elements are also used in delay locked loops (DLLs). Although, a few types of digitally controlled delay elements have been proposed, an analytical expression for the delay of these circuits has not been reported. In this paper, we propose a new delay element architecture and develop an analytical equation for the output voltage and an empirical relation for the delay of the circuit. The proposed circuit exhibits improved delay characteristics over previously reported digitally controlled delay elements.**

***Index Terms*—Analysis, delay, design, digital CMOS, locked-loop, test.**

I. Introduction

VARIABLE DELAY elements have many applications in VLSI circuits. They are extensively used in digital delay locked loops (DLLs) [1], phase locked loops (PLLs) [2], [3], digitally controlled oscillators (DCOs) [4], [5], and microprocessor and memory circuits [6], [7]. In all these circuits, the variable delay element is one of the key building blocks. Its precision directly affects the overall performance of the circuit. Moyer extended the scope of delay elements by constructing a system to achieve precise vernier delay patterns [8]. As the operational frequency of digital circuits is increased, the debugging and testing of these circuits is becoming ever more challenging. Recently, some techniques have been proposed that allow testing of high-frequency circuits using slow automatic test equipment (ATE) [9], [10]. In these methods, a precisely delayed clock is generated using delay elements.

There are several different methods for implementing a delay element. Each of these methods has its advantages and drawbacks. In this paper, we propose and analyze a digitally controlled delay element and compare it with two existing delay elements. The proposed circuit exhibits improved controllable delay characteristics over the existing delay elements. It demonstrates a monotonic delay behavior with respect to the digital input vector and exhibits lower-temperature sensitivity making it suitable for high-precision applications.

This article is organized as follows: In Section II, a brief review of various approaches for delay elements is provided. In Section III, we discuss two of the commonly used digitally controlled delay elements (DCDE) and highlight the shortcomings of these approaches. In Section IV, we propose a new DCDE circuit. A detailed analysis of the circuit is also provided. The simulated results are compared with the analytical results. The discrepancy between the two is found to be less than 10%. Furthermore, an empirical model for the proposed DCDE is introduced and a design procedure is outlined. In the subsequent section, the proposed DCDE is compared with other two DCDEs discussed in Section III. Finally, in Section VI, conclusions are drawn.

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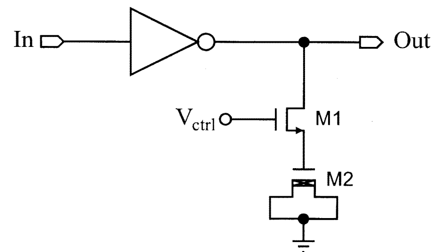


Fig. 1. Shunt capacitor delay element.

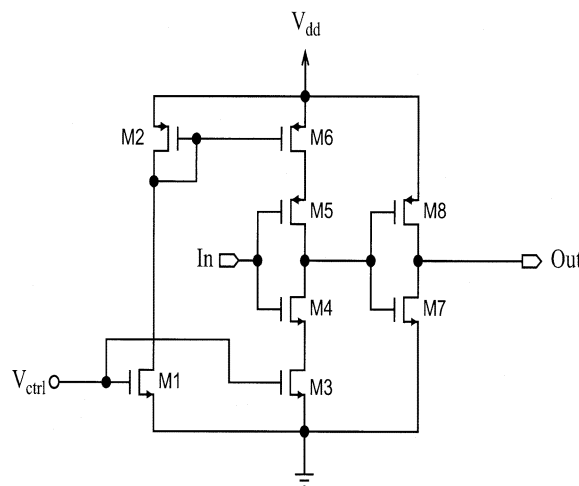


Fig. 2. Current starved delay element.

II. Variable Delay Elements: Design Techniques

There are three popular techniques for designing a variable delay element. These are known as: shunt capacitor technique, current starved technique, and variable resistor technique.

Fig. 1 shows the basic circuit of using a shunt capacitor. In this circuit, M2 acts as a capacitor. Transistor M1 controls the charging and discharging current to the M2 from the NOR gate. The M1 gate voltage, V_{ctrl}, controls the (dis)charge current. As a consequence, the NOR gate delay can be controlled. An interested reader is referred to [2] for further details.

Fig. 2 illustrates the basic building block of a current starved delay element. As can be seen in this figure, there are two inverters between input and output of this circuit. The charging

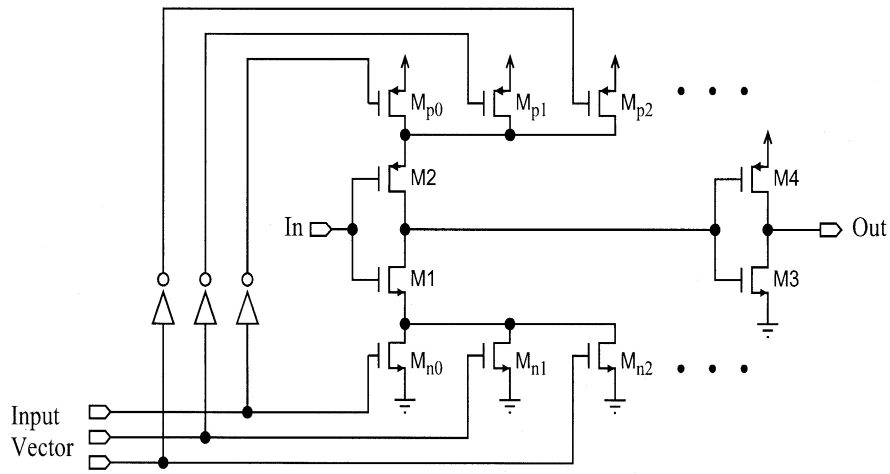


Fig. 3. Digitally controlled delay element.

and discharging currents of the output capacitance of the first inverter, composed of M4 and M5, are controlled by two MOS transistors, M3 and M6. Charging and discharging currents depend on the gate voltage of M6 and M3 transistors, respectively. M1 and M2 constitute a current mirror for controlling the gate voltage of M6. In this delay element, both the rising and falling edges of the input signal can be controlled. If in a given application only the control of rising (falling) edge is required, then $V_{\rm ctrl}$ may directly be applied to M3 (M6). The second stage inverter (composed of M7 and M8) is for improving the rise and fall times of the circuit. Sometimes, multiple cascaded inverters are used for this purpose.

In both of the above techniques, a continuous voltage is used to control the delay. In some applications, we need a delay which can be controlled digitally [2], [4], [9]. The current starved circuit can be modified for this purpose. Fig. 3 shows a current starved DCDE [3], [4]. As can be seen, by applying a specific binary vector to the controlling transistors (M_{n0}, $M_{n1}, \ldots M_{p0}$, $M_{p1}, \ldots$), a combination of transistors are turned on at the sources of the M1 and M2 transistors. Such an arrangement, controls the rise and fall times (and hence, the delay) of the output voltage of the first inverter. The W/L ratios of the controlling transistors are usually chosen in a binary fashion so as to achieve binary, incremental delay. Unfortunately, as it will become apparent in the following sections, neither the binary, nor any other way of weighing can make a linear, monotonic relationship between the input vector and the output delay.

Another technique for implementing a DCDE is illustrated in Fig. 4. In this circuit, a variable resistor is used to control the delay [6]. A stack of n rows by m columns of nMOS transistors is used to make a variable resistor. This resistor subsequently controls the delay of M1. In the circuit of Fig. 4, only the rising edge of the output can be changed with the input vector. Another stack of pMOS transistors can be used at the source of the pMOS transistor, M2, to have control over the falling edge delay.

III. Drawbacks of DCDEs

One of the major problems with existing DCDE architecture, is the nonmonotonic delay behavior with ascending binary input

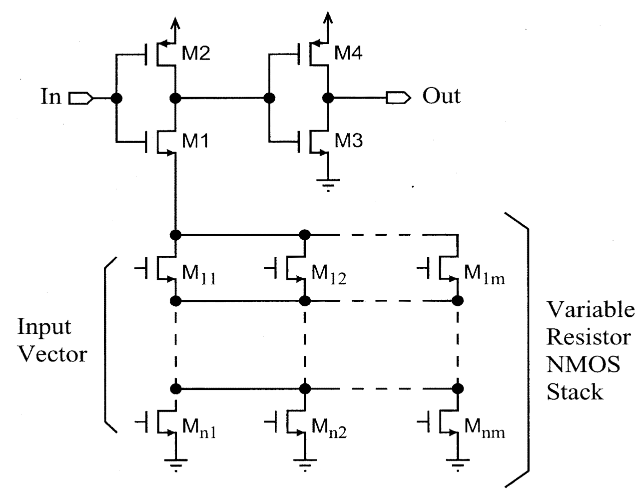
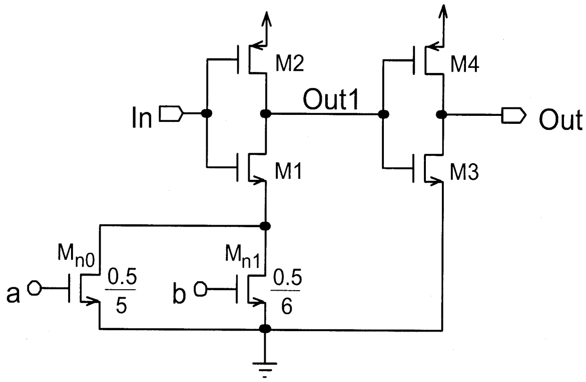


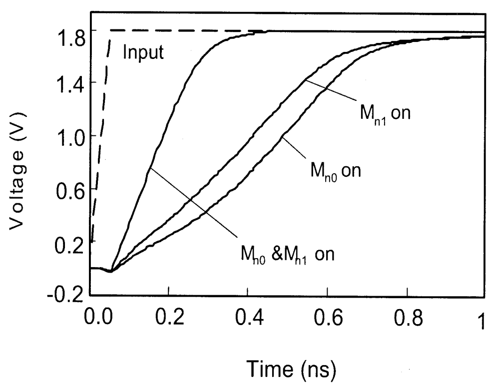
Fig. 4. Delay element using variable resistor.

pattern. This can further be explained by Fig. 5. This figure illustrates a specific arrangement of DCDE of Fig. 3 and associated HSpice simulation results. In Fig. 5(a), a digitally controlled current starved delay element with two transistors connected to the source of M1 is shown. The W/L ratios of these two transistors are chosen as $(W/L)_{M_{n0}} = 0.5/5$ (=0.1) and $(W/L)_{M_{n1}} = 0.5/6$ (=0.083). The output voltage waveform of this circuit for three different input vectors is shown in Fig. 5(b). It is worth noting that with two transistors, we can get at most three different delays because at any time at least one transistor must be ON at the source of M1. Furthermore, it should be mentioned that the transistor length, L, instead of transistor width, W, is used to control the W/L ratio. This is because we cannot otherwise realize a small W/L ratio of a transistor which gives us the desired delay.

One usually expects to have a longer circuit delay for a smaller W/L ratio of controlling transitor(s) (i.e., M_{n1}). This is not necessarily true for this kind of delay element. As can be seen in Fig. 5(b), the delay of the circuit for $W/L = 0.1$ ($td = 467$ ps) is larger than the delay for $W/L = 0.083$ ($td = 385$ ps). In such circuit configurations, the circuit delay is influenced by two factors.



(a)



(b)

Fig. 5. (a) Digitally controlled current starved delay element and (b) its output voltage.

1) The resistance of the controlling transistor: by increasing/decreasing the effective ON resistance of the controlling transistor(s) at the source of M1, the circuit delay can be increased/decreased.
2) The capacitance of the controlling transistor: as the effective capacitance at the source of M1 increases the charge sharing effect causes the output capacitance to be discharged faster and the overall delay of the circuit decreases.

Therefore, by decreasing the W/L ratio of controlling transistor(s), it is not apparent whether the delay will be increased or decreased. The effective capacitance seen at the source of M1 depends on which controlling transistor(s) is/are on. This is due to the fact that the ON and OFF capacitances between drain and ground of a MOSFET are different. As a consequence, it is difficult to predict the circuit delay for a given input vector.

Fig. 6 further illustrates the impact of the effective capacitance at the source of M1. The figure shows the node Out1 voltage for three different configurations of controlling transistors. As can be seen from the figure, as M1 turns on, the Out1 node immediately charge shares with the effective capacitance at the source of M1. The subsequent fall of this intermediate nodal voltage is controlled by the effective ON resistance of the controlling transistors. The amount of voltage drop due to charge sharing is different for the two cases when M_{n0} is ON or M_{n1} is ON. When only M_{n0} is ON, the effective capacitance at the source of M1 is equal to $C1 = C_{dn0,\,\mathrm{lin}} + C_{dn1,\,\mathrm{off}}$ where $C_{dn0,\,\mathrm{lin}}$ ($C_{dn1,\,\mathrm{lin}}$) is the total capacitance between drain of M_{n0} (M_{n1}) and ground when M_{n0} (M_{n1}) is in the linear region and $C_{dn1,\,\mathrm{off}}$ ($C_{dn0,\,\mathrm{off}}$) is the total capacitance between drain of M_{n1} (M_{n0}) and ground when M_{n1} (M_{n0}) is OFF. On the other hand, when only M_{n1} is ON, the capacitance $C_2 = C_{dn0,\,\mathrm{off}} + C_{dn1,\,\mathrm{lin}}$ is at the source of M1. Clearly, $C_1 \neq C_2$ because M_{n0} and M_{n1} have different sizes. Therefore, when only M_{n1} (with smaller W/L) is ON, the effective capacitance seen by the source of M1 is larger compared to the case when only M_{n0} is ON. This fact is further illustrated by simulation results. The voltage at the source of M1 falls lower when only M_{n1} is ON than compared to the voltage when only M_{n0} is ON. The situation is further complicated as the number of controlling transistors is increased. It becomes very difficult to predict the circuit delay for a given input vector.

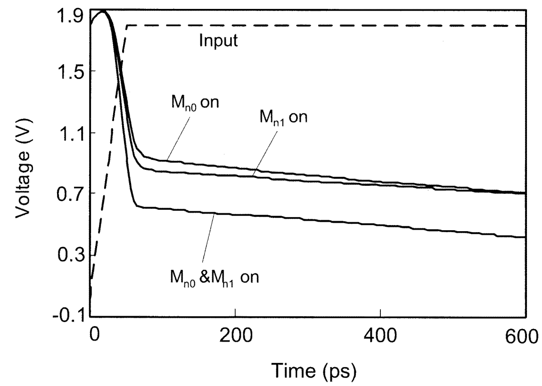


Fig. 6. Output voltage of the first stage of the circuit in Fig. 5(a).

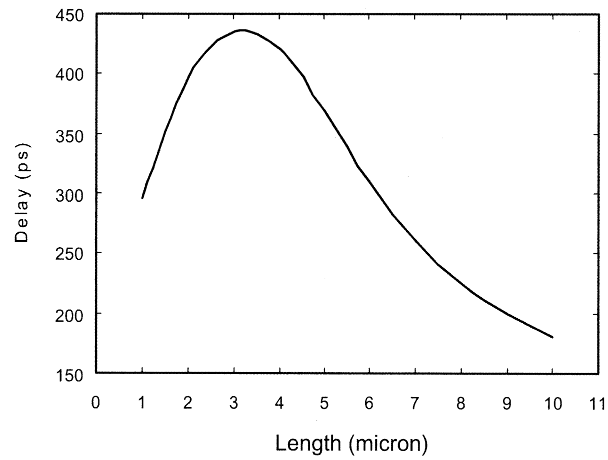


Fig. 7. Effect of channel length of Mn0 on delay.

The determination of W/L ratio of a controlling transistor becomes an issue. Fig. 7 depicts the simulated circuit delay as a function of M_{n0} channel length when M_{n1} is OFF. In this figure the W of M_{n0} is kept constant (0.5 μm) while L is changed. As can be seen, increasing L up to approximately 3.2 μm causes the delay to increase as expected. However, further increasing L beyond 3.2 μm decreases the delay, which is in contrast to what one would expect. As a result, one may have more than one transistor length for a given circuit delay.

The DCDE architecture shown in Fig. 4 has drawbacks similar to the DCDE shown in Fig. 3. In this kind of circuit, at any time, at least one transistor should be ON in each of the rows. Hence, with six transistors in two rows, there are at most nine

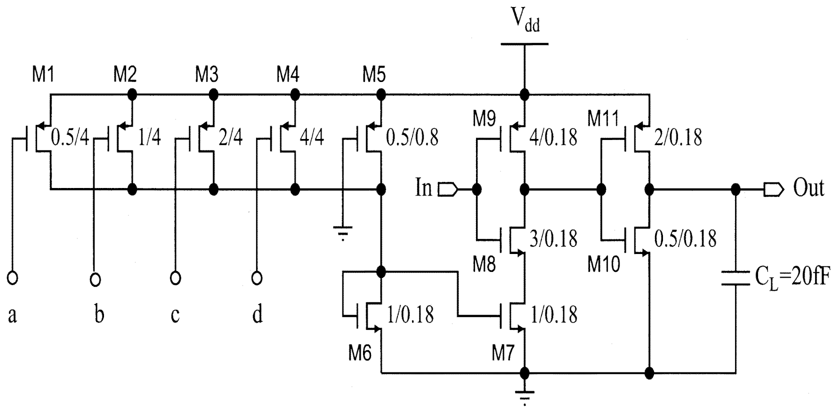


Fig. 8. The proposed delay element.

different resistance combinations. The delay prediction in this structure for a given input vector is even more complicated than the current starved DCDEs. Besides changing the equivalent resistance, a change in input vector causes a change in the effective capacitance seen at the source of M1 and other intermediate nodes in the NMOS stack. Saint Laurent and Swaminathan [6] designed a programmable delay element with two rows and four columns. Their results show the unpredictable nature of the circuit delays and they realized desirable circuit delays through a complicated method of optimal coding.

The problem of finding the W/L ratios of the transistors in both of the above mentioned methods is difficult. The result of any change in W/L parameter can not be estimated and the circuit should be simulated for every change in the W/L. To overcome this problem we propose a new configuration for a DCDE in the following section. In this circuit, finding the W/L ratios of the transistors is straightforward and determining the input vector for a specific delay is simpler than the methods mentioned above.

IV. The Proposed DCDE

Fig. 8 shows the architecture of the proposed circuit. As can be seen in this figure, a current starved buffer, M7–M11, is the main element. The controlling current through this buffer is controlled by a current mirror circuit composed of transistors M6–M7. An appropriate current through M7 can be adjusted by turning-on transistors M1–M4, while transistor M5 is always on.

At the instance when M8 turns on, the capacitor at its output node starts to discharge. The discharging current is controlled by transistor M7 acting as a current source. The passing current through this transistor is determined by the gate voltage of M6. The gate voltage of M6, in turn, is determined by the current passing through its drain. pMOS transistors M1–M5 control the current flowing through M6 nMOS transistor. Therefore, the overall delay of this circuit is digitally controlled by M1 to M4. The W/L ratio of transistors M5 can be designed for maximum delay of the circuit. The input vector for a specific delay is applied to the gates of M1 to M4 (a, b, c, d). In this circuit, depending on the input vector, one may realize 16 different delay settings. In Section IV-A we provide an analytical delay model for this circuit.

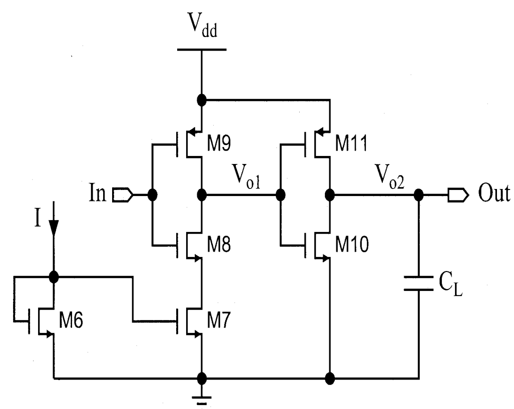


Fig. 9. Part of the proposed delay element.

A. Mathematical Model of the Proposed Delay Element

Fig. 9 shows part of the delay element. In order to have a better controllability, the W/L ratio of transistor M8 should be much bigger than that of M7. In such an arrangement the current is controlled by M7.

In order to find a relationship between V_g (the gate voltage of transistor M7 and/or M6), and the delay of the circuit (t_d), we should calculate the current passing through transistor M7. Once this current is known, one can find the output voltage. Transistor M7 is a relatively small transistor with a channel length of 0.18 μm. It shows a velocity saturated behavior for gate voltages more than about 0.65 V. Hence, we can consider the following for the drain current of this transistor:

$$i_d = \frac{k_n W_7}{2L_7}(V_g - V_{T7})(1 + \lambda_7 V_{DS7}). \tag{1}$$

Equation (1) is valid as long as the transistor is in the saturation region. This is true for most of the transition time because the gate voltage of M7 is not much bigger than its threshold voltage. Moreover, we assume that the voltage drop across M8 is very small so that $V_{DS7} \simeq V_{o1}$. The output voltage (V_{o1}) can be found from the following equations:

$$-C_{L1}\frac{dV_{o1}}{dt} = \frac{k_n W_7}{2L_7}(V_g - V_{T7})(1 + \lambda_7 V_{DS7}) \tag{2}$$

$$-C_{L1}\frac{dV_{o1}}{dt} = K_1 + K_1 \lambda_7 V_{o1} \tag{3}$$

where C_{L1} represents the overall capacitance at node V_{o1} and

$$K_1 = \frac{k_n W_7}{2L_7}(V_g - V_{T7}).$$

Solving the above differential equation with initial condition of $V_{o1} = V_{dd}$ at $t = 0$ results to the following for V_{o1}

$$V_{o1} = (V_{dd} + 1/\lambda_7)e^{-t/\tau_1} - 1/\lambda_7 \tag{4}$$

where $\tau_1 = C_{L1}/(K_1\lambda_7)$. At $t = t_{d1}$ (inverter delay from In to V_{o1}) $V_{o1} = V_{dd}/2$. Hence

$$t_{d1} = \tau_1 Ln\,\frac{1 + \lambda_7 V_{dd}}{1 + \lambda_7 V_{dd}/2}. \tag{5}$$

To compute the circuit delay of this delay element, we should find V_{o2} as a function of time. At the instance when the input voltage (V_{in}) goes high, V_{o1} starts to fall and M10 starts to turn off. When V_{o1} becomes less than $V_{dd} - |V_{T11}|$, transistor M11 starts to conduct while transistor M10 starts to turn off. Hence, for a period of time, both M10 and M11 transistors are on. Owing to the current starved nature of the first inverter, the fall time of V_{o1} is not very small. Therefore, the direct current passing through transistors M10 and M11 is not negligible. It is necessary to consider the current in both of these two transistors in order to find V_{o2}. However, this complicates the equations and defeats the purpose of a simple analytical model. We assume that the direct path current is negligible and can be ignored in these calculations. Moreover, ignoring the channel length modulation effect of M_{11}, we can write

$$i_{d11} = \frac{k_p W_{11}}{2L_{11}}(V_{gs11} - V_{T11})^2 \tag{6}$$

and

$$i_{d11} = C_L \frac{dV_{o2}}{dt}. \tag{7}$$

The initial condition for the above differential equation is $V_{o2} = 0$ at $t = 0$. We can substitute V_{gs11} in the above equation by $V_{dd} - V_{o1}(t + t_p)$ where t_p is the time when V_{o1} reaches $V_{dd} - |V_{T11}|$ that is

$$t_p = \tau_1 Ln\,\frac{1 + \lambda_7 V_{dd}}{1 + \lambda_7(V_{dd} - |V_{T11}|)}. \tag{8}$$

Combining (6)–(8) and solving the resulting equation, V_{o2} can be found as the following:

$$V_{o2} = K_3 K_2^2 \tau_1 \left(\frac{t}{\tau_1} + 2e^{-t/\tau_1} - \frac{1}{2}e^{-2t/\tau_1} - 1.5\right) \tag{9}$$

where

$$K_2 = V_{dd} + \frac{1}{\lambda_7} - |V_{T11}|$$
$$K_3 = k_p W_{11}/2L_{11}C_L.$$

From (9) the delay time of the circuit can be computed. Fig. 10 plots the circuit delay as a function of gate voltage (V_g). In this figure, the simulated data of the circuit shown in Fig. 8, is compared with the analytical model as well as with a simple empirical model. This empirical model is discussed in Section IV-B . In this simulation W/L ratio of 0.18/10 is selected for M10 so as to make the direct path current negligible. The error between simulated and the analytical model for $V_g > 0.6$ V, is found to be less than 10%. This error becomes larger as V_g is reduced because the analytical model is developed assuming M_7 is velocity saturated [see(1)]. This assumption requires $V_g > 0.65V$. In most practical applications this assumption is acceptable.

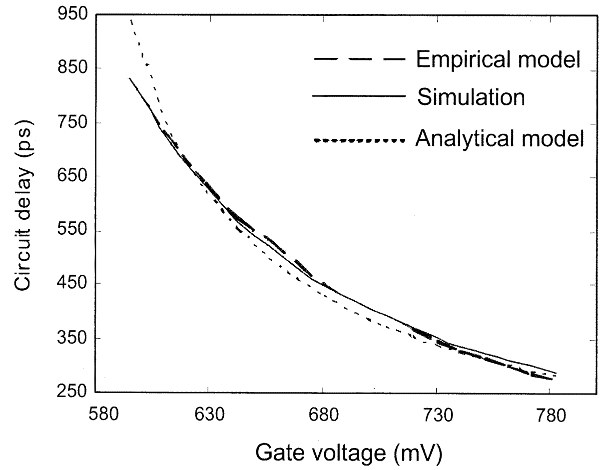


Fig. 10. Delay of the proposed delay element from simulation, analytical model, and empirical model.

B. *Empirical Equations for the Proposed Variable Delay Element*

In spite of ignoring the direct path current in M10/M11, and channel length modulation effect in transistor M11, (9) is too complicated to be used as a means for delay element circuit design. Therefore, in this section, we introduce an empirical formula for the circuit delay of the proposed DCDE.

By curve fitting, a simple equation is found for the proposed delay element. That is

$$t_d = \frac{A_1}{(V_g - V_1)} \tag{10}$$

where A_1 and V_1 are constants. This equation illustrates the relationship between V_g and t_d of the delay element. The V_g, in turn, is a function of the current passing through M_6. The drain current of M_6 is the sum of the drain currents of all the pMOS transistors (M_1 through M_5). Since, M_6 is working in saturation, V_g can be found from the following:

$$V_g = V_2 + A_2\sqrt{I} \tag{11}$$

where V_2 and A_2 are constants and depend on M6. V_2 is actually the threshold voltage of M6 and A_2 is the inverse of the root of its transconductance M6. In (11), the current I can be calculated from

$$I = I_0 + I_1\overline{a} + I_2\overline{b} + I_3\overline{c} + I_4\overline{d}. \tag{12}$$

The coefficients I_0, I_1, I_2, I_3 and I_4 depend on W/L ratio of the pMOS transistors. All the parameters in the above formulas can be found by simulating the circuit for five different input vectors ($abcd = 1111, 0111, 1011, 1101, 1110$). Once all the above parameters are known from simulation, the circuit delay

TABLE I
EMPIRICAL MODEL PARAMETER VALUES

	V_1 1111	V_2 1110	V_3 1101	V_4 1011	V_5 0111	Parameter Value
I_0	*					$23\mu A$
I_1		*				$5\mu A$
I_2			*			$10\mu A$
I_3				*		$19\mu A$
I_4					*	$39\mu A$
A_1	*				*	$50.9ps.V^2$
A_2	*				*	$37.03\frac{mV}{\mu A^{1/2}}$
V_1	*				*	$344.5mV$
V_2	*				*	$416.4mV$

for any input vector can be found from (10)–(12). Simulation of a small number of input vectors (five out of 16) is sufficient to determine the constants in above mentioned equations. Fig. 10 also plots the circuit delay obtained by the empirical model with reasonable success. The values of the parameters in the empirical model which are used for the delays of Fig. 10 are shown in Table I. In this table, it is also shown that which vectors are used for the extraction of each parameter.

In the case of eight controlling bits, we need to perform only nine simulations out of a total of 256 possible cases. Hence, this method has small computational complexity.

Fig. 11(a) shows the simulated output voltage of the circuit for all the possible input vector (a, b, c, d) combinations. Similarly, Fig. 11(b) illustrates the delay behavior with respect to input vectors. These simulation results show a monotonic circuit rising delay behavior. The circuit falling delay remains the same in all input vector combinations. However, similar to the rising circuit delay, the falling circuit delay can also be controlled by adding additional transistors.

C. Design Procedure

In this section, we outline the design procedure of the proposed DCDE. As will be seen, the design of the proposed delay element is more straightforward compared to the commonly used architectures. In order to find the design steps, first we should examine the effect of W/L ratios of the pMOS controlling transistors on the circuit delay. Fig. 12(a) shows the effect of W/L ratio of M5 on the circuit delay while M1–M4 are kept constant. As can be seen, M5 mainly affects the maximum delay of the circuit. In Fig. 12(b), the W/L ratio of M5 is kept constant and that of M1–M4 are changed. Clearly, these transistors have no effect on the maximum delay while they affect the minimum delay of the circuit. Based on observations of Fig. 12, the following steps can be considered as general guidelines for transistor sizing of the proposed DCDE (Fig. 8).

1) The size of transistors M8 to M11 are basically determined by the load capacitance. Transistor M7 should be much smaller than M8 such that the discharging current be controlled by M7. M6 can be the same size as M7.
2) The number of pMOS controlling transistors (N) can be obtained from the number of different delays (m) one may want to get from the delay element such that $m = 2^N$. Moreover, the circuit must contain one more pMOS transistor (M5) which is always on.
3) Place M5 and size it to get the maximum delay.

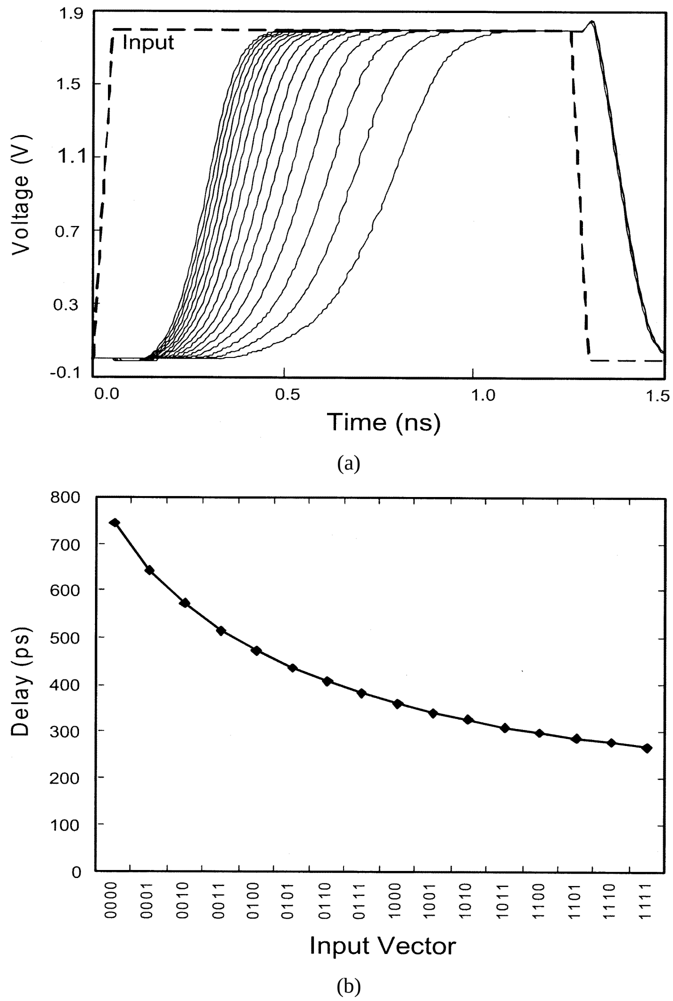


Fig. 11. The transient response of the proposed delay element for all the input vector combinations. (a) Output waveforms. (b) Delay versus input vector.

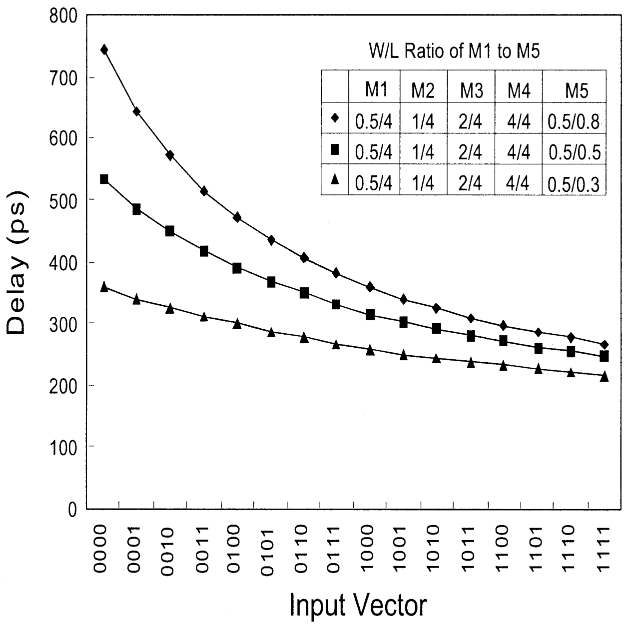
4) After sizing M5, place one pMOS transistor (e.g., M0) in parallel to M5 and size it to obtain the minimum required delay.
5) Now M0 should be broken into N transistors, (M_{p1} to M_{pN}), in a binary fashion. That is

$$\left(\frac{W}{L}\right)_{M_{pi}} = \frac{2^{i-1}}{2^N - 1}\left(\frac{W}{L}\right)_{M_0} \tag{13}$$

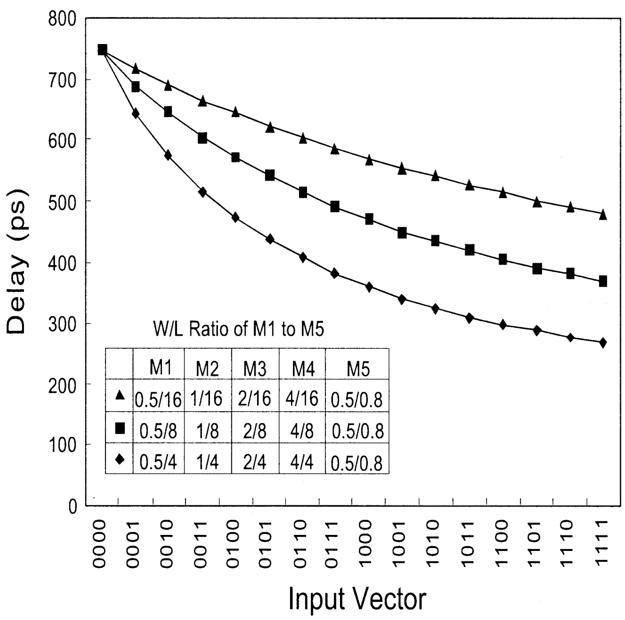
for $i = 1, 2, \ldots, N$.
6) The delay of the circuit for all the possible input vector combinations can be obtained from (10)–(12). If we need a higher resolution for the circuit delay, we should increase N and repeat steps 5) and 6) to reach the desired resolution.

V. COMPARISON OF THE THREE DELAY ELEMENTS

In order to compare the proposed delay element with the two other architectures discussed, we simulated these three delay elements. The W/L ratios of the transistors of all three circuits are chosen to get an approximately equal delay. Fig. 13 shows the output of the three different delay elements. In this figure, the rise time, delay time, and the average power consumption of the three delay elements are also shown. Another important performance parameter of a delay element is the effect of temperature



(a)



(b)

Fig. 12. The proposed circuit delay versus input vector for three different W/L ratios of pMOS transistors (M1–M5).

variations. The stability of a delay element is very important because in most applications we need a very precise and stable delay. We have simulated the three circuits in two different temperatures and the results are shown in Table II. As can be seen, the proposed circuit has the least sensitivity to temperature variations. This is because part of the variations in the characteristics of transistors M1 to M5 is cancelled out by the same variation in transistor M6 and M7.

The proposed delay element consumes substantially higher power compared to the other two architectures. Unlike previous architectures, the proposed circuit has the static power consumption. This circuit consumes a total power of 211 μW at 400 MHz. The static and dynamic power components constitute

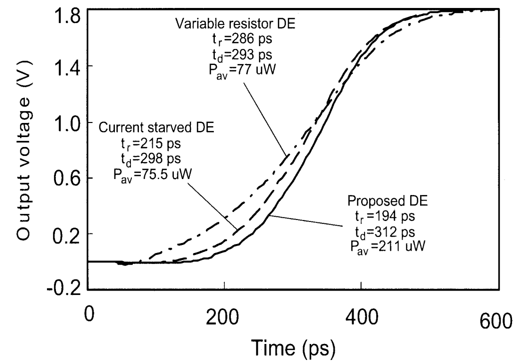


Fig. 13. The output of the three different delay elements.

TABLE II
EFFECT OF TEMPERATURE ON THE THREE DELAY ELEMENTS

	T=25 (°C)	T=75 (°C)	% of change
Current starved DE	298 (ps)	336 (ps)	12.8%
Variable resistor DE	293 (ps)	327 (ps)	11.6%
Proposed DE	312 (ps)	323 (ps)	3.5%

136 μW, and 75 μW, respectively. In many applications such as battery operated systems, this can be restrictive. However, with a clever design, the static component may be minimized. Furthermore, as the operational frequency increases, the static power consumption component becomes less important.

The proposed circuit exhibits some interesting characteristics. The static power consumption of the circuit can be optimized independent of its delay behavior. In order to reduce the static power, the current I in Fig. 9 must be reduced. This can be achieved by scaling down the W/L ratios of transistors M1 to M6. The key issue in such an exercise is to keep V_g constant. In order to examine the effectiveness of this method, we scaled down the W/L ratio of M1–M6 transistors by half. The resulting circuit was simulated and found to be consuming 112 μW of power while its delay remained unchanged. However, it should be mentioned that as the current I is reduced, it becomes more susceptible to interference. Therefore, there is a tradeoff between power consumption and noise immunity of the circuit.

VI. CONCLUSION

In this paper we proposed a new architecture for a digitally programmable delay element. The proposed circuit is compared with two other architectures. It is shown that the existing architectures make it difficult to find the optimal W/L ratios of the transistors and predict the input vector for a given delay. The proposed circuit is analyzed to find a mathematical formula for the output voltage and ultimately the circuit delay. Moreover, simple empirical equations for finding the delay of the circuit are investigated. These equations can determine the delay of the circuit with an error of less than 6%. The main advantage of the proposed delay element is that finding the input vector for a specific delay is straightforward compared to the two other DCDEs. Furthermore, the delay behavior is monotonic. The proposed DCDE also exhibits improved temperature sensitivity. This characteristic may be exploited in high-precision applications.

The proposed DCDE has some shortcomings. This circuit consumes finite amount of static power. However, this power component may be minimized with clever design techniques. For some applications, such as delay fault testing at low frequencies [9] this may be acceptable.

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