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A DIGITIZING AND MEMORY SYSTEM FOR WIRE SPARK CHAMBERS*

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Abstract

A new digitizing and memory system for use with magnetostrictive wire spark chambers is described. Features include a 1000 spark per event 20 MHz shift register memory and a live CRT display of spark positions. Our design experience with state-of-the-art MOS shift registers and Schottky TTL circuits is presented, together with comments on our experience with the working system. This principle has applications in many other situations requiring the digitization and storage of the arrival times of a burst of pulses.

Introduction

In a previous paper[1] a system was described which reduced the cost by approximately a factor of 10 and expanded the capabilities of wire spark chamber readout systems. This system replaced the conventional scaler system which required many individual scalers, one for each spark recorded, and instead used a single counter and an inexpensive 20 MHz memory to store individual spark arrival times and the identification codes. A completed system is currently in use and has the capability of storing 1028 sparks from 64 different magnetostrictive wands and in addition provides a real time CRT display of the stored spark information.

Summary

The system (Fig. 1) uses a set of multiplexed 5 MHz shift registers to form the memory element. This memory records the value of a single 20 MHz counter and a wand identification code whenever a spark signal is detected on one or more of the 64 inputs. Included in the system is a scheme for compacting the wand identification code, to reduce the size of each memory word, and a method for resolving the arrival and identification of coincident spark pulses.

Basically, the unit begins a read-in cycle with a master coincidence signal from the experiment. This signal resets all functions and starts the 20 MHz clock. As spark inputs arrive, the time counter and wand information are strobed into memory. The read-in of data is ended by the time counter overflow signal which sets the unit into an advance mode to transfer data in memory to the end of the registers for output. When the data reaches the end of the shift register memory it is read into the computer. Finally the CRT display is refreshed by recirculating the data through the memory while waiting for the next master coincidence signal.

Design

Design Evolution

The unit was laid out and constructed with an emphasis on functional design whereby a section could be built and tested separately as the components became available. Clearly the key to this system is the memory and therefore we decided to build the memory first on PC boards and then add input identification, the synchronous clock, control, test and refresh logic around this basic memory. The first design was based on 20 MHz ion implanted 1K MOS shift registers which did not require multiplexing. These shift registers, however, did not become available as expected and we were forced to multiplex the available 5 MHz shift registers. The fact that these INTEL 1102 shift registers were quad 256 bit units made them especially suitable for multiplexing to the 20 MHz rate. An extra bonus was that the Intel memory was about $1000 or 1/4 of the cost of the ion implanted memory.

The 15-bit 20 MHz synchronous counter presented some special problems. Simultaneously with our design of a counter using individual flip-flops and gates, T.I. and Signetics introduced 20 MHz MSI synchronous counters. We found that 4 Signetics 8284 units could be made to operate at 20 MHz and, by loading their output into latches, provide the required time reference. The advantage of these units is that the carry output of each stage is not ANDed with the clock signal thereby eliminating one extra gate delay. To compensate for propagation delay through 15 stages, the clock to the associated N8200N latches is delayed by approximately 25 ns from the synchronous counter and then further delayed to coincide with the latch output. This further delayed clock becomes the reference clock for the entire system since it is set to be in extremely close synchronization with the 15 bits of time information changing simultaneously "on the fly" at the latch outputs.

The wand input identification is encoded in order to reduce the amount of memory required. The scheme encodes the inputs within the 50 ns time period and has a provision for handling coincident arrival of pulses.

Approximately one year ago we selected a logic family which could accomplish the input priority decisions and do input encoding within the time restriction of 50 ns. At that time the only logic available to meet the requisite requirements was the well known emitter coupled logic (ECL). However, T.I. announced a limited family of Schottky TTL logic which would soon become available. Schottky TTL can be mixed with other TTL families and can directly drive memory without the need for level shifters and utilizes the same voltage power supplies. In addition, all inputs are diode-clamped, providing protection from negative voltage transients. We decided to order the Schottky logic and construct the unit while waiting for delivery. Finally, we solved the problems of ringing and excessively long delays in a couple of weeks after we got the system going.

The scope display was included in the system not only to provide a real time display of spark position but as a very necessary test provision.

Memory

The memory (Fig. 2) is composed of 4 parallel banks of 28 × 256-bit 5-MHz shift registers (INTEL 1402). The 4 parallel banks are required to achieve the 20 MHz rate needed to obtain sufficient resolution of spark position. The 5 MHz shift registers require about 200 ns to load, and, since the minimum interval between events is 50 ns, a buffer is required. The 30-bit latches serve this purpose — they are enabled in sequence by the spark detector. The first event will be loaded into latch A by the spark detector output which also advances a 2-bit counter steering the next load command to latch B, etc. Thus, each of the 4 memory banks receives 1/4 of the data and operates at a maximum 5 MHz rate while the entire memory

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operates at 20 MHz. The memory is driven by a 2 phase clock[2] and we found that the most reliable method was to change the phases simultaneously with a 40 ns delay to the clock going negative and the shortest possible delay to the clock going positive.

Input Encoding and Multiplexing

The input identification is loaded into memory in a 12-bit code composed of a coincidence bit, a 3-bit Mth address, and the 8 selected inputs. The 64 inputs are multiplexed into memory by 8 multiplexers having 8 inputs each. The probability of coincident pulses requires a priority encoder of the Mth address (Fig. 3). With the Schottky circuits the time from clocking the input latch (Fig. 4) to presenting the information to memory through the 8 gates is approximately 35 ns. The input latches directly turn on the associated or gate which drives the priority encoder and spark detector. The priority encoder through the inverter selects the Mth input of each multiplexer and provides the reset signal to the 8 latches selected. Obviously, a Schottky 8 input NAND circuit would drastically reduce the complexity and delay of this scheme. The coincidence circuit D13 and 14 is a simple digital comparator of the input and output of the priority encoder.

Since our PDP-9 computer is not fast enough to encode the selected 8 inputs to a 3-bit code, we were forced to encode at the memory output at a much slower rate during computer read-in. The basic method is the same as the encoding at the memory input but utilizes MSI logic.

Construction

The mechanical layout (Fig. 5) utilizes vertical doors and wire wrap technology providing an easy construction scheme and meeting our requirement of fast and reliable operation. The advantages of wire-wrap were its relatively high density, needed for the high clock rate (20 MHz) as well as the number of I.C.'s used (approximately 208) (Fig. 6), its automatic wiring capability, and the ease with which wiring can be changed, which is essential to a one-of-a-kind unit of this size. The large number of interconnections warranted the use of semiautomatic wiring. The cost including wire lists and software charges was about equivalent to that of a technician hand wrapping from a schematic. Error rate is, however, much lower and should more than one unit be built the cost would drop dramatically since wire-list and software charges are only one time charges.

In retrospect it seems that the physical and electrical layout of the unit was generally good. The mounting of all components on hinged vertical panels has made it a very convenient unit to work on and trouble shoot. The layout of the logic circuitry could have probably been improved, however, by the use of larger (160 socket) wire-wrap IC socket boards. This would have eliminated the mounting and aligning of the smaller boards and would also have allowed all circuitry to be wired as a unit. (About a third of the total wiring was between the three logic panels and had to be done by hand.) Also, more care in placement of individual IC's and the making up of wire-lists would have saved some time in tracking down excessive delays due to long wiring paths. These paths gave trouble both in excessive delay (up to 6 ns) and in excessive ringing of the line. Shortening the line as much as possible, plus terminating it at the load end with a 150 Ω pullup resistor (and at times a 150 Ω to ground) and when long lines could not be avoided (over 6") using a twisted pair seemed to cure most of the ringing and excessive delay problems.

Wand Instrumentation

With the type of system described it is necessary to measure the center of the pulse to accurately determine the input arrival time. The wand amplifier (Fig. 7) drives a zero crossing discriminator (Fig. 8) which provides a 75 ns pulse to set the associated wand latch at a time representing the center. The first stage of the wand amplifier is a video amplifier which drives the second stage line driver. The first stage of the zero crossing discriminator is a precision rectifier discriminator. The second stage differentiates this signal and the differential comparator triggers on the one-shot output.

The amplifier has a noise level of about 25 millivolts with a 175 turn coil and maximum gain of about 3600 including the auto transformer. The zero crossing discriminator has a 25 millivolt cut off and slews approximately 75 ns from 50 mV to 2 V.

System Operation

The block diagram is shown in Fig. 9. The system is started by a pulse from the spark chamber trigger system which starts the 20 MHz counter and enables the spark detector output. Each event is stored in the memory and advances the spark counter. This process continues until the 20 MHz counter overflows.

The overflow (carry signal from the 20 MHz counter) disables the counter, blocks the path from the spark detector to the 10-bit spark counters, transfers the reading of the spark counter to its associated 10-bit latch, and allows the 20 MHz clock to directly advance the spark counter and shift registers. The spark counter and shift register continue advancing until the spark counter overflows, which stops the advance pulses and turns off the busy signal. Since the spark counter overflows on the 1028th pulse and the shift register memory is 1024 + 4 latch words long, the first event stored is now at the output end of the memory regardless of the actual number of sparks recorded. The number of sparks recorded is still held in the spark counter latch. The readout process now begins.

The computer under program control may read the 10-bit spark latch or sense the end transfer signal to determine the number of sparks recorded. In our present computer setup we sense the end transfer (DONE) signal since read-in is by DMA operation. Because the computer is limited by memory the program sets up a maximum word count and either this overflow or the end transfer pulse interrupts the computer, signalling that the event has been transferred under ready/sync operation. The system actually has 5 major states after an event signal. FF1 is set, causing a one clock reset blast pulse followed by the record flip-flop 2 on. New time (position) and address spark information is loaded into memory until the 15-bit synchronous counter overflows. Then this new information is advanced to the memory output by the advance flip-flop 3 setting computer flip-flop 4 which allows the data to be recirculated and read into the computer. The data is read in first as a 15-bit time byte followed by a byte of 6 bits of address and the coincidence bit. After computer read-in the data is recirculated by flip-flop 5 to refresh the x-y display scope. The time data drives the scope in the x direction and the address data in y forming the 64 rows of spark information. Since the time information is 15 bits we provide front panel switches (Fig. 5) to provide the option of selecting any 10-bit segment. In addition a test pattern may be selected by the 64 wand switches and inserted into memory at a time selected by the time switches.

The clock operates at 20 MHz during the record period but is slowed to 1.25 MHz during advance and computer read-in. Refresh is at 250 kHz to allow the DAC's and scope to settle and still provide flicker free operation.

Conclusion

The system speed is limited by the memory, synchronous counter and encoder. In the near future Schottky circuits having MSI and LSI functions should simplify the design and allow for more inputs. The price of the memory has recently dropped to $270 making the cost of this system insignificant when compared to the cost of the chambers themselves.

References

1. R. G. Friday, D.W.G.S. Leith, K. D. Mauro, and B. Richter, Nucl. Instr. and Methods 93, 237-24 (1971).

2. Gordon B. Hoffman, Texas Instrument Application Report CA-114.

Figure Captions

FIG. 1--Simplified block diagram.

FIG. 2--Memory.

FIG. 3--Input priority encoder.

FIG. 4--8 input multiplexer.

FIG. 5--Front panel.

FIG. 6--IC layout.

FIG. 7--Wand amplifier. a) Schematic
b) Photograph c) Output

FIG. 8--Zero crossing detector.

FIG. 9--Overall system.

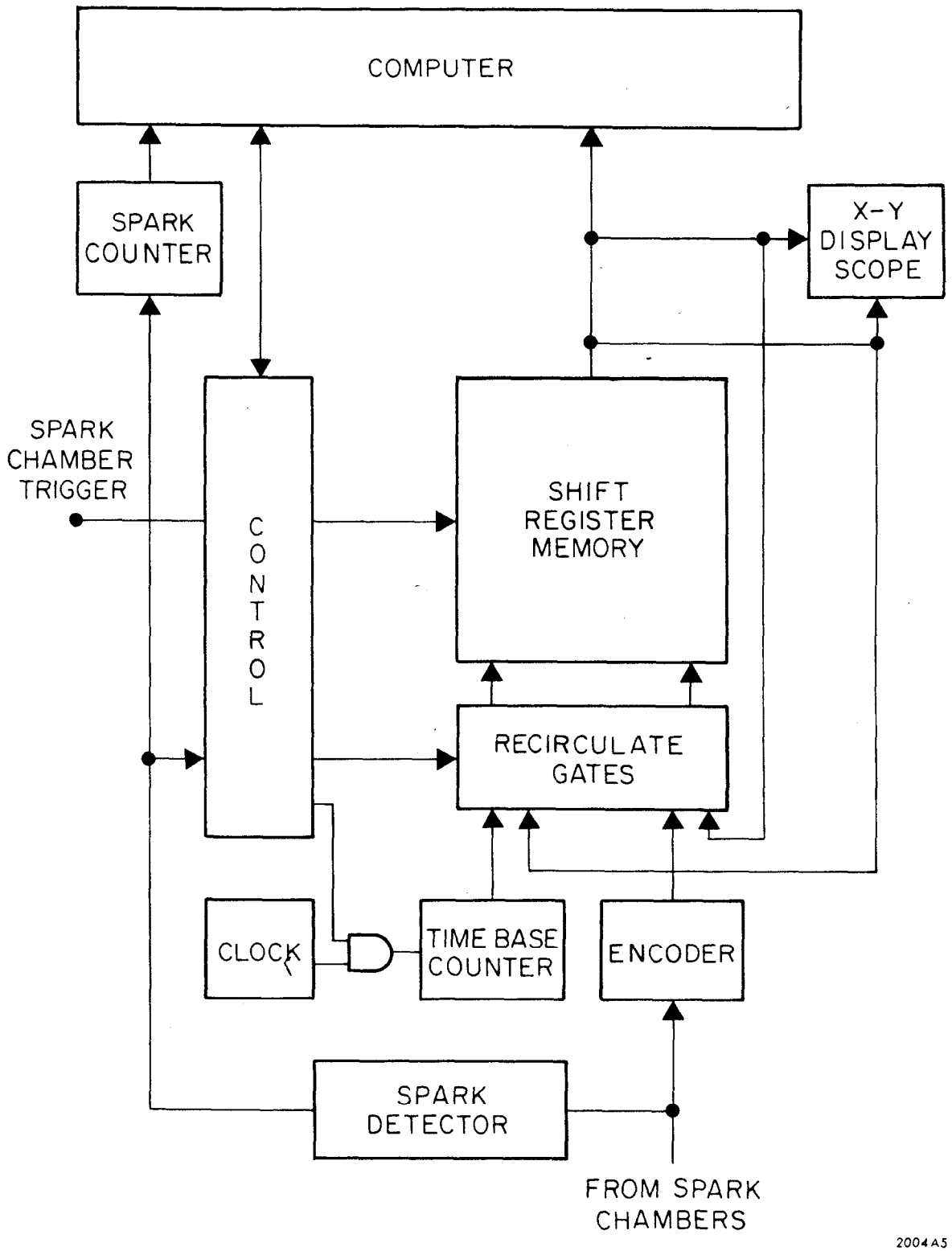

COMPUTER
SPARK COUNTER
X-Y DISPLAY SCOPE
SPARK CHAMBER TRIGGER
CONTROL
SHIFT REGISTER MEMORY
RECIRCULATE GATES
CLOCK
TIME BASE COUNTER
ENCODER
SPARK DETECTOR
FROM SPARK CHAMBERS
2004A5

Fig 1

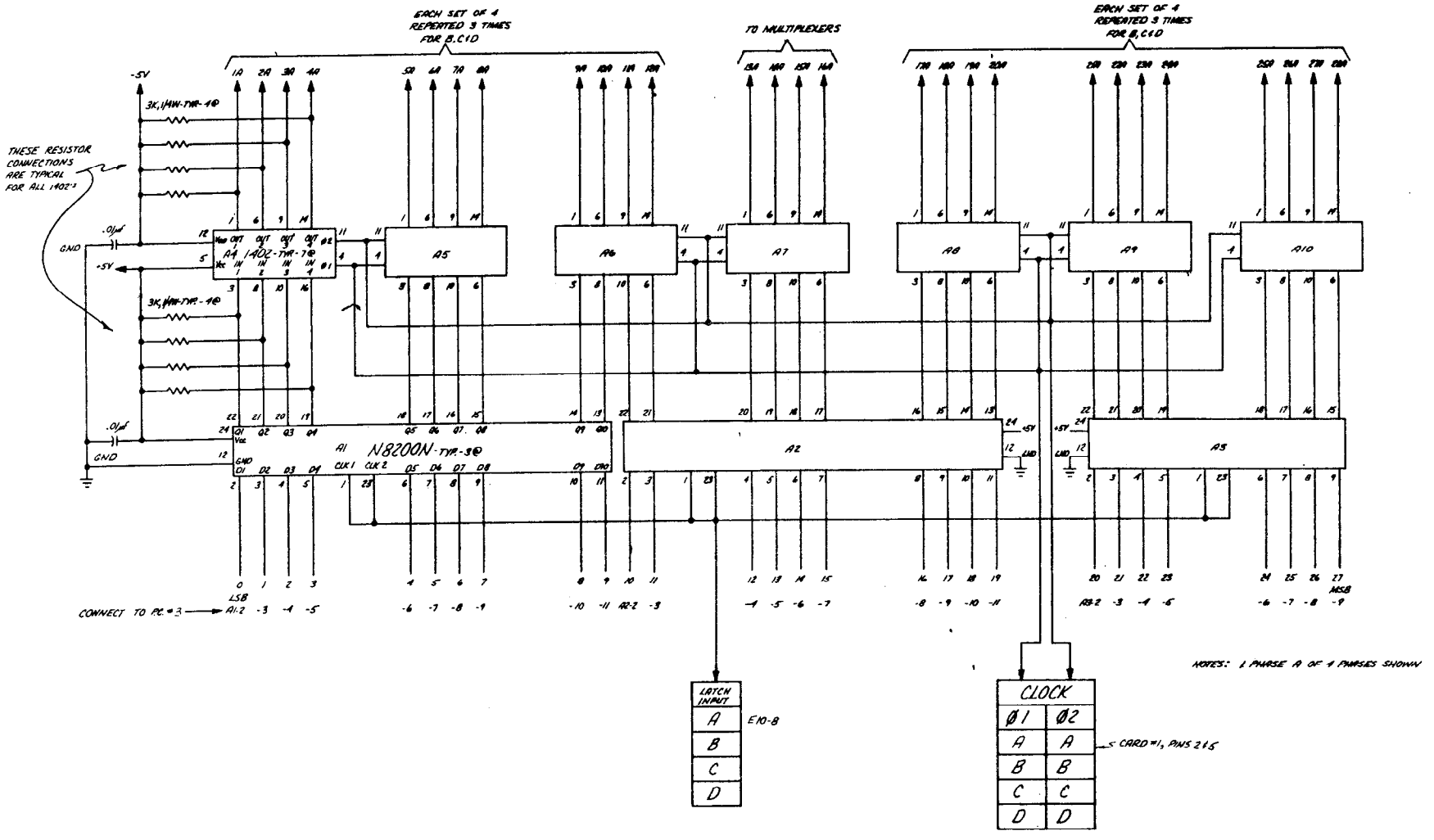
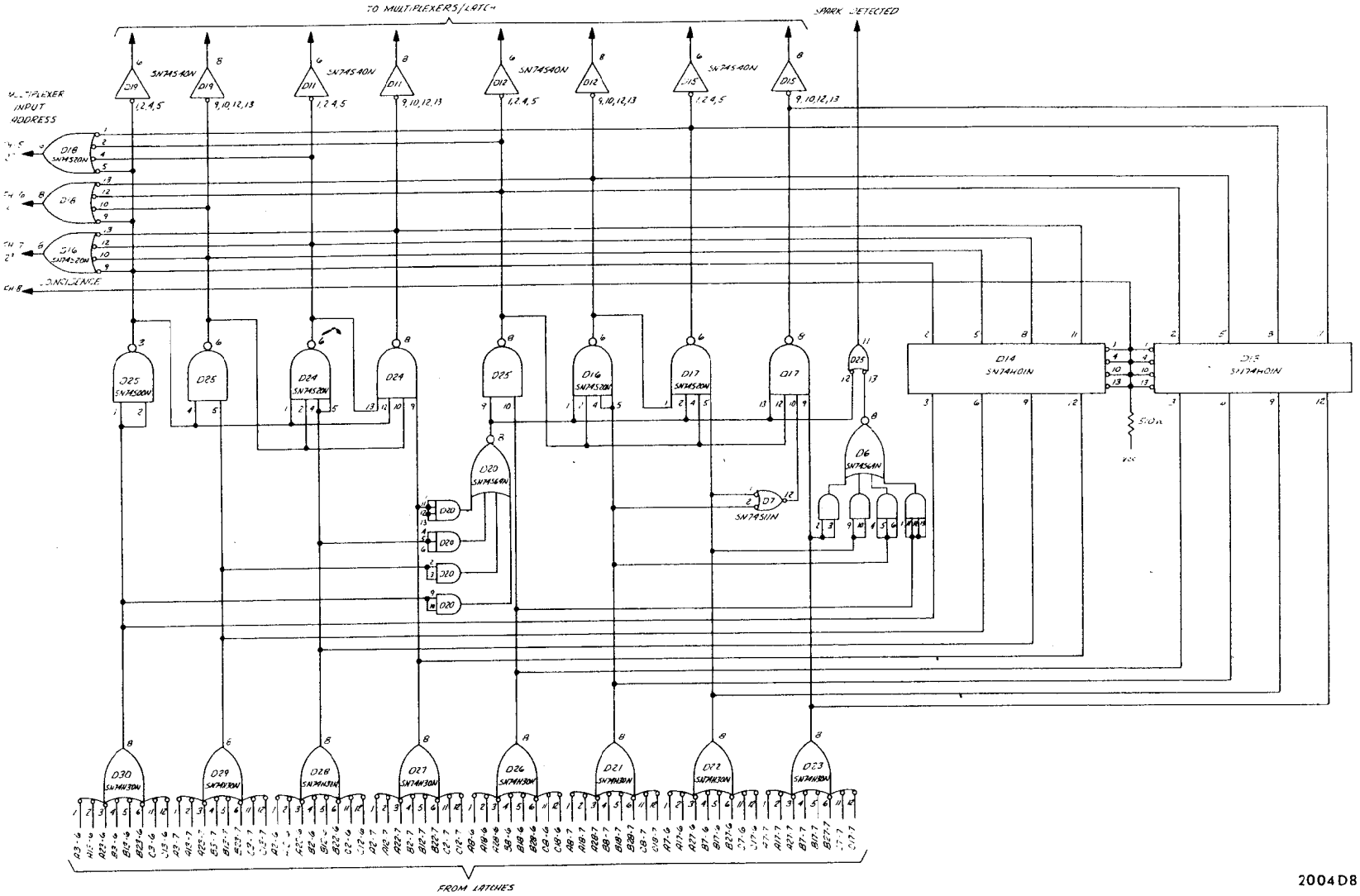

EACH SET OF 4 REPEATED 3 TIMES FOR B,C1D
TO MULTIPLEXERS
EACH SET OF 4 REPEATED 3 TIMES FOR B,C&D
-5V
3K, 1/4W-TYP-4Ø
THESE RESISTOR CONNECTIONS ARE TYPICAL FOR ALL 1402's
.01µf
GND
+5V
A4 1402-TYP-7Ø
A1 N8200N-TYP-3Ø
A5
A6
A7
A8
A9
A10
A2
A3
CONNECT TO PC #3
AI:2 -3 -4 -5
LSB
MSB
LATCH INPUT
A
B
C
D
E10-8
CLOCK
Ø1
Ø2
= CARD #1, PINS 2 & 5
NOTES: 1 PHASE A OF 4 PHASES SHOWN
P.C. #2
2004D11

Fig. 2


TO MULTIPLEXERS/LATCH
SPARK DETECTED
MULTIPLEXER INPUT ADDRESS
SN74S40N
SN74S20N
SN74S00N
SN74H30N
SN74H01N
SN74S11N
SN74S64N
5.0n
Vcc
COINCIDENCE
FROM LATCHES

2004D8

Fig. 3

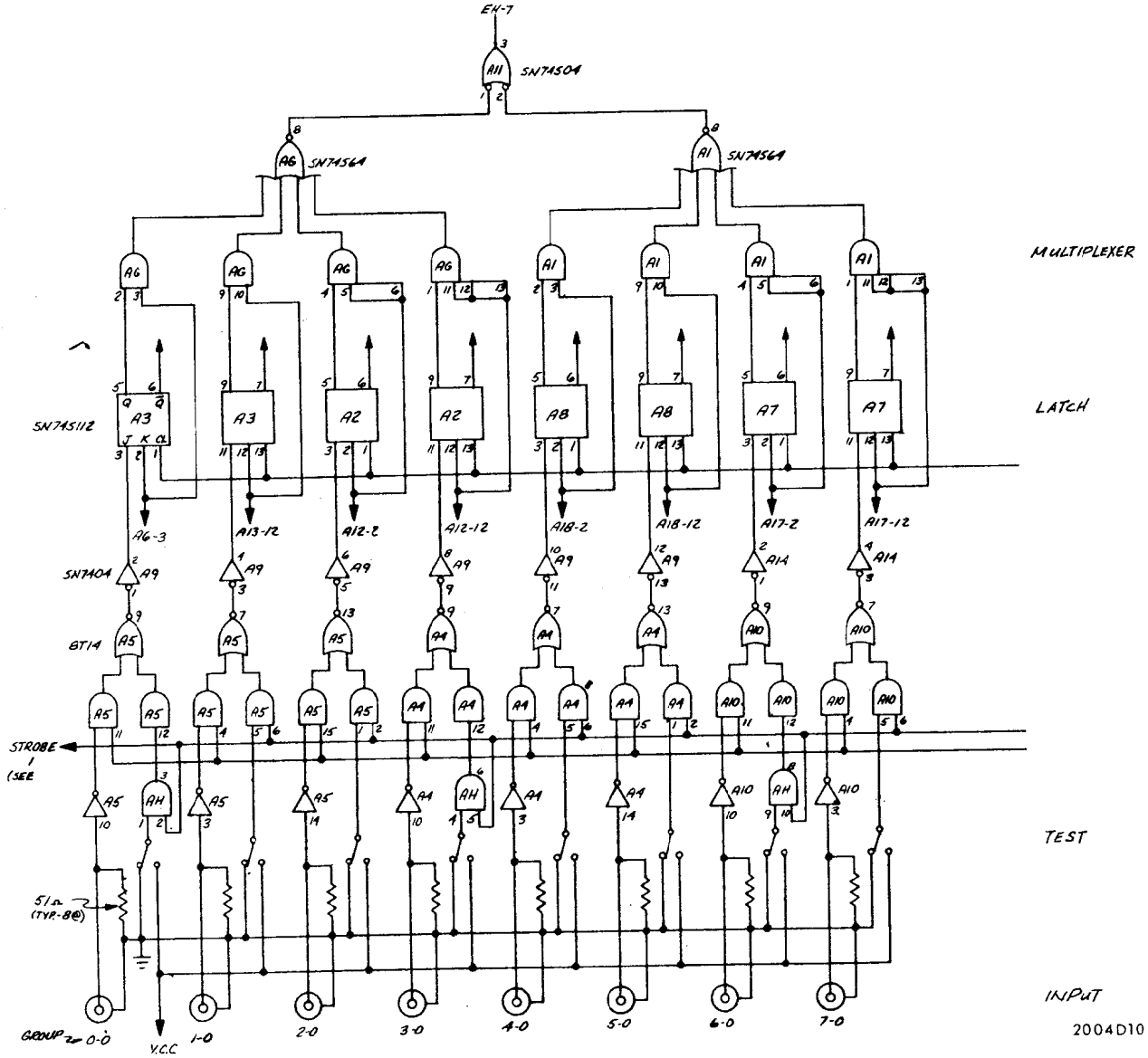

EN-7
A11 SN74S04
A6 SN74S64
A1 SN74S64
MULTIPLEXER
LATCH
SN74S112
A3
A2
A8
A7
A6-3
A13-12
A12-2
A12-12
A18-2
A18-12
A17-2
A17-12
SN7404
A9
A14
GT14
A5
A4
A10
STROBE
(SEE
A5
AH
A4
A9
A10
5 Ω
(TYP-8Ø)
TEST
INPUT
GROUP 0-0
Y.C.C
1-0
2-0
3-0
4-0
5-0
6-0
7-0
2004D10

Fig. 4

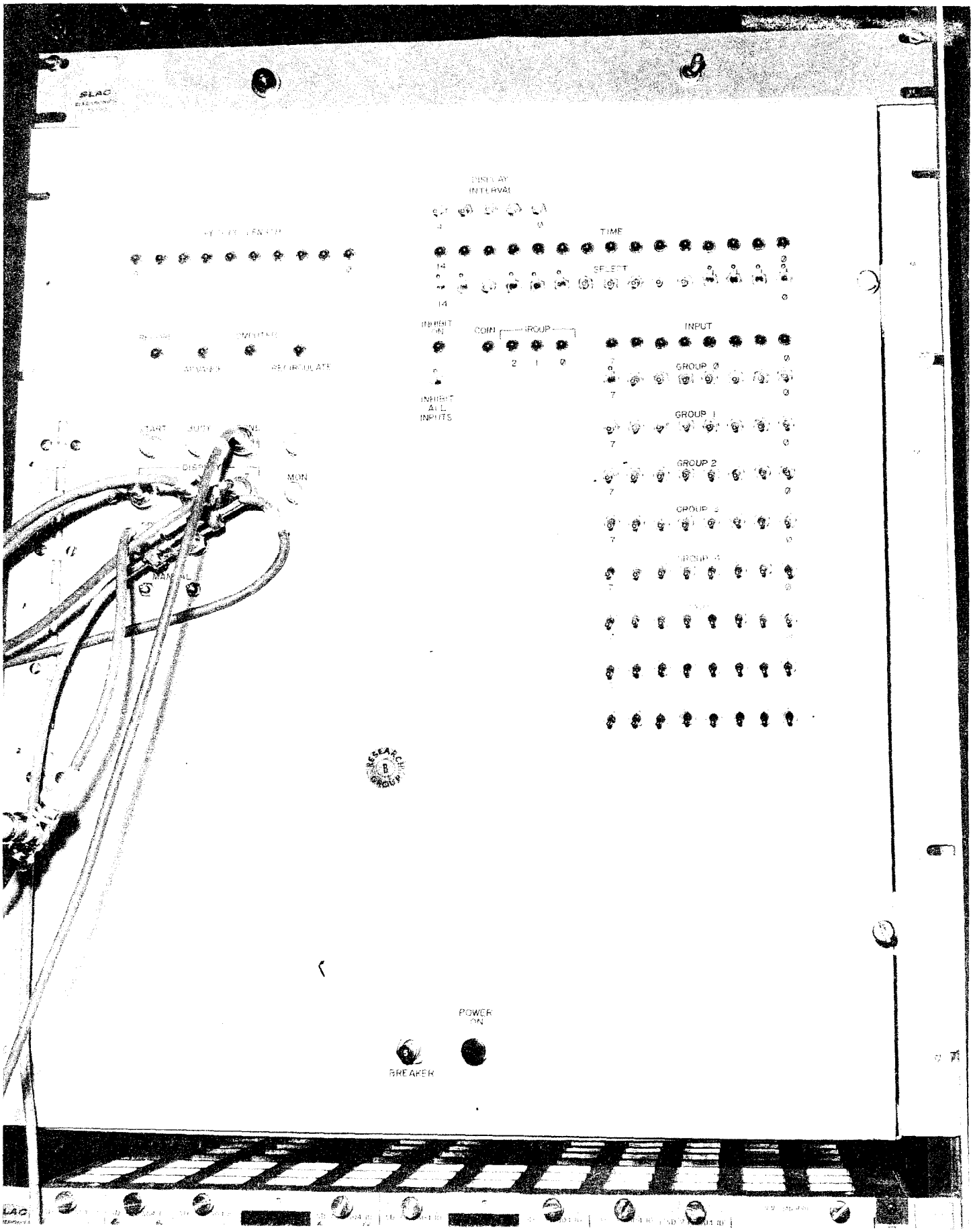
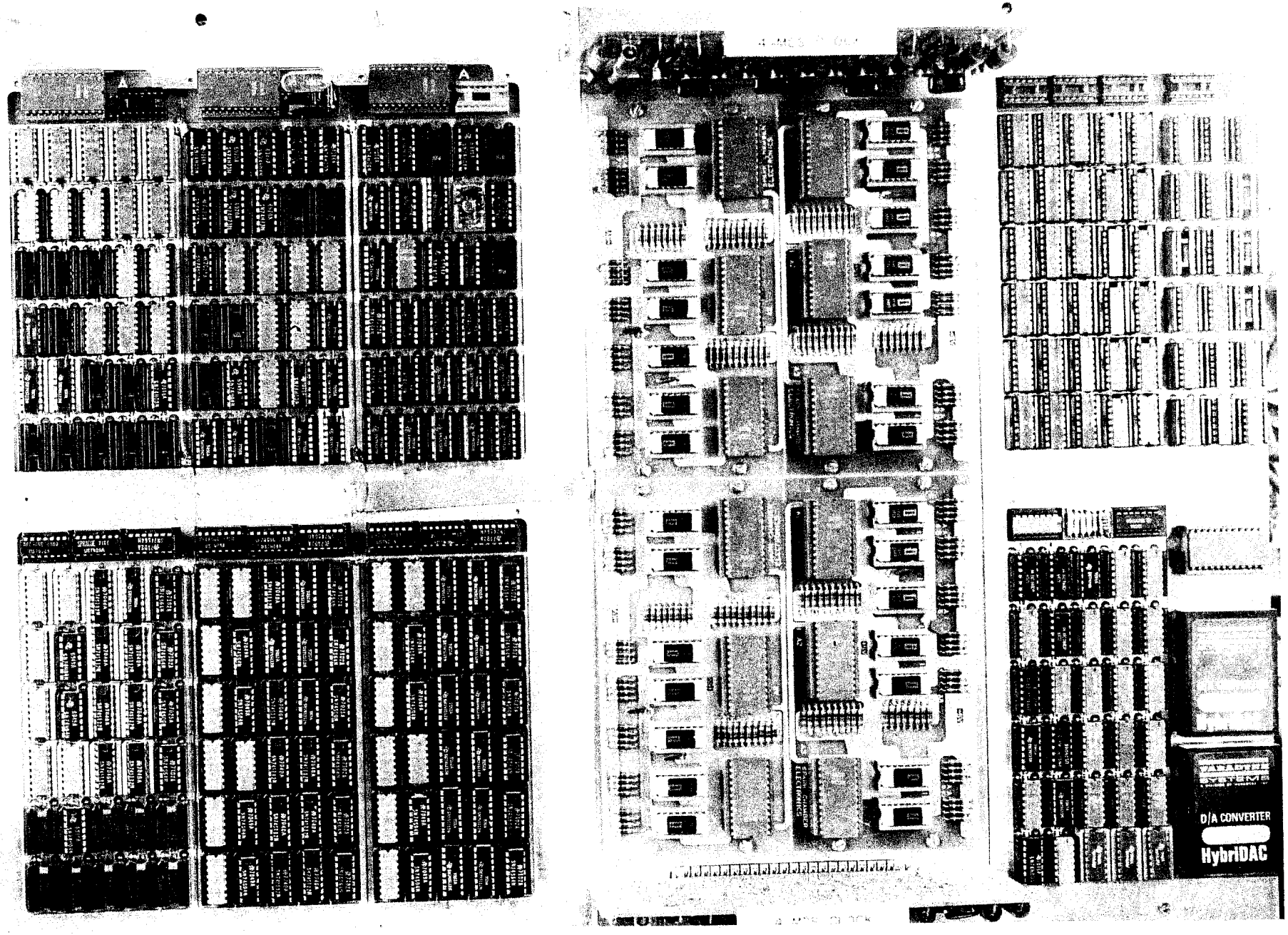

DISPLAY INTERVAL
TIME
SELECT
INPUT
GROUP
COIN
INHIBIT IN
INHIBIT ALL INPUTS
GROUP Ø
GROUP 1
GROUP 2
RECIRCULATE
MON
POWER ON
BREAKER

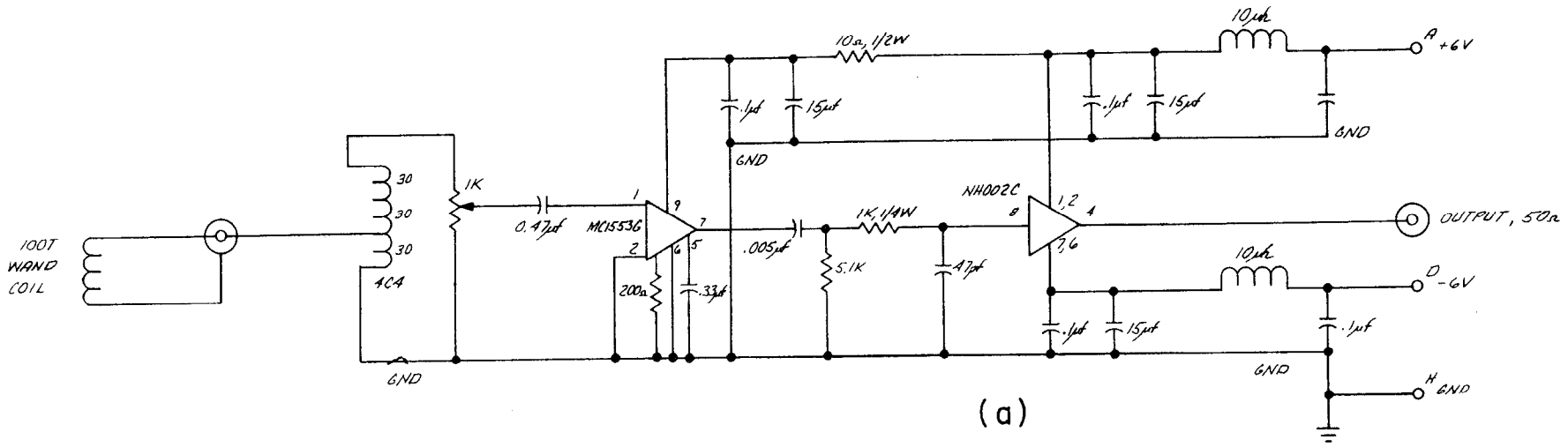
Fig. 5

2004A6

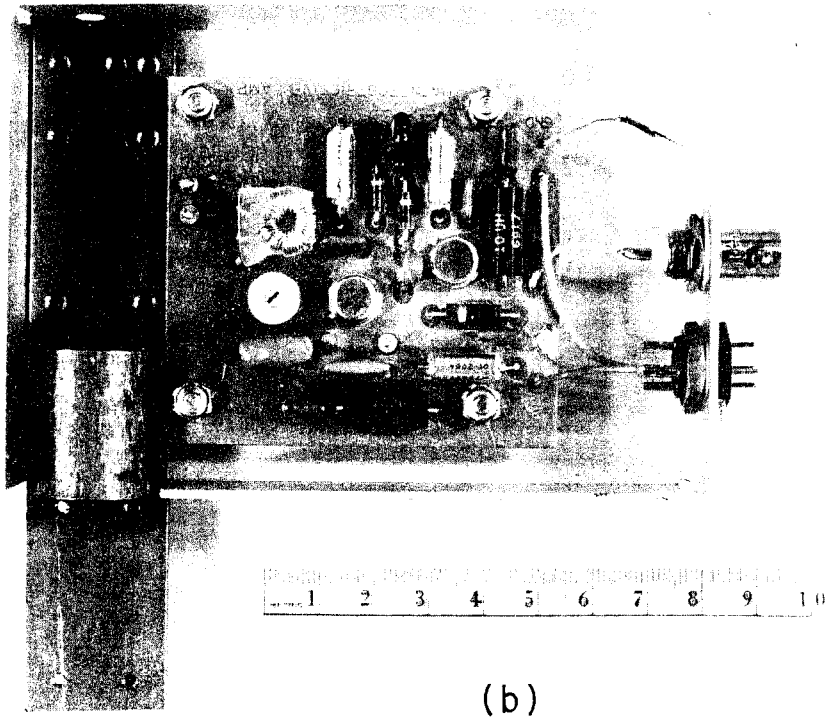


2004A7

Fig. 6



(a)



(b)

(c)

2004D3

Fig. 7

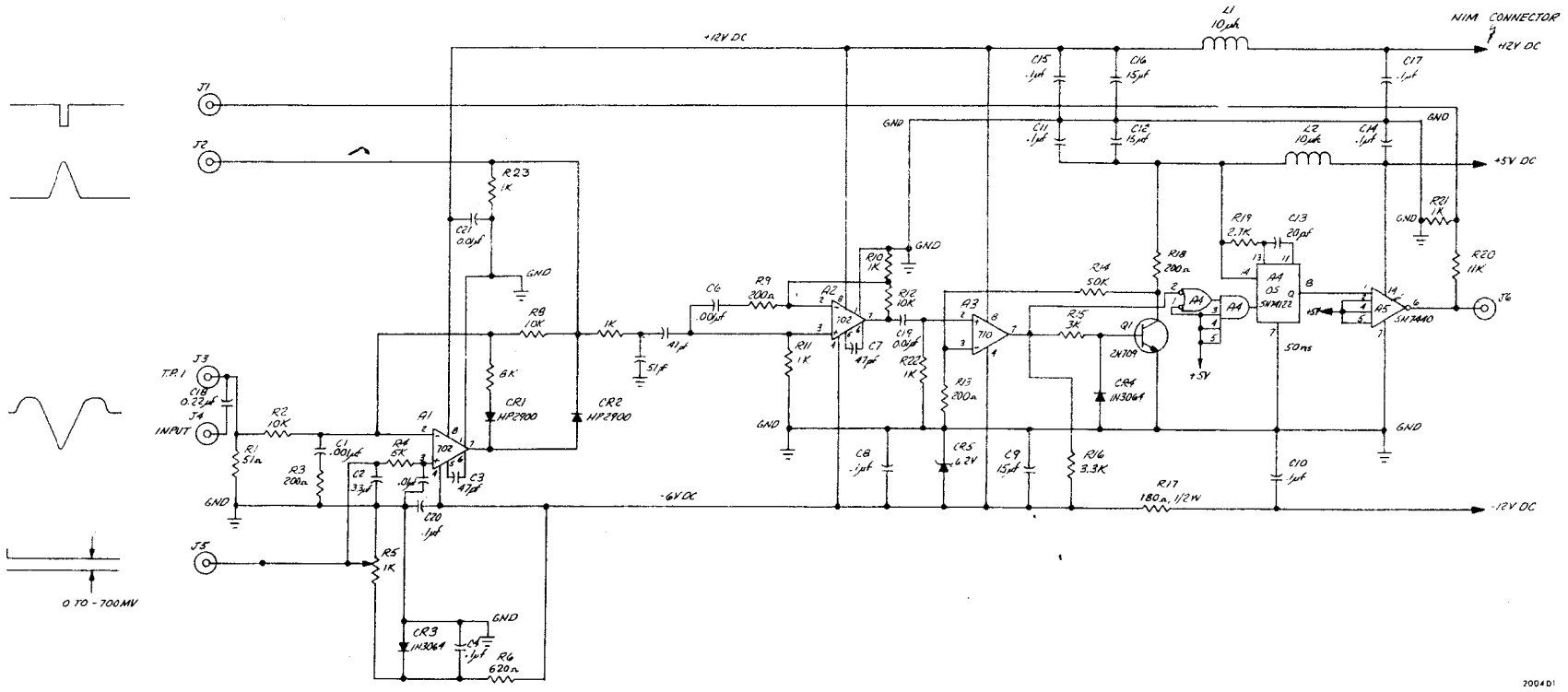

+12V DC
NIM CONNECTOR
+12V DC
L1
10μh
C15
.1μf
C16
15μf
C17
.1μf
GND
C11
.1μf
C12
15μf
L2
10μh
C14
.1μf
GND
+5V DC
J1
J2
R23
1K
C21
0.01μf
GND
R8
10K
1K
A1μf
51μf
C6
.001μf
R9
200Ω
A2
102
R10
1K
GND
R12
10K
C7
47μf
C19
0.01μf
R22
1K
A3
710
R14
50K
R18
200Ω
R15
3K
Q1
2N709
+5V
CR4
1N3064
R19
2.7K
C13
20pf
AA
OS
SN74122
50ns
AA
AS
SN7440
R21
1K
R20
11K
J6
GND
J3
T.P.1
C18
0.22μf
J4
INPUT
R2
10K
A1
102
8K
CR1
HP2900
CR2
HP2900
R1
51Ω
C1
.001μf
R4
5K
R3
200Ω
C2
33pf
.01μf
C3
47pf
GND
-6V DC
R13
200Ω
CR5
6.2V
C8
.1μf
C9
15μf
R16
3.3K
R17
180Ω, 1/2W
C10
.1μf
-12V DC
C20
.1μf
J5
R5
1K
0 TO -700MV
CR3
1N3064
C4
.1μf
R6
620Ω
2004D1

Fig. 8

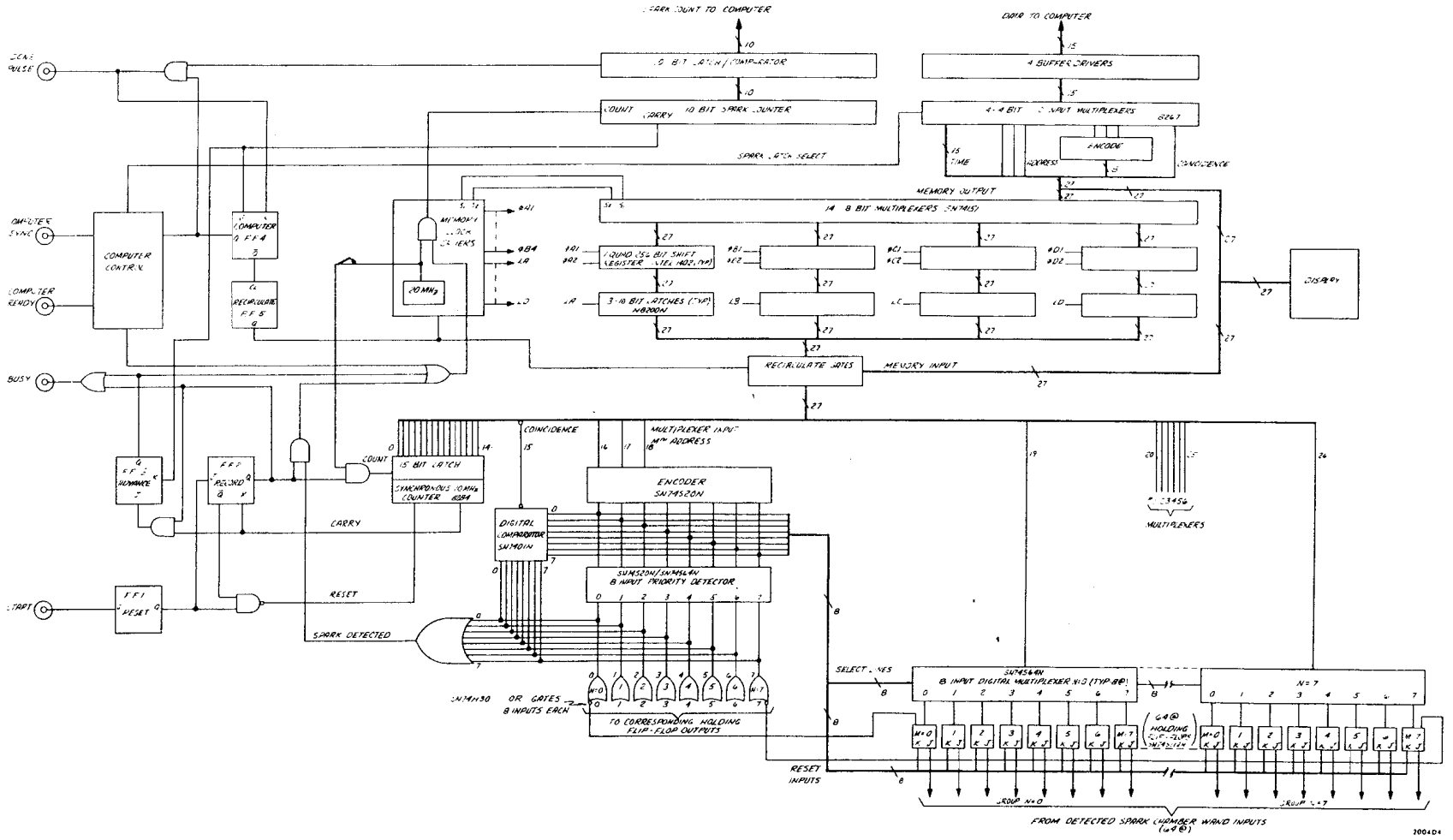

SPARK COUNT TO COMPUTER
DATA TO COMPUTER
10 BIT SPARK COUNTER
4 BUFFER DRIVERS
4-4 BIT 2 INPUT MULTIPLEXERS
ENCODE
MEMORY OUTPUT
14 8 BIT MULTIPLEXERS (SN74151)
QUAD 256 BIT SHIFT REGISTER
3-10 BIT LATCHES (TYP)
RECIRCULATE GATES
MEMORY INPUT
DISPLAY
COMPUTER CONTROL
COMPUTER SYNC
COMPUTER READY
BUSY
START
COMPUTER R.F.F.
RECIRCULATE F.F.
MEMORY CLOCK DRIVERS
10 MHz
F.F. 2 MONITOR
F.F. RECORD
15 BIT LATCH
SYNCHRONOUS 10 MHz COUNTER
COINCIDENCE
MULTIPLEXER INPUT M BIT ADDRESS
ENCODER SN74520N
DIGITAL COMPARATOR SN7401N
SN74520N/SN74S64N 8 INPUT PRIORITY DETECTOR
CARRY
RESET
SPARK DETECTED
SN74H30 OR GATES 8 INPUTS EACH
TO CORRESPONDING HOLDING FLIP-FLOP OUTPUTS
SELECT LINES
SN74S64N 8 INPUT DIGITAL MULTIPLEXER N=0 (TYP 8P)
N=7
MULTIPLEXERS
RESET INPUTS
GROUP N=0
GROUP N=7
FROM DETECTED SPARK CHAMBER WAND INPUTS (64)
2004D4

Fig. 9