A 1GHz Direct Digital Frequency Synthesizer Based on the Quasi-Linear Interpolation Method

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***Abstract*—The paper presents a novel architecture for a direct digital frequency synthesizer (DDFS) based on the Quasi-Linear interpolation (QLIP) method. The four-segment QLIP is utilized to realize a DDFS with a spurious free dynamic range (SFDR) of 63.2dBc. The DDFS chip featuring a 5-stage pipeline is implemented in TSMC 0.13μm technology. The chip occupies 9874μm^2, consumes 8.2μW/MHz, and runs at 1GHz clock rate.**

I. INTRODUCTION

Direct digital frequency synthesizers (DDFS) play a very important role in modern digital communication systems. They are essential parts in Spread Spectrums such as Bluetooth devices and Radars due to their high speed frequency hopping capability, fine frequency resolution, and very short settling times. The main challenge in their design is reducing their chip area and power consumption as well as increasing their clock frequency.

In a DDFS, the amplitude of a sinusoidal signal is digitally generated by the phase-to-sine mapper (PSM) [1]. Fig. 1 shows the structure of a basic DDFS. The input of the accumulator and its wordlength determine the output frequency and its resolution, respectively. The frequency of the output sinusoidal signal is

$$f_{out} = \frac{F_r}{2^L} f_{clk}, \qquad (1)$$

where, F_r, L and f_{clk} are the input of the accumulator, the accumulator wordlength, and the clock frequency, respectively [1].

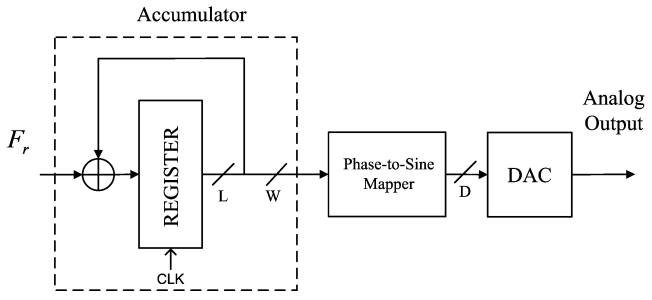

Fig. 1. Block diagram of a basic DDFS.

The accumulator and the PSM occupy most of the DDFS chip area. Unlike the PSM, the accumulator has a very simple structure and it cannot be optimized significantly. Therefore, to achieve a high performance DDFS, the PSM should be optimized. Originally, a ROM look-up table was used as a PSM, but this method results in a very large chip with high power consumption [1].

Two approaches, phase truncation and wave symmetry, are commonly used in all DDFS architectures to reduce the complexity of the PSM. The output of the accumulator is truncated from L to W bits. This truncation can decrease the overall wordlength of the PSM parameters, and consequently reduce the chip area. The quarter wave symmetry of the sinusoidal signal allows us to evaluate only the first quadrant of the sinusoid in the PSM, whereas the other quadrants can be generated from the first one. In addition to the aforementioned techniques, several other methods are proposed to simplify the complexity of the PSM [1]. These methods can be categorized into two fundamental groups, the phase rotation and the polynomial interpolation methods.

In this paper, we present a new DDFS architecture based on the Quasi-Linear interpolation (QLIP) method, which was introduced in [3], to create a single-output high-speed DDFS with the SFDR of 63.2dBc. The DDFS chip is implemented using TSMC-0.18μm technology with 1.2-V supply.

The rest of the paper is organized as follows. Section II gives a short description of the QLIP method. Section III presents the proposed DDFS design, while Section IV describes the chip implementation. Section V gives a short comparison of the proposed design and its implementation with recent state-of-the-art designs from the open literature. Section VI concludes the paper.

II. THE QLIP METHOD

The sequence created by varying the input of the PSM from 0 to $2^W - 1$ is called the signature sequence [2]. This sequence along with the phase-truncated wordlength W, determines the overall spurious free dynamic range (SFDR) of the output. Therefore, knowing the SFDR of the signature sequence is crucial to find the overall SFDR and spur locations of any DDFS output [2].

In the QLIP method the first quadrant of the cosine signal

$$f(x)=\cos\left(\frac{\pi}{2}x\right), \qquad 0\le x\le 1 \tag{2}$$

is divided into $s=2^u$ (u is an integer number) segments and each segment is approximated by either an even quadratic polynomial or a linear polynomial according to

$$P_k(x)=\begin{cases} c_0^{(k)}+c_2^{(k)}x^2 & 1\le k\le\theta \\ c_0^{(k)}+c_1^{(k)}x & \theta+1\le k\le s \end{cases} \qquad 0\le x\le 1, \tag{3}$$

where k is the segment number and $c_0^{(k)}$, $c_1^{(k)}$ and $c_2^{(k)}$ are the polynomial's coefficients and θ is the location in the first quadrant where the even quadratic polynomial is replaced by a linear polynomial. In [3], it has been shown that the SFDR is maximized when

$$\theta=\frac{3s}{4}. \tag{4}$$

Fig. 2 illustrates the QLIP technique. The theoretical upper bounds of the QLIP method are evaluated in [4]. For example, the theoretical upper bound for $s=4$ is 66.64dBc and for $s=8$ is 79.08dBc. Thus, any attempt to find an appropriate digital implementation has to be made to achieve a SFDR as close as possible to the theoretical SFDR upper bounds.

III. DDFS DESIGN

Since the QLIP method is very similar to the linear interpolation method, we can modify the architecture introduced in [5] to implement the QLIP method. The proposed design is illustrated in Fig. 4. In order to realize the quadratic polynomials we add a squarer to the original design described in [5]. The output of the squarer has twice the wordlength of its input and it needs to be truncated for the following stages. However, it is more beneficial to partially truncate the input of the squarer, thus reducing logic complexity. Therefore, the input wordlength of the squarer ($W-2$) is reduced by λ and the entire squarer's partial product table is truncated such that its output has the same wordlength as its input, i.e., $W-2$. To consider the error of this truncation in the waveform evaluation, the effect of truncation should be taken into account in the final optimization. To further simplify the squarer, the merger squarer architecture is employed [6].

The quantization of the coefficients is performed in two different ways. The coefficients $c_1^{(k)}$ and $c_2^{(k)}$ are determined by approximating their ideal values with a summation of integer powers of two

$$c_i^{(k)}=\sum_{j=0}^{r}h_{jk}2^{g_{jk}},\ h_{jk}\in\{+1,-1\}, \tag{5}$$

where r is the number of terms, h_{jk} is the sign of each term, and g_{jk} and i are defined as follows

$$g_{jk}\in\{\cdots,-2,-1,0,+1,+2,\cdots\} \tag{6}$$

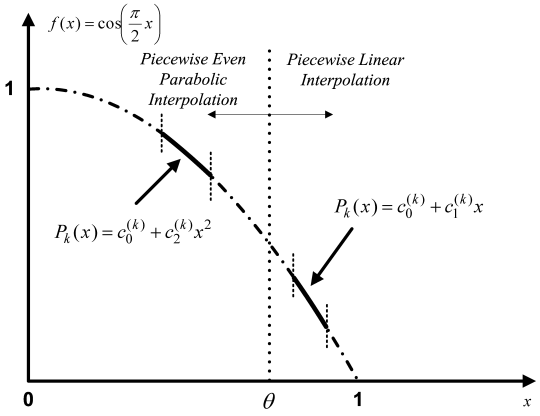

Fig. 2. The QLIP method

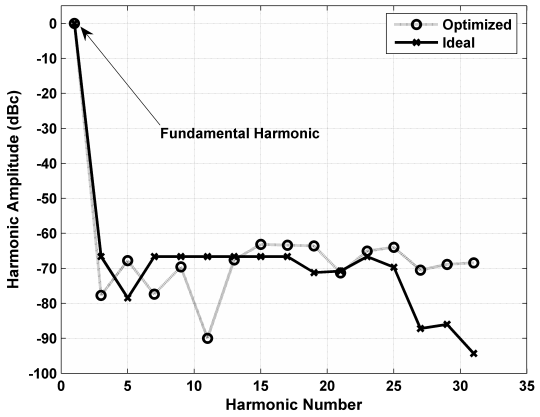

Fig. 3. The signature sequence spectrum of the optimized and the ideal four-segment QLIP DDFS.

Table 1. The parameters of a QLIP DDFS for s=4, W=11, D=10, r=2, and λ=3.

	$k=1$	$k=2$	$k=3$	$k=4$
g_{0k}	0	0	0	0
g_{1k}	2	3	5	1
g_{2k}	10	6	8	6
q_k	504	498	483	778

$$i=\frac{\mathrm{sgn}(3s/4-k)+3}{2}. \tag{7}$$

The ideal values of $c_1^{(k)}$ and $c_2^{(k)}$ are evaluated in the algorithm that gives the SFDR upper bound [4]. This method obviates the multiplier, which would have been needed to perform the product of x and x^2 with $c_1^{(k)}$ and $c_2^{(k)}$, respectively, as described in (3). For the targeted DDFS (QLIP with $s=4$), the chosen value of r is 2. The other coefficients $c_0^{(k)}$ should be determined using an integer optimization algorithm. The quantized version of the $c_0^{(k)}$ coefficients obtained for the SFDR upper bound case, can be

used as the initial value for the optimization algorithm. Table 1 shows the optimized parameters for the four-segment QLIP DDFS with $W=11$, $D=10$ (output wordlength), $r=2$ and $\lambda=3$. The coefficients q_k are the optimized integer coefficients corresponding to $c_0^{(k)}$. It is worth mentioning that the parameters g_{0k} are always zero because the coefficients $c_1^{(k)}$ and $c_2^{(k)}$ are always greater than one.

The parameters are obtained using the nonlinear Nelder-Mead optimization method. The optimized SFDR obtained for this DDFS is 63.2dBc that is the closest possible SFDR to the upper bound of 66.64dBc for the given architecture. The spectrum of the signature sequence of the optimized DDFS is compared with the signature sequence of the ideal DDFS providing the SFDR upper bound in Fig. 3.

Fig. 4 shows the overall block diagram of the proposed DDFS. The MUX's are employed to avoid using a multiplier. This is done by logical shifts to the right or left of the squarer output (for the quadratic terms) and the phase variable (for the linear terms), and then performing addition of all the shifted terms. The sign of the terms h_{jk} are implemented by negating the corresponding terms. This causes a slight distortion in the output signal. To avoid this distortion, the effect of the logical negation has been considered in finding the optimized coefficients q_k.

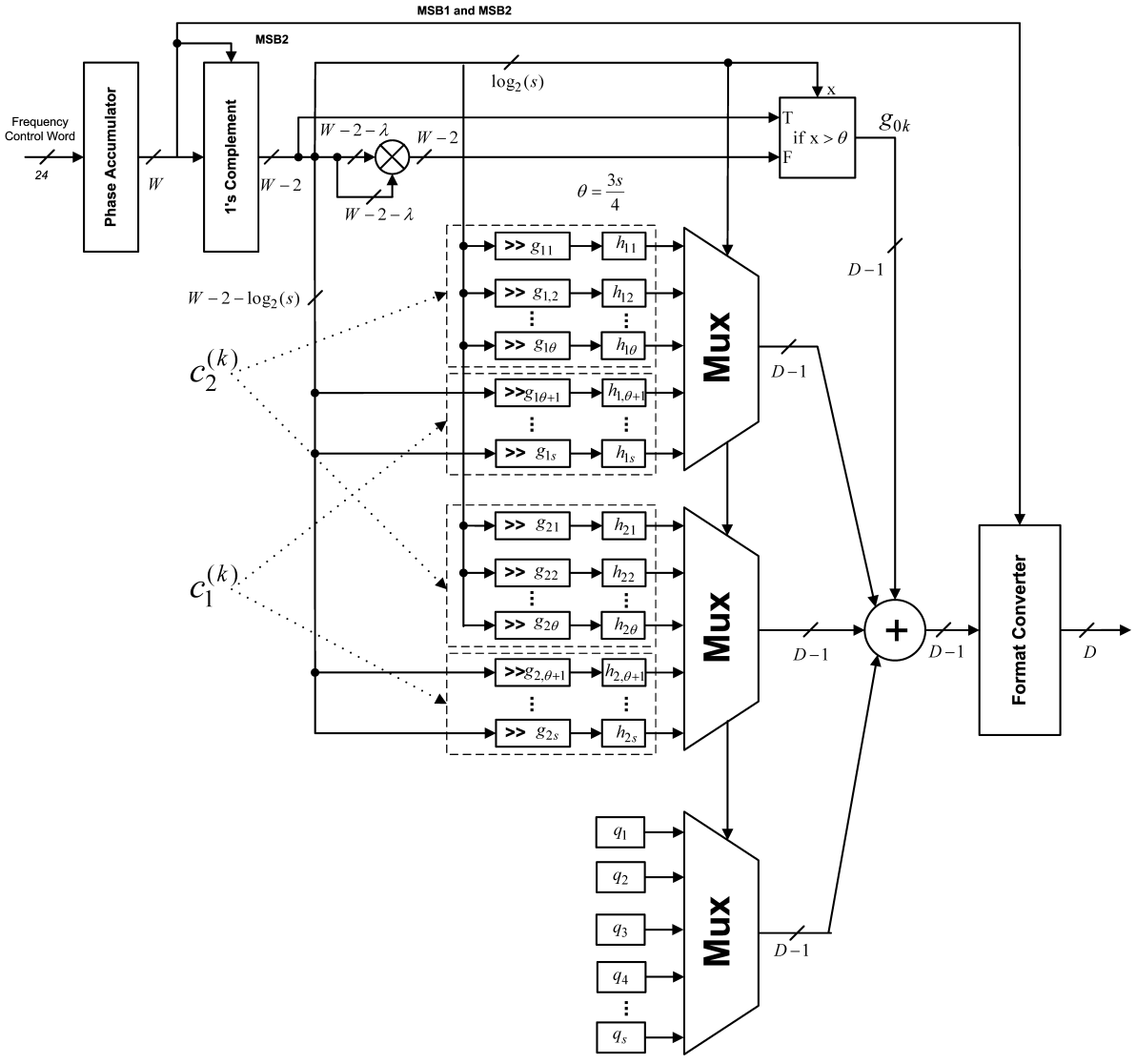

Fig. 4. The block diagram of the proposed architecture for the QLIP method for $r=2$.

IV. IMPLEMENTATION

The proposed DDFS is implemented using TSMC-0.13µm, 1.2V supply standard cell library. Four pipeline registers are inserted to increase the clock frequency. The design is modeled by Verilog RTL and then synthesized by Cadence PKS tool. The place and route procedure is also performed by Cadence Encounter SOCE tool. The core size of the chip is 9874µm^2 comprising of 964 cells. The maximum clock frequency of the chip is 1GHz and its average power consumption is 8.2µW/MHz. The average power consumption of the chip core is obtained by applying a randomly changing frequency control word (F_r) to the chip.

V. COMPARISON WITH RECENT DESIGNS

A fair comparison of performance for various DDFS implementations is a challenging task. Several parameters are involved in designing a digital VLSI chip such as a DDFS. Software tools for logic synthesis, cell placement and routing utilize a wide variety of algorithms, mathematical and heuristic methods. Each of these algorithms, by no means, can be considered as the best. Moreover, different design approaches make the comparison even more difficult. For example, optimizing the design for maximum clock frequency or maximum SFDR could cause a significant increase in the chip area and its power consumption. Therefore, the comparison should be made between the designs having similar characteristics i.e., close SFDR values, accumulator and output wordlengths. In addition to similar characteristics, the employed manufacturing technology can significantly affect several parameters such as power and chip area. Thus, this factor should also be considered in a fair comparison.

Table 2 presents a comparison between the chip simulated in this paper and three other DDFS chips recently reported in the literature [7], [8], [9]. The table shows that the proposed design in this paper outperforms the other three.

Table 2. Performance Comparisons

Design	SFDR (dBc)	Input Wordlength (L)	Pipeline Registers	Area (µm^2)	Power (µW/MHz)	Process ((µm)	Mac. Clock (MHz)
This paper	63.2	24	4	9874	8.2	0.13	1000
[7]	60	16	0	11000	12.5	0.18	25
[8]	62.3	24	0	16800	39.3	0.25	224
[9]	60.7	N/A	1	115000	112	0.35	106

VI. CONCLUSIONS

A novel DDFS design based on the four-segment QLIP method is reported in this paper. The proposed design has the SFDR of 63.2dBc. The design is implemented using TSMC-0.13µm, 1.2V technology. A maximum clock frequency of 1GHz is achieved. The chip power consumption and area are 8.2µW/MHz and 9874µm^2, respectively. The performance comparison between the proposed and three recently reported DDFS chips shows significant improvement in all features.

VII. REFERENCES

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