A Discrete-Time Battery Model for High-Level Power Estimation

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Abstract

In this paper, we introduce a discrete-time model for the complete power supply sub-system that closely approximates the behavior of its circuit-level (i.e., HSpice), continuous-time counterpart. The model is abstract and efficient enough to enable event-driven simulation of digital systems described at a very high level of abstraction and that include, among their components, also the power supply. Therefore, it can be successfully used for the purpose of battery life-time estimation during design optimization, as shown by the results we have collected on a meaningful case study. Experiments prove also that the accuracy of our model is very close to that provided by the corresponding Spice-level model.

1 Introduction

During the development of a low-power system, the attention of designers is focused on the minimization of the power dissipated by the circuitry that performs the required computations. Accurate and efficient power models for digital circuits at various levels of abstraction have been developed to support design space exploration [1]. Unfortunately, much less attention has been dedicated to power supply models. In many cases, it is implicitly assumed that the power supply provides a constant voltage and delivers a fixed amount of energy. This assumption is not valid in the case of battery-operated devices.

Even though power dissipation is a primary concern in the design of portable electronic devices, top-level specifications are not given in terms of maximum average power (or energy), but rather in terms of *minimum battery life-time*. Furthermore, the portability requirement imposes tight constraints on maximum battery weight. These are the reasons why successful portable applications combine low-power design techniques with careful battery selection and power supply design.

As observed in [2, 3], a battery is not an ideal, finite-charge power supply. The energy stored in a fully-charged battery cannot be supplied to the digital circuitry to its full extent, and the usable energy cannot be supplied at a constant rate. This is because the amount of energy a battery can provide depends on the current drawn from the battery itself: The higher the discharge current, the higher the energy waste of the battery [4, 2]. Design and optimization of digital circuits in portable systems demands a careful understanding of battery behavior. Furthermore, accurate simulation models for battery and DC-DC conversion circuitry are required to properly tune the various design and optimization steps during system development.

Circuit-level, continuous-time battery models [4, 5, 6, 7] have been developed to help designers estimating the discharge characteristics of common batteries, much before such characteristics can be measured by connecting the actual battery to a system prototype. Unfortunately, such models require load models at the same abstraction level. Obviously, modeling the entire system loading a battery at the circuit level is a challenging task. Furthermore, circuit-level simulation of a system over the typical life-time of a battery would require an enormous amount of time.

On the other hand, battery-conscious power metrics [2, 3] suffer two major limitations. First, they relate battery life-time to the average current absorbed by active circuits. However, life-time of actual batteries does not depend only on average current, but also on the characteristics of the time-domain current waveform [9, 10]. Second, they neglect the presence of voltage conversion circuits which can be responsible for a significant fraction of the total power.

In this paper, we propose a discrete-time, VHDL model of a battery that approximates the continuous-time behavior but, at the same time, is fast and efficient enough to enable high-level, event-driven simulation of a complete system description. Therefore, it can be used for the purpose of battery life-time estimation of systems described at a very high level of abstraction. We first illustrate the continuous-time battery and DC-DC converter models used as a reference for evaluating the accuracy of our VHDL model. Then, we describe the corresponding discrete-time models, that constitute the main contribution of this paper; in fact, to the best of our knowledge, no similar work has been proposed in the literature up to now. We describe experiments proving the accuracy and efficiency of the proposed models, and we show their usefulness in the context of power optimization of battery-operated applications.

2 Continuous-Time Power Supply Model

Several circuit-level battery models have been proposed in the past [4, 5, 6, 7]. In this section, we identify the key features of such models that need to be reproduced in a discrete-time setting to achieve accurate life-time estimation. Notice that the actual physical capacity of any group of cells may vary as much as 20% between identical units, due to manufacturing variances [5]. Therefore, only those phenomena that exhibit changes greater than this quantity must be modeled. We also briefly describe the principle of operation and introduce a modeling technique for DC-DC converters, which are the main components of the power distribution circuitry in portable systems.

2.1 Battery

Charge storage in a battery can be modeled as a capacitor with capacitance $C = 3600 \cdot CAP$, where CAP is the nominal capacity in *Ahr*, which is usually provided in the battery's data-sheet. By setting the initial voltage across the capacitor $V_C = 1$, we initialize the battery to its fully charged state. Unfortunately, the simple linear capacitor model is not accurate enough to model complex phenomena observed during battery discharge. In fact, the following three major effects must be taken into account:

- *Battery voltage has non-linear dependence on its state of charge (SOC)*: Voltage V_{in} decreases monotonically as the battery is discharged, but the rate of decrease is not constant.
- *The actual usable capacity of a battery cell depends on the discharge rate*: At higher rates, the cell is less efficient at converting its chemically stored energy into available electrical energy.
- *The "frequency" of the discharge current affects the total amount of charge the battery can deliver*: The battery does not react instantaneously to load changes, but it shows considerable inertia, caused by the large time constants that characterize electro-chemical phenomena.

These effects can be modeled at the circuit level as shown in Figure 1.

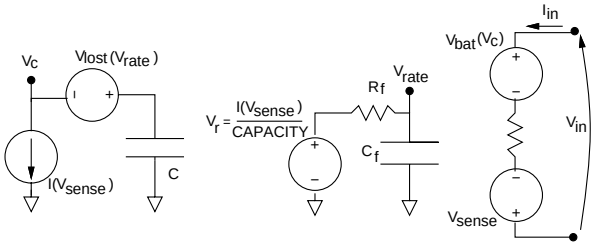

Figure 1: Continuous-Time Battery Model.

Dependency on the SOC is taken into consideration by storing several points of the curve in a look-up table (LUT) addressed by the value of the state of charge (V_C). The model is accurate up to a minimum *cut-off voltage*, after which the battery is considered fully discharged.

Dependency on discharge rate is modeled with a voltage source V_{lost} in series with the charge storage capacitor. Voltage V_{lost} reduces the apparent charge of the battery (which controls output voltage). The value of V_{lost} is a non-linear function of the discharge rate (which can be modeled by another LUT).

Dependency on the discharge frequency is modeled by averaging the discharge rate used to control V_{lost} through a low-pass filter (R_f, C_f).

According to [5, 7], this model fits measured data fairly well (within 15%). This accuracy is acceptable, since the actual capacity of any group of cells may vary as much as 20% between identical units, when we take into account manufacturing variances [5].

2.2 DC-DC Converter

The output voltage of a battery depends on its chemistry and its state of charge. During operation, battery voltage is not well controlled. Thus, the battery cell cannot be connected directly to active circuits, but it requires the presence of a *DC-DC converter* for shifting and stabilizing the voltage supply. The most common DC-DC converter circuits for battery-operated devices are *switching converters* [8]. A basic switching down-converter known as *buck converter* [8], is shown in Figure 2.

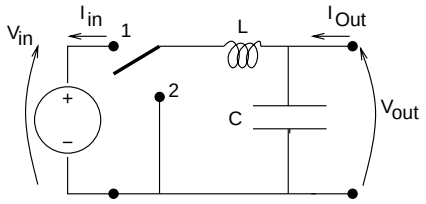

Figure 2: DC-DC Buck Converter Structure.

A single-pole, double-throw switch is alternatively connected to the DC input voltage and to ground. The switch output is connected to a LC low-pass filter. If the switch position is changed periodically, at a frequency f much larger than $1/2\pi\sqrt{LC}$ and with duty cycle $D \leq 1$, the output voltage of the converter is nominally $V_{out} = DV_{in}$; therefore, voltage down-conversion is performed. It is important to note that the buck converter is only one of the many switching converter topologies described in the literature. We focus on a specific topology for the sake of explanation, although our high-level model can be used for generic switching converters.

All real-life DC-DC converters have sizable losses, usually collapsed in a single figure of merit, called *efficiency*: $\eta = P_{out}/P_{in}$. Typical efficiencies are within the range $[0.8, 0.9]$. For a given fixed output voltage value V_{out}, we can represent η as a non-linear function $\eta(V_{in}, I_{out})$. Efficiency curves are usually plotted in the data-sheets of commercial DC-DC converters.

We can envision three classes of circuit-level DC-DC converter models, namely, transistor-level, behavioral white-box and behavioral black-box. Conversely from the others, black-box behavioral models do not contain information on the internal structure of converters, but they just mimic their I/O characteristics. They can thus be simulated very efficiently, all information on internal high-frequency switching being abstracted away. Also, they can be inferred directly from data-sheet information and do not require disclosure of the internal structure of the converters. For these reasons, we adopted the black-box model. It consists of a two-port circuit; the output port is connected to the load, and it appears as a voltage source with fixed V_{out} and small output impedance. The input port is connected to the battery and it appears as a current sink. The input current has the following expression:

$$I_{in} = \frac{V_{out} I_{out}}{\eta(V_{in}, I_{out}) V_{in}} \quad (1)$$

which is obtained directly from the definition of efficiency.

3 Discrete-Time Power Supply Model

This section describes a discrete-time power supply model that can be easily implemented within any system-level design environment. For the sake of concreteness, we will assume that system-level simulation is performed in VHDL. Hence, VHDL is the language of choice for the implementation of our abstract model.

3.1 Battery

The battery is defined as a VHDL entity. Its interface has one input, I_{in}, representing the current absorbed by the DC-DC converter, and one output, V_{in}, representing the voltage supplied by the cell to the DC-DC converter (see Figure 1). Both signals have analog values. A specialized resolved type has been defined for current signals, with the purpose of allowing multiple current loads connected to the same current signal. The resolution function simply sums over all currents.

The internal structure is based on the circuit-level model of Figure 1, and consists of two concurrent, communicating processes. The first one computes the value of node V_C in Figure 1, the instantaneous state of charge of the battery (taking into account losses due to high discharge rate). The second process computes the value of V_{lost}, i.e., it implements the low-pass filter shown in Figure 1. The output voltage of the battery, V_{in}, is a function of V_C. It is implemented in VHDL with a continuous assignment: $V_{in} = F(V_C)$, where F is realized by a LUT with linear interpolation.

The main challenge in the implementation of the voltage update processes is caused by the fact that they model voltages which are changing in a continuous fashion over time, thus some form of discretization is required to simulate them in an event-driven setting. To address this challenge, we implemented an autonomous source of events that generates events at a fixed frequency. The state of charge V_C and the value of V_{rate} are updated when the autonomous source generates an event. The update rule is obtained by integrating the differential equations of the continuous-time model on the update period. Notice that, in our case, the differential equations governing the evolution of V_C and V_{rate} over time can be integrated exactly. The differential equation for V_C, with fixed $V_{lost}(V_{rate})$ and $I(V_{sense})$ is:

$$C\frac{d(V_C + V_{lost}(V_{rate}))}{dt} = -I(V_{sense}) \qquad (2)$$

which has the solution $V_C(t) = V_C(0) - I(V_{sense})t/C$. The differential equation for V_{rate} with fixed V_r is:

$$V_r = V_{rate} + C_f R_f \frac{dV_{rate}}{dt} \qquad (3)$$

which can be integrated in closed form, giving $V_{rate}(t) = (V_{rate}(0) - V_r(0))e^{-t/R_f C_f} + V_r(0)$. Given a Δt corresponding to the cycle time of our autonomous event source, we can compute the new value of V_{rate} and V_{lost} by simply replacing $t = K \cdot \Delta t$ in the closed-form solution of the two differential equations (K is the number of cycles elapsed from time 0).

One last complication arises if we observe that the two equations are not mutually independent, and that both depend on $I(V_{sense})$. To solve this problem, whenever $I(V_{sense})$ changes, counter K is reset to 0, and new integration constants are computed for the two differential equations. The value of $V_{rate}(0)$ is known because the voltage across a capacitor must be a continuous function. Consequently, the value of $V_C(0)$ is known as well. In other words, the battery model reacts to an event on I_{in} by resetting time increments and re-computing the boundary conditions in the solutions of the differential equations. After the change, the voltage update rule is re-established for both V_C and V_{rate}. Note that the functional dependence of V_C from V_{rate} imposes the re-evaluation of V_C even when V_{rate} changes. The voltage update period can be set based on the time constant of the battery's low-pass filter $\tau = R_f C_f$ (for real-life batteries this interval is in the order of one second). Hence, a $\Delta t = \tau/5$ is sufficient to model the transient behavior of node V_{rate} in response to changes of I_{in}. The number of events can be further reduced by observing that we do not need to generate events for modeling the transient behavior of V_{rate} if there are no new events on I_{in} and the time after the last I_{in} event is $t \geq 4\tau$. In this case, V_{rate} has reached its asymptotic value, and does not need to be updated. The value of V_C must still be updated periodically, but the time constant for this update is in the order of a few tens of seconds (C has a large value). We implemented a variable frequency source of voltage update events that automatically reduces update frequency when V_{rate} transients are exhausted.

3.2 DC-DC Converter

The DC-DC converter is modeled as a VHDL entity with two input ports, I_{out} (coming from the load) and V_{in} (coming from the battery), and one output port I_{in} (connected to the battery). There is no V_{out} port, because the output voltage is kept constant by the DC-DC converter. The value of I_{in} is computed with Equation 1. Efficiency η is a function of both V_{in} and I_{out}. Its value is obtained by table look-up and linear interpolation. The computation of I_{out} is stateless and it is implemented in VHDL as a continuous signal assignment with zero delay. The interaction between DC-DC converter and the battery is based on pairs of V_{in}, I_{in} events. Whenever a new V_{in} event is generated by the battery, the DC-DC converter responds with an I_{in} event with zero delay. The generation of zero-delay event loops is avoided because V_{in} cannot change in zero time in response to a I_{in} variation (remember that V_{in} is a function of voltages across capacitors that cannot change in zero time). A new I_{in} event is also generated in response to an I_{out} event: By doing this, changes on the load are propagated to the battery.

In summary, the models for battery and DC-DC converter have limited complexity; in addition, they generate a small number of events over a battery life-time (a few events per second, in the worst case). Therefore, they are well-suited for interfacing with system-level descriptions at any level of abstraction without sizable simulation overhead.

4 Model Validation

In this section we present data concerning the validation of the discrete-time model. For the experiments we consider Lithium-Ion batteries, since they have a dominant position as the chemistry of choice for notebook and laptop computers. The main reason for this fact is that Li-Ion batteries have the best volumetric energy density (as well as the best gravitometric energy density) among all competing cells. In simple terms, Li-Ion batteries provide more energy than other cells for a given volume (or weight). On the other hand, they have higher cost than traditional secondary batteries like Nickel-Cadmium, because their fabrication technology is still quite expensive and not fully optimized. High performance and high cost have limited the market expansion of Li-Ion batteries to high-end products, where energy drain is high and high capacity is required to obtain acceptable life-time with reasonable weight.

Safety of Li-Ion batteries is an additional issue. If Li-Ion cells are over-charged, they may be damaged, leak, or even explode. Hence, smart battery chargers are required, thereby further increasing ownership costs. Li-Ion battery producers are steadily improving their technologies, both by cell chemistry optimization and by embedding low-cost electronic controllers within the battery package, in order to reduce the external support needed for operating the battery safely. Currently, Li-Ion batteries are expanding their market dominance in the portable computer arena, and thanks to lower production costs, they are also extending their competitiveness to low-end products.

To show how closely the discrete-time model is able to track the continuous-time one we have simulated both models under various conditions, corresponding to a set of different output loads, characterized by different maximum currents and time-domain behaviors. More specifically, we have considered a total of 10 types of current load stimuli:

- CC: Constant loads of magnitude 0.1, 0.2, and $1.0A$.
- SW: Square waves with 50% duty-cycle, average value of $1.0A$, and current levels of $(1.1A, 0.9A)$, $(1.3A, 0.7A)$, and $(1.8A, 0.2A)$.
- $STEP$: Periodic waveform with 6 different levels of current loads (average value $1.083A$).
- SP: Pulses with durations 1, 5, and $20s$.

Table 1 reports the results of the simulations. For each type of load, we give the battery life-time (LT), in seconds, obtained by simulating both the HSpice model (Column $HSpice$) and the VHDL model (Column $VHDL$), and the corresponding relative errors (Column ΔLT). Column $RMSRE$ reports the root mean square relative error of the HSpice vs. the VHDL battery output voltage waveforms. Life-time estimates are very accurate (the average error is 0.525%). The void entries for the SP loads are due to the fact that the maximum pulse duration is 60 seconds, for which only a negligible life-time degradation was observed. The purpose of the SP loads is in fact to evaluate the short-time behavior of the model. Battery output voltage results are also satisfactory: The $RMSRE$ ranges from 0.08% to 1.667% (0.695% on average), depending on the load.

The errors are mainly due to the intrinsic difference of the implementation of the two models. In the VHDL model, the non-linear relationship between the two quantities is obtained by piece-wise linear approximation of values tabulated in an array. Conversely, in the HSpice model the interpolation of the tabulated values is obtained by imposing the continuity of the first derivative.

The results are in agreement with the expected behavior of the battery/DC-DC converter system. For example, the comparison of the $CC4$ type ($1.0A$ constant current load) to the SW loads ($1.0A$ average, but different levels), clearly shows that battery life-time is strongly affected by the current variations, and not only by average current values. Periodically changing the load from $0.2A$ to $1.8A$ ($SW4$) results in a 5% decrease in life-time with respect to a constant $1.0A$ load ($4790s$ vs. $5050s$).

Current Load	*LT*		*ΔLT* [%]	*RMSRE* [%]
	HSpice	*VHDL*		
CC1	51700	51800	0.193	0.048
CC2	26000	26000	0.000	0.080
CC4	5050	5100	0.990	0.365
SW1	5010	4990	0.399	0.271
SW2	4930	4920	0.203	0.347
SW4	4790	4710	1.670	1.108
STEP	4560	4550	0.219	0.804
SP1	–	–	–	0.949
SP2	–	–	–	1.311
SP4	–	–	–	1.667
Average			0.525	0.695

Table 1: Model Validation Results.

5 Use of the Model in Design Exploration

In this section we demonstrate the importance of a system-level battery model in the context of design space exploration. More specifically, we illustrate how the adoption of an accurate and efficient battery model may be helpful in the evaluation of system-level power optimization solutions based on dynamic power management (DPM).

We consider, as case study, the system-level description of a real-life Personal Digital Assistant (PDA) with built-in power management capabilities, whose conceptual block diagram is depicted in Figure 3. In the bottom-left corner of the diagram the model of the battery system can be clearly identified.

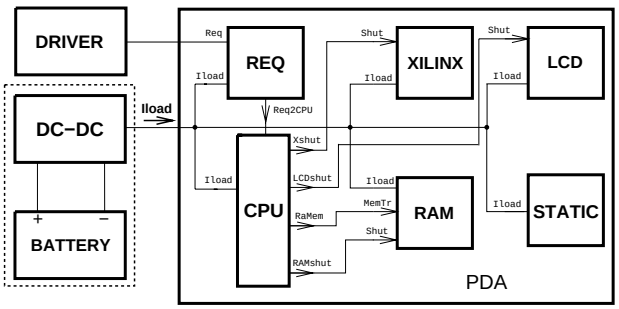

Figure 3: Block Diagram of the PDA.

The PDA consists of a CPU, with an embedded power management unit that can be selectively disabled; a memory block *MEM*, (RAM and flash); some glue logic implemented as FPGAs (*Xilinx*), and a LCD display. Two other blocks are contained in the system: *STATIC*, that emulates the static power dissipation (i.e., not power-manageable) of the PDA, and a block *REQ* that dispatches the incoming requests from block *DRIVER*, that emulates the user. Components are abstractly described using a state-based model similar to that described in [11]. States correspond to modes of operation, and transitions are taken in response to external events. The system model is built as an interconnection of behavioral state machines that communicate using abstract events.

The power model of the system components associates a current load with each mode of operation. During simulation, components change state of operation, thereby changing the current load experienced by the power supply. Every block of the PDA has two signals: *Iload*, that denotes the current drawn from the power supply, and *Shut*, driven by the CPU, that is used to indicate when the module is to be shut down. The model of the system, written in VHDL, can be simulated together with the power supply model for estimating battery life-time.

In a first experiment, we have applied a sequence of input requests to mimic the typical usage of the PDA for an approximate duration of one day. We measured the battery output voltage under the application of such sequence, both with and without power management. Needless to say, system simulation that accounts for the presence of battery and DC-DC converter was possible thanks to the availability of our model. In fact, HSpice simulation of the low-level, synthesized description of the whole system would have been just infeasible (the netlist would be too complex and the duration of the simulation too long).

Results are shown in Figure 4, and refer to the case of a Li-Ion battery with nominal capacity of $0.5Ahr$; as expected, power managing the PDA extends battery life-time of about 26.4% (from $28400s$ to $35900s$). In case the battery is replaced by a constant power supply, on the other hand, average power savings would be around 34.3%, indicating that average power reduction and battery life-time extension are not numerically the same.

The importance of a detailed battery model for accurate life-time estimation is further confirmed by the following experiment. Drawing from the battery a constant current exactly equal to the average value I_{avg}^{DPM} of the current drawn in the power-managed case, we observed an increase in estimated battery life-time of 17.1% (from $35900s$ to $42039s$). This result shows that the model is extremely useful to evaluate the actual impact of power management; the time-dependent load determined by DPM cannot be accurately estimated by simply applying the relative average load to the battery *off-line*. In fact, assuming an equivalent constant load may lead to sensible overestimates of battery life-time.

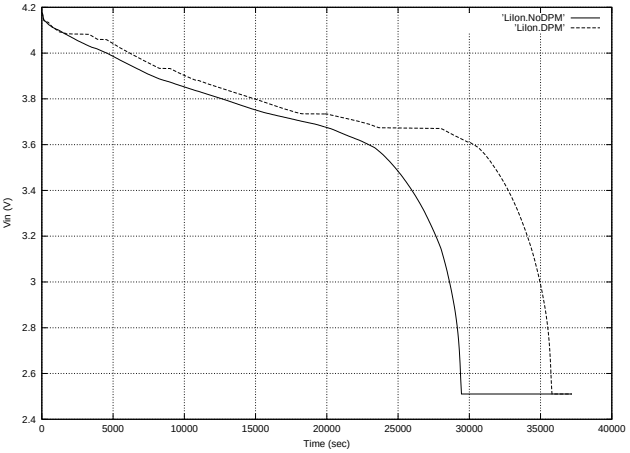

Figure 4: Impact of DPM on Battery Life-Time.

6 Conclusions

We have presented a discrete-time model for batteries and power conversion circuits that is targeted toward system-level simulation of portable systems. The model is efficient enough to enable simulation-based battery life-time estimation. Experimental results show that the accuracy of the estimates obtained by the event-driven model is very close to that of Spice-level simulations.

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