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A Distributed Control Strategy for Coordination of an Autonomous LVDC Microgrid Based on Power-Line Signalling

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***Abstract*—In a MG, an energy management control is essential in order to handle the variety of prime movers which may include different types of renewable energy sources (RES) and energy storage systems (ESS). Specifically, the recharging process of secondary battery, the most prominent ESS, should be done in a specific manner to preserve its life-time, common MG bus voltage must be kept within the bounds and the energy offered by RES should be utilized as efficiently as possible. This paper proposes a method for coordination of an autonomous low-voltage direct-current (LVDC) MG that consists of a number of sources using power-line signaling (PLS), a distributed control strategy in which the units inject sinusoidal signals of specific frequency into the common bus in order to communicate with each other. The control structure that allows the application of this method is revealed and the optimal range of operating PLS frequencies is specified. In order to achieve a zero steady-state error of injected signals in the common bus, primary control of batteries has been extended with dedicated proportional-resonant (PR) controllers that are switched on only during injection period. Finally, a method for coordination among the units using the PLS concept was developed and experimentally tested, confirming its applicability for autonomous LVDC MGs.**

***Index Terms*—Microgrid (MG), voltage-droop (VD) control, battery chargers, power-line signalling (PLS), distributed energy management strategy (DEMS).**

I. Introduction

ROBUSTNESS and compliance with modern dc end-user equipment and dc output type sources such as batteries and renewable energy sources (RES) make dc microgrids (MGs) an increasingly popular solution for interfacing distributed generation systems. In general, dc systems offer several advantages over their ac counterparts, such as increased efficiency and the non-existence of synchronization and reactive power flows issues [1]. Today, power supply of remote sites like telecom stations and data centres, where reliability and power quality are of great importance, is almost exclusively achieved with utilization of dc distribution [2]. Particularly interesting concept is to resolve the power supply of these kinds of systems only using RES [3], [4]. However, the variable nature of RES then imposes a power balancing challenge in case of isolated operation.

The addition of energy storage system (ESS), such as secondary (rechargeable) battery, is an option for maintaining the power balance continuously in small and autonomous systems. Regardless on internal technology, the price of the battery string generally plays an important part in the overall cost here and a special care should be therefore taken to preserve its lifetime [5]. In that context, it is the best practice to implement charging methods proposed from battery manufacturers and avoid frequent deep discharge cycles [6]. However, once the regulated charging process is started, the battery looses its power-balancing capability as the current that it extracts from the grid is determined from its internal control circuit. If the activation of this event is enabled without monitoring, lack of available capacity for supplying load or stability issues can occur in small and weak systems [7]. Moreover, if there are more battery strings connected in parallel, some kind of coordination strategy becomes mandatory.

Several techniques have been proposed for coordination of RES and ESS in ac and dc stand-alone systems. Some of them are based on central supervisory controller with enabled communication interface to every unit [8], [9]. However, although it offers the best control capability, the reliability of this kinds of systems is low as its proper operation relies on a single component. Moreover, with an increase in the number of units, their connectivity may require extensive hardware. For spatially compacted applications, a concept termed distributed bus signaling (DBS) was proposed to avoid the use of central controller. There, the interconnected units use the common bus voltage as a communication medium [10], [11]. This class of control methods is also commonly used for industrial islanded systems and is normally incorporated within the standalone plug-and-play dc/dc converters available in the market [12]. However, even though the need for supervisory controller is eliminated when DBS strategy is used, some other major issues are opened. For instance, fixed common voltage deviations are inherent to particular system operating mode, limiting the number of modes that can be reliably used. Thus, the application of secondary control makes no sense as the cancellation of voltage error will cause improper DBS operation.

In order to tackle the issues of previously mentioned strategies, a method based on power-line signalling (PLS) is proposed in this paper. The concept of power-line communication

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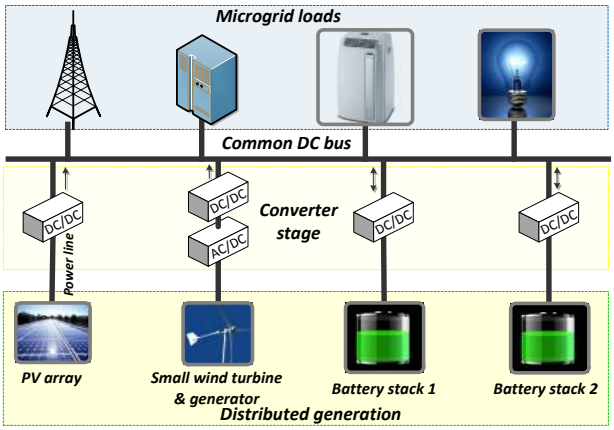


Fig. 1. Diagram of a small-scale LVDC microgrid.

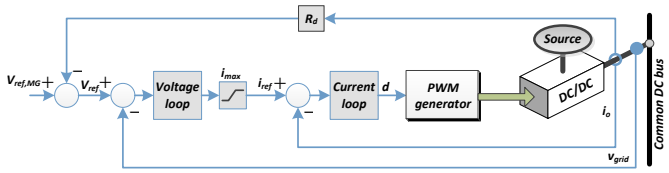


Fig. 2. Block diagram of a VD unit.

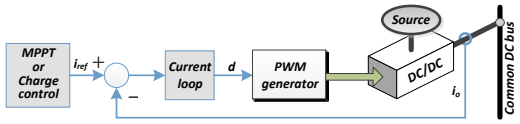


Fig. 3. Block diagram of a CP unit.

(PLC) has been widely used by electric utility companies to shut off the corrupted parts of the network and for information transmission [13]. As the main focus for PLC is data transmission, frequencies from few kHz up to several hundred MHz have been used in order to achieve acceptable physical layer rate [14]. Here, the power lines are used as a carrier of sinusoidal logic signals only and the PLS concept has been proposed as a more flexible extension of DBS. The advantage over DBS is that instead of having fixed voltage deviation throughout the particular operating mode, PLS signals are used as triggers for mode transitions where deviation can be optionally canceled by secondary control action without affecting proper operation. Moreover, for typical small-scale stand-alone low-voltage direct current (LVDC) MGs, there is no need to use separate PLS signal injection and extraction devices to utilize this concept, as it can be done directly from primary control loops.

The paper is organized as follows. In Section II, the physical configuration of LVDC MG is shown, and the primary control of each of its elements is revised. In Section III, a viable PLS frequency range with respect to all possible states of the system has been proposed. As only batteries need to inject the PLS signals in the proposed scheme, their control diagrams have been expanded with dedicated proportional-resonant (PR) controllers for ensuring zero steady-state error of injected references in the common voltage. In Section IV, a PLS distributed energy management strategy (DEMS) has been proposed, where PLS signals are used to guide the coordinated operation of the units. Practical applicability of the proposed method is examined in Section V. DEMS concept was verified in Section VI through experimental results, where it was showed that LVDC MG can be effectively supervised and controlled using only distributed PLS signals. The paper is concluded with Section VII where obtained results are discussed.

II. LVDC MG Structure and Control

Fig. 1 represents an autonomous LVDC MG formed around a common dc bus to which the sources and loads are directly connected. Typical loads can be roughly divided into passive and active ones, but all of them are usually designed for a specific main bus voltage. A voltage-droop (VD) method is a widely accepted way to obtain control over it using a parallel operation of variety of sources [15]. The functioning principle is to enforce the sources to jointly govern the common bus voltage according to total consumption by introducing the internal virtual resistance R_d as a control parameter. In case of dc/dc power electronic control interfaces, this is translated to an insertion of the current feedback which is in proportion to R_d on top of the inner voltage and current control loops (see Fig. 2). In this way, it is ensured that the steady-state operating point of the unit stays on the line defined by

$$v_{DC} = v_{ref,MG} - R_d i_o. \tag{1}$$

However, depending on the role of each unit, VD operation may not always be the best control strategy. For instance, instead of using RES for voltage support, it is better to extract all available free power from them with the use of dedicated maximum power point tracking (MPPT) algorithms whenever is possible. Up to date, a number of control strategies for that purpose has been developed for both PV [16] and WTG [17] plants. Still, most of them share the similar dual-stage control structure; 1) An MPPT algorithm responsible for finding a voltage for which the source gives maximum power with respect to environmental conditions, and 2) The primary source voltage loop which ensures tracking of the respective voltage reference and gives rise to the reference current for the inner control loop (i_{ref} in Fig. 3).

On the other hand, in order to recover the state-of-charge (SOC) of connected battery, constant voltage charging method should be applied at the end of the re-charging process. More specifically, a double-stage constant-voltage charging method best fit to the VRLA battery technology, which is still the most common one in stationary applications. The first voltage-stage setting is higher and is often referred to as the ”boost” voltage, whereas the other one is usually termed ”float” voltage. Recommendations of concrete voltage values and respective durations are usually provided by the manufacturers of specific battery. In order to achieve this capability, an internal battery control circuit that incorporates voltage and current loops is active during this process. The voltage loop determines the reference battery current which is required for maintaining the battery voltage on desired level.

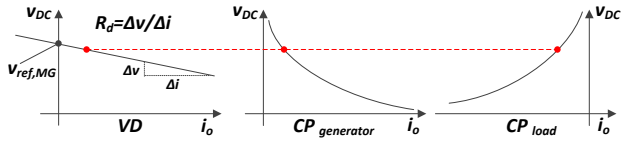


Fig. 4. Static characteristics of a VD, CP generator and CP load units connected to the common dc bus.

TABLE I
LAYOUT OF THE UL MODES WITHIN ALL POSSIBLE SL MODES. THE UL MODES FROM WHICH THE PLS BROADCASTS ARE PERFORMED ARE IN BOLD.

		SL MODE			
		I	II	III	IV
UNIT	Battery 1	**VD**	VD || **CP**	**VD** || CP	**CP**
	Battery 2	**VD**	**CP** || VD	CP || **VD**	**CP**
	PV array	CP	VD	CP	VD
	WTG	CP	VD	CP	VD

Even though it can be seen from the Fig. 3 that associated unit is current controlled, the process of calculation of its input current reference makes it virtually a constant power (CP) unit in the static sense. So, the MPPT algorithm will continuously adjust the RES voltage reference so as to keep extracting maximum power from it. On the other hand, charge algorithm will maintain the regulated charging of the battery. Both of these powers may be considered as constant for given environmental conditions and status of the battery.

The sampling frequency in typical closed-loop MPPT algorithms is much lower than the bandwidth of external control loop. Similarly, the bandwidth of internal battery voltage controller is normally lower than the one of inner control loops. Therefore, for the purpose of frequency response analysis, MPPT and charge blocks are modeled as adjustable current references.

The static characteristics of all types of aforementioned units in i-v plane are shown in Fig. 4, with VD unit on the left hand side, CP_{gen} (corresponds to RES in MPPT mode) in the middle and CP_{load} (corresponds to battery in charging mode) on the right hand side. One may see from that figure how different sources that operate in parallel influence the operating point of the system.

Voltage and current loops may be accomplished by conventional PI controllers and, together with LC filters on the outputs of respective dc/dc converters, define the dynamics of particular unit. If an averaged model of a buck dc/dc converter is considered, VD and CP units from Figs. 2 and 3 can be described by the following dynamical models, respectively:

$$\begin{cases} \frac{\dot{x_V}}{I_v} = -R_d i_L - v_{DC} + v_{ref,MG} \\ \frac{\dot{x_C}}{I_c} = x_V - (R_d P_v + 1) i_L - P_v v_{DC} + P_v v_{ref,MG} \\ L\dot{i_L} = P_c V_{in} x_V + V_{in} x_C - (P_c V_{in}(R_d P_v + 1) + R_p) i_L \\ \qquad -(V_{in} P_v P_c + 1) v_{DC} + V_{in} P_v P_c v_{ref,MG} \\ C\dot{v_{DC}} = i_L - \frac{1}{R_L} v_{DC} \end{cases} \quad (2)$$

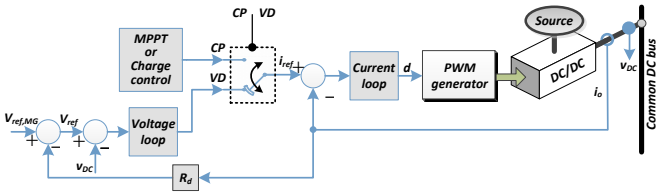


Fig. 5. Block diagram of a source for which unit-level mode can be dynamically overlapped.

and

$$\begin{cases} \frac{\dot{x_C}}{I_c} = -i_L + i_{ref} \\ L\dot{i_L} = V_{in} x_C - (V_{in} P_c + R_p) i_L - v_{DC} + V_{in} P_c i_{ref} \\ C\dot{v_{DC}} = i_L - \frac{1}{R_L} v_{DC} \end{cases} \quad (3)$$

where x_V, x_C, i_L and v_{DC} are the outputs of voltage and current loop integrators, converter inductor current and capacitor voltage respectively. P_v, P_c, I_v and I_c are the control parameters, L and C are inductance and capacitance of the converter output filter, R_p is the total inductor and switch parasitic resistance, R_L is the equivalent resistance of the connected load and V_{in} is the dc source voltage.

In case of having a number of N_d units acting as VD and a number of N_c units acting as CP connected to the same bus, it is convenient to arrange the one-unit equations expressing (2) and (3) into an implicit state-space model form:

$$M_s \dot{x_s} = A_s x_s + B_s u \quad (4)$$

where $\dot{x_s}$ is the complete state vector of dimension $[(3N_d + 2N_c + 1) \times 1]$, u is the input vector of dimension $[(N_d + N_c + 1) \times 1]$, matrices M_s and A_s are of dimension $[(3N_d + 2N_c + 1) \times (3N_d + 2N_c + 1)]$, while B_s matrix is of dimension $[(3N_d + 2N_c + 1) \times (N_d + N_c + 1)]$. As the composition of these system-level matrices is straightforward, their explicit expressions have been omitted here.

Controls of connected units have been designed so that the sources of reference currents can be dynamically overlapped externally, as shown in Fig. 5. Thus, depending on external signal, every source may operate in VD or CP mode, with the currently active mode being termed as the unit-level (UL) mode. It should be noted that RES output power in VD mode should not exceed its maximum available power and that compliance is achieved by providing dynamic limiters to current control loops. Moreover, smooth transitions between UL modes in both ways were ensured by automatic setting of appropriate initial conditions for associated controller integrators. In next section, a communication concept based on exchange of PLS messages between the units is developed.

III. APPLICABILITY OF THE PLS CONCEPT TO LVDC MGS

Taking into account two UL mode possibilities for all units, 2^N different configurations can be achieved in total for a general N-unit MG and frequency response will generally be different for every one of them. However, it will be shown that under the guidance of developed DEMS concept, the

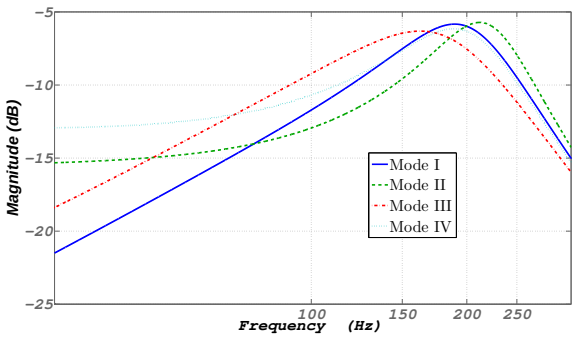
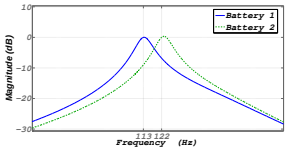
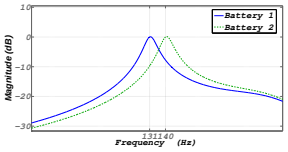


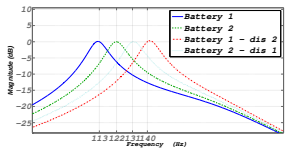
Fig. 6. Frequency magnitude responses from input of current loop to common voltage in all SL modes.



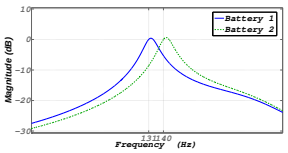
(a) Mode 1 - magnitude responses for frequencies 113 Hz and 122 Hz



(b) Mode 2 - magnitude responses for frequencies 131 Hz and 140 Hz



(c) Mode 3 - magnitude responses for frequencies 113 Hz, 122 Hz, 131 Hz and 140 Hz



(d) Mode 4 - magnitude responses for frequencies 131 Hz and 140 Hz

Fig. 7. Frequency magnitude responses with PR closed control loops for all SL modes.

analysed 4-unit MG from Fig. 1 will transit between only 4 configurations (out of possible 16), termed as system-level (SL) modes. The exact UL combination in each SL mode is given in Table I, where UL modes from which PLS signals are broadcast are in bold. Summing junction of current control loop was chosen as a natural choice for injection spot of PLS reference signals. For good communication, these references should be mapped to a consistent voltage magnitude in the common bus regardless the applied frequency and UL or SL operating modes.

It will be shown in the next section that only batteries need to inject signals. In fact, every battery needs to be able to inject three distinct PLS signals; the main one (with frequency f_i) that governs UL mode changes of other units, the auxiliary one (with frequency $f_{i,aux}$) for indication of its own SOC and auxiliary signal of other battery (with frequency $f_{j,aux}$) for selective change of its UL mode. Consequently, in case of two battery system, four PLS frequencies should be chosen in total.

Bode diagrams can provide help in the selection of optimum frequency values. In order to construct them, a full set of parameters for every converter needs to be specified. In this particular study, the selection of LC filters was governed by the switching frequency of available real-time control platform, which is 10 kHz. Accordingly, the parameters of averaged control loops expressed by (2) and (3) were tuned taking into account those filters. Numerical values of all the parameters are given in Table II and corresponding magnitude frequency responses from summing junction of current control loop to common voltage with respect to Table I have been plotted in Fig. 6. One may observe from the figure the magnitude peaks occurring at frequencies between 150 and 220 Hz. They denote the frequencies for which the mapping of the input reference to output voltage is achieved with minimum additional current loading to converters. According to the response, also the frequencies between 100 and 250 Hz can be considered to be in the favorable frequency region. Therefore, it is advisable to choose the frequencies in that range. However, it is worth mentioning that different switching frequencies of particular converters would imply selection of distinctive filters and hence the settings of control parameters. For the same reason, the impact of extra units should be examined as well. In any case, Fig. 6 should be replotted to study the impact of different parameters on optimal PLS frequencies. This issue is studied in more detail in Section V.

The selected frequencies should not be to close to each other so as to have a clear differentiation of the PLS signals. Also, the minimum PLS frequency should not be too low in order to avoid interaction with converters' primary control loops and not too close to 100 Hz as it could interact with optional AC loads. Having the aforementioned facts in mind, the main and auxiliary frequencies for battery 1 have been chosen as 113 Hz and 131 Hz, and for battery 2 as 122 Hz and 140 Hz. This way, still there is room to expand the concept with additional frequencies. However, if the frequency resources are exhausted, one may go out of the proposed range but taking care not to overburden the PLS signal injecting converters.

The complete control structure of the PLS coordination concept is shown in Fig. 8. The resolutions on which unit should perform a broadcast and which ones should change their UL mode are done in a distributed fashion, within the dedicated localized controllers termed as distributed logic blocks (DLBs). Two types of DLBs have been developed; Battery DLB and RES DLB. Changes of UL modes can be done by both RES and batteries via the locally computed signal "UL mode". On the other hand, broadcast can be performed exclusively by batteries. So, according to batteries' DLB internal mechanism which is presented in next section, they perform broadcasts by giving rise to the respective voltage references (marked with red color in Fig. 8).

In order to ensure a zero steady-state error of these references in the common bus, three proportional resonant (PR) controllers per battery have been implemented ($G_{PR1}(s)$, $G_{PR2}(s)$ and $G_{PR3}(s)$). $G_{PRi}(s)$ is defined as [18]

$$G_{PRi}(s) = k_p + k_r \frac{s}{s^2 + \omega_i^2} \tag{5}$$

where ω_i ($\omega_i = 2\pi f_i$) is the frequency at which the PR provides tracking by introducing an infinite gain for ω_i. The introduction of PR controllers may alter the dynamics of the system by creating two additional complex poles per controller. In order to avoid this during normal operation,

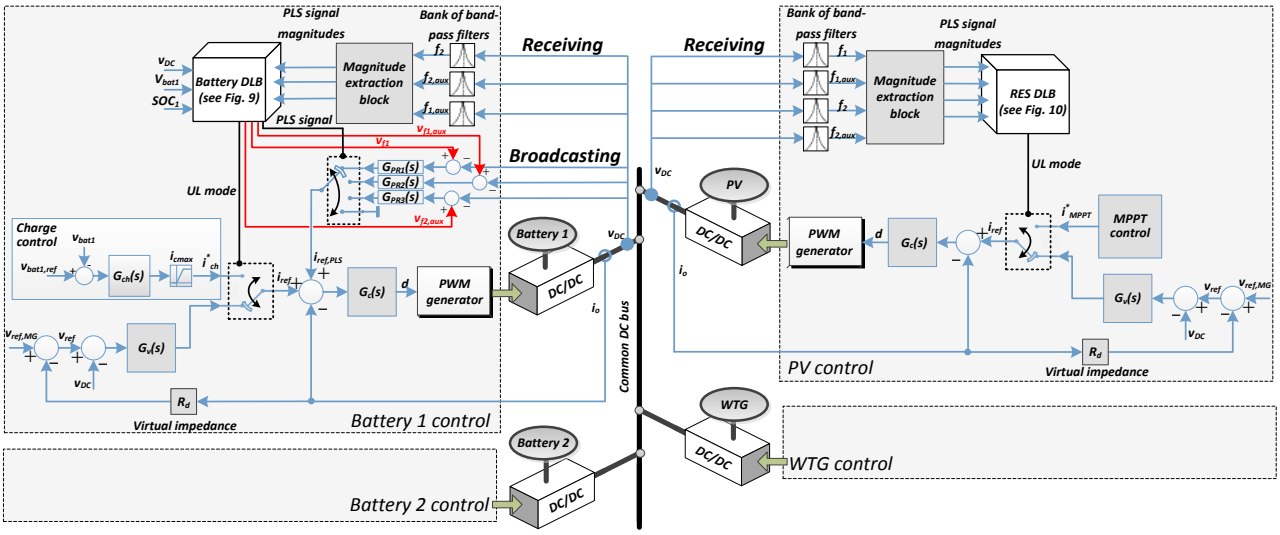


Fig. 8. Block diagram of the PLS based distributed supervisory control scheme.

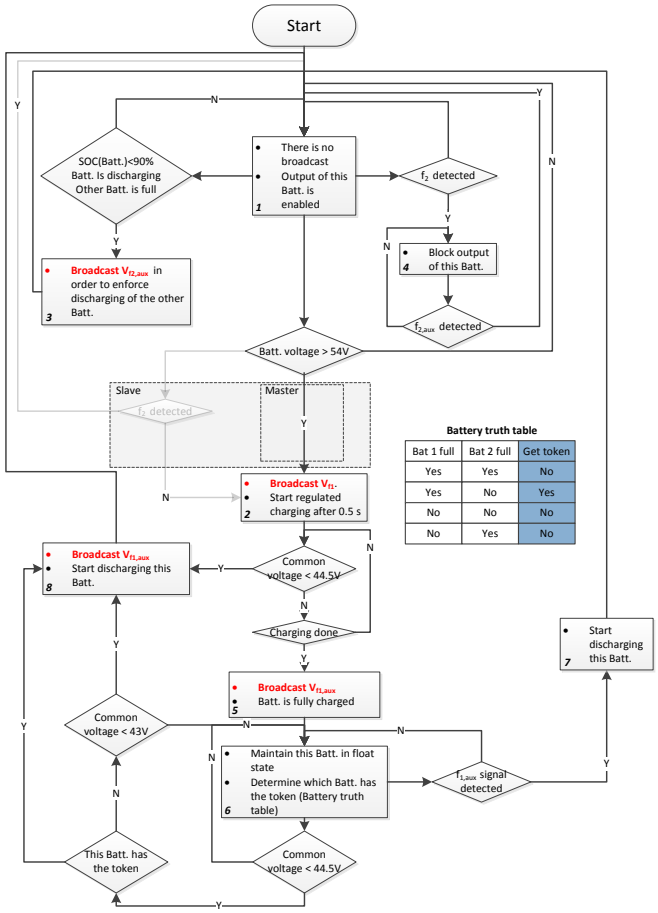


Fig. 9. Master battery DLB flowchart (Battery 1 in this case).

connection switch of respective PR controllers was designed to pass their outputs only during signal injection periods. This is achieved with a 4-port switch that is externally controlled by the signal "PLS signal" which is automatically induced when the battery is ordered perform broadcast.

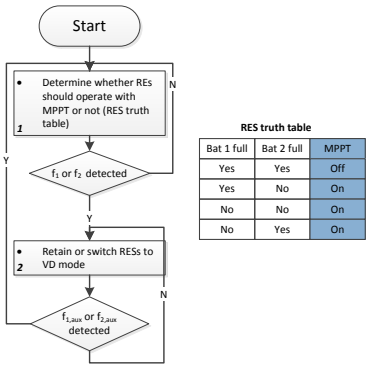


Fig. 10. RES DLB flowchart.

For the purpose of extraction of PLS signals in the common bus, banks of bandpass filters with the magnitude extraction blocks have been implemented. They consist of second-order generalized integrators and d-q transformation tuned at selected frequencies. In case of batteries, the number of banks is three (detection of both signals from other battery and its own auxiliary signal which is broadcast by the other battery under certain circumstances), and four in case of RESs (detection of all signals from both batteries). The extracted magnitudes are passed to DLBs which process them together with local measurements in order to determine further moves. To allow enough time for these blocks to detect the PLS signals, the duration of all broadcasts was selected to be 0.5 seconds.

The dynamics of VD and CP units shown in (2) and (3) were expanded with resonant terms and a new system model has been composed to analyze the frequency response for appropriate input to output (common DC bus voltage) communication channels with respect to Table I. As there are two equal battery stacks in this sample dc MG, in terms of preserving the consistence of the system model in (4), it does not matter which battery is in which UL mode. Thus, only 4 configurations are used for obtaining PLS channel transfer

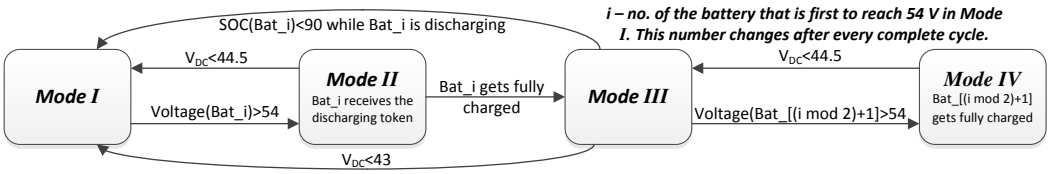


Fig. 11. Transitions between SL modes.

functions.

The single unit equations with resonant controllers were systematized into appropriate configurations according to Table I. The respective models contained 12 (Mode III), 13 (Modes I and IV) or 14 (Mode II) states and were not represented here. Instead, only arising magnitude responses have been calculated using the parameters that correspond to the experimental setup (see Table II). The responses from PLS inputs junctions to common voltage for the main and auxiliary frequencies in all respective SL modes are shown in Fig. 7. The results provide an analytical proof that the magnitude of reference PLS signals is indeed mapped to the common DC bus with good tracking.

Finally, the PLS magnitude that appears in the common bus should be selected. Experimental tests have shown that 0.4 V is a value that provides good compromise between the visibility of the signals in the presence of measurement noise and distortion of the common bus voltage. As an implication of that selection, a magnitude of 0.3 V has been set as a decision triggering value in DLBs so as to avoid the impact of measurement noise and interaction with other PLS signals that can give rise to extracted magnitudes of other signals which are not actively injected at the time.

IV. PLS Based Distributed Energy Management System

It will be shown in this section how the PLC communication concept can be utilized to meet the imposed operation tasks by proposing the respective DLBs internal decision making mechanisms which allow for coordinated control over all connected units of the exemplary MG from Fig. 1. In order to continue, several demands that should be followed during both short-term and long-term operation of the MG are being set. They may be sorted by priority:

1) Continuous regulation of the common bus voltage within the specified limits
2) Optimized performance of the batteries
3) Maximizing the use of the available power from RES

where the first item may be considered as a technical constraint related to the power balance in the network, while the other two are more of an economic nature. Due to interdependence of imposed requirements, they have to be harmonized at all times. For instance, regulated charging at high SOC is recommended to avoid damaging batteries that are usually expensive. Moreover, round-robin charging strategy is often utilized as an efficient way of distributing the managing effort on a number of batteries [19]. In order to keep the voltage control in this case, the best general solution is to ignore the third item in favor of second. The overall management objective was therefore defined as to use the power available from RES to guide the charging of associated batteries in a round-robin manner, while ensuring that at least one unit operates in VD mode.

In order to meet the energy management objectives, Matlab Stateflow® was used for development of the DLBs. It provides user-friendly graphical interface for modeling sequential decision and temporal logic flow charts and has a full compatibility with dSPACE 1103, which is used as an interface for real-time converter control. Two types of DLBs (Battery and RES) are presented in next two subsections.

A. Battery DLB

Flowchart of DLB for battery 1, which was selected as the master battery, is shown in Fig. 9. It reveals the mechanism for performing the transitions between UL modes for battery 1 and for determining the time of broadcast of PLS signals. Additionally, the DLB comprises also the monitoring scheme for the charge status of other battery. It uses the auxiliary signal of that battery to determine whether it is fully charged or not. So, every time the respective signal is detected, it is a priori known that the other battery changed its status.

One may note that the battery may find itself in 8 different states, which are labeled with numbers. A slight modification to the scheme, i.e. the conditional transition to the state 1 (shown in shadowed mode) should be additionally applied if the battery is selected to be the slave. Therefore, the DLB of battery 2 utilizes this kind of schematic. This transition is enabled if both batteries note that they are ready for regulated charging at the same time, and gives the priority to master battery. In state 5, a logic truth-table (shown within the same figure) is invoked to determine the distribution of discharging tokens.

B. RES DLB

The fastest possible recharging of depleted batteries will be done if all RES operate simultaneously in CP mode, following the references from their respective MPPT algorithms. On the other hand, once one of the batteries starts regulated charging, RES should be concurrently shifted to VD mode due to following two reasons; 1) The more units operate in VD mode, the less is voltage deviation in the common bus, and 2) If one or more RES remain in CP mode, a sudden power imbalance in the system may reverse the power flow and start to inject power back to RES in VD mode, which is highly undesirable. The general state machine for RES, shown in Fig. 10, was designed with respect to these considerations

and is applicable to any RES in the system, thus allowing the plug'n'play capability for additional units.

A truth-table that is invoked in state 1 serves as a backup UL mode determination for distinction between SL Modes I and IV (both batteries are charged in Mode IV) is shown within the same figure. RES use the same principle as batteries for detecting their charge statues. However, as both batteries need to be monitored in this case, RES interpret each auxiliary signal separately.

C. Elaboration of Coordination Control

Depending on load and environmental conditions, the MG is automatically guided through four SL operating modes, as shown in Fig. 11. A detailed description of events occurring within the particular SL mode, as well as of those that activate transitions from one mode to another, is given below. While inspecting the contents of this subsection, one can confirm that the configurations of UL modes within all SL modes coincide with those presented in Table I.

1) Mode I: Initially, both batteries operate in VD mode and are considered as not completely full, while RES are in the CP mode. If there is a deficiency of available power, batteries are discharged and once their stored energy is completely depleted, load shedding is the only option for avoiding their damage while maintaining the common voltage control at the same time. Design of intelligent load shedding scheme is out of the scope of this paper. On the other hand, surplus of power charges the batteries, causing the increase in their voltages. Once one of the batteries reaches 54 V margin, it moves from state 1 to state 2 and broadcasts its main signal (113 Hz and 122 Hz from batteries 1 and 2 respectively) that is mapped to a 0.4 V sinusoidal waveform in the common bus voltage.

2) Mode II: Due to the broadcast of the main signal from one battery, the other one then transits to state 4, while RES are moved to state 2. Eventually, first battery stops the broadcast and activates its double-stage regulated charging process which is executed for the specified amounts of time that can be defined using the manufacturer data. If the process of charging is done successfully, the first battery passes through state 5 where it is internally declared as completely full. Also, it broadcasts its auxiliary signal (131 Hz and 140 Hz from batteries 1 and 2, respectively) which other units use to interpret the change in its status.

3) Mode III: Once other units detect the auxiliary signal, the other battery (the one that is not full yet) moves from state 4 back to state 1, while RES return to state 1 after the 0.5 sec delay (in order to ensure that the other battery is in VD mode at first). To avoid chattering here, the delay for these transitions has been chosen to be 1 sec. Newly charged battery goes to state 5 where it remains in the floating charge regimen, and a discharging token is given to it as it is the first one that was fully charged (See truth table in Fig. 9). Moreover, according to truth table in Fig. 10, RES now reactivate their MPPT algorithms as only one battery is fully charged. Thus, the sequel of surplus of power causes the charging of non-full battery. Once its voltage reaches 54 V, the similar sequence as the one described in Mode I occurs and system moves to Mode IV.

TABLE II
EXPERIMENTAL SETUP PARAMETERS

Parameter	Symbol	Values
Converters		
DC power supply	V_{in}	100 V
Switching frequency	f_{sw}	10 kHz
Input capacitance	C_{in}	0.55 mF
Output capacitance	C	0.55 mF
Converter inductances	L	1.8 mH
Inductor+switch loss resistance	R_p	0.1 Ω
Primary control		
Reference voltage	$v_{ref,MG}$	48 V
Proportional current term	P_c	1
Integral current term	I_c	100
Proportional voltage term	P_v	0.5
Integral voltage term	I_v	1000
Inductor current limits	i_{max}	±8 A, (+8A/0A in RES)
Virtual resistances	R_d	0.5 Ω
Resonant control		
Proportional term	k_p	0.02
Resonant term	k_r	150
Charging algorithm		
Proportional voltage term	P_{ch}	5
Integral voltage term	I_{ch}	20
Charge triggering voltage	v_{trig}	54 V
Boost voltage	v_{boost}	58 V
Float voltage	v_{float}	55 V
Charging current limit	i_{cmax}	6 A
PLS DEMS		
Broadcast period	Δt_b	0.5 sec
Triggering magnitude	det	0.3 V
Upper mode switch trigger	$v_{low,1}$	44.5 V
Lower mode switch trigger	$v_{low,2}$	43 V

4) Mode IV: Now, this battery goes to state 2 and broadcasts its main signal which does not affect the fully charged battery, but enforces RES to change their operation to VD mode due to activated transition to state 2. Charging algorithm is executed again, and, if completed successfully, the associated battery is internally declared full and its auxiliary signal is broadcast. Other units than consequently conclude that it is full as well, which has an important implication for RES UL mode. In that sense, as RES are moved to state 1, the evaluation of truth-table from Fig. 10 commands them to stay in VD mode. Finally, both batteries are operated in the float charging condition which keeps their full SOC, while RES regulate the common bus.

5) Closing the Cycle of Operation: In case of a sudden power deficit caused by either increase of load or decrease of RES production, the management system was designed to sequentially guide the MG back to Modes III and I, which may be considered as the fundamental modes. According to imposed control priorities, then it is better to stop the regulated charging and return the battery to VD mode so as to restore the common bus voltage.

If the power dis-balance occurs in Modes II or III, the only other mode that can possibly offer enough power is Mode I. However, if it occurs in Mode IV, it is possible that Mode III may be sufficient. If that is the case, one of the batteries will

not be unsettled from its fully charged state and control over the order of discharging by means of tokens can be utilized.

Then, the system stays in Mode III until the SOC of the battery that has the token falls below 90%, and then goes to Mode I. This particular SL mode transition is realized with the broadcast of auxiliary signal of the other battery once it moves to state 3. These conditions assure that the other battery moves from state 6 to 7 and system is again in Mode I.

On the other hand, if the voltage still does not settle in Mode III, the MG is returned to Mode I. In order to determine which is the correct mode after voltage fall, two low voltage limits were designed to act as an external resets. Higher one ($v_{low,1}$) guides the system from Mode IV to Mode III and lower one ($v_{low,2}$) resets the states of all the sources to initial, guiding the system automatically to Mode I.

One may notice that the battery with the token has lower SOC than the other one after returning to Mode I and, if the sequence of shown events is reproduced, it will be in the second place in regulated charging queue. The roles of two batteries will now be exchanged and their long-term charging will be performed in a round-robin manner.

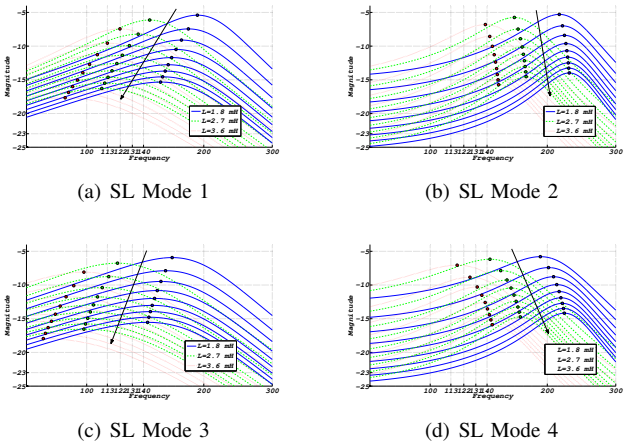
V. Practical Issues of the Proposed Method

Development of a distributed PLS control method has so far been focused on 2 RES and 2 ESS, with all of them having the same control and filter parameters (see Table II). However, since it is unlikely that this situation will appear in a real system, the various practical factors that affect the proposed method are discussed here. Two basic types of implications, which are analysed in more detail in next two subsections, can be distinguished; 1) Dealing with additional units from higher level control point of view (Subsection V-A), and 2) Impact of additional and different converters on system dynamics (Subsection V-B). Since the resulting transfer functions for the latter case are rather complicated, they are omitted here and only the tendencies of frequency magnitude responses for changes in control parameters and for the increase in the number of RES units are plotted. For interested readers, the details of the system's complete state-space diagram may be found in [20].

A. Plug-and-Play Capability of Additional Units

If a new RES is connected to the system, one may treat it in the same way as already present RES units from the higher level control point of view. In that sense, a plug-and-play capability may be easily achieved if the new RES adopts the identical control structure as its precursors (see Fig. 10).

On the other hand, if a new ESS is added, one should select three new PLS frequencies to enable it to send messages. However, for the boundedness of a favorable frequency range and necessary distance between two adjacent frequencies, there is a limit in the total number of frequencies that can be used. Thus, if the number of battery units becomes too large, a more advanced communication protocol should be composed. Possible enhancement in that sense is to combine several basic PLS signals in more complex structures. With an increase in the number of used basic signals, the number of possible messages that can be sent into the common bus then rises rapidly. The authors are currently conducting research on the aforementioned expansion.



(a) SL Mode 1 (b) SL Mode 2

(c) SL Mode 3 (d) SL Mode 4

Fig. 12. Family of frequency magnitude responses for the fixed 2 ESS and increase in the number of RES units from 2 to 10 using 3 sets of system parameters in all SL modes.

Hence, since only the addition of new RES is supported in terms of plug-and-play connection, the changes in system dynamics are explored for that case hereinafter.

B. Impact on System Dynamics

It can be safely assumed that the parameters of converters in original system's configuration are known and the selection of PLS frequencies can then be done following the procedure proposed in Section III. However, with addition of new converters, the dynamics of the system change and the optimal PLS frequencies may then differ from those that were initially selected. First of all, it is likely that some of those converters are operated at switching frequencies that do not exactly coincide with 10 kHz. If the respective differences are in range of several hundreds of Hz, there is a concern of creating subharmonics in the common dc bus voltage which may interact with originally selected PLS frequencies. On the other hand, if the difference is substantial, design of output filters and inner control loops will also differ in order to comply with the prescribed limits of switching ripples [21]. Then, the sensitivity of frequency response should be studied analytically.

1) Small differences in PWM frequencies: In order to analyse the possibility of subharmonic interaction with PLS frequencies, one should take a look on the expression of the voltage ripple magnitude in the common dc bus [21]:

$$\Delta v_{DC} = \frac{\Delta i_L T_{sw}}{8 C_{DC}}, \tag{6}$$

with Δi_L being the inductor current ripple, T_{sw} the switching frequency and C_{DC} the equivalent capacitance in the common dc bus, calculated as $C_{DC} = N \times C$ (C is the output capacitance of single unit and N is the number of units). Recognizing that Δi_L is

$$\Delta i_L = \frac{V_{in} - v_{DC}}{2L} d T_{sw}, \tag{7}$$

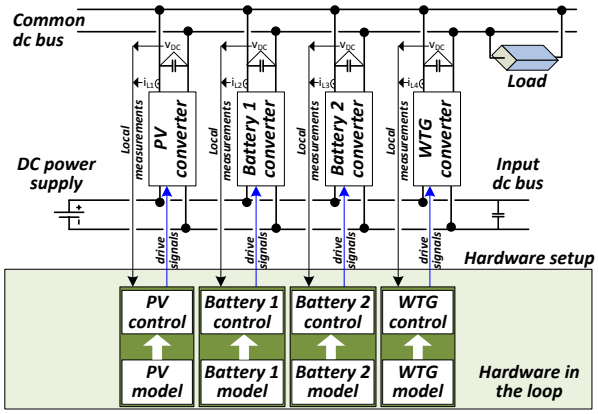


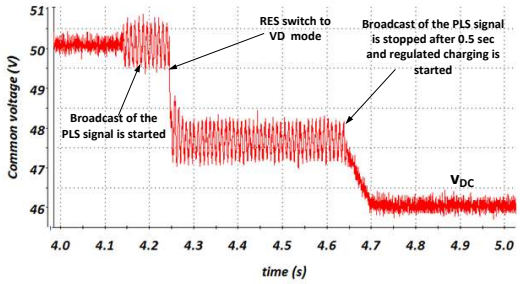
Fig. 13. Layout of the experimental setup.

with V_{in} being the input voltage and d the duty ratio, one may estimate the voltage ripple component of one converter by substituting the values from Table II into (6) and (7). The overall worst-case (if all PWMs are synchronized) ripple magnitude can be calculated as

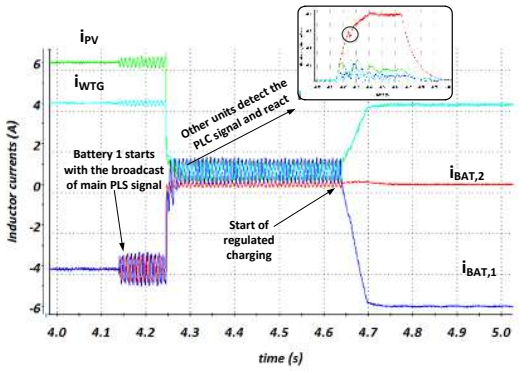
$$\Delta v_{DC,tot} = N \times \Delta v_{DC} = \frac{\Delta i_L T_{sw}}{8C} \approx 0.0158V. \quad (8)$$

Hence, the upper limit of ripple magnitude is consistent regardless of the number of units. Now, if converters with same nominal ratings are operated with different switching frequencies, the magnitude of common dc bus ripple will oscillate, but will again be limited by value calculated in 8. Accordingly, any eventual subharmonics caused by the difference in switching frequencies will be bounded by the same value, which is around 25 times lower than the PLS magnitude and is therefore harmless for the proper operation of proposed method.

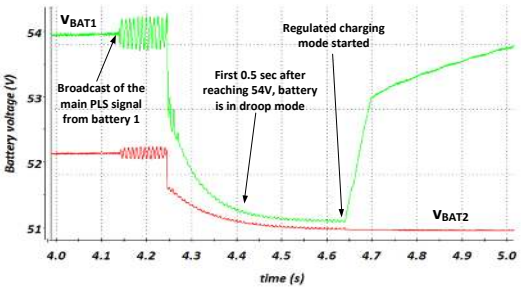
2) Substantial differences in PWM frequencies: In this case, it is expected that output filters and inner control loops are designed differently as well. In general, twice the lower switching frequency implies selection of twice bigger output inductor and output capacitor so as to keep the ripples in inductor current and capacitor voltage consistent. Consequently, the settings of current loop PI controller would change as well. Since it is normally tuned to cancel the pole introduced by the R-L element in the output filter, the proportional term of current loop PI should be changed with the same ratio as inductor. Taking into account this fact, the propagation of frequency magnitude responses in all SL modes for three values of output inductor, i.e. 1.8, 2.7 and 3.6 mH (and accordingly for the values of capacitor 0.55, 0.825 and 1.1 mF and P_c 1, 1.5 and 2) have been plotted in Fig. 12 in blue, green and red color, respectively. It should be noticed that the plots on top correspond to original system configuration, i.e. 2 batteries and 2 RES, whereas the lower ones show how the system dynamics change with increasing number of RES units, the instance which is explained in following subsection. It can be seen that all the responses are shifted slightly towards left with increase of inductance, moving the optimal frequencies more towards selected ones. Hence, the system exhibits behavior that is even more prone to selected



(a) Common DC voltage.



(b) Inductor currents.

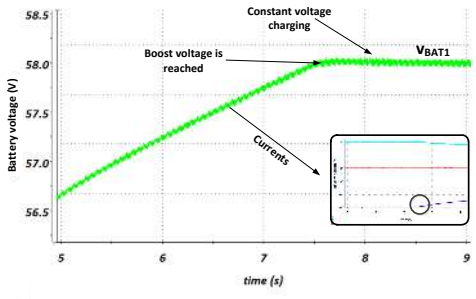


(c) Battery voltages.

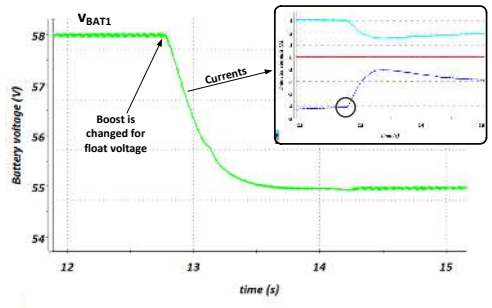
Fig. 14. Results for transition from Mode I to Mode II.

PLS frequencies in this case.

3) Increasing Number of Units: In order to clarify the construction process of respective functions for this matter, it should be noted that the overall system model in SL mode 1 comprises a fixed two sources operating in VD UL mode, one of which is responsible for PLS emission, and a number of sources acting in CP UL mode. In SL mode 2, fixed one source in CP UL mode performs PLS emission, whereas all other sources operate in VD UL mode. Similar implications follow for the remaining two SL modes. Then a family of transfer functions from input of current control loops to common dc voltage have been constructed by combining the equations (2) and (3) with respect to three groups of system parameters (as explained in previous subsection) for increasing number of RES units. Results for all modes are given in Fig. 12. It can be seen that the magnitude responses become more attenuated as the number of sources increases. This increase of the equivalent impedance seen by the PLS emitting source is

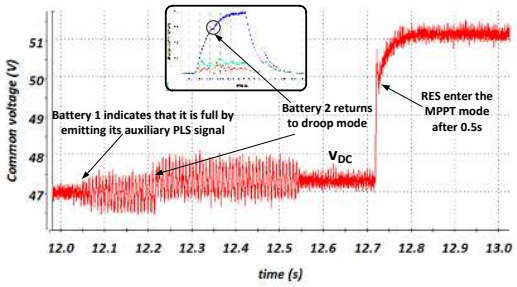


(a) Battery 1 reaching the boost voltage.

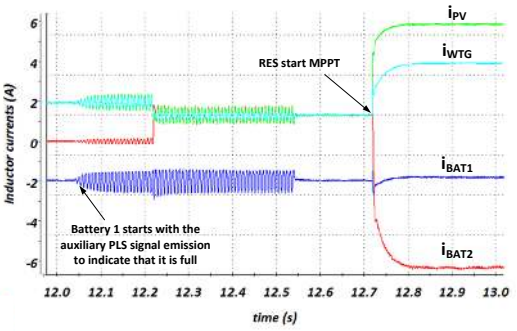


(b) Battery 1 moved from boost to float voltage.

Fig. 15. Charging algorithm for Battery 1 in Mode II.



(a) Common voltage.



(b) Inductor currents.

Fig. 16. Results for transition from Mode II to Mode III.

justified by additional output filters connected to the common dc bus. In turn, an extra effort is required from the PLS source for injecting a sinusoidal voltage waveform of the imposed magnitude. However, since the optimal frequencies do not show too much drift in comparison with the original configuration for all cases of analysed system parameters, also the attenuation in the originally proposed frame of PLS frequencies (113-140 Hz) remains fairly low. As the matter a fact, it can be noticed that in either mode the attenuation for 2 ESS and 10 RES is not more than approximately -23 dB, which requires additional 5.6 A from PLS source in order to produce 0.4 V in the common bus. This value is approximately 3.5 times bigger than additional current requirement in original configuration of 2 ESS and 2 RES. Hence, there is a limitation in expandability of the system using proposed method and trade-off between maximum number of modules and additional current requirement should be taken into account.

VI. Experimental Results

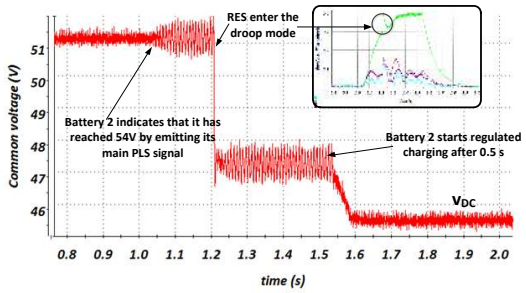
A dc MG prototype of Fig. 1 has been implemented and tested in the lab. Hardware platform was assembled from a dc power supply that fed four dc/dc synchronous buck converters, where every converter contains LC filter on the output, and all of them were connected in parallel to form a common dc bus. Electronic load was used to emulate the power deficiency periods. Control diagrams that correspond to elaboration in previous sections were developed in Matlab/Simulink and Matlab/Stateflow and were compiled to the dSPACE 1103, which was utilized for real-time control of converter switches.

For the reason that the experiments with real PV array, wind turbine and batteries would be impractical due to long waiting times for batteries to charge and discharge and difficulties in invoking different scenarios for mode transitions with unpredictable RES production, they have been emulated in real time using dSPACE 1103 as well. To that end, a detailed model of the battery (according to [22]) was implemented for the purpose of impact analysis on the overall system operation.

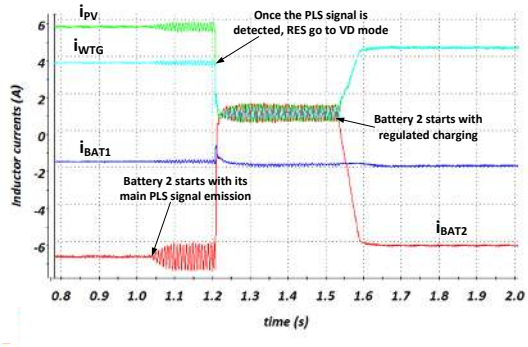
The layout of the experimental setup that shows the bounds between the hardware-in-the-loop and hardware part is shown in Fig. 13. The associated parameters are given in Table II.

Developed distributed control was tested for most of possible events related to production and consumption mismatches and battery charging requirements that should trigger the transitions between operation modes. In that sense, given experimental tests follow one cycle of operation of the system presented in Subsection IV-C. It was assumed that the system is initially in Mode I, i.e. both batteries are at moderate SOC and operate in VD mode, while RES operate in CP mode, having their MPPT algorithms turned on. Power injected from PV array was set to 300 W, while the power from WTG was set to 200 W. As the sum of these powers was more than the consumption in the system, batteries are charged with the remainder. Currents for both batteries are determined from their respective virtual resistances and are used to compute the internal voltages using the battery models.

At one point (see Fig. 14(c)), battery 1 reaches the 54 V margin and, according to Fig. 9, performs the broadcast of its main PLS signal (113 Hz). Due to battery internal resistance, one may note the mapping of the 113 Hz frequency component to the battery side as well. On the other hand, bandpass filters of other units detect this signal in the common

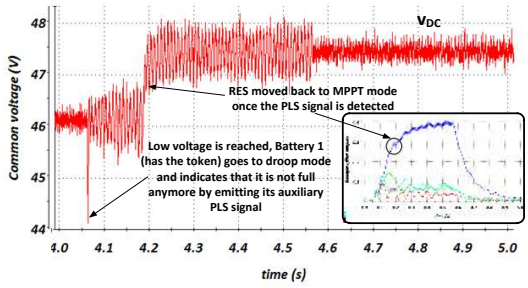


(a) Common voltage.

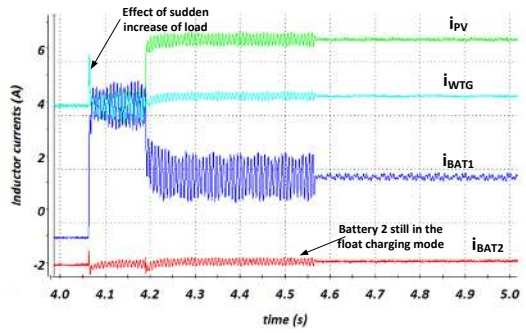


(b) Inductor currents.

Fig. 17. Results for transition from Mode III to Mode IV.



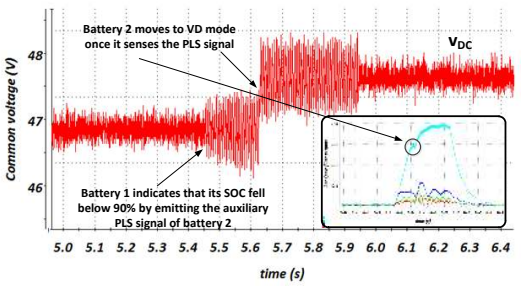
(a) Common voltage.



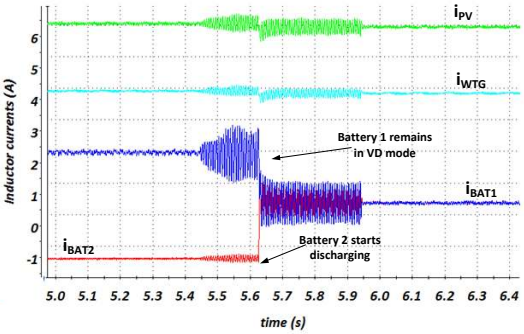
(b) Inductor currents.

Fig. 18. Results for transition from Mode IV to Mode III.

bus and forward it to dedicated blocks so as to extract the magnitude and pass it to associated DLBs. According to Fig. 10, RES then change their UL mode and battery 2 is moved to



(a) Common voltage.



(b) Inductor currents.

Fig. 19. Results for transition from Mode III to Mode I.

a state 4. On the other hand, battery 1 goes into state 2. This sequence, which corresponds to a transition from Mode I to Mode II, can be seen in the common voltage and currents of the sources in Figs. 14(a) and 14(b) respectively. The details of events associated with execution of charging algorithm for battery 1 can be seen in Fig. 15(a) (instance of reaching the boost voltage) and Fig. 15(b) (changing the reference charging voltage from boost to float).

Once the appointed charging time elapse, battery can be considered as completely recharged. The occurrence of this event and corollaries are depicted in Fig. 16. Here, battery 1 performs the broadcast of its auxiliary signal (131 Hz) to inform other units that it is full. Looking back at Figs. 9 and 10, this will cause transition of battery 2 back to state 1 and RES will internally pronounce the battery 1 full and return to MPPT mode (state 1). Now, the system is in Mode III and will stay in it until extended excess of power from RES causes the increase of battery 2 voltage up to 54 V (see Fig. 17). Then, the transition to Mode IV is activated by the broadcast of main signal (122 Hz) from battery 2. Similar sequence of events as in the case of transition from Mode I to Mode II occurs, but having a difference in a face that battery 1 is now charged and it does not move away from state 6. The results of execution of charging algorithm for battery 2 are omitted here as they are very similar as in the case of charging battery 1.

Voltage drop in the common dc link to upper threshold value 44.5 V, which triggers the transition from Mode IV to Mode III is shown in Fig. 18. If system is unable to restore voltage in Mode III, voltage would further drop to lower threshold value 43 V, triggering the transition to Mode I, as explained

in previous section. However, battery 1 holds the discharging token in this case, and it is the first to start the discharging. It broadcasts its auxiliary signal to indicate that it is not completely full any more which influences the operation of RESs (they switch to MPPT mode). After a certain discharge period, its SOC falls below 90 %, and it injects the auxiliary signal of other battery (140 Hz) which triggers its transition from floating regimen to VD mode (see Fig. 19). Then, the system is back in Mode I.

VII. Conclusion

A PLS based DEMS for autonomous LVDC MGs has been proposed in this paper. Here, the power network serves as a communication channel for exchanging messages in the form of PLS signals which are injected directly from converters' primary control loops.

To consolidate the applicability of proposed communication method, a DEMS system with an ability to coordinate internal mode transitions relying only on distributed PLS signals has been developed. It has been shown that application of this kind of coordination can be used for simultaneous management of multiple battery strings and RES. The expandability of proposed method to more units has been discussed from both higher-level control standpoint and from limitations brought by system's dynamics viewpoint. Experimental results of the whole operation cycle of the system were shown, further confirming the validity of proposed approach.

References

[1] H. Valderrama-Blavi, J. Bosque, F. Guinjoan, L. Marroyo, and L. Martinez-Salamero, "Power adaptor device for domestic dc microgrids based on commercial mppt inverters," *IEEE Trans. Ind. Electron.*, vol. 60, pp. 1191–1203, Mar. 2013.

[2] A. Kwasinski, "Quantitative evaluation of dc microgrids availability: Effects of system architecture and converter topology design choices," *IEEE Trans. Power. Electron.*, vol. 26, pp. 835 –851, Mar. 2011.

[3] M. Sechilariu, B. Wang, and F. Locment, "Building integrated photovoltaic system with energy storage and smart grid communication," *IEEE Trans. Ind. Electron.*, vol. 60, pp. 1607–1618, Apr. 2013.

[4] T. Dragicevic, J. Guerrero, J. Vasquez, and D. Skrlec, "Supervisory control of an adaptive-droop regulated dc microgrid with battery management capability," *IEEE Trans. Power. Electron.*, vol. 29, pp. 695–706, Feb. 2014.

[5] B. Borowy and Z. Salameh, "Methodology for optimally sizing the combination of a battery bank and pv array in a wind/pv hybrid system," *IEEE Transactions on Energy Conversion*, vol. 11, pp. 367 –375, Jun. 1996.

[6] A. Chaouachi, R. Kamel, R. Andoulsi, and K. Nagasaka, "Multiobjective intelligent energy management for a microgrid," *IEEE Trans. Ind. Electron.*, vol. 60, pp. 1688–1699, Apr. 2013.

[7] S. Anand and B. Fernandes, "Reduced-order model and stability analysis of low-voltage dc microgrid," *IEEE Trans. Ind. Electron.*, vol. 60, pp. 5040–5049, Nov. 2013.

[8] S.-K. Kim, J.-H. Jeon, C.-H. Cho, J.-B. Ahn, and S.-H. Kwon, "Dynamic modeling and control of a grid-connected hybrid generation system with versatile power transfer," *IEEE Trans. Ind. Electron.*, vol. 55, pp. 1677 –1688, Apr. 2008.

[9] G. Byeon, T. Yoon, S. Oh, and G. Jang, "Energy management strategy of the dc distribution system in buildings using the ev service model," *IEEE Trans. Power. Electron.*, vol. PP, p. 1, Apr. 2012.

[10] J. Schonberger, R. Duke, and S. Round, "DC-Bus Signaling: A Distributed Control Strategy for a Hybrid Renewable Nanogrid," *IEEE Trans. Ind. Electron.*, vol. 53, no. 5, pp. 1453–1460, 2006.

[11] K. Sun, L. Zhang, Y. Xing, and J. M. Guerrero, "A Distributed Control Strategy Based on DC Bus Signaling for Modular Photovoltaic Generation Systems With Battery Energy Storage," *IEEE Trans. Power. Electron.*, vol. 26, no. 10, pp. 3032–3045, 2011.

[12] "TS-MPPT-60, Solar System Controller." http://www.morningstarcorp.com/en/tristar%20mppt, 2013. [Online; accessed 22-March-2013].

[13] H. Ferreira, L. Lampe, J. Newbury, and T. Swart, *Power Line Communications: Theory and Applications for Narrowband and Broadband Communications over Power Lines*. John Wiley & Sons, 2010.

[14] S. Galli, A. Scaglione, and Z. Wang, "Power line communications and the smart grid," in *Smart Grid Communications (SmartGridComm), 2010 First IEEE International Conference on*, pp. 303 –308, Oct. 2010.

[15] J. M. Guerrero, J. C. Vasquez, J. Matas, L. G. de Vicuna, and M. Castilla, "Hierarchical Control of Droop-Controlled AC and DC MicrogridsA General Approach Toward Standardization," *IEEE Trans. Ind. Electron.*, vol. 58, no. 1, pp. 158–172, 2011.

[16] M. de Brito, L. Galotto, L. Sampaio, G. de Azevedo e Melo, and C. Canesin, "Evaluation of the main mppt techniques for photovoltaic applications," *IEEE Trans. Ind. Electron.*, vol. 60, pp. 1156–1167, Mar. 2013.

[17] J. Chen, J. Chen, and C. Gong, "New overall power control strategy for variable-speed fixed-pitch wind turbines within the whole wind velocity range," *IEEE Trans. Ind. Electron.*, Jul. 2013.

[18] R. Teodorescu, F. Blaabjerg, M. Liserre, and P. Loh, "Proportional-resonant controllers and filters for grid-connected voltage-source converters," *Electric Power Applications, IEE Proceedings* -, vol. 153, pp. 750 –762, Sep. 2006.

[19] J. Kaiser, J. L. S. Romain, and J. T. Charles, "Battery charger," US Patent Application 20110084650, April 2011.

[20] T. Dragicevic, *Hierarchical Control of a Direct Current Microgrid with Energy Storage Systems in a Distributed Topology*. PhD Thesis, 2013.

[21] R. Erickson and D. Maksimovic, *Fundamentals of Power Electronics*. Power electronics, Springer, 2001.

[22] T. Dragicevic, T. Capuder, M. Jelavic, and D. Skrlec, "Modelling and simulation of isolated dc microgrids supplied by renewable energy resources," in *2011, Conference on Sustainable Development of Energy, Water and Environment Systems*, vol. 1.

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