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A Dividerless PLL With Low Power and Low Reference Spur by Aperture-Phase Detector and Phase-to-Analog Converter

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***Abstract*—A 2.1-GHz dividerless PLL with low power, low reference spur and low in-band phase noise is introduced in this paper. A new phase detection mechanism using aperture-phase detector (APD) and phase-to-analog converter (PAC) generates an analog voltage in proportion to the phase error between reference and VCO, and then controls the current amplitude of the following charge pump (CP). The charging and discharging currents in the proposed CP have equal pulse width and equal small amplitude in locked state, which reduces the reference spur and power consumption of the CP effectively. Moreover, compared to the conventional CP with the same bias current in locked state, the proposed CP can contribute a much lower noise to the PLL output. In addition, a method of tunable loop gain with theoretical analysis is introduced to reduce the PLL output jitter. The proposed PLL is fabricated in a standard 0.13-μm CMOS process. It consumes 2.5 mA from a 1.2-V supply voltage and occupies a core area of 0.48 mm $\times$ 0.86 mm. The reference spur of the proposed PLL is measured to be -80 dBc/-74 dBc and an in-band phase noise of -103 dBc/Hz at 100 kHz offset is achieved.**

***Index Terms*—Aperture-phase detector, clock generation, dividerless, dual-loop, jitter, low in-band phase noise, low power, low reference spur, phase locked loop (PLL), phase-to-analog converter.**

I. Introduction

THE growing demands for PLL designs with low power, low reference spur and low phase noise have been explored recently for varieties of applications such as frequency synthesizers, communication systems and RF transceivers. The classical single-loop PLL [1]–[3] is shown in Fig. 1, which consists of a phase/frequency detector (PFD), a charge pump (CP), a loop filter (LF), a voltage controlled oscillator (VCO), and a frequency divider with a division ratio of N. In the classical PLL, the VCO dominates the out-of-band phase noise while CP and divider dominate the in-band phase noise. In the PLL feedback system, the closed-loop transfer function of CP noise is in inverse proportion to the gain from PLL output to the CP output current, which is defined as a feedback gain of CP ($\beta_{\rm CP}$) [4]. A larger $\beta_{\rm CP}$ means the same CP current will contribute less phase error to the PLL output, namely, more CP noise can be suppressed. The in-band CP noise is suppressed by $(\beta_{\rm CP})^2$ when transferred to the PLL output [4]. The block diagram and the characteristic of classic PFD/CP are shown in Fig. 2. PFD output pulse widths are converted to the switch-on time of CP as an average over one reference cycle. The averaging function over a reference cycle introduces the mechanism of divide-by-N in the feedback path. The $\beta_{\rm CP,CON}$ of the conventional PLL is given by

$$\beta_{\rm CP,CON} = \frac{\Delta i_{\rm cp}}{\Delta\phi_{\rm vco}} = \frac{\frac{I_{\rm CP,CON}}{2\pi}\cdot\Delta\phi_{\rm div}}{\Delta\phi_{\rm vco}} = \frac{I_{\rm CP,CON}}{2\pi}\cdot\frac{1}{N} \quad (1)$$

where $I_{\rm CP,CON}$ is the amplitude of CP current. Therefore, CP noise power is multiplied by N^2 when transferred to the PLL output. Larger $I_{\rm CP,CON}$ is beneficial to achieve larger $\beta_{\rm CP,CON}$, but simultaneously increases thermal noise and power consumption of CP itself. Furthermore, as described in Fig. 3, the PFD converts the phase error between REF and DIV into the charging ($I_{\rm up}$) and discharging ($I_{\rm dn}$) currents according to the switch-on time difference of $(t_{\rm up,on} - t_{\rm dn,on})$. In case that $I_{\rm up}$ and $I_{\rm dn}$ mismatch, one of them has to be switched on for a longer time until the charge is zero at CP output node, and then steady state condition can be achieved [5]. This causes output current ripple and leads to a high reference spur. In order to reduce the reference spur in classical PLL, rail-to-rail amplifiers are usually used to reduce the mismatch of CP charging and discharging currents [6]–[8]. This increases design complexity, noise, area and consumes significantly larger current. In summary, the classical single-loop PLL entails a difficult trade-off among power, noise, spur and design complexity.

By contrast, a dual-loop PLL has advantage to balance different specifications such as noise and power by new phase

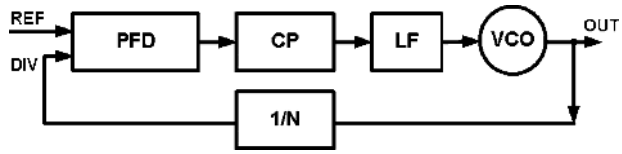

Fig. 1. Topology of the classical PLL.

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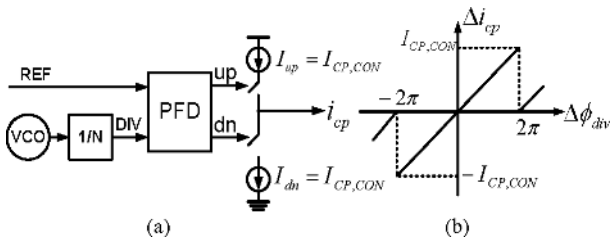

Fig. 2. Classic PFD/CP (a) Block diagram, (b) Characteristic.

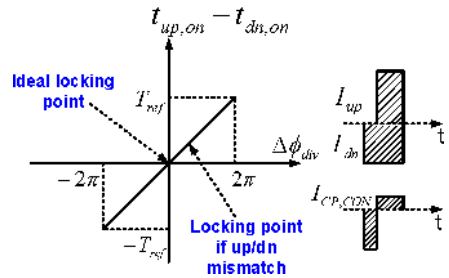

Fig. 3. The mechanism of reference spur generation in the classical PLL.

detectors [4], [9], spur and power by dual-path tuning control VCOs [10]–[12]. The dual-loop dividerless PLL in [9] incorporating a phase detector that operates on a windowing technique eliminates the need for frequency divider, and hence the power and noise contributions from divider are eliminated. However, as the phase detection mechanism remains the same with the conventional CP, CP noise contribution is still multiplied by N^2. The mismatch in CP still leads to a high reference spur. The dual-loop sub-sampling PLL in [4] reduces the in-band phase noise with low power consumption. Due to the sub-sampling phase detector, no divider is needed in the locked state and the CP noise is not multiplied by N^2. However, the disturbances of VCO by the sampler switching activity cause high spur and can possibly make the PLL out of lock. Since the spur is proportional to the VCO gain [13], the dual-loop PLLs in [10], [11] using two CPs and a dual-control VCO are presented to reduce spur and VCO noise due to the reduced VCO gain. The dual-loop PLL in [12] is the extension of the previous works in [10], [11], which employs only one CP with low VCO gain and extended fine-tuning range to reduce spur. The PLLs in [10]–[12] achieve a low spur without rail-to-rail amplifiers. Thus the power consumption of the amplifiers can be avoided. However, due to the switch-on-time controlled CP as conventional PLL, CP and divider noise contributions are still multiplied by N^2, which leads to high in-band phase noise of the PLL.

To overcome the aforementioned drawbacks, we describe our proposed PLL topology [14] by aperture-phase detector (APD) and phase-to-analog converter (PAC) to reduce noise, spur and power simultaneously.

Firstly, for the new CP circuit, equal pulse width of charging and discharging currents and equal small amplitude [5] in locked state are designed for achieving low reference spur and low power. Secondly, compared with the classical PLL and the dividerless PLL in [9], the proposed one can reduce the CP noise contribution by increasing the CP feedback gain dramatically. Thirdly, due to the introduction of APD, the dividers in the proposed PLL can be powered off in locked state, eliminating the power and noise contributions from the dividers. Finally, there is no need to design rail-to-rail amplifiers in the CP, which reduces the design complexity and power consumption. Therefore, the proposed PLL can achieve a good trade-off among power, noise, spur and design complexity.

The organization of this paper is as follows. Section II introduces the PLL topology with the loop noise analysis. Section III describes the details of the circuit level design and implementation. Experiment results and discussions are shown in Section IV and conclusions are drawn in Section V.

II. PLL Topology and Loop Noise Analysis

General design considerations to the operation of the proposed dual-loop PLL, loop noise analysis, loop parameters design and optimization of PLL phase noise are discussed in this section.

A. Dual-Loop PLL Topology

Fig. 4 shows the block diagram of the proposed dual-loop PLL. The main loop consists of APD, PAC, CP1, third-order LF, VCO, differential-to-single (D2S) and inverter chain. The differential sine-wave outputs of VCO are converted into single-ended steep square-wave (VCO_BUF) for phase detection by the D2S and inverter chain. A frequency locked aid (FLA) loop is added to ensure a correct frequency locking, eliminating the concern of locking in a sub-harmonic mode [4], [9]. The FLA shares the LF and VCO with the main loop. Similar to the classical PLL, FLA uses a divider and PFD/CP, except that a dead-zone (DZ) creator is inserted between PFD and CP2 [4].

At the beginning of the frequency acquisition process, FLA senses the phase error between REF and DIV, and the main loop senses the phase error between REF and VCO at the same time. However, FLA overrules the main loop due to its higher gain. When the phase/frequency error between REF and VCO is small enough, the DZ creator closes the CP2 in FLA automatically. Then the main loop dominates the final locking process, which determines the phase noise, reference spur and power consumption of the PLL. After phase locking, CP2 and divider in FLA have no influence on the main loop and do not introduce noise any more, which can be turned off to save power. In the dynamic locking process, the FLA plays a role of coarse tuning and the main loop plays a role of fine tuning. FLA adjusts the VCO frequency close to N times REF frequency, and then the main loop makes the VCO align with REF in the final locking process. Combining with the two loops, we can achieve the locking correctly.

In contrast to the previous dual-loop PLL designs [4], [9], the proposed PLL in this paper can improve the performance from the following perspectives. Firstly, both the sub-sampling CP and the proposed CP are inherently amplitude controlled CPs, which intend to cause small current ripple at the CP output node and lead to low spur [5]. However, the phase detector in the sub-sampling PLL directly samples the sine-wave output voltage of the VCO, which disturbs the VCO operation and causes high reference spur. To avoid such problem, the phase detector introduced in our PLL generates a shaped voltage signal through APD and PAC instead of directly sampling the VCO output. As

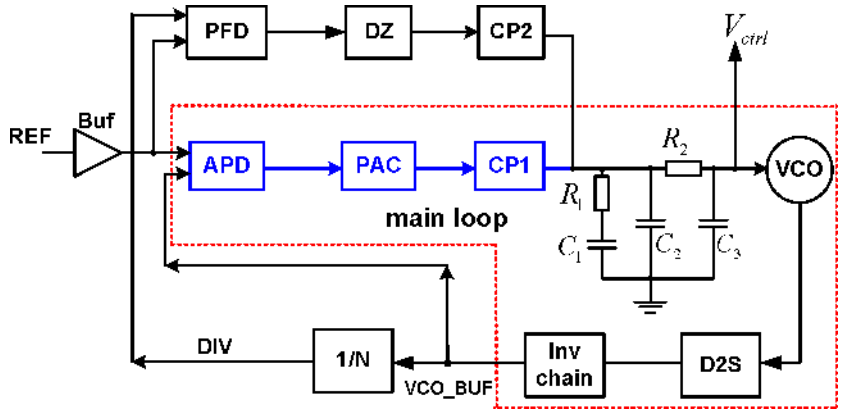

Fig. 4. Block diagram of the proposed dual-loop PLL.

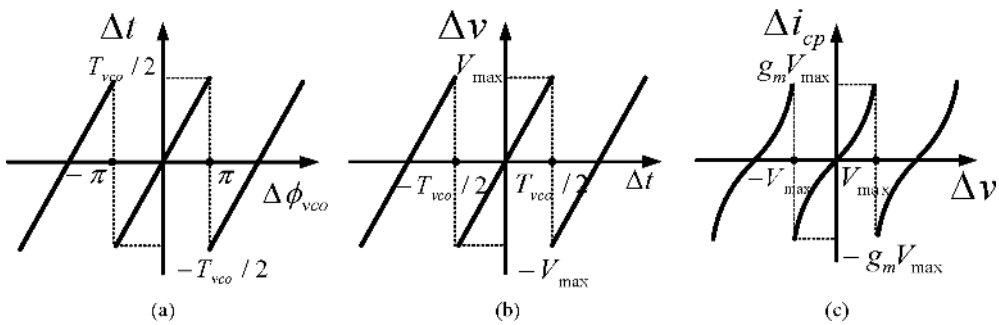

Fig. 5. Transfer curves (a) APD, (b) PAC, (c) CP.

a result, the reference spur can be reduced by the proposed PLL. Secondly, the shaped voltage generated by APD and PAC can improve the stability of the PLL. Thirdly, the proposed PLL can reduce the CP noise contribution dramatically compared with the dividerless PLL in [9] and can also reduce the power consumption of CP.

The main loop directly senses the phase error ($\Delta\phi_{\rm vco}$) between REF and VCO in a time window by the proposed APD, and then the PAC generates an analog voltage in proportion to the phase error to control the output current amplitude of CP. Fig. 5(a)–(c) shows the transfer curves of APD, PAC and CP circuits, respectively.

The pulse width of the APD output is proportional to $\Delta\phi_{\rm vco}$. The gain of APD is given by

$$K_{\rm APD} = \frac{\Delta t}{\Delta\phi_{\rm vco}} = \frac{T_{\rm vco}}{2\pi} = \frac{1}{\omega_{\rm vco}} \tag{2}$$

Then PAC converts the output pulse signals of APD into analog voltage signals and then controls the amplitude of the CP current. The gain of PAC is calculated as

$$K_{\rm PAC} = \frac{\Delta v}{\Delta t} = \frac{V_{\max}}{T_{\rm vco}/2} \tag{3}$$

where $V_{\max}$ is the maximum voltage of PAC. The gain of CP is given by

$$K_{\rm CP} = \frac{\Delta i_{\rm cp}}{\Delta v} = g_m \tag{4}$$

where g_m is the transconductance of the transistor in the proposed CP, which can be calculated as [15]

$$g_m = \sqrt{2\mu C_{ox}(W/L)I_{\rm CP}} \tag{5}$$

where μ is the mobility of charge carriers, $C_{\rm ox}$ is the gate oxide capacitance per unit area, W/L is the size of the transistor and $I_{\rm CP}$ is the CP current amplitude. Thus, g_m is a variable that changes with the $I_{\rm CP}$.

Fig. 6(a) shows the conceptual schematic of APD/PAC/CP. APD directly compares the phases between REF and VCO, then obtains up and dn signals. PAC converts up/dn to analog voltage signal VP/VN and holds VP/VN for the entire reference period (ignoring the finite reset time of the PAC). Finally, CP converts VP/VN to charging current $I_{\rm up}$ and discharging current $I_{\rm dn}$. Fig. 6(b) shows the characteristic of the proposed APD/PAC/CP, where the CP current ($\Delta i_{\rm cp}$) is proportional to $\Delta\phi_{\rm vco}$. As such, the ideal locking point is achieved when $\Delta i_{\rm cp}$ is equal to zero. As shown in Fig. 6(b), the feedback gain ($\beta_{\rm CP,APD}$) is always positive in the whole VCO cycle, which is preferable for the stability of PLL. By contrast, the characteristic of sub-sampling PD/CP is shown in Fig. 6(c), where $A_{\rm VCO}$ is the amplitude of VCO output and g_m is the transconductance of the transistor in sub-sampling CP. Note that the characteristic of sub-sampling PD/CP is ideally a sine waveform. As a result, a negative value can occur in $\beta_{\rm CP,SSPD}$, which worsens the loop stability and increases settling time. Similar to sub-sampling PLL, the $\beta_{\rm CP,APD}$ in this design also varies with the phase error. A manually tunable CP bias current has been adopted according to the

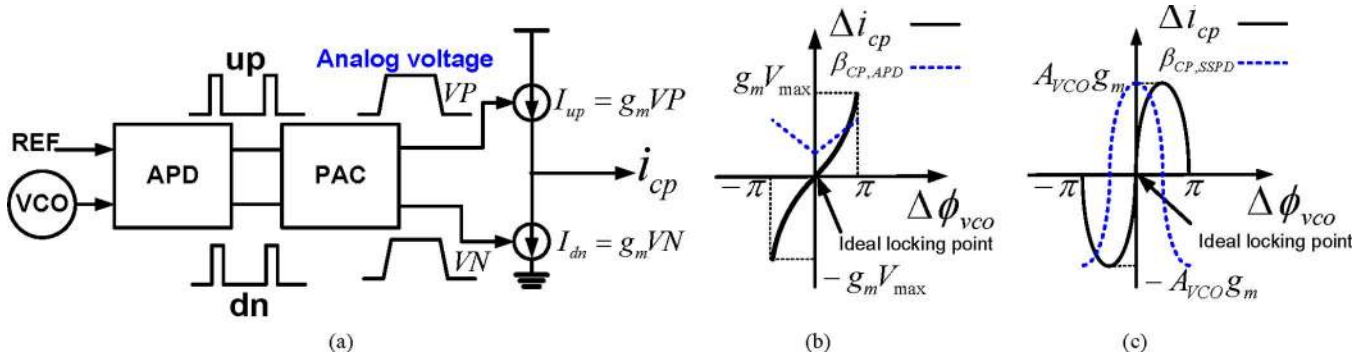

Fig. 6. (a) Conceptual schematic of the proposed PLL, (b) Characteristic of APD/PAC/CP, (c) Characteristic of sub-sampling PD/CP.

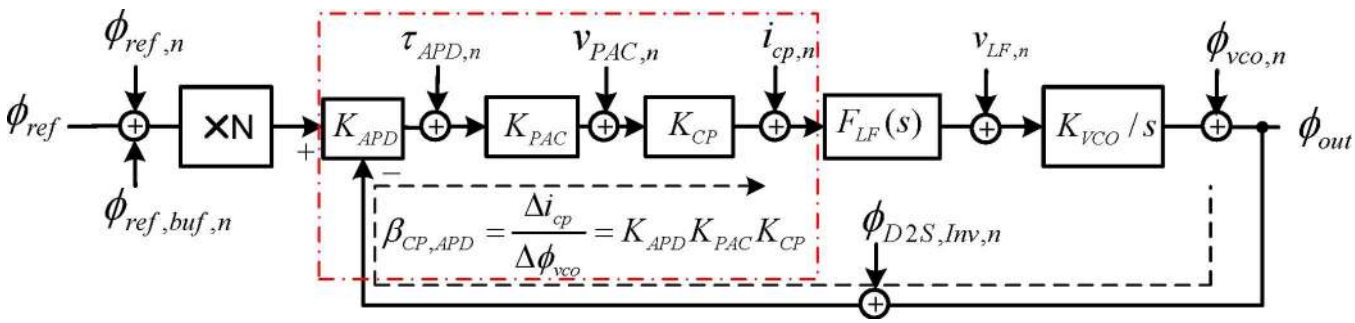

Fig. 7. Noise model of the main loop.

extensive PVT (process-temperature-voltage) analysis to ensure that the PLL can work well in a wide variation range.

B. Loop Noise Analysis

To demonstrate the low in-band phase noise of the main loop, a noise model is presented in Fig. 7. Here we model the proposed main loop as a time continuous system, which is valid as long as the PLL bandwidth is an order of magnitude smaller than reference frequency [4], [16].

In classical PLL and dividerless PLL in [9], the upsampling block introduces '$N-1$' zeros between successive pulses of CP current [17]. This block does not correspond to a physical circuit in the classical PLL and dividerless PLL in [9]. Instead it models the fact that the CP is activated only once in every N PLL clock cycles in order to adjust the $V_{\rm ctrl}$, while it remains off during the rest of the time [17]. The combination of the downsampling and upsampling blocks keeps the sampling frequencies consistent around the PLL loop [17]. However, in the proposed PLL, since the PAC holds the output voltage for the entire reference period, the upsampling results in repetition of the first generated voltage instead of filling it with '$N-1$' zeros. This change in the signal processing results in a replication by N or upsampling with repetition of N, and hence the block diagram needs to include a virtual '$\times N$' in front of the input phase. Furthermore, since there is no frequency division in D2S and invert chain, the gain of the two blocks in the phase domain is regarded as one.

The noise analysis of the main loop is shown as follows. The PLL open-loop transfer function is calculated as

$$G(s) = \beta_{\rm CP,APD} \cdot \frac{K_{\rm VCO}}{s} \cdot F_{\rm LF}(s) \tag{6}$$

where $K_{\rm VCO}$ is the VCO gain and $F_{\rm LF}(s)$ is the impedance transfer function of LF. The APD gain is inversely proportional to $f_{\rm vco}$, which means that when $f_{\rm vco}$ is larger or the division ratio $N(f_{\rm vco}/f_{\rm ref})$ is larger, the APD gain will drop. Thus, the APD noise when transferred to the output will be larger for a larger N. The noise contribution of the PAC can be calculated by relating the voltage noise at the PAC output. Similar to the noise analysis of CP, we can define a feedback gain ($\beta_{\rm PAC}$) from PLL output to PAC output voltage. The closed-loop transfer function of PAC noise is shown as

$$H_{{\rm PAC},n}(s) = \frac{\phi_{{\rm out},n}}{v_{{\rm PAC},n}} = \frac{1}{\beta_{\rm PAC}} \frac{G(s)}{1+G(s)} \tag{7}$$

The amplitude of PAC output voltage is given by

$$v_{\rm PAC} = K_{\rm PAC}(t_{\rm vco} - t_{\rm ref}) \tag{8}$$

where $t_{\rm vco}$ denotes the time of the first VCO rising edge in the time window of APD, and $t_{\rm ref}$ is the time of the REF rising edge in the time window. Equations relating edge time to signal phase are

$$t_{\rm vco} = \frac{\phi_{\rm vco}}{\omega_{\rm vco}}, t_{\rm ref} = \frac{\phi_{\rm ref}}{\omega_{\rm ref}} \tag{9}$$

When the loop is in lock, $\omega_{\rm vco} = N\omega_{\rm ref}$. As such, (8) can be rewritten as

$$\begin{aligned} v_{\rm PAC} &= K_{\rm PAC}(t_{\rm vco} - t_{\rm ref}) = \frac{i_{\rm cp}}{K_{\rm CP}} \\ &= K_{\rm APD} K_{\rm PAC}(\phi_{\rm vco} - N\phi_{\rm ref}) \end{aligned} \tag{10}$$

Therefore, the feedback gain of PAC can be calculated as

$$\beta_{\mathrm{PAC}} = \frac{\Delta v_{\mathrm{PAC}}}{\Delta \phi_{\mathrm{vco}}} = \frac{1}{\omega_{\mathrm{vco}}} K_{\mathrm{PAC}} = \frac{V_{\max}}{\pi}. \tag{11}$$

The noise contribution of the CP can be calculated by relating the current noise at the CP output. The closed-loop transfer function of CP noise is shown as

$$H_{\mathrm{CP},n}(s) = \frac{\phi_{\mathrm{out},n}}{i_{\mathrm{cp},n}} = \frac{1}{\beta_{\mathrm{CP,APD}}} \frac{G(s)}{1+G(s)}. \tag{12}$$

The amplitude of CP output current is given by

$$\begin{aligned} i_{\mathrm{cp}} &= K_{\mathrm{PAC}} K_{\mathrm{CP}} (t_{\mathrm{vco}} - t_{\mathrm{ref}}) \\ &= K_{\mathrm{APD}} K_{\mathrm{PAC}} K_{\mathrm{CP}} (\phi_{\mathrm{vco}} - N\phi_{\mathrm{ref}}). \end{aligned} \tag{13}$$

Therefore, the CP feedback gain can be calculated as

$$\beta_{\mathrm{CP,APD}} = \frac{\Delta i_{\mathrm{cp}}}{\Delta \phi_{\mathrm{vco}}} = \frac{1}{\omega_{\mathrm{vco}}} K_{\mathrm{PAC}} \cdot g_m = \frac{V_{\max}}{\pi} \cdot g_m. \tag{14}$$

From the (11) and (14), it is difficult to estimate if β_{PAC} and $\beta_{\mathrm{CP,APD}}$ are related to N now. Considering the real circuit implementation, there are two different situations shown as follows, leading to two opposite conclusions. When K_{PAC} is proportional to f_{vco}, or $V_{\max}$ is a constant and not related to f_{vco}, β_{PAC} and $\beta_{\mathrm{CP,APD}}$ in locked state will be independent on N. Contrarily, β_{PAC} and $\beta_{\mathrm{CP,APD}}$ will depend on N if K_{PAC} is a constant and not related to f_{vco}. We will further discuss this issue in the next section.

In addition, the inverter chain and the D2S circuits will consume power and introduce noise in the proposed PLL. The noise contributions of the D2S and inverter chain can be calculated by relating the phase noise at the output of D2S and inverter chain. Since there is no frequency division in D2S and inverter chain, the feedback gain from PLL output to D2S and inverter chain output phase is one, which is not related to N. Furthermore, as shown in Fig. 7, noise transfer function of the REF and REF buffer is still multiplied by N as the classical PLL. As explained later, the noise contributions from REF and REF buffer will dominate the in-band noise of PLL when CP noise contribution is small.

C. Operating Principle of the Proposed CP

The timing diagram of CP is shown in Fig. 8. In each reference period T_{ref}, the pulse widths of CP charging current I_{up} and discharging current I_{dn} are set to a fixed value T_d, but the current amplitudes vary with $\Delta\phi_{\mathrm{vco}}$. When REF_BUF leads VCO_BUF and $\Delta\phi_{\mathrm{vco}}$ is decreased in the locking process, I_{up} is reduced while I_{dn} is equal to the minimum current of CP ($I_{\min}$). Contrarily, I_{dn} is reduced with decreasing $\Delta\phi_{\mathrm{vco}}$ while I_{up} is equal to $I_{\min}$ when REF_BUF lags VCO_BUF. When phase locked, both of I_{up} and I_{dn} will come to $I_{\min}$. T_d/T_{ref} is designed as 0.26 in our work. Since the effective CP output current is reduced by T_d/T_{ref}, $\beta_{\mathrm{CP,APD}}$ is finally decreased by T_d/T_{ref}.

The characteristics of the proposed CP and the sub-sampling CP currents are shown in Fig. 9(a) and (b) respectively. $I_{\max}$ and $I_{\min}$ represent the maximum and minimum currents of each

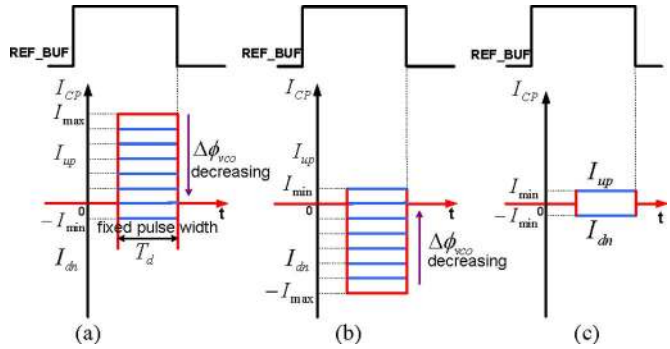

Fig. 8. Timing diagram of the proposed CP (a) REF_BUF leads, (b) REF_BUF lags, (c) Phase locked.

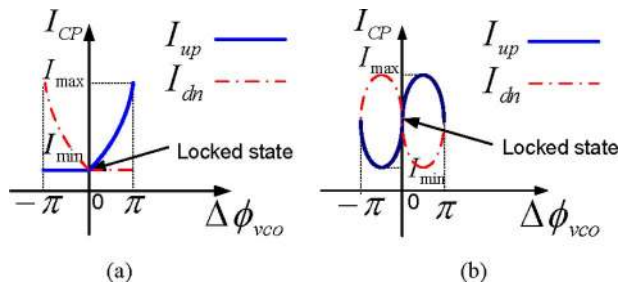

Fig. 9. Characteristic of CP charging and discharging currents (a) Proposed APD/PAC/CP, (b) Sub-sampling PD/CP.

CP respectively. Firstly, I_{up} and I_{dn} in locked state are the minimum currents of the proposed CP, not the average value of the maximum and minimum currents of the sub-sampling CP. Secondly, in half of the VCO period, I_{up} or I_{dn} in the proposed CP is always equal to $I_{\min}$, while I_{up} or I_{dn} in the sub-sampling CP is always above $I_{\min}$ in the VCO period. Since the CP current is simply defined by how much g_m is needed in locked state, it is difficult to compare the $I_{\min}$ of the two CPs.

D. Loop Parameter Design and Optimization of PLL Noise

As shown in Fig. 4, third-order loop filter is used to suppress the reference spur, which consists of a passive RC filter where a resistor R_1 is in series with a capacitor C_1. In addition, capacitor C_2 is added to reduce the voltage ripple of the VCO control signal (V_{ctrl}). Moreover, another pole consisted of R_2 and C_3 is used to improve reference spur attenuation. The PLL open-loop bandwidth ω_c can be expressed as

$$\omega_c = \frac{\beta_{\mathrm{CP,APD}} \cdot K_{\mathrm{VCO}} \cdot R_1 \cdot C_1}{C_1 + C_2 + C_3}. \tag{15}$$

In general, $C_1 \gg C_2$ and C_3, (15) can be simplified as

$$\omega_c \approx \beta_{\mathrm{CP,APD}} \cdot K_{\mathrm{VCO}} \cdot R_1. \tag{16}$$

A constant loop bandwidth can be achieved if $\beta_{\mathrm{CP,APD}}$ and K_{VCO} are constant.

To achieve low integrated phase noise (jitter), the PLL bandwidth needs to be delicately designed. The optimal bandwidth ($\omega_{c,\mathrm{opt}}$) for the minimum jitter usually occurs at the intersection of the VCO phase noise and the other loop noise [18], [19].

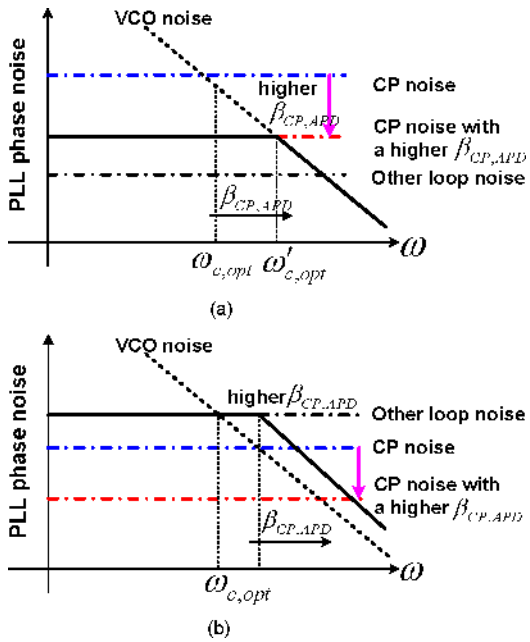

Fig. 10. PLL phase noise (solid line) (a) CP noise dominant, (b) Other loop noise dominant.

TABLE I
DESIGNED PARAMETERS OF THE LOOP FILTER

Parameters	Value	Parameters	Value
R_1	3.2 kΩ	R_2	1.9 kΩ
C_1	80 pF	C_2	3.2 pF
C_3	3.2 pF		

In the proposed PLL design, different $\omega_{c,\mathrm{opt}}$ is selected considering the proportion of CP noise and other loop noise contributions. As shown in Fig. 10, the solid line indicates the PLL output phase noise. When CP noise is dominant, $\omega_{c,\mathrm{opt}}$ is shifted to a higher level with a higher $\beta_{\mathrm{CP,APD}}$, as shown in Fig. 10(a) [4]. In this case, we can choose a higher $\beta_{\mathrm{CP,APD}}$ to achieve a lower PLL jitter. Oppositely, when other loop noise becomes dominant, as shown in Fig. 10(b), $\omega_{c,\mathrm{opt}}$ is the intersection of the VCO phase noise and the other loop noise [4], which is not related to $\beta_{\mathrm{CP,APD}}$. Therefore, to achieve the minimum PLL phase noise, the constant loop bandwidth has to be guaranteed when $\beta_{\mathrm{CP,APD}}$ is changed. However, higher $\beta_{\mathrm{CP,APD}}$will require smallerR_1 and larger C_1 in LF to ensure the loop stability condition and constant bandwidth [4]. Note that larger capacitor will make the full integration difficult. However, when we set R_1 and K_{VCO}, a higher $\beta_{\mathrm{CP,APD}}$ in Fig. 10(b) leads to a wider bandwidth and a worse phase noise. Based on this analysis, there is no need to increase $\beta_{\mathrm{CP,APD}}$ further when the in-band phase noise is dominated by the other loop noise. In the same way, the analysis and the conclusion of the PAC feedback gain β_{PAC} is similar to $\beta_{\mathrm{CP,APD}}$.

As a result, in order to avoid such unnecessarily high $\beta_{\mathrm{CP,APD}}$and optimize the PLL phase noise, a tunable $\beta_{\mathrm{CP,APD}}$ is introduced in this paper. The tunable method will be discussed in the following section with details. The designed loop parameters of LF are shown in Table I.

III. Circuit Design and Implementation

In this section, we introduce the circuit design and implementation in details. The design considerations of APD, PAC and CP circuits are firstly presented. Then the behavior of the new phase detector in the main loop is illustrated. Finally, the gain control method of APD/PAC/CP is shown and the designs of VCO and other circuits are discussed as well.

A. Aperture Phase Detector

APD directly compares the phases between REF_BUF and VCO_BUF in a time window, which eliminates the need for frequency dividers. The schematic of APD is shown in Fig. 11(a) and the timing diagram in locked state is shown in Fig. 11(b). When the timing control signal PUL_window becomes low, APD captures the first rising edge of VCO_BUF and REF_BUF signals. Both the two signals will be reset to '0' when PUL_window goes high, just as if the two signals are truncated in the time window. A classical PFD compares the phases of the truncated signals and then produces up and dn signals. The PUL_window has the same frequency as REF, and the width of time window Wd must be a little wider than the VCO period to avoid edge missing in phase comparison. The middle time point of Wd is the rising edge of REF_BUF, then APD can sense the positive and negative phase errors symmetrically. The timing error at this point is negligible as long as APD can sense both positive and negative phase errors. The generation of the time window will be discussed later.

Note that the truncated signal is different from the real output up/dn of APD. The pulse width of truncated signal in locked state is half of T_{vco}, but the pulse width of up/dn in locked state is determined by the reset time of the classical PFD (t_{rst}). The t_{rst} is related to the loop gain and a value of 100 ps is designed in this work.

B. Phase to Analog Converter

The diagram of PAC is shown in Fig. 12. PAC converts up/dn into analog voltage signal VP/VN. The up/dn signal controls the on-time of the current flowing in C_p, which finally generates an analog voltage proportional to the pulse width of up/dn. After the conversion, PAC will further hold the output voltage until the reset control signal is active. The output voltage and the gain of PAC can be rewritten as

$$V = \frac{Q_{\mathrm{PAC}}}{C_p} = \frac{I_{\mathrm{PAC}}\Delta t}{C_p} \tag{17}$$

$$K_{\mathrm{PAC}} = \frac{\Delta V}{\Delta t} = \frac{I_{\mathrm{PAC}}}{C_p} \tag{18}$$

where Q_{PAC} is the charge stored at the output node and I_{PAC} is the current amplitude flowing in C_p. Here Δt is the pulse width of up/dn from APD and it is equal to t_{rst} in locked state. VP/VN in locked state can be calculated as

$$VP = VN = V_{\mathrm{lock}} = \frac{I_{\mathrm{PAC}} t_{\mathrm{rst}}}{C_p} \tag{19}$$

Note that no matter how large the phase error is, the largest pulse width of APD output is $T_{\mathrm{vco}}/2$. Accordingly, the highest output voltage can be designed lower than V_{DD}. In addition, the loop property is mainly determined by the voltage in the locked state,

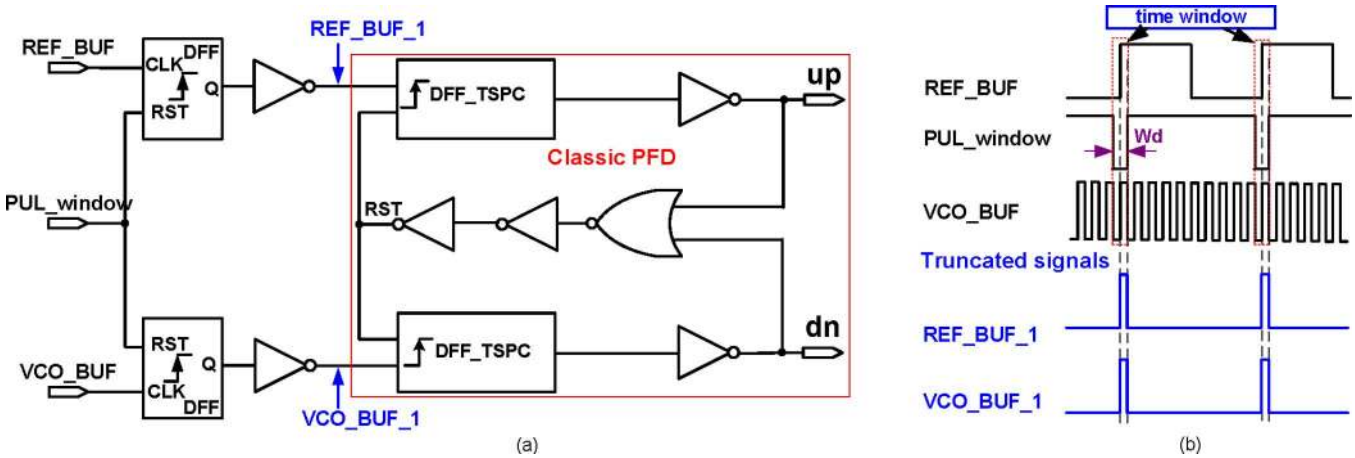

Fig. 11. (a) Schematic of APD, (b) Timing diagram in locked state.

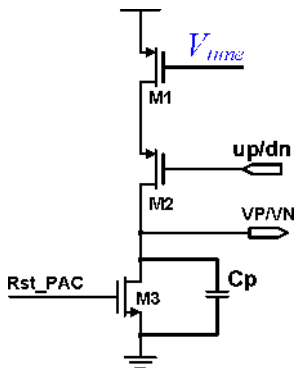

Fig. 12. Schematic of PAC.

which is always lower than $V_{\rm DD}$. Therefore, the circuit can work well as long as VP/VN is designed below $V_{\rm DD}$ with the largest pulse width. There is a trade-off between the power and noise in PAC. Larger $I_{\rm PAC}$ and smaller C_p will lead to higher $\beta_{\rm PAC}$ and $\beta_{\rm CP,APD}$, which suppresses more PAC and CP noise. However, the power will be increased. In addition, smaller capacitor will be more sensitive to process variation. $I_{\rm PAC}/C_p$ is related to the loop gain of the PLL, which is determined by the requirement of the loop parameter design. Here $V_{\rm tune}$ is used to control the amplitude of the charging current $I_{\rm PAC}$ as well as the amplitude of the output analog voltage, and finally control the current amplitude of the following CP. Though PAC suffers from the PVT variations, this controllable $I_{\rm PAC}$ can guarantee the circuit work well in a wide variation range. $I_{\rm PAC}$ can be estimated as

$$I_{\rm PAC} = \frac{1}{2}\mu_p C_{ox}\left(\frac{W}{L}\right)_1 (V_{\rm tune} - V_{\rm DD} - V_{\rm thp})^2 \qquad (20)$$

where μ_p is the mobility of charge carriers, C_{ox} is the gate oxide capacitance per unit area, $(W/L)_1$ and $V_{\rm thp}$ are the size and the threshold voltage of M1, respectively. In addition, after the phase detection in a reference period, a control signal Rst_PAC is used to reset the output analog voltage and prepare for the next conversion.

From (18), we can see that $K_{\rm PAC}$ is a constant which is not proportional to $f_{\rm vco}$ in our PAC circuit design and different from sub-sampling PLL where the sampled maximum voltage $(A_{\rm VCO})$ is independent on $f_{\rm vco}$, $V_{\max}$ of our PAC is actually a variable dependent on $f_{\rm vco}$. This will make $\beta_{\rm PAC}$ depend on $N(f_{\rm vco}/f_{\rm ref})$, which can be understood in the time domain as follows. When a timing error Δt between the VCO and REF is detected, the PAC will output a voltage with amplitude $K_{\rm PAC}\cdot\Delta t$. If N is increased while keeping the same VCO phase error $(\Delta\phi_{\rm vco})$ which is equal to $f_{\rm vco}\cdot\Delta t$, Δt will be decreased. Due to the constant $K_{\rm PAC}$, the PAC output voltage becomes smaller with larger N, leading to a lower $\beta_{\rm PAC}$.

Combining (2) and (18), the feedback gain of PAC in locked state (ignoring the finite reset time of the PAC) with the practical circuit parameters can be rewritten as

$$\begin{aligned}\beta_{\rm PAC} &= K_{\rm APD}\cdot K_{\rm PAC} = \frac{V_{\max}}{\pi} = \frac{I_{\rm PAC}}{C_p}\frac{T_{\rm vco}}{2\pi}\cdot\frac{T_{\rm ref}}{T_{\rm ref}} \\ &= \frac{1}{2\pi N}\frac{I_{\rm PAC}}{C_p}\cdot T_{\rm ref}. \end{aligned} \qquad (21)$$

Therefore we see that $\beta_{\rm PAC}$ depends on N.

C. Charge Pump

Fig. 13 shows the diagram of CP in the main loop. It has two main advantages. Firstly, CP outputs current amplitude in proportion to $\Delta\phi_{\rm vco}$ and achieves low phase noise. Secondly, CP outputs equal pulse widths and equal amplitudes $I_{\rm up}$ and $I_{\rm dn}$ to achieve low reference spur.

The amplitude of $I_{\rm up}(I_{\rm dn})$ is proportional to the analog voltage signal VP(VN) from PAC, which finally achieves CP current amplitude proportional to $\Delta\phi_{\rm vco}$. A differential pair in CP converts the analog voltage into current and current mirror (M5, M6) is used to inject the charging current into the loop filter. In order to avoid the mismatch of switches in conventional CP, the pulse width of $I_{\rm up}(I_{\rm dn})$ is controlled by a pair of anti-phase signals PUL_CP and PULB_CP which have the same capacitive load. When the timing control signal PUL_CP is high, $I_{\rm up}$ and $I_{\rm dn}$ will be connected to the loop filter. Inversely, when PUL_CP goes low, the current sources are steered away to Cs instead of switched off to alleviate the charge sharing between the loop filter and the current sources [4]. Ideally, a constant $\beta_{\rm CP,APD}$ is produced. In fact, since the amplitude of $I_{\rm up}(I_{\rm dn})$ is the square of the input analog voltage

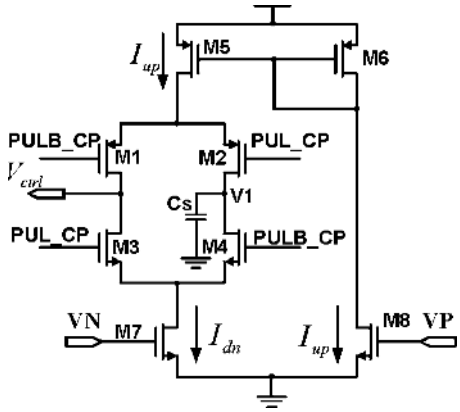

Fig. 13. Schematic of CP.

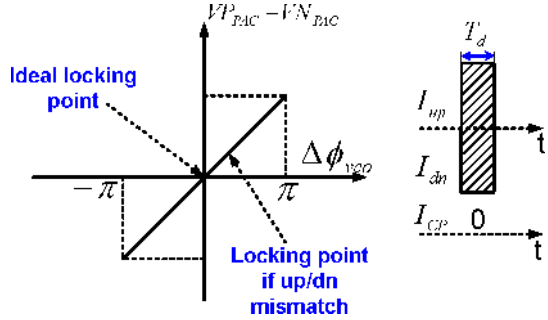

Fig. 14. Principle of the reference spur in the proposed PLL.

due to the nonlinearity of the transistors, $\beta_{\mathrm{CP,APD}}$ is not a constant. The gain of CP can be rewritten as

$$K_{\mathrm{CP}} = \frac{\Delta i_{\mathrm{cp}}}{\Delta v} = g_m = \mu_n \cdot C_{\mathrm{ox}} \left(\frac{W}{L}\right)_{7,8} (V_{GS} - V_{\mathrm{thn}}) \tag{22}$$

where μ_n is the mobility of charge carriers, V_{GS} and V_{thn} are the gate-source voltage and the threshold voltage of the MOS transistors (M7, M8 in Fig. 13), respectively. V_{GS} is determined by VP/VN from PAC. We can see that K_{CP} varies with VP/VN. I_{up} and I_{dn} in locked state can be expressed as

$$\begin{aligned} I_{\mathrm{up}} &= I_{\mathrm{dn}} = I_{\mathrm{lock}} \\ &= \frac{1}{2}\mu_n \cdot C_{ox} \left(\frac{W}{L}\right)_{7,8} \left(\frac{I_{\mathrm{PAC}} t_{\mathrm{rst}}}{C_p} - V_{\mathrm{thn}}\right)^2 \end{aligned} \tag{23}$$

In locked state, g_m is a constant which is not related to REF/VCO frequency, then $\beta_{\mathrm{CP,APD}}$ is mainly determined by $V_{\max}$ of PAC. Similar to the analysis of the PAC feedback gain, $\beta_{\mathrm{CP,APD}}$ is dependent on N due to the variable $V_{\max}$ related to f_{vco}.

Combining (2), (18) and (22), and considering the effective CP output current reduction by T_d/T_{ref}, the feedback gain of CP in locked state using the practical circuit parameters can be rewritten as

$$\begin{aligned} \beta_{\mathrm{CP,APD}} &= K_{\mathrm{APD}} \cdot K_{\mathrm{PAC}} \cdot K_{\mathrm{CP}} \cdot \frac{T_d}{T_{\mathrm{ref}}} \\ &= \frac{1}{\omega_{\mathrm{vco}}} \cdot \frac{I_{\mathrm{PAC}}}{C_p} \cdot g_m \cdot \frac{T_d}{T_{\mathrm{ref}}} \\ &= \frac{1}{2\pi N} \frac{I_{\mathrm{PAC}}}{C_p} \cdot \mu_n C_{\mathrm{ox}} \cdot \left(\frac{W}{L}\right)_{7,8} \\ &\quad \cdot \left(\frac{I_{\mathrm{PAC}} t_{\mathrm{rst}}}{C_p} - V_{\mathrm{thn}}\right) \cdot T_d. \end{aligned} \tag{24}$$

Therefore, $\beta_{\mathrm{CP,APD}}$ depends on N and has the smallest value in locked state due to the minimum current amplitude. However, as explained in Section II, there is no need to design an unnecessarily high feedback gain which will consume large area due to large capacitor in LF for the stable condition [4]. Although $\beta_{\mathrm{CP,APD}}$ depends on N, the proposed PLL can still reduce the CP noise contribution compared with the classical PLL, which will be discussed later.

The low spur property of the proposed CP can be explained as follows. Firstly, the pulse widths of I_{up} and I_{dn} are set to a fixed value T_d, assuming ideal switching, the following equation must be satisfied to meet the steady-state locking condition of zero net CP output charge [5]

$$I_{\mathrm{up}} \cdot T_d = I_{\mathrm{dn}} \cdot T_d \Rightarrow I_{\mathrm{up}} = I_{\mathrm{dn}}. \tag{25}$$

Namely, I_{up} and I_{dn} must have equal amplitude in locked state. Therefore the proposed CP eliminates the mismatch problem in the classical PLL and produces a much smaller ripple, as shown in Fig. 14. The ideal locking point is achieved when VP is equal to VN. However, there is still mismatch between the switches due to the non-ideal current source switches. Once there is some mismatch in CP, the loop will shift the locking point from the ideal point and tune VP (VN) to make the I_{up} and I_{dn} equal to each other to satisfy the steady condition. Therefore, the mismatch between the current source transistors still causes static phase error as in a conventional CP, but here it does not generate CP output current ripple and introduce spur [5].

D. Clock Generation and Timing Diagram of APD/PAC/CP

The CLK generation circuit is critical for the proposed main loop, as shown in Fig. 15. Two identical delay cells are used for the time window generation, which makes the middle time point of Wd occur at the rising edge of REF_BUF. The schematic of the delay cell is shown in Fig. 16. To cover the PVT variations, the width of Wd is designed to be tunable by VC. To reduce the power consumption of the two delay cells, an additional transistor M2 is inserted between M1 and M3, as shown in Fig. 16. The gate of M2 is controlled by input signal IN. The branch labeled as $\mathrm{B_c}$ will be switched on when IN is active, while it is switched off when IN is inactive. The branch $\mathrm{B_c}$ does not need to be turned on all the time in contrast to the delay cell in [4]. With this method, a current of 100 μA can be saved. Moreover, the input reference signal REF is processed in the CLK block to generate the final timing control signals of the main loop. Note that PUL_CP and PULB_CP must be active after the PAC charges to a steady analog voltage. As shown in Fig. 15(b), Rst_PAC must come later than PUL_CP and PULB_CP and ensure CP to capture the correct analog voltage. Moreover, an additional latch is used to make the PUL_CP and PULB_CP have perfect symmetry, which can reduce the mismatch of switches

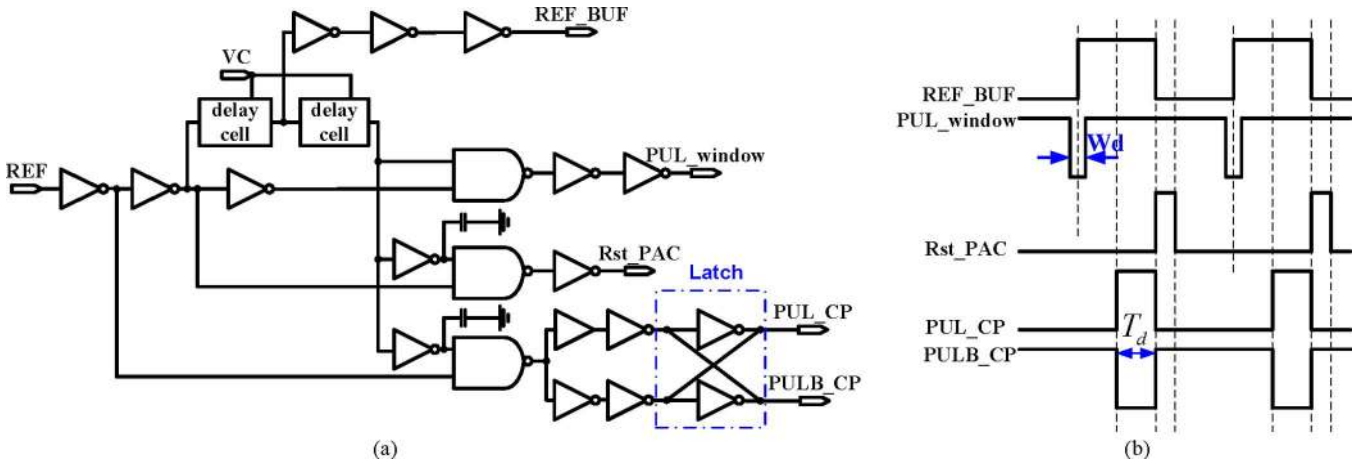

Fig. 15. CLK generation circuit (a) Schematic, (b) Timing diagram.

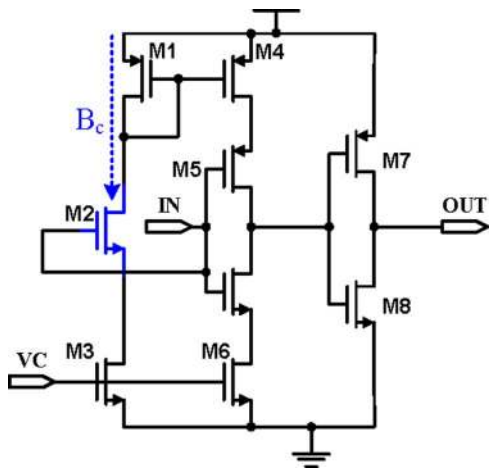

Fig. 16. Schematic of delay cell.

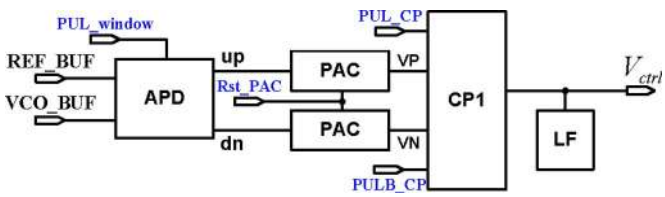

Fig. 17. Block diagram of the proposed APD/PAC/CP with CLK signals.

in CP and then reduce the reference spur. Considering the reset time of PAC, $\beta_{\rm PAC}$ will be divided by 0.5 finally. REF_BUF is fed to the PFD in FLA and APD as the real reference signal. The detailed connection relationship between CLK timing control signals and APD/PAC/CP is shown in Fig. 17.

The principle of the new phase detection mechanism is shown in Fig. 18. When the VCO_BUF and REF_BUF are phase aligned, the pulse width of up/dn is equal to the reset time of the classic PFD in APD ($t_{\rm rst}$).

In order to avoid the phase detection dead zone similar to the classical PLL, $I_{\rm PAC}$, $t_{\rm rst}$ and C_p are carefully selected to guarantee that $V_{\rm lock}$ is larger than $V_{\rm thn}$. When REF_BUF lags VCO_BUF, the pulse width of dn will be larger than $t_{\rm rst}$ while the pulse width of up remains the same. VN will be higher than $V_{\rm lock}$ while VP is equal to $V_{\rm lock}$. This increases the discharging current in CP, then $V_{\rm ctrl}$ will be decreased and the frequency of VCO will be decreased to make it aligned with REF frequency. In a similar way, when REF_BUF leads VCO_BUF, the charging current will be increased to make the VCO catch up with REF.

Furthermore, the sub-sampling CP current is always on in the whole REF period [4]. As shown in Figs. 13 and 18, the proposed CP current is, however, only active when VN/VP is larger than $V_{\rm thn}$, which is less than half of the REF period. As such, when compared to the previous sub-sampling CP, the proposed CP can reduce the power consumption.

E. CP Noise Comparison

To demonstrate the CP noise reduction we can achieve using the proposed PLL instead of a classical PLL, we compare the CP noise contributions of the two PLLs. By simply increasing the CP bias current of both PLLs in locked state, the CP noise contribution can be reduced. For a fair comparison, we assume that the two CPs use equal CP current amplitude ($I_{\rm CP,CON}$) in locked state. The CP feedback gain of the proposed PLL is given by

$$\begin{aligned}\beta_{\rm CP,APD} &= K_{\rm APD}\cdot K_{\rm PAC}\cdot K_{\rm CP}\cdot\frac{T_d}{T_{\rm ref}}\\ &= \frac{1}{2}\cdot\frac{1}{2\pi N}\frac{I_{\rm PAC}}{C_p}\cdot\mu_n C_{\rm ox}\\ &\quad\cdot\left(\frac{W}{L}\right)_{7,8}\cdot\left(\frac{I_{\rm PAC}t_{\rm rst}}{C_p}-V_{\rm thn}\right)\cdot T_d. \quad (26)\end{aligned}$$

The additional factor of 1/2 in (26) compared with (24) is due to the reset time of PAC (neglecting the charging time of PAC). Since the CP current in locked state can be expressed as (23), then (26) can be rewritten as

$$\beta_{\rm CP,APD}=\frac{I_{\rm CP,CON}}{2\pi N}\cdot\frac{T_d}{t_{\rm rst}-\frac{C_p}{I_{\rm PAC}}\cdot V_{\rm thn}}>\frac{I_{\rm CP,CON}}{2\pi N}\cdot\frac{T_d}{t_{\rm rst}}. \quad (27)$$

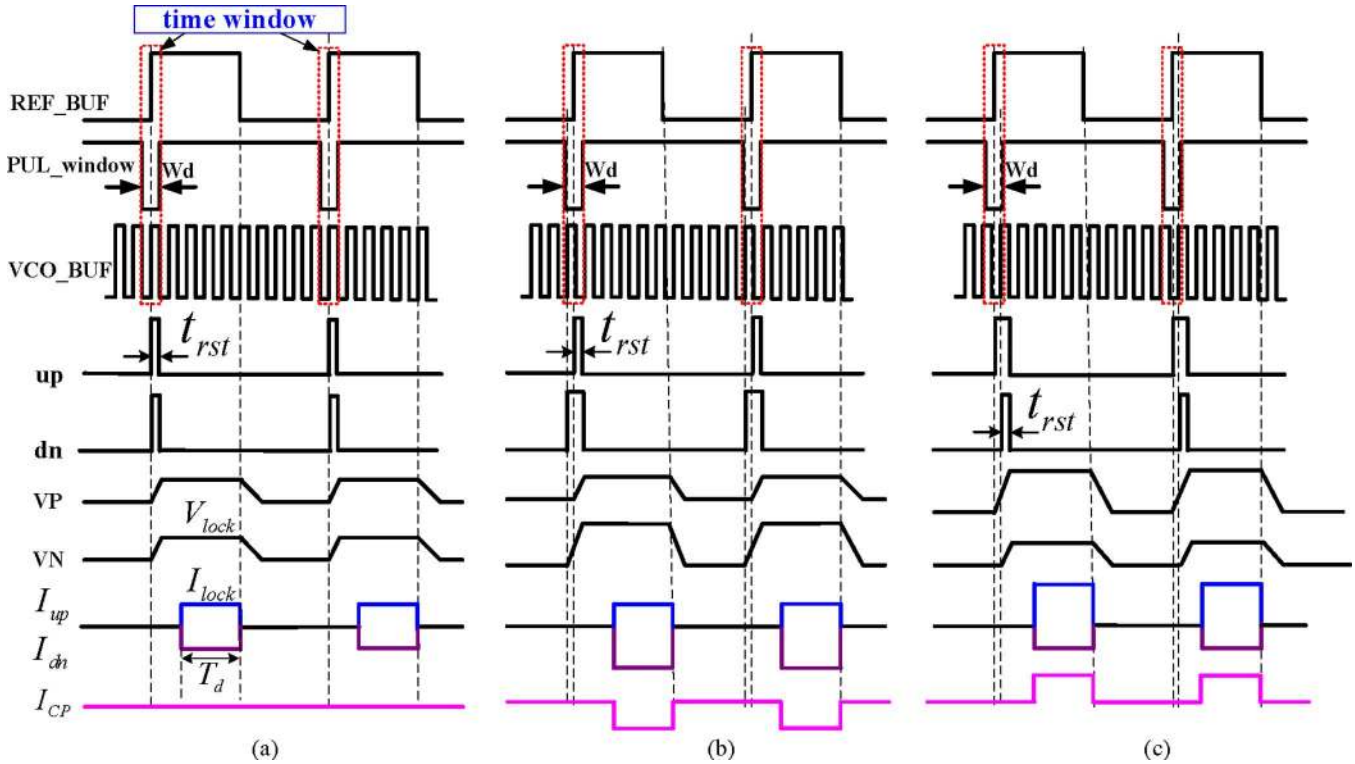

Fig. 18. Timing diagram of APD/PAC/CP (a) Phase locked, (b) REF_BUF lags, (c) REF_BUF leads.

Note that $I_{\rm PAC}$, $t_{\rm rst}$ and C_p are carefully selected to guarantee that $t_{\rm rst}$ is larger than $C_pV_{\rm thn}/I_{\rm PAC}$. Combining (1) and (27), we can obtain

$$\frac{\beta_{\rm CP,APD}}{\beta_{\rm CP,CON}} > \frac{T_d}{t_{\rm rst}} \tag{28}$$

$T_d/t_{\rm rst}$ is designed as 40 in our PLL, which indicates the CP feedback gain of the proposed PLL can be 40 times larger than a classical PLL with the same CP current amplitude in locked state. In other words, if we realize the same CP feedback gain, the current amplitude of the proposed CP will be 40 times lower than the classical CP. Thus much lower power will be consumed by the proposed CP.

Moreover, since we assume the two CPs use equal CP current amplitude in locked state, the power spectral density (S_{iCP}) of the (thermal) noise generated by the two CPs can be compared as

$$\frac{S_{i\rm CP,APD}}{S_{i\rm CP,CON}} = \frac{T_d}{t_{\rm PFD}} \tag{29}$$

where $t_{\rm PFD}$ is the reset time of the PFD in the classical PLL. Combining (28) and (29), the in-band phase noise due to the CP of the two PLLs can be compared as

$$\frac{\pounds_{\rm in-band,CP,APD}}{\pounds_{\rm in-band,CP,CON}} = \frac{\beta^2_{\rm CP,CON}}{\beta^2_{\rm CP,APD}}\frac{T_d}{t_{\rm PFD}} < \frac{t_{\rm rst}}{T_d}\cdot\frac{t_{\rm rst}}{t_{\rm PFD}}. \tag{30}$$

Since the reset time of the proposed APD is determined by the rest time of a classical PFD, we can assume that $t_{\rm rst}$ is equal to $t_{\rm PFD}$. Thus, with the same CP current amplitude in locked state, the proposed CP noise contributed to the PLL output will be 40 times lower than a classical CP, which makes the proposed CP contribute a very low in-band phase noise to the PLL output.

TABLE II
LOOP PARAMETERS WITH DIFFERENT $V_{\rm tune}$

V_{tune} (V)	$\beta_{CP,APD}$ (μA/rad)	f_c (MHz)	PM (deg)	$I_{up}(I_{dn})$ in locked state (μA)
0.55	3.6	0.8	46	15
0.5	6.5	1.4	55	28
0.45	9.8	2.1	53	45

F. APD/PAC/CP With Gain Control

Based on the issues discussed in Section II, a tunable $\beta_{\rm CP,APD}$ is proposed to reduce the PLL output jitter. According to (18) and (22), the gain of PAC and CP can be changed by $I_{\rm PAC}$. As shown in (20), $I_{\rm PAC}$ can be changed by $V_{\rm tune}$, and thus $\beta_{\rm PAC}$ and $\beta_{\rm CP,APD}$ can be easily tuned by $V_{\rm tune}$. Since $\beta_{\rm PAC}$ and $\beta_{\rm CP,APD}$ are changed, the other loop parameters will be changed simultaneously. Furthermore, we calculate $\beta_{\rm CP,APD}$, bandwidth f_c, PM and $I_{\rm up}(I_{\rm dn})$ in locked state at different values of control voltage $V_{\rm tune}$. The experiment results are shown in Table II.

When we decrease $V_{\rm tune}$, the analog voltage of PAC and the current amplitude of CP will be both increased. Then $\beta_{\rm CP,APD}$ and bandwidth of PLL will be increased at the same time. However, since we fix the loop parameter in LF, the PM of the PLL will be changed with the $\beta_{\rm CP,APD}$ and f_c at the same time. The relationship between settling time and PM is described in [20]. There is an optimal value of PM for the fast settling of PLL, and a high PM does not mean that it is always good for a PLL system. The loop can work well as long as appropriate PM is guaranteed.

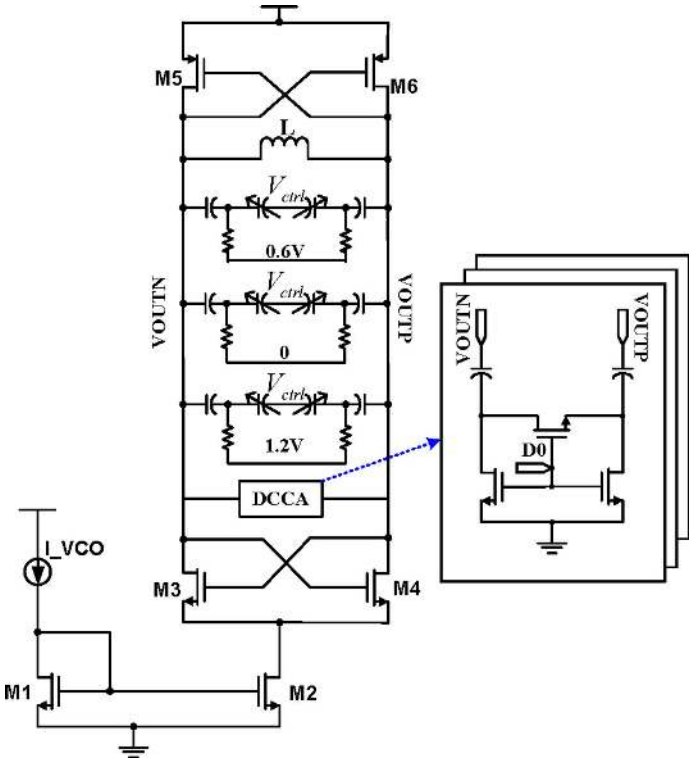

Fig. 19. Schematic of VCO.

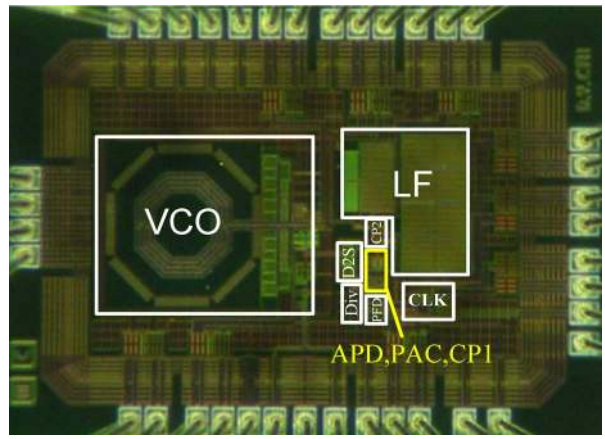

Fig. 20. Chip photo of the proposed PLL.

As shown in Table II, $I_{\rm up}(I_{\rm dn})$ in locked state is much smaller than the CP in the classical PLL. Considering the ratio of on-state time of CP current to reference period, the power of CP can be reduced further. For example, when $V_{\rm tune}$ is equal to 0.5 V, the power consumption of CP is less than 28 μA as well as a high $\beta_{\rm CP,APD}$ is achieved simultaneously. In conclusion, the proposed CP can reduce the in-band phase noise as well as reference spur with an ultra-low power dissipation, which is further verified by our measurement results.

G. VCO and Other Circuits

As shown in Fig. 19, in order to trade off between the power consumption and phase noise, complementary cross-coupled structure is adopted to form the negative transconductance in the VCO design. Three digitally controlled capacitor arrays (DCCA) are used to achieve a frequency range more than 400 MHz to cover the process variations. To reduce the loop gain variations resulting from changes in the $K_{\rm VCO}$, the VCO using an averaging varactor based split-tuned LC-tank [21] is employed in the proposed PLL. The gain of VCO can be described as

$$K_{\rm VCO} = \left|\frac{\partial \omega_{\rm osc}}{\partial V_{\rm ctrl}}\right| = \left|\frac{\partial \frac{1}{\sqrt{L(C_{\rm fixed}+C_{\rm var})}}}{\partial V_{\rm ctrl}}\right| = \frac{L}{2}\cdot\omega_{\rm osc}^3\cdot\left|\frac{\partial C_{\rm var}}{\partial V_{\rm ctrl}}\right| \quad (31)$$

where L and $C_{\rm fixed}$ are the inductance and the fixed capacitance of the LC tank, respectively, $\omega_{\rm osc}$ is the oscillation frequency and $|\partial C_{\rm var}/\partial V_{\rm ctrl}|$ is the voltage sensitivity of the varactor which is related to the varactor's linearity. Different from the fixed DC bias voltage used in the traditional varactor design, the averaging varactor uses distributed voltage values (0 V, 0.6 V, 1.2 V) for three varactors. Therefore, the nonlinearities of the varactors are nearly cancelled. $K_{\rm VCO}$ is designed to be 70 MHz/V in our VCO.

To reduce area and design complexity, five stages of TSPC dividers are employed to achieve a 32-division-ratio in the proposed PLL. Since the CP2 in the FLA loop will be closed automatically after phase locking, CP2 will not introduce reference spur. Moreover, rail-to-rail amplifiers in the classical PLL are avoided. Therefore a simple charge pump circuit with feedback [22] is applied in the FLA.

IV. Experiment Results and Discussions

To validate the proposed design concept, a chip-prototype was implemented in TSMC 0.13-μm 1.2-V CMOS process, as shown in Fig. 20. This chip occupies a core area of 0.48 mm $\times$ 0.86 mm excluding PADs and the proposed components of APD/PAC/CP consume very small area. The frequency of reference signal is 66 MHz and the measured PLL output frequency is 2112 MHz. Fig. 21 shows the PLL output phase noise from Agilent Spectrum Analyzer E4440A when we set $V_{\rm tune}$ to 0.55 V. The measured in-band phase noise is -103 dBc/Hz at 100 kHz offset and out-of-band phase noise is -137 dBc/Hz at 10 MHz offset. The in-band phase noise is greatly limited by the reference signal quality. It is already verified by testing the phase noise of the 66 MHz reference signal generated from Agilent E4438C, as shown in Fig. 22. Considering the frequency multiplication, $20\log N$ is added to predict the ideal phase noise of PLL output. If we only consider the reference signal noise contribution to the PLL output, the ideal phase noise is only -108 dBc/Hz at 100 kHz offset. The phase noise of our reference signal is 25 dB higher than the reference signal derived from the low noise crystal oscillator in [4]. It indicates that the reference signal noise contributes significantly to the in-band phase noise of the proposed PLL.

When we decrease the gain control signal $V_{\rm tune}$ to 0.5 V, $\beta_{\rm CP,APD}$ is increased and the PLL bandwidth is extended at the same time, as shown in Fig. 23. However, the in-band phase noise remains the same as in Fig. 21. Note that the phase noise of our PLL is dominated by the other loop noise, and CP is not

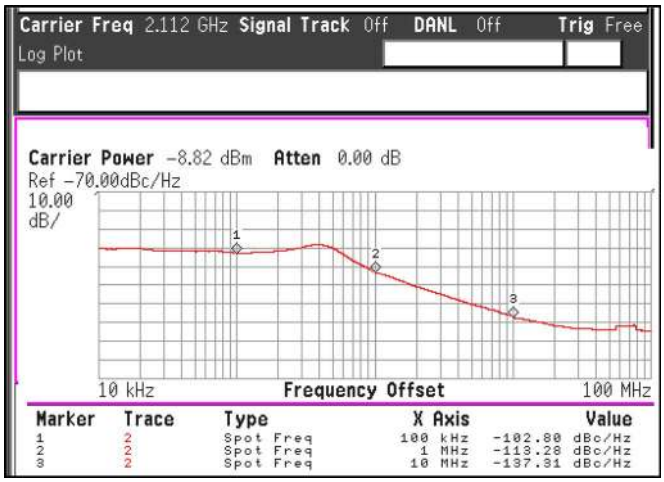

Fig. 21. Measured PLL output phase noise when $V_{\rm tune} = 0.55$ V.

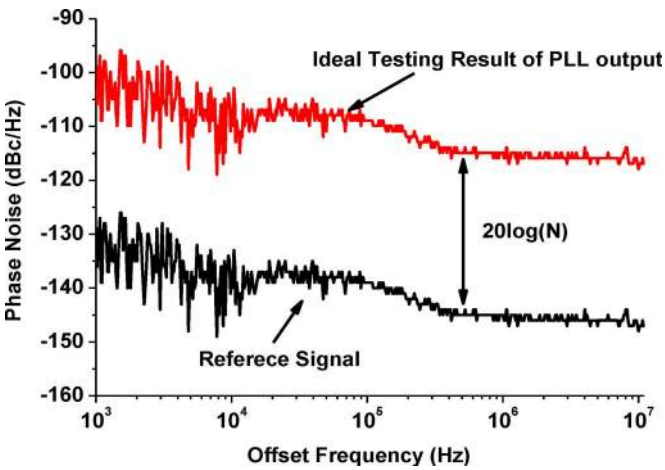

Fig. 22. Measured phase noise of the reference signal.

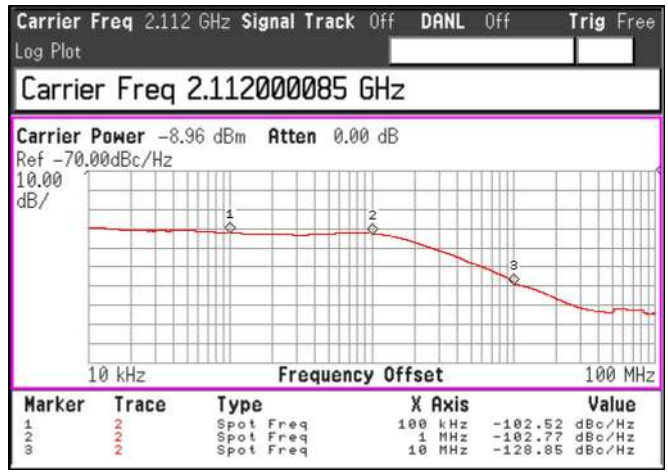

Fig. 23. Measured PLL output phase noise when $V_{\rm tune} = 0.5$ V.

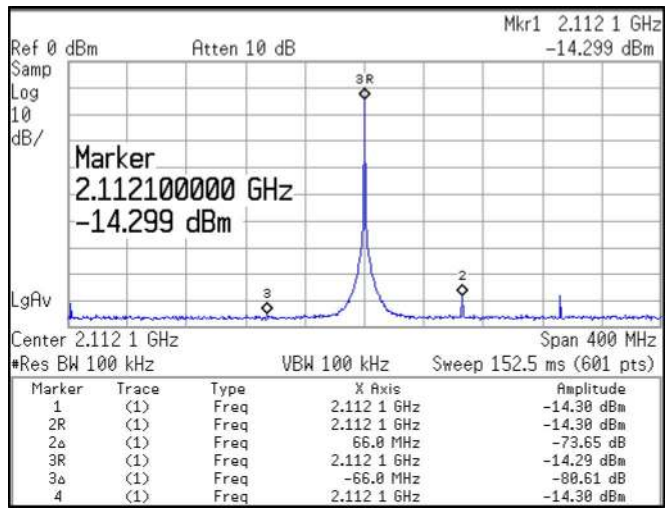

Fig. 24. Measured reference spur of the proposed PLL.

the main in-band noise source any more. This explains why the in-band phase noise cannot be improved when we increase the $\beta_{\rm CP,APD}$. In this case, the small $\beta_{\rm CP,APD}$ and the narrow bandwidth according to the analysis in Section II are beneficial to reduce the phase noise at 1 MHz offset and the jitter of PLL output. The measured phase noise results thereby validate our previous theoretical analysis in Sections II and III.

When the PLL is locked, the power supplies of the dividers and CP2 in FLA are turned off and the reference spur is also measured with Agilent Spectrum Analyzer E4440A to be -80 dBc/-74 dBc at 66 MHz offset as shown in Fig. 24. The VCO dissipates 1.9 mA, and the rest circuits 0.6 mA. The FLA consumes a current of 1.7 mA and is powered down after phase locking. For our PLL, the power consumption blocks are only VCO, buffers and some control circuits. The power contributions from CP and dividers are nearly eliminated. Thus the proposed PLL can achieve an ultra-low power consumption of 3 mW.

Furthermore, to clearly illustrate the locking process of the proposed PLL, the measured locking curve of the proposed PLL is shown in Fig. 25. The locking process is totally different from the classical PLL. In phase 1, the VCO frequency is higher than the REF signal, and the two loops operate at the same time to align the REF and the VCO frequency. In phase 2, the discharging current in CP2 is switched on and $V_{\rm ctrl}$ is decreased at the same moment. This reduces the phase error between REF and VCO gradually. At the end of phase 2, the phase error finally falls into the DZ of FLA and the CP2 in FLA is closed automatically. Afterwards, the main loop dominates the final locking process, as shown in phase 3. As mentioned previously, the FLA operates as coarse tuning and main loop operates as fine tuning in the dynamic locking process. With the use of the dual-loop architecture, the correct frequency locking can be achieved as demonstrated.

Table III summarizes the proposed PLL performance with a comparison of a few published integer-N PLLs. To fairly compare the in-band phase noise with other work, a normalized in-band phase noise is calculated as [24]

$$\pounds_{\rm norm} = \pounds_{\rm in-band} - 20\log N - 10\log f_{\rm ref}. \qquad (32)$$

This work achieves the lowest power dissipation and reference spur as well as a moderate in-band phase noise.

TABLE III
PLL PERFORMANCE SUMMARY AND COMPARISON

	This work	[5] 10' JSSC	[4] 09' JSSC	[12] 09' TMTT	[23] 08' JSSC	[10] 06' TCAS
Freq. (GHz)	**2.112**	2.21	2.21	5	5.2	5.3
CMOS Tech.	**130 nm**	180 nm	180 nm	90 nm	180 nm	180 nm
Fref. (MHz)	**66**	55.25	55.25	1	10	20
Ref. Spur (dBc)	**−80/−74**	−80	−46	−70	−69	−74
In-band Phase Noise (dBc/Hz)	**−103@100kHz**	−121@200kHz	−125@200kHz	−75@10kHz	−76@20kHz	−79@10kHz
Normalized In-band Phase Noise (dBc/Hz^2)	**−211@100kHz**	−230@200kHz	−235@200kHz	−209@100kHz	−200@400kHz	−201@200kHz
Power (mW)	**3.0@1.2V**	3.8@1.8V	7.6@1.8V	11@1.2V	19.8@1.8V	36@1.8V

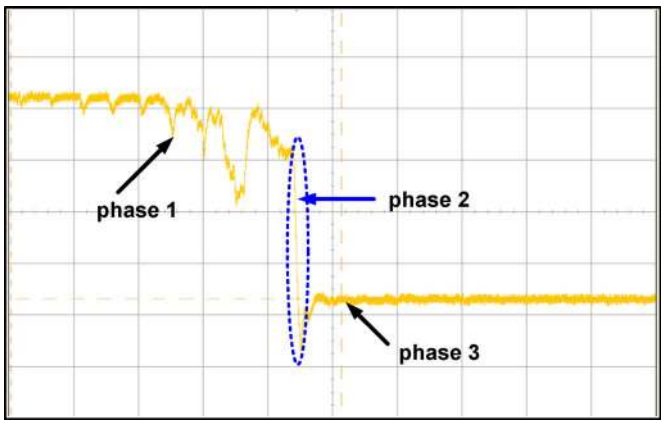

Fig. 25. Measured locking curve of the proposed PLL.

V. CONCLUSION

A 2.1-GHz PLL with low power low reference spur and low in-band phase noise has been presented. By the new phase detection mechanism based on APD/PAC/CP, the amplitudes of CP charging and discharging currents have equal small amplitude with equal pulse width after phase locking. Thus leads to a much low reference spur. Furthermore, compared with the classical PLL, the proposed PLL can increase the CP feedback gain dramatically with the same CP bias current as classical PLL in locked state. Thus the proposed CP contributes a very low noise to the PLL output. Due to the APD, the dividers in the proposed PLL can be turned off in locked state, eliminating the power and noise contributions from the dividers. In addition, a tunable loop gain (with theoretical analysis) is introduced to reduce the PLL integrated phase noise. As such, one can achieve low power consumption, low reference spur. As demonstrated by a chip-prototype in TSMC 0.13 CMOS process, the proposed PLL has a power consumption of 3 mW, a reference spur of -80 dBc/-74 dBc at 66 MHz offset and an in-band phase noise of -103 dBc/Hz at 100 kHz offset.

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