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A DSP-based Active Disturbance Rejection Control Design for a 1-kW H-bridge DC-DC Power Converter

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A DSP-Based Active Disturbance Rejection Control Design for a 1-kW H-Bridge DC–DC Power Converter

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***Abstract*—This paper presents the design and implementation of an advanced digital controller for a 1-kW H-bridge dc–dc power converter. A new control algorithm based on the active disturbance rejection concept is developed to cope with the highly nonlinear dynamics of the converter and the disturbances. An experimental digital control system is used to implement the new control strategy. It consists of a digital control board based on the TMS320C6711 digital signal processor chip, an analogy I/O board, and a complex programmable logic device pulsewidth-modulation generation board. Using a newly developed bandwidth-paramerization technique, an autotuning method based on noise quantification is also developed and tested. Experimental results show the advantages and flexibilities of the new control method for the H-bridge dc–dc power converter.**

***Index Terms*—Autotuning, disturbance rejection, digital signal processor (DSP), H-bridge dc–dc converter.**

I. Introduction

THE dc–dc converter control design problem is a challenging one because of its nonlinear dynamics and external disturbances. This is particularly true for the 1-kW H-bridge converter studied in this research. The H-bridge circuit operates in three different topologies during one duty cycle, which makes it discontinuous and nonlinear. The converter dynamics are also complex and susceptible to electrical magnetic interference, input line voltage disturbance, load disturbance, and single-event upset (SEU), if used in space applications. All of these factors prevent engineers from getting an accurate mathematical model for the converter.

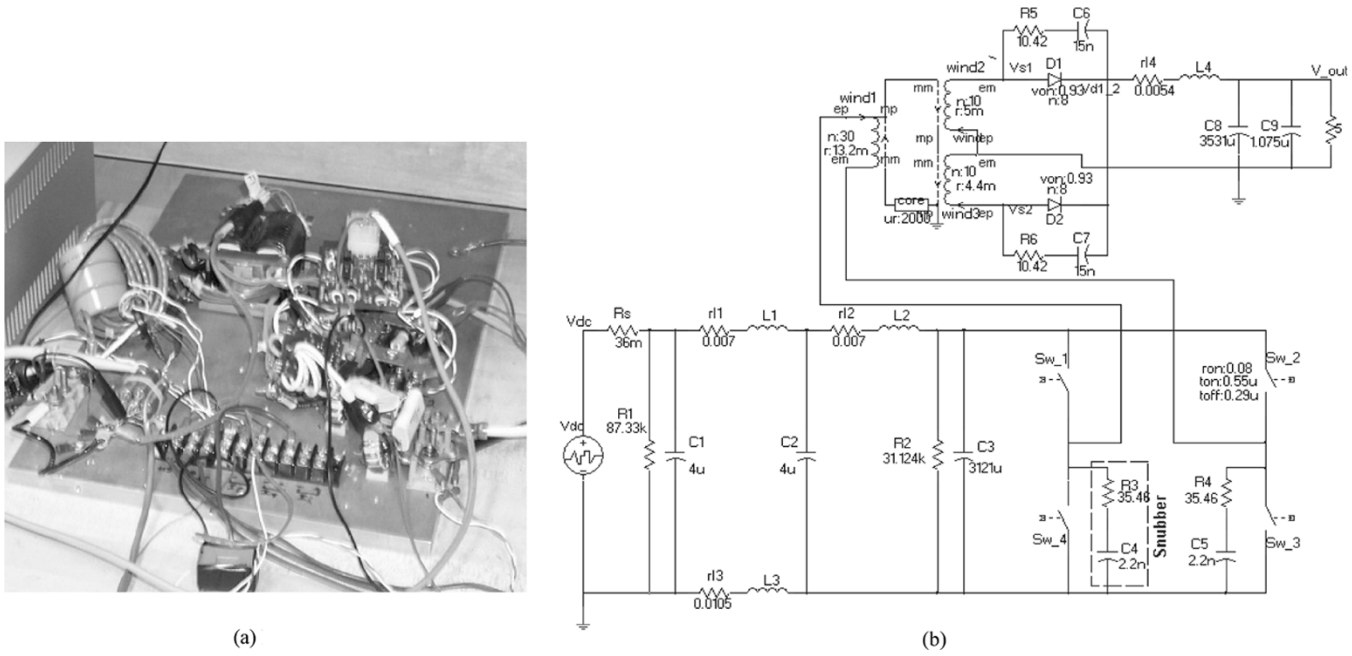
For many years, controllers for dc–dc converters could only be implemented in analog circuits, which limited them to primarily the proportional–integral (PI) form. Although the PI controller proved to be versatile and was successfully used previously in many converter controllers, its performance is obviously quite limited. With the advances of digital control hardware, the digitally controlled dc–dc converter began to appear [1]–[4]. One of the key advantages of a digital controller is its ability to implement sophisticated and/or flexible control algorithms. Digital controllers are also easy to change and test, as well as including lower weight, smaller size, lower implementation cost, and higher reliability and fault tolerance.

As reported in the literature, different digital control algorithms have been developed for dc–dc converters, either in a microcontroller or a digital signal processor (DSP) chip, including nonlinear proportional–integral–derivative (PID), fuzzy logic, adaptive fuzzy, and feedforward control [2]–[4]. They rely on either a mathematical or a heuristic model of the converter. That is, the development of these controllers requires much detailed information about the converter. Mathematical equations are deduced either from experimental data or by circuit analysis. However, in reality, the highly nonlinear characteristic of the converter makes it difficult to obtain an accurate model [5], [6]. On the other hand, the heuristic-based control algorithms such as fuzzy logic and artificial neural networks are usually quite complex and take a long time to develop. In addition, these solutions are not portable, i.e., the control algorithms cannot be easily adjusted and reused for a different problem.

Finally, tuning is an important issue for most of the control methods, especially for nonlinear plants, because it is still done mostly on a trial and error basis. The lack of knowledge in relationship to design objectives and controller parameters could make the tuning process quite tedious.

This paper presents a new converter control algorithm known as Active Disturbance Rejection Control (ADRC). It has the unique characteristics of model independence and it actively rejects both internal and external disturbances. The basic idea of this control strategy is the use of an observer to track the plant dynamics and unknown disturbance in real time and dynamically compensate for it. The purpose of this research is to use this new control method to develop a better digital controller for the 1-kW ED408043-1 Westinghouse H-bridge dc–dc converter, which was designed for NASA to provide reliable, efficient, well-regulated dc–dc power conversion for on-board space electronics. To address the tuning problem, an autotuning method is introduced using a bandwidth-based parameterization technique.

The paper is organized as follows. A brief introduction of a Westinghouse H-bridge dc–dc converter is given in Section II. The ADRC theory is presented in Section III. Hardware implementation and results are provided in Section IV. The autotuning method is developed and implemented in Section V. A conclusionis given in Section VI.



(a) (b)

Fig. 1. ED408043-1 converter. (a) Hardware setup. (b) Circuit diagram.

II. Westinghouse H-Bridge DC–DC Converter

The 1-kW ED408043-1 Westinghouse H-bridge dc–dc converter, which was designed to be used in aerospace, is shown in Fig. 1. This converter was designed to accept an input voltage between 100–160 V dc and provide a regulated and isolated output dc voltage of 28 V for a load of up to 36 A. The frequency of the pulsewidth-modulation (PWM) signal is 20 kHz.

The converter consists of an input electromagnetic interference (EMI) filter, an input low-pass filter, four active switches (MOSFET), two passive switches (diode), a step-down isolation transformer, and an output low-pass filter. The H-bridge operates in the following manner: When switches sw_1 and sw_3 turn on, the input dc voltage is applied on the primary side of the transformer. Next, when switches sw_2 and sw_4 turn on, the input dc voltage is again applied on the primary side of transformer, but in the opposite direction. In the whole duty cycle, the voltage at the primary of the transformer is the combination of these two voltages. Details of the converter can be found in [5].

Through this H-bridge, the dc is changed to ac. Then it goes through a step-down transformer, which has a turns ratio of 3 : 1. The output voltage of the transformer is rectified by two diodes and filtered to provide a 28-V dc output. If the duty ratio is changed, the output voltage also changes. The objective of the control is to use the PWM of the switching devices to accomplish closed-loop voltage regulation.

A transfer function model of this power converter with input line voltage change disturbances and load change disturbance is shown in Fig. 2.

This linear model was developed by applying step input experiments on the converter. The time response data were collected and curve-fit approximations to this data were used to determine the linear transfer function. The readers are referred to [6] for more details.

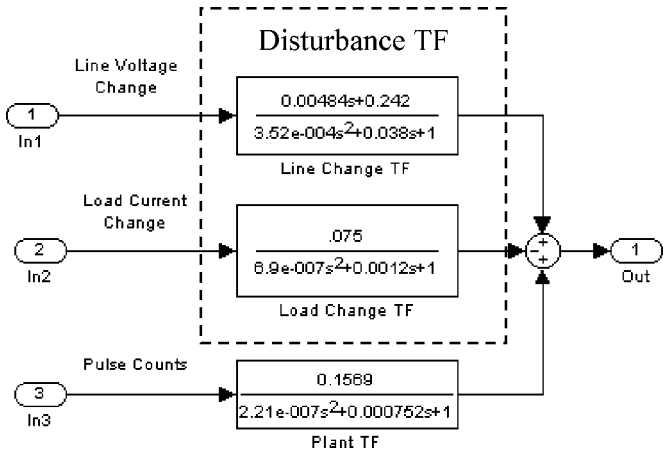


Fig. 2. Linear model of H-bridge converter.

III. Active Disturbance Rejection Control

ADRC [7]–[9] is a relatively new control design concept and method. It is well known that the primary reason for using feedback control is to deal with the variations and uncertainties of the plant dynamics and unknown disturbance from the outside. Consider the linear model in Fig. 2: the converter is approximated as a second-order plant with the form of

$$\ddot{y} = -a_1\dot{y} - a_2 y + w + bu \tag{1}$$

where y is the output, u is the input, and w is the external disturbance. Rewrite it as

$$\begin{aligned}\ddot{y} &= -a_1\dot{y} - a_2 y + w + (b - b_0)u + b_0 u \\ &= f(t, y, \dot{y}, w) + b_0 u\end{aligned} \tag{2}$$

where $f(t, y, \dot{y}, w) = -a_1\dot{y} - a_2 y + w + (b - b_0)u$ represents both the internal dynamics $-a_1\dot{y} - a_2 y + (b - b_0)u$ and the

external disturbance w. Here, b_0 can be seen as the initial acceleration, $\ddot{y}(0)$, for a step input. Most of the existing control design methods require the detailed understanding of $f(t, y, \dot{y}, w)$ before the control design can be carried out. ADRC stipulates that if these disturbances, i.e., $f(t, y, \dot{y}, w)$, can be observed (estimated) in real time, then they can be actively compensated without an explicit mathematical expression of it. In the following section, a new type of observer, the extended state observer (ESO), satisfies this need.

A. ESO and Observer Parameterization

Let $\mathrm{x}_1 = \mathrm{y}$, $\mathrm{x}_2 = \dot{y}$, and $\mathrm{x}_3 = f(t, y, \dot{y}, w)$, and assume $h = \dot{f}(t, y, \dot{y}, w)$ is unknown but bounded, a state-space form of (2) is

$$\begin{cases} \dot{x} = Ax + Bu + Eh \\ y = Cx \end{cases} \tag{3}$$

where $A = \begin{bmatrix} 0 & 1 & 0 \\ 0 & 0 & 1 \\ 0 & 0 & 0 \end{bmatrix}$, $B = \begin{bmatrix} 0 \\ b_0 \\ 0 \end{bmatrix}$, and $C = [1\ 0\ 0]$, $E = \begin{bmatrix} 0 \\ 0 \\ 1 \end{bmatrix}$. A standard linear observer for (3), also known as the Luenberger observer, is

$$\begin{cases} \dot{z} = Az + Bu + L(y - \hat{y}) \\ \hat{y} = Cz \end{cases} \tag{4}$$

where $L = [\beta_1\ \beta_2\ \beta_3]^T$ is the observer gain. As shown in [10], the selection of the observer gains

$$\beta_1 = 3\omega_o \quad \beta_2 = 3\omega_0^2 \quad \beta_3 = \omega_o^3 \tag{5}$$

results in the characteristic polynomial of (4) to be

$$\lambda(s) = s^3 + \beta_1 s^2 + \beta_2 s + \beta_3 = (s + \omega_o)^3. \tag{6}$$

This is known as bandwidth parameterization [10], which greatly simplifies the observer design and tuning by making all observer gains a function of the observer bandwidth, ω_o. The bigger the ω_o, the faster the observer. In practice, this bandwidth is limited by hardware constraints such as noise and sampling rates.

The ESO is unique in that the state is extended (augmented) to include $\mathrm{x}_3 = f(t, y, \dot{y}, w)$. This allows it to be estimated using the observer (4). The parameterized observer gains in (5) make it convenient to tune the observer as fast as it is physically feasible.

B. Control Algorithm and Its Parameterization

Once the observer is built and well tuned, its output will track y, $\dot{y}$, $f(t, y, \dot{y}, w)$, respectively. By canceling the effect of $f(t, y, \dot{y}, w)$ using z_3, ADRC actively compensates for $f(t, y, \dot{y}, w)$ in real time. The controller is designed as follows. First, the control law

$$u = \frac{-z_3 + u_0}{b_0} \tag{7}$$

approximately reduces the original plant (2) to

$$\ddot{y} = u_0 \tag{8}$$

which is a much simpler control problem to deal with. A simple PD controller of the form

$$u_0 = k_p(r - z_1) - k_d z_2 \tag{9}$$

is usually sufficient. To make the controller tuning straightforward, the PD gains can be set as

$$k_p = \omega_c^2 \quad k_d = 2\omega_c \tag{10}$$

which yields an approximate closed-loop transfer function

$$G_{cl} = \frac{\omega_c^2}{s^2 + 2\xi\omega_c s + \omega_c^2}. \tag{11}$$

Similarly to ω_o, ω_c is the bandwidth of the closed-loop control system. Obviously, the bigger the ω_c is, the faster the disturbance rejection. Of course, this bandwidth is also limited by hardware constraints such as actuator saturation and sensor noise.

C. Simulation Result

The ADRC algorithm described above is first tested in simulation, using the Simulink model of the converter, as illustrated in Fig. 2. Measurement noises, quantization errors, line voltage, and load current changes are added to make the simulation as realistic as possible [12]. The ADRC is quite simple to set up and tune. Fig. 3 demonstrates the response of ADRC and its disturbance rejection capability. Note that the startup from 0 to 28 V is fast, smooth, and without an overshoot. More importantly, with two disturbances simultaneously applied at 0.03 s, one is the input line voltage changing from 120 to 100 Vdc and the other is load current changing from 3 to 36 A, the output voltage has less than 1% deviation from the set point, and it recovers within 2 ms. These results were obtained with $\omega_c = 6000$ and $\omega_o = 10\,000$.

IV. DSP-Based Hardware Implementation

A. DSP-Based Digital Controller Architecture

As mention before, a digital controller is chosen because it has many advantages, such as high reliability, more flexibility, lower implementation costs, smaller size, and lower weight, etc. Much work has been done with DSP-based controllers for this H-bridge dc–dc converter [2], [11]. Fig. 4 shows the block diagram of this DSP-based controller.

The output voltage is sensed every 50 μs, and the galvanic isolation is provided by a signal conditioning board. This analog signal is digitized and sent to a DSP computational unit, which executes the ADRC control signal and outputs the new PWM duty ratio. A CPLD PWM device is then used to convert the duty ratio to a PWM signal. This PWM signal goes through a gate driver board to drive the MOSFETs of the converter.

The CPLD is used to offload the task from the DSP and provide a fail-safe feature for the controller. If the DSP fails for

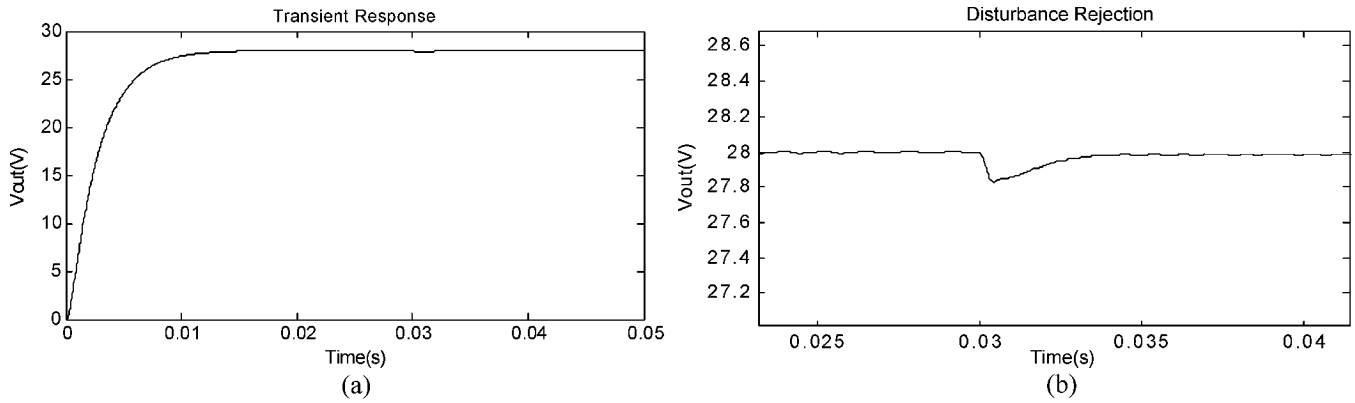


Fig. 3. Transient response and disturbance rejection of ADRC. (a) Transient response. (b) Disturbance rejection (zoomed in).

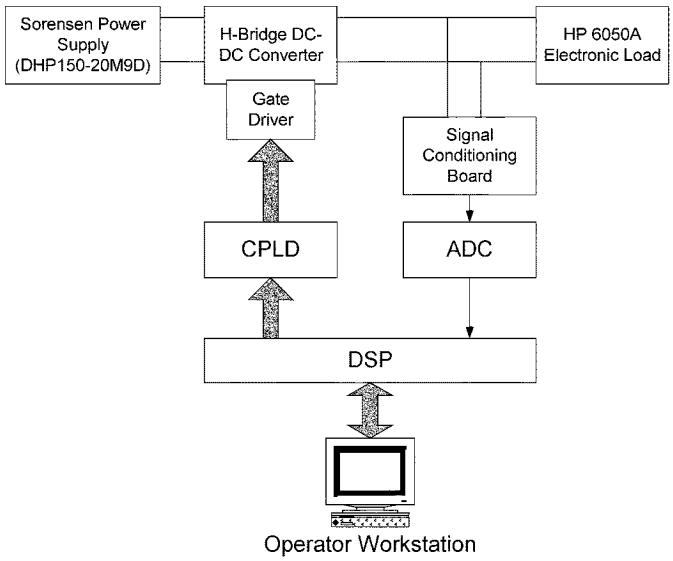


Fig. 4. Digital control development platform block diagram.

Fig. 5. Stand-alone DCDS.

some reason, the CPLD will continue to generate PWM signals based on the last duty ratio.

Fig. 5 is a photograph of the stand-alone Digital Control Development Station (DCDS).

There are three boards in this unit. The bottom one is a TI development kit unit featuring the TMS320C6711 DSP processor. The middle board is a prototyping board on which custom CPLD circuitry has been implemented for PWM generation. The top board is a TI multichannel A/D board for digitizing the conditioned analog sensor signals.

B. Software Development and Testing Results

The Code Composer Studio v1.2, which comes with the Digital Control Development Station's 6711 DSP, is used to implement and test the ADRC control algorithm. The algorithm is written in C, and then compiled, debugged, and linked via Code Composer. An output file is generated and then downloaded into the DSP. A watch window is provided by Code Composer. Through the watch window, the variable values can be set and retrieved while the system is running. This feature makes tuning control variables on-the-fly possible.

The tuning process is as follows: estimate b_0 (which can also be determined by experiment), set initial values of ω_o and ω_c; increase them gradually until the noise level and oscillation in the control signal and output exceed the tolerance. Note that the converter behaves differently as the load is increased or removed. For load increase, the converter gets more power from the source by increasing the duty ratio. For load removal, however, since the current cannot go back to the source because of the diodes, the power stored in the output capacitors can only be dissipated by the load. To deal with this discrepancy, different ω_o and ω_c are used for different load disturbances, although they are very close.

The experimental comparison of ADRC with a well-tuned PI controller [13] is shown in Figs. 6 and 7. Two extreme scenarios are used to test disturbance rejection: one is a load step-up (from 3 to 36 A), the other is load step-down (from 36 to 3 A). The results are also shown in Table I. ADRC clearly shows a marked improvement in terms of output voltage deviation from the set-point and in terms of recovery time in both test scenarios. Furthermore, the ADRC transient response at the maximum load of 36 A, as shown in Fig. 8, demonstrates a smooth transition from 0 to 28 V.

Robustness tests were carried out using the following tests: 1) sweep the load currents from 3 to 36 A and back with an interval of 1 A, while keeping the input voltage at 120 Vdc; 2) randomly change load current between 3–36 A while the input voltage is fixed at 120 Vdc; and 3) randomly change the load current between 3–36 A, and the input voltage between 110–140

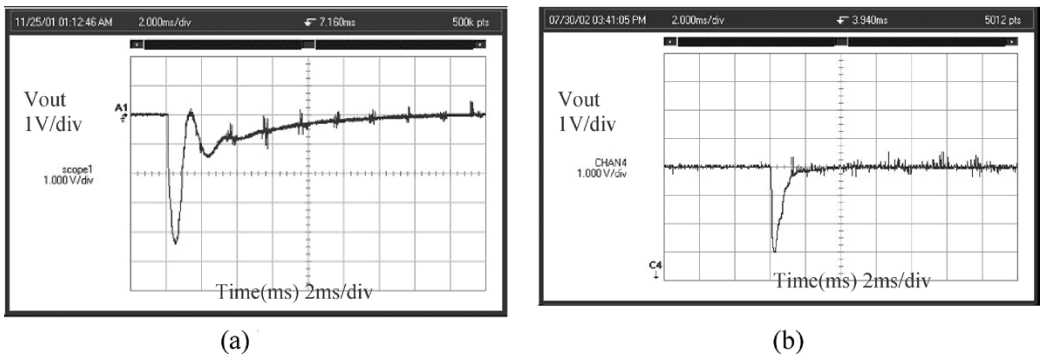


Fig. 6. PI and ADRC disturbance rejection comparison: load step-up. (a) PI controller. (b) ADRC.

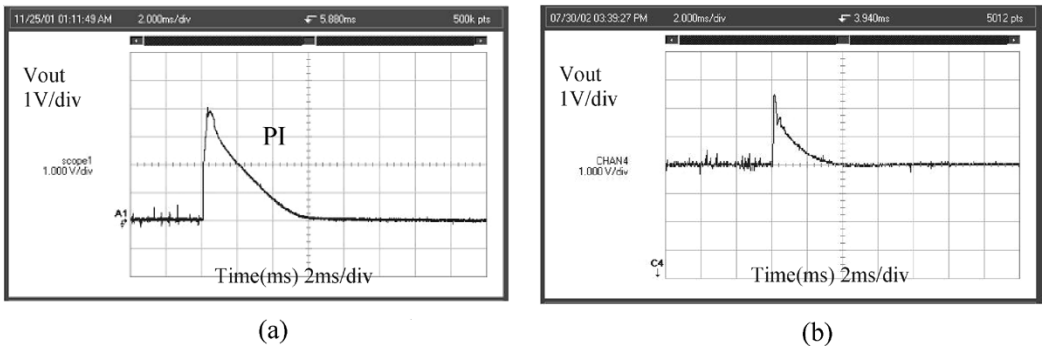


Fig. 7. PI and ADRC disturbance rejection comparison: load step-down. (a) PI controller. (b) ADRC.

TABLE I
LOAD DISTURBANCE REJECTION COMPARISON

Deviation of Voltage (V)	PI	ADRC	Improvement
Step-Up	4.34	3.0	1.34
Step-Down	3.9	2.6	1.3

Recovery time (ms)	PI	ADRC	Improvement
Step-Up	13	2.0	11
Step-Down	7	3.1	3.9

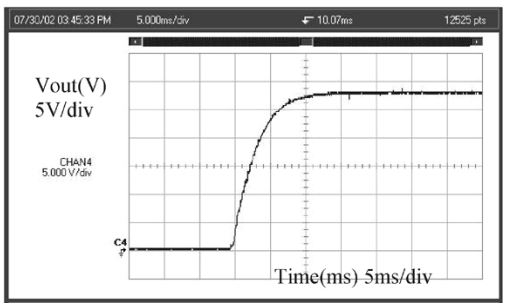


Fig. 8. Transient response at 36 A.

Vdc at the same time. The ADRC controller for the Westinghouse converter was found to be robust and stable under all these conditions.

V. AUTOTUNING

As mentioned above, the ADRC control algorithm has only two tuning parameters, ω_o and ω_c, which represent the bandwidth of the observer and the controller, respectively. The bigger the ω_o and ω_c, the faster the disturbance is observed and rejected by the controller. More details this tuning process can be found in [10].

Theoretically, ω_o and ω_c can be made very large, but the presence of sensor noise and practical considerations, such as the smoothness of the control signal, prevent ω_o and ω_c to be increased beyond certain point. For every application, there is an optimal bandwidth where the performance is maximized subject to the physical constraints. In dc–dc converter applications, it appears that the tradeoff is between the bandwidth of the control loop and the noise level in the control signal. If the noise of the control signal is quantified and a tolerance level is established, then the closed-loop bandwidth can be automatically adjusted to match a given noise tolerance level. This would be an entirely new way of tuning for controllers in general and ADRC in particular.

A. Noise Quantification

The noise level in the control signal is an important measure that affects performance and the health of the actuator in a feedback control system. To use it as criteria in the autotuning process, it must be quantified mathematically. Given a control signal data set, one indicator of the noise level is its standard

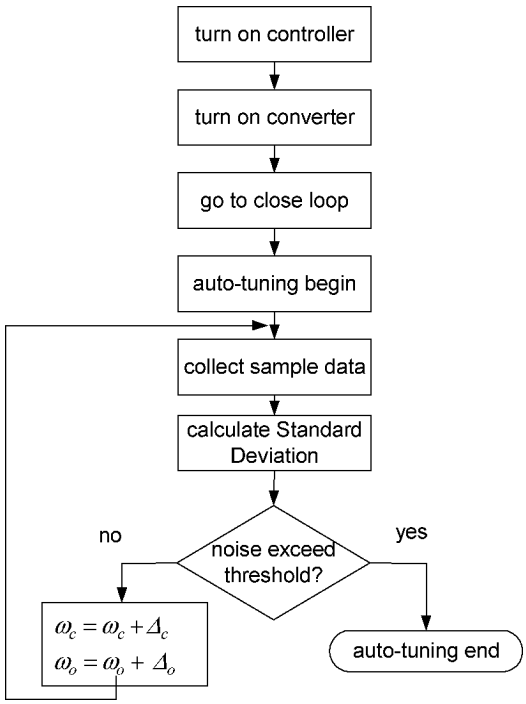


Fig. 9. Flowchart of autotuning.

deviation. Let $\mathrm{U} = \{u_1, u_2, \ldots, u_n\}$ be a set of n sampled control signal, the noise level indicator is defined using the standard deviation

$$s = \sqrt{\frac{1}{n-1}\sum_{i=1}^{n}(u_i - \overline{u})^2}, \qquad \overline{u} = \frac{1}{n}\sum_{i=1}^{n} u_i. \tag{12}$$

When the sampling rate is relatively fast compared to the rate of change in the control signal, the bigger the noise level is, the bigger the standard deviation s, while the average of control signal $\overline{u}$ changes very little. The accuracy of this measure depends on the length of the data set, the sampling rate, and the speed of change in the control signal. When the output is close to a steady state, which corresponds to a fixed PWM duty ratio u, this noise measure is especially effective.

B. Hardware Implementation and Results

The autotuning process is illustrated in Fig. 9. First, turn on the converter and controller, then go to closed-loop control mode. Set initial values of ω_o and ω_c to be small, and the output will reach steady state. Once it is in steady state, turn on the autotuning algorithm, and it will collect n (20 in this case) sampled control signals and calculate the standard deviation. If the standard deviation is less than the given threshold, increase ω_o and ω_c by a predetermined small size, then collect another n sampled control signals and repeat the procedure. Once the standard deviation reaches the given threshold, autotuning is completed.

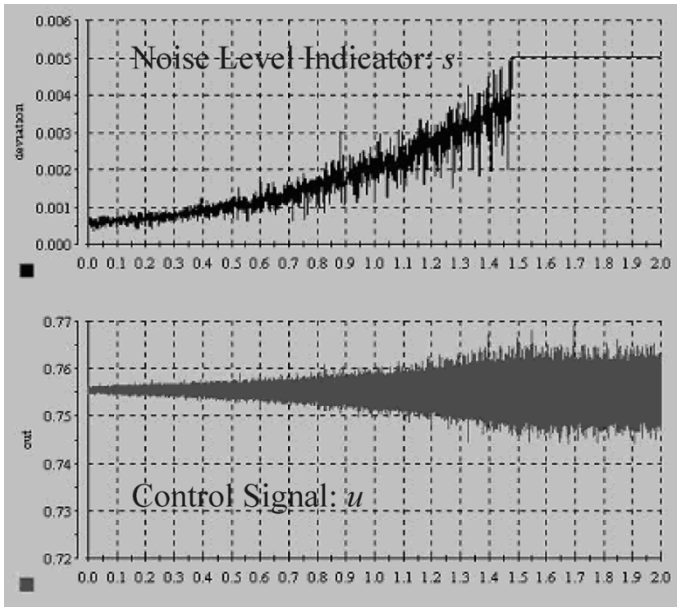


Fig. 10. Noise level indicator and control signal during autotuning.

As mentioned above, all calculation tasks must be done in 50 μs. To save execution time and memory in the DCDS, the calculation of (12) is implemented in an equivalent form of

$$s = \sqrt{\frac{1}{n-1}\left(\sum_{i=1}^{n} u_i^2 - 2 \times \overline{u} \times \sum_{i=1}^{n} u_i + n \times \overline{u}^2\right)}. \tag{13}$$

In every sampling cycle, the $\sum u_i^2$ and $\sum u_i$ are calculated, only after getting all n samples, the average $\overline{u}$ and the standard deviation s are then calculated.

The ControlDesk in the dSPACE platform is used instead of the stackable DSP since the ControlDesk can track variables continuously. This makes it easier to plot the standard deviation and control signal in real time. Also, variables values can be set and retrieved in ControlDesk while the system is running, which makes it possible to adjust the variables in the autotuning algorithm, such as the sample number n, the step size $\Delta\omega_o$ and $\Delta\omega_c$, the noise level threshold, in real time. Consequently, the autotuning algorithm is quickly set up successfully.

The behaviors of the noise-level indicator s and the corresponding control signal u are shown in Fig. 10 during the autotuning process. Clearly, as ω_o and ω_c are increased, the noise in control signal u is also increased, which is reflected in the noise level indicator, s. As s reaches a predetermined threshold, ω_o and ω_c are locked and the autotuning is complete.

VI. Conclusion

A new control algorithm and an autotuning method have been developed for a 1-kW H-bridge dc–dc power converter. The new controller is, firstly, model independent, which makes it easier to design and more tolerant of nonlinear dynamics. Secondly, the new control algorithm actively estimates the effects of the disturbance on the converter and compensates for it in real time. This results in a better disturbance rejection performance, as is shown in experimental results. A stand-alone DCDS with

TMS320C6711 DSP chip has been employed for the realization of the digital control scheme. An autotuning method based on noise quantification, which makes the tuning process simple and automatic, has been developed and tested successfully.

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