A Dual-Mode NAND Flash Memory: 1-Gb Multilevel and High-Performance 512-Mb Single-Level Modes

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***Abstract*—A 116.7-mm^2 NAND flash memory having two modes, 1-Gb multilevel program cell (MLC) and high-performance 512 -Mb single-level program cell (SLC) modes, is fabricated with a 0.15-μm CMOS technology. Utilizing simultaneous operation of four independent banks, the device achieves 1.6 and 6.9 MB/s program throughputs for MLC and SLC modes, respectively. The two-step bitline setup scheme suppresses the peak current below 60 mA. The wordline ramping technique avoids program disturbance. The SLC mode uses the 0.5-V incremental step pulse and self-boosting program inhibit scheme to achieve high program performance, and the MLC mode uses 0.15-V incremental step pulse and local self-boosting program inhibit scheme to tightly control the cell threshold voltage V_{th} distributions. With the small wordline and bitline pitches of 0.3 -μm and 0.36-μm, respectively, the cell V_{th} shift due to the floating gate coupling is about 0.2 V. The read margins between adjacent two program states are optimized resulting in the nonuniform cell V_{th} distribution for MLC mode.**

***Index Terms*—CMOS memory integrated circuits, EPROM, flash memory, floating gate coupling, multilevel programming, multilevel programmed cell, NAND flash memory, wordline ramping.**

I. Introduction

EMERGING portable mass storage applications, such as digital still cameras, digital audio players, personal digital assistants, and electronic books, have accelerated the development of high-density flash memories. Nowadays, such applications require high-performance flash memories as well. From this viewpoint, NAND flash memories have great potential because they have very small unit cells and operate by multibyte unit, which leads to low bit cost and high data throughput. A multilevel program cell (MLC) technique drastically reduces the bit cost, doubling or even tripling the memory density with the same chip size of NAND flash memory using the single-level program cell (SLC) technique. However, the need for tight threshold voltage V_{th} control decreases the program performance. Therefore, MLC NAND flash memories are suitable for low bit cost and high-density applications, such as digital audio players which require CD-quality music recording with somewhat low program throughput, while SLC NAND flash memories are suitable for high-performance applications, such as digital still cameras which require high program throughput.

Though MLC NAND flash memories have very low bit cost, they have been deprived of their market by SLC NAND flash memories even in the low-performance market. This comes from the small gap of time-to-market between MLC and SLC NAND flash memories having the same density. Nowadays, the density of SLC NAND flash memory grows twice a year while the chip size remains the same from density to density. Therefore, MLC NAND flash memories based on SLC NAND technology should be developed at the same time to take the advantage of the higher density with the same chip size. In this paper, we report the dual-mode NAND flash memory having 1-Gb MLC and 512-Mb SLC modes with the slightly increased chip size compared to a only 512-Mb SLC NAND flash memory. The mode selection is not opened for general use, but provided for simultaneous development of the MLC and SLC NAND flash memory.

It is well known that the incremental step pulse programming (ISPP) scheme can effectively adjust a cell V_{th}, because a cell V_{th} follows the ISPP step pulse [1]. Therefore, the cell V_{th} distribution can be tightly controlled by decreasing the ISPP step pulse at the expense of program performance. Also, the local self-boosting (LSB) scheme, which can be achieved by keeping the wordlines adjacent to selected wordline 0 V, is more effective in reducing the widening of cell V_{th} distribution due to program disturbance than the self-boosting scheme [2]. However, the LSB scheme restricts the programming order to ascending order. The key to dual-mode NAND flash memory is not sacrificing one mode for the other mode. The SLC mode uses 0.5-V ISPP step pulse to achieve high program throughput, and the self-boosting scheme to provide random-order page programming, while the MLC mode uses 0.15-V ISPP step pulse to tightly control the V_{th} distribution, and the LSB scheme to reduce the program disturbance.

The memory is fabricated on a 0.15-μm CMOS process with a die size of 116.7 mm^2. The effective cell size is 0.14 μm^2. The chip architecture is determined to minimize the chip size, the skew of page-buffer control signals, and the noise distribution. The detailed device organization is shown in Section II. With such small cell transistors, a bitline precharge-and-sense scheme [3] is adopted to sense the bitline for specific length of time. In order to improve program throughput, a 4× program mode (4× PGM) is adopted by dividing the cell array into four banks. However, the 4× PGM operation generates a large peak current that should be reduced. A two-step bitline setup scheme reduces the peak current. In addition, a wordline ramping technique suppresses the wordline-coupling that causes a serious program disturbance for the memory with small wordline pitch. The bitline precharge-and-sense scheme, the two-step bitline setup scheme, and the wordline ramping technique are presented in Section III.

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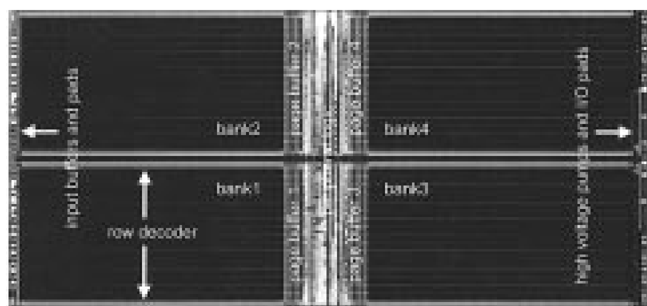


Fig. 1. Chip micrograph.

The widening of MLC $V_{\rm th}$ distribution due to a floating gate (FG) coupling has not been reported yet, but it would limit the scaledown of MLC NAND flash memory cell pitches. An optimization of the MLC $V_{\rm th}$ distribution with the FG coupling, in consideration, is the key to MLC design for high program speed. This is described in Section IV.

II. Chip Architecture

Fig. 1 illustrates the micrograph of the dual-mode NAND flash memory. The 1-Gb MLC array is divided into four banks. The four banks are arranged in a 2 × 2 matrix, with page buffers located on one side facing the chip center to minimize the chip size and the skew of control signals. The input control buffers are located near the input control pads, which are far from the internal noise sources such as page buffers and high-voltage charge pumps. Cells in each bank are organized in a single 16-k row by (8 k + 64) column array. Sixteen rows form a block and 1 k block decoders are split into left and right side of each bank so that a block decoder layout can be drawn within a two block pitch to accommodate the tight wordline pitch of 0.3 μm. The extra 256-column so-called spare data field is typically used to store system data and/or ECC data. Each 1-b sense-and-latch (SL) unit of a page buffer shares two adjacent bitlines in order to minimize the overall page buffer size and also to make page buffer layout easy. One 2-b SL unit comprised of two 1-b SL units is shared by four adjacent bitlines through an SLC option transistor, which allows 1-Gb MLC NAND flash memory to operate as 512-Mb SLC NAND flash memory. The SL sharing divides a row of 8 k cells into four pages to have unit program depth (512 B + 16 B) compatible with the unit of conventional SLC NAND flash memory. The page buffer schematic diagram is shown in Fig. 2. Program and read operations are performed in one page unit therefore the unselected bitlines, 3/4 of 8 k bitlines, should be shielded during the operations. Erase is performed in two block units of 64 kB.

For the SLC mode, the 1-b SL unit is shared by two adjacent bitlines, which divides a row of 8 k cells into two pages. One half of 8 k bitlines are shielded during program and read operations, and the erase unit is a block of 16 kB.

III. Issues

A load-current sensing method is no longer practical because the small size of the cell reduces the worst-on-cell current to only 0.5 μA, which is insufficient to sense the bitline within given time. Instead, the bitline precharge-and-sense scheme is adopted [3]. During read operation, the unselected line(s) between adjacent selected bitlines are shielded to ground level. The selected bitlines are rapidly precharged to 1.0 V by fully turning on the PRE transistors and setting the corresponding SBL level to 1.6 V, while the unselected SBL level is 0 V. Then the bitline levels are split by on cell states and off cell states where the selected SBL transistors are turned off. Finally, the small splitting of the selected bitline level is amplified by setting the selected SBL level to 1.0 V and reflected on the sense out (SO) node to V_{cc} and 0 V, where the SBL transistors coupled to on-cell transistors are turned on and the SBL transistors coupled to off-cell transistors are turned off. Consequently, the SLs can sense and latch the on and off cell states with sufficient sense margin.

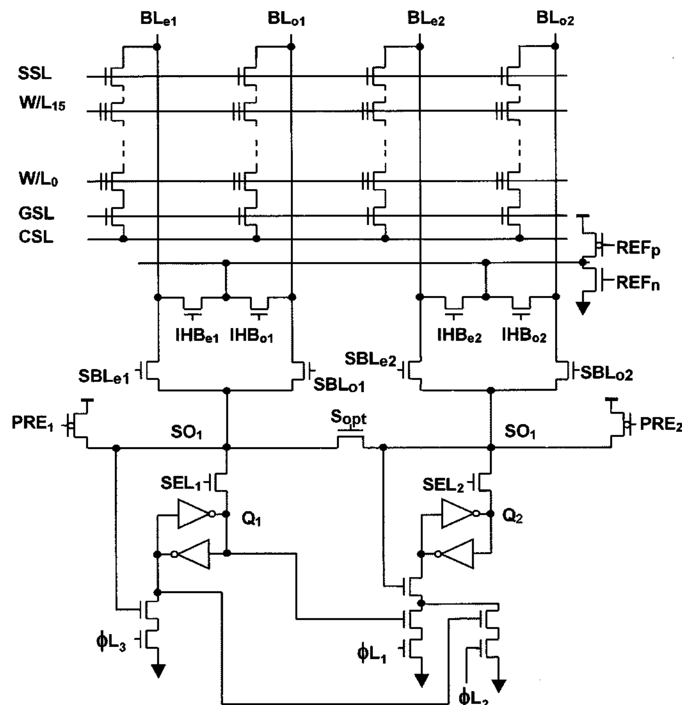


Fig. 2. Simplified schematic diagram of the sense-and-latch unit(s) and four strings.

Bitlines should be set to V_{cc} or 0 V before program voltage is applied to the selected wordline. The worst case occurs in 4× PGM for SLC mode when all selected bitlines should be programmed. In that case, the inhibited bitlines adjacent to the selected bitlines should be charged to V_{cc}, whereas the selected bitlines remain at 0 V. A long bitline setup process degrades program performance because it is performed every ISPP steps. On the other hand, a short bitline setup process generates large peak current. We adopt the two-step bitline setup scheme. For the first 2 μs, all bitlines are charged up to V_{cc} with constant current supplied by the pMOS coupled to IHB transistors. Then for the next 2 μs, the selected bitlines are selectively discharged to ground level according to the latched data. The peak discharge current is suppressed by stepping the SEL level. Finally, another 1 μs is needed to stabilize the bitline setup sequence. The bitline setup sequences are schematically shown in Fig. 3.

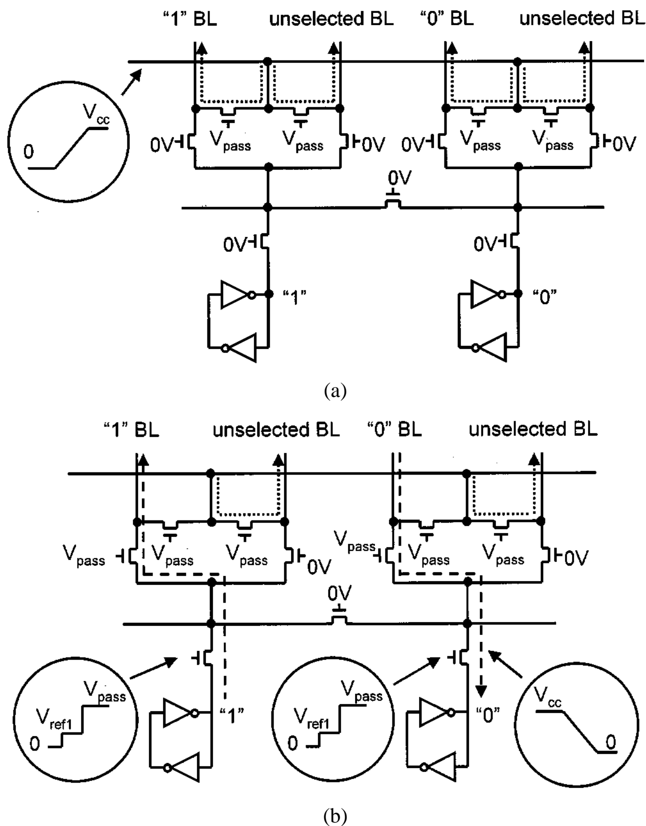


Fig. 3. Two-step bitline setup sequence. (a) Precharge all bitlines. (b) Selectively discharge bitlines coupled to "0"-loaded sense-and-latch.

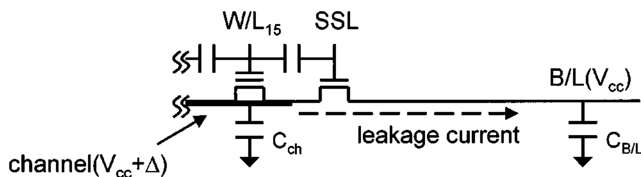


Fig. 4. Schematic of W/L_{15} to SSL coupling.

Fig. 4 is a schematic diagram showing the wordline coupling problem. During the program operation which utilizes the LSB scheme, the SSL level of the selected block is set to V_{cc} and the program inhibit bitlines are set to V_{cc} so that the program inhibit strings are precharged to V_{cc}–$V_{\rm th}$ and the corresponding SSL transistors are shut off. The channel underneath the selected wordline is localized once a program pass voltage $V_{\rm pass}$ is applied to all wordlines except the selected wordline and the wordlines adjacent to the selected one. After the $V_{\rm pass}$ is stabilized, a program voltage $V_{\rm pgm}$ applied to the selected wordline boosts only the localized channel. Therefore, it is important to decouple the localized channel from the others to increase the efficiency of LSB. The worst case occurs when the W/L_{15} is selected. When the $V_{\rm pgm}$ is applied to the W/L_{15}, the SSL is coupled to W/L_{15} and the boosted level is around 1.4 V if any efforts to reduce the $V_{\rm pgm}$ slope are not made. Even though the string select transistor is in the subthreshold regime, the localized channel loses its charges in an instant because the channel capacitance is rather small, about 0.5 fF. Therefore, the program-inhibited cells are disturbed by the $V_{\rm pgm}$. It becomes more serious with low V_{cc}, because the lower bitline precharge level decreases the body effect of the SSL transistor, and hence the effective threshold voltage $V_{\rm th}$. Fig. 5 shows the I_d–V_g characteristics of an SSL transistor with the various V_{cc} (effective body bias) levels. In the case of V_{cc} equal to 2.0 V, the localized channel charges are swept away by about 200 nA where the boosted level is about 1.4 V, which lowers the localized channel potential by 5 V in 30 ns. Therefore, it is impossible to inhibit cells by the LSB scheme.

A voltage-ramping technique is used to suppress the wordline coupling. However, there is a tradeoff between program efficiency and wordline coupling suppression efficiency. Fig. 6(a) shows the peak coupling level between W/L_{15} and

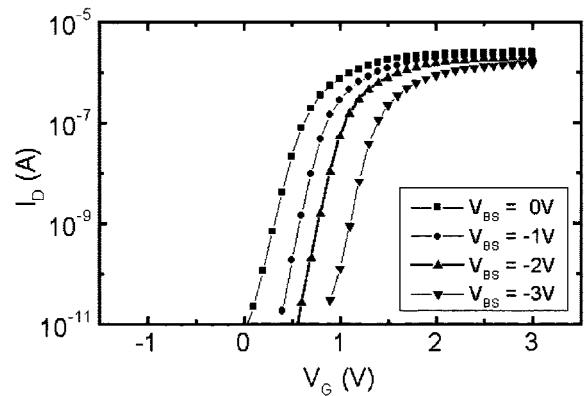
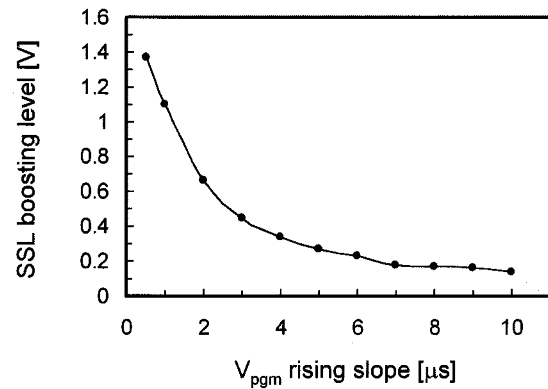


Fig. 5. SSL transistor I_d–V_g characteristic with various body bias.



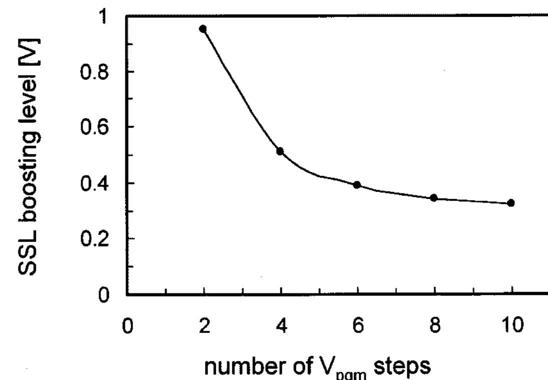


Fig. 6. Peak coupling between W/L_{15} and string-select-line transistor with (a) $V_{\rm pgm}$ rising time and (b) the number of $V_{\rm pgm}$ steps within 5 μs at a ISPP step.

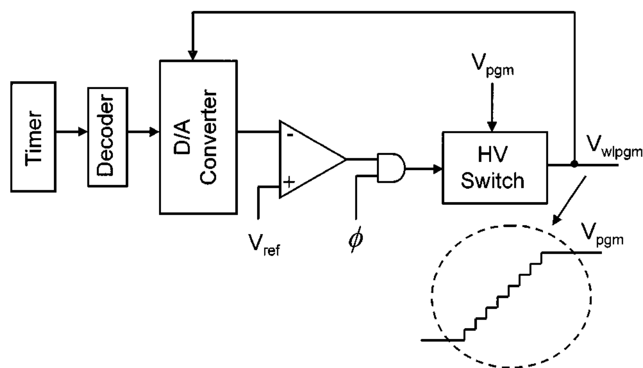


Fig. 7. Schematic of ramping circuit.

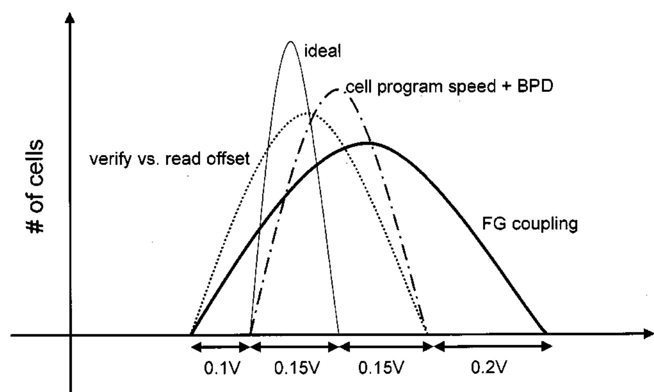


Fig. 8. Ideal V_{th} distribution width and the real V_{th} distribution widened by parasitic effects.

SSL coupling level with the V_{pgm} rising time, where the shape of the ramping output is ideal. As shown in Fig. 6(a), the wordline-to-SSL coupling suppression efficiency is rapidly increased with V_{pgm} rising time until 5 μs. We adopt a staircase wave form generator instead of an ideal ramping circuit because the layout overhead of the ideal ramping circuit is large. Fig. 6(b) shows the wordline-to-SSL coupling level with the number of ΔV_{pgm} steps for given 5 μs. The ramping efficiency is saturated after eight steps, as shown in Fig. 6(b). According to these simulation results, we designed the wordline ramping circuit to have eight ΔV_{pgm} steps in 5 μs.

The ramping circuit is comprised of a timer, a decoder, an 8-b digital-to-analog (D/A) converter, a comparator, and a high-voltage switch pump (HVSP), as shown in Fig. 7. The D/A converter divides the V_{wlpgm} at a given step. The HVSP raises V_{wlpgm} until the output of the D/A converter is equal to the reference voltage V_{ref}. At the next step, the change of input digital coding lowers the output level of the D/A converter below the V_{ref} and the HVSP raises V_{wlpgm} until the V_{wlpgm} reaches the target value (V_{pgm}). As a result, the wordline-to-SSL coupling is reduced to 0.4 V to have lower than a few picoamperes subthreshold current of the SSL transistor, which drastically reduces the program disturbance caused by wordline coupling.

IV. Threshold Voltage Distribution

Fig. 8 shows how much the parasitic effects widen the ideal V_{th} distribution. The ideal cell V_{th} width should be slightly smaller than the stepping voltage of the ISPP (ΔISPP) if the

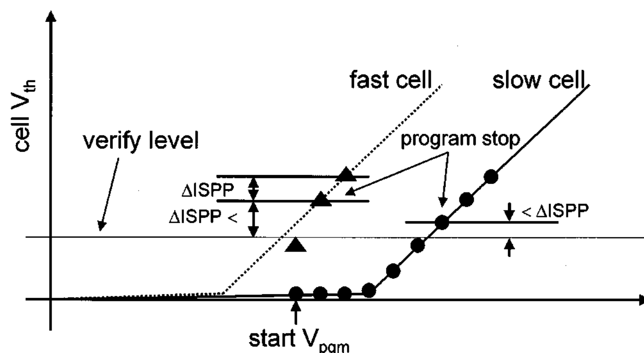


Fig. 9. Nonideal ISPP behavior of fast cell in an early ISPP step and the ideal V_{th} level of slow cell after verify operation.

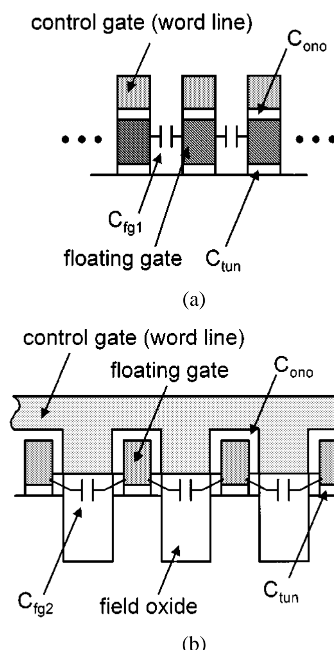


Fig. 10. Schematic cross-sectional view of the NAND flash memory cell array and the parasitic capacitance between adjacent two floating gates. (a) C_{fg1} in the bitline direction. (b) C_{fg2} in the wordline direction.

cell program speeds are the same for all the cells. Unfortunately, there exists process variation, which widens the cell V_{th} distribution width even without any noise. This is schematically shown in Fig. 9. The cell V_{th} shift follows the ΔISPP after the floating gate of the cell transistor is saturated. Therefore, the start program voltage should be lower than the critical voltage at which the programming of the fastest cell starts, so that the fastest cell can be saturated before the cell V_{th} reaches verify level. The low start program voltage, however, degrades the program performance. In this process, the ΔISPP of 0.15 V is used to reduce the ideal cell V_{th} distribution width for MLC mode at the expense of program performance compared to the previous design [2], while the ΔISPP of 0.5 V is used for the SLC mode to achieve high program performance. The cell V_{th} shift due to the nonuniformity of cell program speeds and the system noise is about 0.1 V.

The FG coupling arises from the parasitic capacitance between adjacent two floating gates in a string and in a wordline as shown in Fig. 10(a) and (b). If we assume that the cell tran-

sistor that is being read is fully turned on, the FG coupling ratio in a string $\gamma_{\rm fg1}$ and in a wordline $\gamma_{\rm fg2}$ can approximately be expressed as

$$\gamma_{\rm fg1} = \frac{C_{\rm fg1}}{C_{\rm ono} + C_{\rm tun} + 2C_{\rm fg1}} \quad (1a)$$

and

$$\gamma_{\rm fg2} = \frac{C_{\rm fg2}}{C_{\rm ono} + C_{\rm tun} + 2C_{\rm fg2}} \quad (1b)$$

where $C_{\rm ono}$ is the capacitance between a control gate and a floating gate, $C_{\rm tun}$ is the capacitance between a floating gate and a channel, and $C_{\rm fg1}$ and $C_{\rm fg2}$ are the capacitance between adjacent two floating gates in a string and in a wordline, respectively. The order of page program is restricted to ascending order in a block because the random order of page programming significantly shifts the cell $V_{\rm th}$ when LSB scheme is used [2]. Therefore, in the worst case a cell is coupled by five neighbor cells; the right, left, upside, upper right, and upper left cells. If we ignore the effect of upper right and upper left cells, the change of cell $V_{\rm th}$ read from the control gate after five neighbor cells are programmed can be written as

$$\Delta V_{\rm th}^{(p,q)} = \gamma_{\rm fg1}\Delta V_{\rm th}^{(p,q+1)} + \gamma_{\rm fg2}\Delta V_{\rm th}^{(p-1,q)} + \gamma_{\rm fg2}\Delta V_{\rm th}^{(p+1,q)} \quad (2)$$

where p and q denote the pth bitline and the qth wordline, respectively. In the worst case, the neighbor's $V_{\rm th}$ shift from the erase state ("11") to the highest program state ("00"), $\Delta V_{11\rightarrow 00}$, and the FG coupling can be simplified as

$$\Delta V_{\rm th}^{(p,q)} = (\gamma_{\rm fg1} + 2\gamma_{\rm fg2})\Delta V_{11\rightarrow 00} \text{ for MLC mode.} \quad (3)$$

In this process, the worst FG coupling is about 0.2 V where $\gamma_{\rm fg1} \approx 0.02$, $\gamma_{\rm fg2} \approx 0.006$, and $\Delta V_{11\rightarrow 00} \approx 5.4$ V. The FG coupling can be reduced by lowering the height of the floating gates and the thickness of field oxide facing the floating gates. Lowering the floating gate height, however, degrades the program performance because it lowers the $C_{\rm ono}$, hence the program coupling ratio, $\gamma_{\rm pgm} = C_{\rm ono}/(C_{\rm ono} + C_{\rm tun})$. The thickness of the field oxide affects the isolation between adjacent two cells. Therefore, the FG coupling, program performance, and cell isolation should be carefully optimized. The total coupling of the worst case should be modified for SLC mode utilizing self-boosting scheme as

$$\Delta V_{\rm th}^{(p,q)} = 2(\gamma_{\rm fg1} + \gamma_{\rm fg2})\Delta V_{1\rightarrow 0} \quad (4)$$

because the random order of page is permitted. Therefore, the worst FG coupling for SLC mode is about 0.2 V where $\Delta V_{1\rightarrow 0} \approx 4$ V.

The differences of noise levels such as pocket p-well (p-pwell) noise, common source line (CSL) noise, and power noise between program verify operation and read operation cause an underprogram of 0.1 V. In early ISPP step, just a few cells (fast cells) are programmed. In that case, almost whole bitlines are discharged from the precharged level to ground level except a few bitlines coupled to the programmed cells. The CSL level rise high by the discharge current because of the CSL resistance, which effectively leads to the positive body bias of the fast cells. Consequently, the CSL noise reduces the sensing current of fast cells. The CSL noise may not be a problem if the same amount of CSL noise exists during read operation because the cells feel the same body bias. However, there is no CSL noise after all cells are programmed in a page. Thus, the SLs sense larger sensing current during read operation than during program verify operation for the same selected wordline level. This causes the underprogram problem. Therefore, the selected wordline level should be lower during read operation than during program verify operation, which means underprogram margin. Decreasing the CSL resistance can reduce the CSL noise at the expense of chip size. An undershooting of p-pwell noise caused by the capacitive coupling between bitlines and p-pwell is added to the CSL noise. The p-pwell straps in a cell array reduce the p-pwell noise [4]. Together with the CSL and p-pwell noise, the larger power noise of program verify operation causes the underprogram. The underprogram is slightly larger for SLC mode because 4 k bitlines operate simultaneously. However, the underprogram problem is less serious for SLC mode than for MLC mode because of the sufficient underprogram margin of SLC mode.

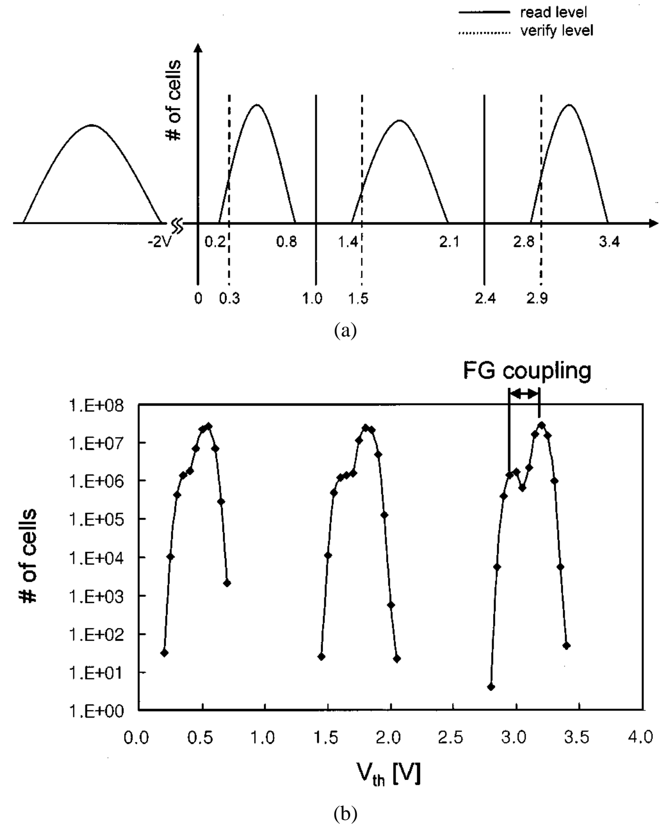


Fig. 11. (a) Target and (b) measured $V_{\rm th}$ distributions.

Another important effect is the interplay of maximum cell $V_{\rm th}$ and read pass voltage $V_{\rm read}$ applied to the unselected wordline during read operation. The higher the $V_{\rm read}$, the smaller the background pattern dependency (BPD) [2]. However, the retention failure limits the maximum allowable $V_{\rm read}$. Therefore, it is required to optimize the gaps between two adjacent program states to lower the maximum cell $V_{\rm th}$ of the highest state. In this device, the worst-case $V_{\rm th}$ shift due to BPD is about 0.05 V for a $V_{\rm read}$ of 6.0 V with the maximum cell $V_{\rm th}$ around 3.0 V [2]. The

TABLE I
DEVICE PARAMETERS

Process	0.15-μm CMOS, STI, triple-well, 2-metal
Tunnel oxide	8 nm
Interpoly dielectric	15 nm (effective)
Gate oxide	35 nm (H.V), 8 nm (L.V)
Cell size	0.14 μm^2 (effective)
Chip size	116.7 mm^2

TABLE II
DEVICE CHARACTERISTICS

	MLC	SLC
Density	1 Gb	512 Mb
Page size	512 B + 16 B	512 B + 16 B
Erase block size	128 kB @4x mode	64 kB @4x mode
Program inhibit scheme	Local self-boosting	Self-boosting
ISPP step pulse	0.15 V	0.5 V
Program throughput	1.6 MB/s @4x mode	6.9 MB/s @4x mode
Read transfer time	20 μs	9 μs
Erase time	2 ms	2 ms

$V_{\rm read}$ of 4.5 V is sufficient to reduce the BPD-caused $V_{\rm th}$ shift for SLC mode because the maximum cell $V_{\rm th}$ is below 2.0 V.

The downward cell $V_{\rm th}$ shifts due to charge loss are 0.3, 0.2, and 0.1 V for the highest, the second, and the lowest program states, respectively. The target $V_{\rm th}$ distributions of the four cells states are shown in Fig. 11(a). In addition, the measured $V_{\rm th}$ distributions of the three program states are shown in Fig. 11(b). Only the sequential programming is permitted for MLC mode. Therefore, the cells under the fifteen wordlines $(W/L_0–W/L_{14})$ are under the influence of the FG coupling, but the cells under the top wordline (W/L_{15}) are free from the FG coupling problem. Thus, the distributions shown in Fig. 11(b) have two peaks for each state after all cells are programmed. The distribution having the first peak is the distribution of the cells coupled to W/L_{15} and the distribution having the second peak is the summation of the distributions of the other cells.

V. CONCLUSION

The dual-mode NAND flash memory has been fabricated using a 0.15-μm CMOS technology, resulting in an effective cell size of 0.14 μm^2 and a chip size of 116.7 mm^2. Fusing changes the mode from the 1-Gb MLC mode to the high-performance 512-Mb SLC mode. The program throughputs of 1.6 MB/s and 6.9 MB/s are achieved by adopting 4$\times$ PGM operation for MLC and SLC mode, respectively. The two-step bitline setup scheme suppresses the peak current below 60 mA. Also, the wordline-ramping technique reduces the wordline coupling below 0.4 V. The LSB scheme is used to effectively reduce the program disturbance and restricts the order of page program to ascending order for MLC mode. On the other hand, the SLC mode utilizes the self-boosting scheme to allow random-order page program because the program disturbance problem is relatively small. The ISPP with 0.15-V step pulse is used to keep narrow $V_{\rm th}$ distribution width of 0.6 V for MLC mode. For SLC mode, the ISPP with 0.5-V step pulse is used to achieve high program throughput. The FG coupling is found to be the most serious parasitic effect widening the cell $V_{\rm th}$ distribution width by 0.2 V. The cell $V_{\rm th}$ distributions are optimized not to degrade program performance for MLC mode resulting in the nonuniform distributions. The device parameters and key technology are summarized in Tables I and II, respectively.

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From 1995 to 2000, he was with Samsung Electronics Corporation, Kiheung, Korea, where he worked on the design of the high-speed synchronous SRAMs, such as PBSRAMs, NtRAMs and DDR SRAMs, and high-density NAND flash memories including 256 Mb and 512 Mb. Currently, he is working on the research of VLSI design and verification with emphasis on fault tolerance and reliability.

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While with KAIST, he was engaged in research fields including BiCMOS analog circuit design, thin-film resistor, and microelectromechanical systems. His Ph.D. dissertation was focused on the 2400 $\times$ 2400-dpi monolithic thermal inkjet printhead, which has 3600 nozzles on a chip for high-resolution and high-speed printing. In 1999, he joined Samsung Electronics Company, Ltd., Kyungki-Do, Korea. He is responsible for cell device of NAND flash memory. His research interests include cell structure design, cell device modeling, and cell reliability, such as endurance and data retention characteristics.

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He joined Samsung Electronics Company, Korea, where he was engaged in the CMOS logic IC design. Since 1991, he has been developing EEPROMs, flash memories, and MROMs. Currently, he is an Engineering Director with the Flash Team.