A Dual-Path Bandwidth Extension Amplifier Topology With Dual-Loop Parallel Compensation

Hoi Lee, *Student Member, IEEE*, Ka Nang Leung, *Member, IEEE*, and Philip K. T. Mok, *Senior Member, IEEE*

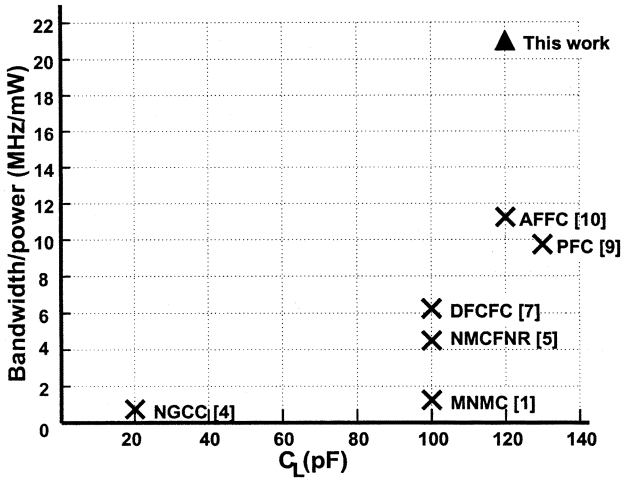
***Abstract*—A dual-path amplifier topology with dual-loop parallel compensation technique is proposed for low-power three-stage amplifiers. By using two parallel high-speed paths for high-frequency signal propagation, there is no passive capacitive feedback network loaded at the amplifier output. Both the bandwidth and slew rate are thus significantly improved. Implemented in a 0.6-μm CMOS process, the proposed three-stage amplifier has over 100-dB gain, 7-MHz gain-bandwidth product, and 3.3-V/μs average slew rate while only dissipating 330 μW at 1.5 V, when driving a 25-kΩ//120-pF load. The proposed amplifier achieves at least two times improvement in bandwidth-to-power and slew-rate-to-power efficiencies than all other reported multistage amplifiers using different compensation topologies.**

***Index Terms*—Amplifiers, dual loop, dual path, frequency compensation, multistage amplifiers.**

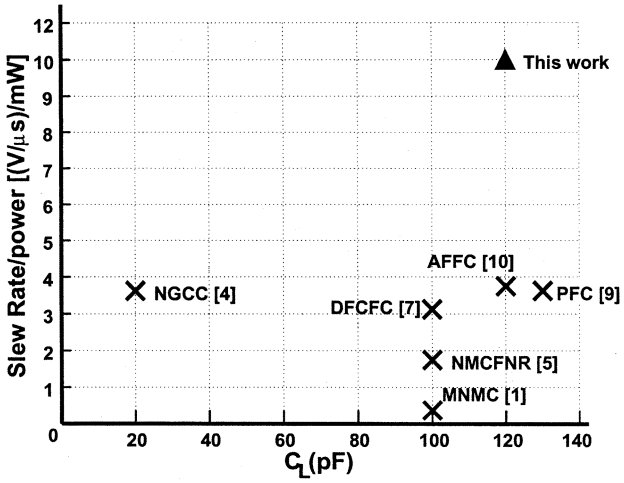
I. Introduction

DRIVEN by the proliferation of battery-powered portable electronic equipment, three-stage amplifiers have become increasingly important as they can provide high gain ($\sim$100 dB) in low-voltage conditions. In three-stage amplifiers, frequency compensation is required to ensure stability. Existing compensation topologies, however, limit both the bandwidth and slew rate of the amplifier in low-power conditions. Based on pole-splitting compensation approach, three-stage amplifiers with nested Miller compensation (NMC) [1]–[3], multipath nested Miller compensation (MNMC) [1], [2], nested G_m-C compensation (NGCC) [4], and NMC with feedforward transconductance stage and nulling resistor (NMCFNR) [5] use two nested Miller capacitors to form passive capacitive feedback networks for stabilization. However, the passive capacitive feedback slows down the speed of the amplifier, as this feedback cannot effectively control the position of the nondominant poles. In addition, the nested Miller capacitors increase the loading at the output of the amplifier, resulting in bandwidth reduction [6]. Other advanced compensation techniques have been proposed to improve the bandwidth. Damping-factor control frequency compensation (DFCFC) [7], [8] and positive-feedback compensation (PFC) [9] remove the inner Miller capacitor loaded at the amplifier output for bandwidth enhancement. On the other hand, active-feedback frequency compensation (AFFC) [10] uses an active capacitive feedback network to create a high-speed feedback path for high-frequency signal propagation, and hence, bandwidth is improved. However, DFCFC, PFC, and AFFC only have a single high-speed path to propagate signals at high frequencies and the output of the amplifier is still loaded by a passive compensation capacitor, thereby limiting the number of design parameters to control the position of the nondominant poles. Therefore, the bandwidth of those topologies is still not optimized.

This brief proposes a dual-path amplifier topology with dual-loop parallel compensation (DLPC) technique to remove all passive capacitive feedback networks loaded at the output of a three-stage amplifier and thus provide two high-speed paths for signal propagation at high frequencies. As a result, both the bandwidth and slew rate of the amplifier can be significantly improved in low-power condition. Fig. 1 shows that



(a)



(b)

Fig. 1. Comparison of (a) small-signal and (b) large-signal performance of multistage amplifiers with different frequency compensation topologies.

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The authors are with the Department of Electrical and Electronic Engineering, The Hong Kong University of Science and Technology, Clear Water Bay, Hong Kong (e-mail: eemok@ee.ust.hk).

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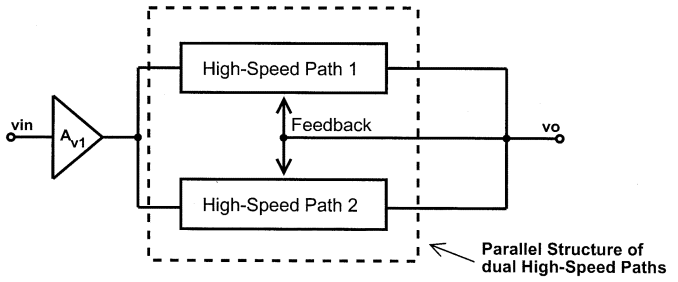

Fig. 2. Conceptual block diagram of the proposed dual-path amplifier topology.

a three-stage amplifier using the proposed dual-path topology achieves better bandwidth-to-power and slew rate-to-power efficiencies compared with other reported multistage amplifiers using different pole-splitting compensation topologies.

In Section II, the structure and operational principle of the dual-path amplifier topology are introduced. Different design issues of DLPC such as dimension conditions, bandwidth, and slew rate are discussed in Section III. The circuit implementation and experimental results of the DLPC amplifier are presented in Section IV. Finally, conclusions are given in Section V.

II. Proposed Dual-Path Amplifier Topology

The conceptual block diagram of the proposed dual-path amplifier topology for a three-stage amplifier is shown in Fig. 2. The amplifier shares a common input stage and has two high-speed paths connected in parallel for high-frequency signal propagation. Both high-speed paths in the proposed dual-path topology do not have any output-loaded passive capacitive feedback network; therefore, they have no bandwidth reduction. By paralleling two high-speed paths, controllable design parameters from each high-speed path can contribute positively to each other and push the nondominant poles to much higher frequencies, resulting in bandwidth enhancement.

Fig. 3 depicts the implementation of the proposed dual-path amplifier topology by using a damping-factor control block [7] and an active capacitive feedback network [10] in the high-speed paths. In fact, both high-speed paths share the active capacitive feedback network that consists of the compensation capacitor C_a connected in series with a noninverting gain stage A_{va} where the voltage gain of A_{va} is larger than 1. The forward portion of the top high-speed path contains only a single gain stage A_{v5}, while that of the bottom high-speed path has two gain stages A_{v2} and A_{v3} cascaded together with an additional inverting gain stage of A_{v4}. The gain of the amplifier is dominated by the gain stages of the bottom high-speed path A_{v2} and A_{v3} together with the input gain stage A_{v1}. Therefore, this implementation of the amplifier can achieve over 100-dB gain. The presence of both A_{v3} and A_{v5} in the dual-path structure is particularly suitable for realizing a class-AB push-pull output stage such that the slew rate of the amplifier is not limited by the output stage even driving large capacitive loads. In addition, both high-speed paths in Fig. 3 do not have passive capacitive feedback networks loaded at the output of the amplifier and thus fulfill the requirement of the dual-path topology. Dual-loop parallel compensation (DLPC) is proposed not only to stabilize the amplifier, but also to effectively control the position of the nondominant poles by properly adjusting the transconductances of gain stages from both high-speed paths. Bandwidth extension can thus be achieved.

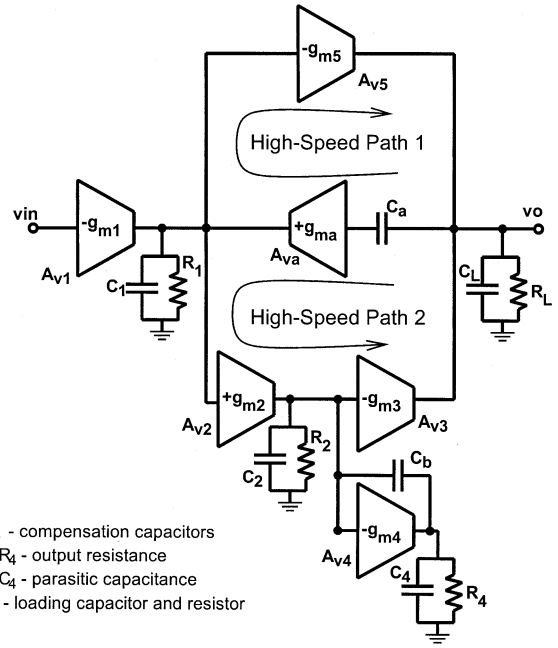

Fig. 3. Dual-path amplifier topology with dual-loop parallel compensation.

III. Design Issues of Dual-Loop Parallel Compensation

In Fig. 3, C_a and C_b are compensation capacitors, while g_{mi}, C_i, and R_i represent the transconductance, the equivalent parasitic capacitance, and the output resistance of the corresponding gain stages, respectively. C_L and R_L are the loading capacitor and resistor. To analyze the DLPC amplifier, some assumptions are made: 1) C_L, C_a, and $C_b \gg C_1$, C_2, and C_4; and 2) $g_{m(1,2,3,4)}R_{(1,2,L,4)}$, $g_{m5}R_L$, and $g_{ma}R_1 \gg 1$. Based on these assumptions, it can be demonstrated that the gain $A_{v(\mathrm{DLPC})}$ and left-half-plane poles of the DLPC amplifier are given by

$$A_{v(\mathrm{DLPC})} = g_{m1}g_{m2}g_{m3}R_1R_2R_L \tag{1}$$

$$p_{-3\mathrm{dB}} = \frac{1}{C_a g_{m2}g_{m3}R_1R_2R_L} \tag{2}$$

$$p_{2,3} = \frac{g_{ma}}{2C_a} \pm j\frac{g_{ma}}{2C_a}\sqrt{\frac{4C_a^2(g_{m2}g_{m3}+g_{m4}g_{m5})}{C_1C_Lg_{ma}g_{m4}} - 1} \tag{3}$$

where $p_{-3\mathrm{dB}}$ is the dominant pole and $p_{2,3}$ are the nondominant complex poles. From (1) and (2), the gain-bandwidth product of the amplifier GBW $= A_{v(\mathrm{DLPC})} \cdot p_{-3\mathrm{dB}} = (g_{m1}/C_a)$. The position of the nondominant poles $|p_{2,3}|$ can be derived from (3) as

$$|p_{2,3}| = \sqrt{\left(\frac{g_{ma}}{C_1C_L}\right)\left(\frac{g_{m2}g_{m3}}{g_{m4}} + g_{m5}\right)}. \tag{4}$$

From (4), it is verified that the transconductances of gain stages from each of the high-speed paths sum up such that $|p_{2,3}|$ can be pushed to a much higher frequency by maximizing g_{ma}, g_{m2},

g_{m3}, and g_{m5} while minimizing g_{m4}. It also implies that the controllable transconductances of all gain stages contribute to the bandwidth improvement. As $|p_{2,3}|$ is inversely proportional to the geometrical mean of the parasitic and loading capacitance, $|p_{2,3}|$ can be located at a high frequency even if the amplifier drives a large capacitive load. In addition, when the transconductances of output transistors (g_{m3} and g_{m5}) increase or the load capacitance decreases, $|p_{2,3}|$ from (4) is shifted to a much higher frequency and the effect of increasing the complex part of nondominant poles from (3) is minimized. Therefore, the robustness of DLPC for a range of output transconductances and load capacitance is guaranteed.

By using the third-order Butterworth response [2], the stability of the DLPC amplifier is achieved by considering the poles of the DLPC amplifier in unity-gain feedback configuration. The dimension conditions are then given by

$$C_a = C_b = \sqrt{2\left(\frac{g_{m1}g_{m4}}{g_{m2}g_{m3}+g_{m4}g_{m5}}\right)C_1C_L} \quad (5)$$

$$g_{ma} = 4g_{m1}. \quad (6)$$

From (5), $C_a = C_b$ is for simplicity of design. In fact, the value of compensation capacitance can be optimized by setting $C_a > C_b$. For stability concern, the required compensation capacitance in NMC-based amplifiers is proportional to the loading capacitance [1]–[5], while the size of C_a is the geometrical mean of the parasitic and loading capacitance in the proposed DLPC amplifier. Therefore, the required compensation capacitance can be reduced by more than an order of magnitude when driving a capacitive load of hundreds of picofarads in a DLPC amplifier. In a multistage amplifier, most of the chip area will be occupied by the size of the compensation capacitors, especially when driving a large capacitive load. The area of the DLPC amplifier can thus become much smaller as the required compensation capacitors are reduced. Noise due to coupling can also be greatly reduced. Furthermore, in order to realize a push-pull output stage for acquiring better transient responses, the transconductance of A_{v5} is set to equal to that of A_{v3}

$$g_{m5} = g_{m3}. \quad (7)$$

As the DLPC amplifier with dual high-speed paths pushes the nondominant poles to a high frequency and reduces the value of the compensation capacitance, large GBW results, which is given by

$$\text{GBW} = \frac{g_{m1}}{C_a} = \sqrt{\left(\frac{g_{m1}}{2g_{m4}}\right)\left(\frac{g_{m2}g_{m3}+g_{m4}g_{m5}}{C_1C_L}\right)}. \quad (8)$$

From (8), a small g_{m4} and large g_{m2}, g_{m3}, and g_{m5} should be used to maximize the GBW. Since both gain stages A_{v3} and A_{v5} are built in the same current branch to realize the push-pull output stage, large g_{m3} and g_{m5} can be achieved simultaneously for bandwidth extension without any additional static power consumption. In addition, the slew rate of the DLPC amplifier is determined by the amount of biasing current in A_{va} and A_{v2} to charge and discharge the compensation capacitors C_a and C_b, respectively. The slew rate can be increased either by increasing the biasing current or decreasing the compensation capacitance. Based on (5), as the required value of the compensation capacitance is reduced, the slew rate of the DLPC amplifier can then be enhanced without increasing the power. Therefore, the proposed DLPC can improve both the bandwidth-to-power and slew-rate-to-power efficiencies.

TABLE I
SUMMARY OF MEASUREMENT RESULTS

	NMC	**This work, DLPC**
Loading	25 kΩ // 120 pF	
DC Gain	> 100 dB	**> 100 dB**
GBW	0.41 MHz	**7 MHz**
PM	47^o	**46^o**
SR^+/SR^- (V/μs)	0.166/0.146	**2.2/4.4**
T_s^+/T_s^- (μs) (to 1%)	3.35/3.75	**0.315/0.68**
Power Consumption @Vdd	265 μW @1.5 V	**330 μW @1.5 V**
$C_{a(DLPC)}$ / $C_{m1(NMC)}$	75 pF	**4.8 pF**
$C_{b(DLPC)}$ / $C_{m2(NMC)}$	15 pF	**2.5 pF**
Area	0.175 mm^2	**0.050 mm^2**

IV. CIRCUIT IMPLEMENTATIONS AND EXPERIMENTAL RESULTS

The circuit implementation of the DLPC amplifier is shown in Fig. 4(a). In the DLPC amplifier, the input gain stage is realized by transistors M101–M108. Transistor Ma and the compensation capacitor C_a implement the active capacitive feedback network, where the transistor Ma functions as a common-gate amplifier to provide a voltage gain much larger than 1 [10]. Transistors Mc1 and Mc2 are the current sources to bias Ma. To minimize the systematic offset of the amplifier due to the current branch of Ma, replica bias is used [11], which is implemented by transistors Mcb1, Mab, and Mcb2. The gain stage A_{v5} in the top high-speed path is realized by transistor M501, while in the bottom high-speed path, gain stages A_{v2}, A_{v3}, and A_{v4}, are implemented by transistors M200, M301, and M401, respectively. The biasing circuits for the DLPC amplifier are shown in Fig. 4(b). In particular, in order to avoid open-loop control of the bias point vb4 in the gain stage A_{v4}, a local feedback circuitry is used [8], where the loop gain of the feedback circuitry is smaller than that of A_{v4}. To further optimize the chip area and bandwidth, both compensation capacitors C_a and C_b in the DLPC amplifier are fined tuned to be 4.8 and 2.5 pF, respectively, for driving a 120-pF capacitive load. In addition, for the ease of performance comparison, a well-accepted three-stage NMC amplifier has also been designed, in which the two compensation capacitors, C_{m1} and C_{m2}, are 75 and 15 pF, respectively. Both amplifiers have been fabricated in a commercial 0.6-μm CMOS process with $V_{tn} = 0.89$ V and $V_{tp} = -0.81$ V. The chip micrograph is shown in Fig. 5.

The frequency and transient responses of DLPC and NMC amplifiers have been tested with a 0.3-V input common-mode voltage and a 0.3-V step input, respectively. The measured frequency and transient responses are shown in Figs. 6 and 7, respectively. The detailed performances are summarized in

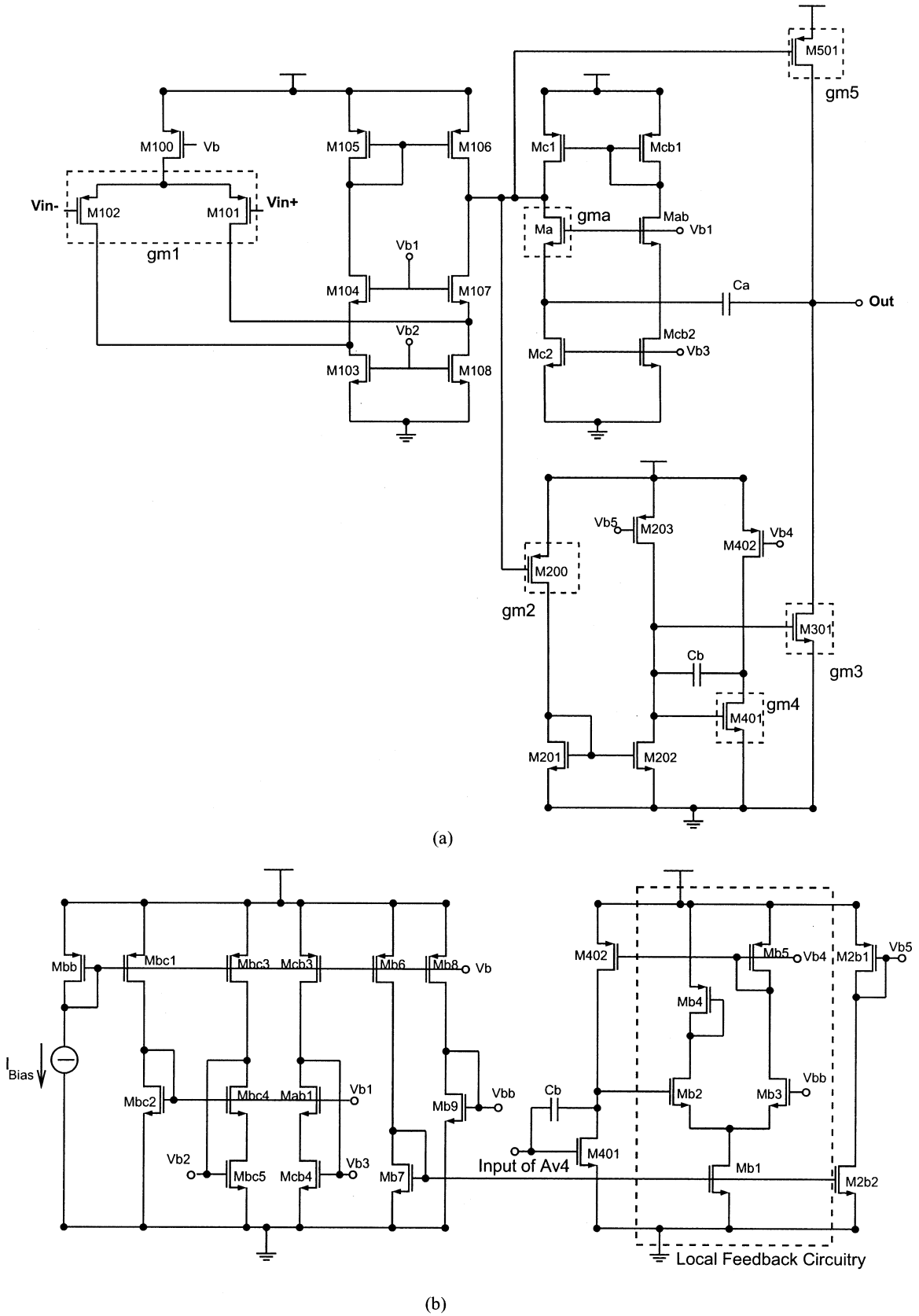

Fig. 4. (a) Circuit schematic and (b) biasing circuits of a three-stage DLPC amplifier.

Table I. When both DLPC and NMC amplifiers are powered by 1.5 V, the DLPC amplifier dissipates extra 24.5% power, but improves the GBW by 17 times and the average slew rate by 21 times compared with the NMC counterpart. In addition, the

TABLE II
COMPARISON OF DIFFERENT MULTISTAGE AMPLIFIERS († AVERAGE VALUE IS USED)

	NMC [1]	MNMC [1]	NGCC [4]	NMCFNR [5]	ETC [6]	DFCFC [7], [8]	PFC [9]	AFFC [10]	**This work DLPC**
C_L (pF)	100	100	20	100	40	100	130	120	**120**
DC Gain (dB)	100	100	100	>100	102	>100	>100	>100	$>$ **100**
GBW (MHz)	60	100	0.61	1.8	47	2.6	2.7	4.5	**7**
SR† (V/μs)	20	35	2.5	0.79	69	1.32	1	1.49	**3.3**
Power (mW@Vdd)	76@8	76@8	0.68@2	0.406@2	6.9@3	0.42@2	0.275@1.5	0.4@2	**0.33@1.5**
FOM_s ($\frac{MHz \cdot pF}{mW}$)	79	132	18	443	272	619	1276	1350	**2545**
FOM_L ($\frac{V/\mu s \cdot pF}{mW}$)	26	46	74	195	400	314	473	447	**1200**
Technology	3 GHz f_t BJT	3 GHz f_t BJT	2 μm CMOS	0.8 μm CMOS	0.6 μm CMOS	0.8 μm CMOS	0.35 μm CMOS	0.8 μm CMOS	**0.6 μm CMOS**

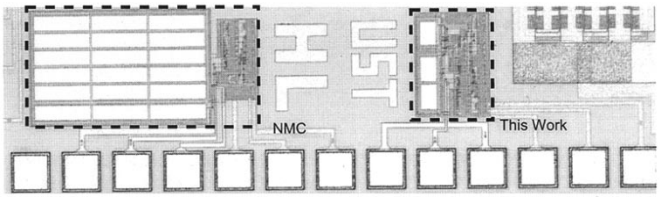

Fig. 5. Chip micrograph of three-stage DLPC and NMC amplifiers.

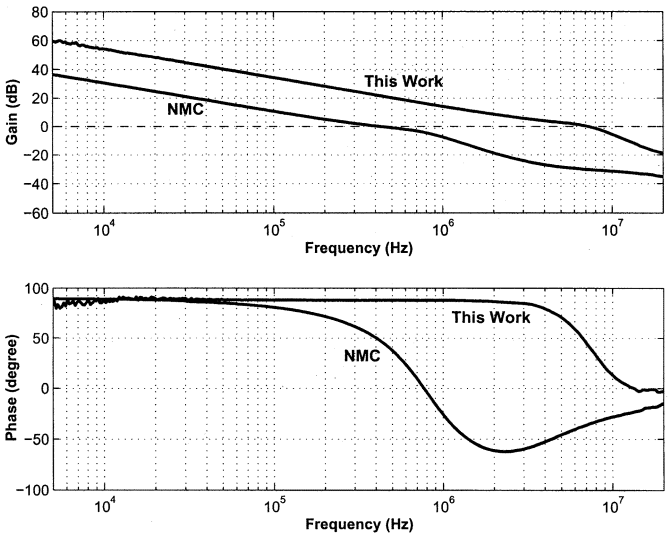

Fig. 6. Measured ac responses of three-stage DLPC and NMC amplifiers driving a 120-pF//25-kΩ load.

chip area of the DLPC amplifier is reduced by 3.5 times due to the smaller compensation capacitors.

To provide a detailed performance comparison between DLPC and other reported compensation topologies, two figures of merit (shown in Table II), $\text{FOM}_S = (\text{GBW} \cdot C_L)/\text{power}$ and $\text{FOM}_L = (\text{SR} \cdot C_L)/\text{power}$, where SR is the slew rate, are adopted to gauge small-signal and large-signal performances of amplifiers [7], [10]. A larger FOM implies a better compensation topology as the amplifier with large FOMs has larger bandwidth-to-power and slew-rate-to-power efficiencies after taking load capacitance into consideration. From Table II, both FOM_S and FOM_L of the proposed DLPC amplifier are significantly larger than all other reported compensation topologies.

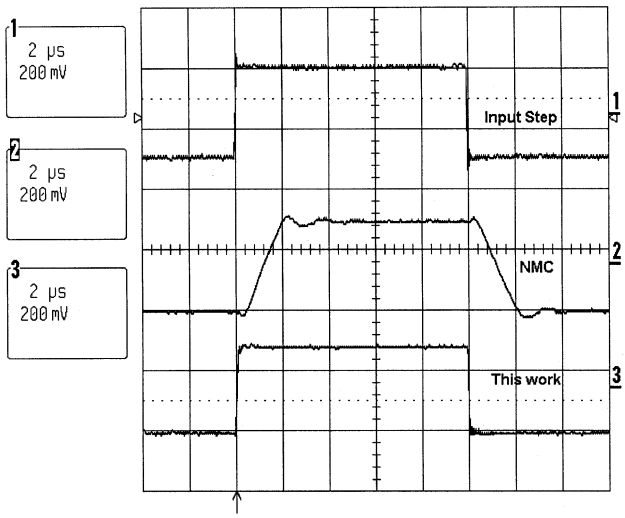

Fig. 7. Measured transient responses of three-stage DLPC and NMC amplifiers driving a 120-pF//25-kΩ load.

V. CONCLUSION

A dual-path amplifier topology with DLPC technique for significant bandwidth enhancement and slew-rate improvement in low-power three-stage amplifiers has been introduced, analyzed, and verified by experimental results. Comparison with other published compensation topologies has been presented. The DLPC amplifier shows better small-signal frequency response and large-signal transient response than all other reported compensation topologies.

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