A Dual Two-Level Inverter Scheme With Common Mode Voltage Elimination for an Induction Motor Drive

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***Abstract*—Pulse-width modulated (PWM) inverters are known to generate common mode voltages which cause motor bearing currents in the induction motor drives. They also result in leakage currents which act as sources of conducted electromagnetic interference in the drive system. The common mode voltage generated by a conventional three-level inverter can be eliminated by switching only the voltage space vectors which do not produce the common mode voltage. This paper presents a PWM switching strategy to eliminate common mode voltage using the open-end winding configuration for the induction motor. The switching strategy presented in this paper, does not generate any alternating common mode voltages in the drive system and hence the electrostatic coupling of the common mode voltage, which results in the bearing currents and the leakage currents, is avoided. The proposed scheme is devoid of neutral point voltage fluctuations and does not require neutral point clamping diodes, when compared to the common mode elimination scheme based on the conventional three-level inverter topology. Also, the present scheme uses a single dc-link with half the voltage compared to the conventional three-level inverter based scheme.**

***Index Terms*—Common mode voltage, open-end winding induction motor drive.**

NOMENCLATURE

$V_{\rm dc}$	The dc-link voltage of the neutral point clamped three-level inverter.
$V_{A1O}, V_{B1O}, V_{C1O}$	The pole voltages of INV1.
$V_{A2O}, V_{B2O}, V_{C2O}$	The pole voltages of INV2.
$V_{A1A2}, V_{B1B2}, V_{C1C2}$	The voltage across the phase windings of the induction machine.
V_s	The combined voltage space phasor for V_{A1A2}, V_{B1B2}, and V_{C1C2}.
$V_{\rm sr}$	The combined reference voltage space phasor for the dual inverter.
$V_{\rm sr1}$	The individual reference voltage space phasor for inverter- 1 (INV1).
$V_{\rm sr}(\alpha), V_{\rm sr}(\beta)$	The components of $V_{\rm sr}$ along the α-β axes.
$V_{\rm sr1}(\alpha), V_{\rm sr}1(\beta)$	The components of $V_{\rm sr1}$ along the α-β axes.
α	The angle of the combined reference space phasor $(V_{\rm sr})$ with the A-phase axis.

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I. INTRODUCTION

THE PULSE-WIDTH modulation (PWM) voltage source inverters have enabled efficient and easy control of the adjustable speed induction motor drives and they are widely used in industrial drives. These PWM inverters also cause high frequency, high level, common mode voltages in the system [1] .These alternating common mode voltages result in motor bearing currents by electrostatic coupling through parasitic capacitances [1]–[3]. The inverter generated common mode voltage also causes motor leakage currents which act as sources of Electromagnetic Interference in the drive system [4]. PWM inverter, which does not generate common mode voltage, is suggested as a solution to eliminate the problems associated with the common mode voltage [3]. Reference [5] presents modulation schemes for eliminating the common mode voltage in the conventional neutral point clamped three-level inverter, using only those voltage space vectors which do not generate common mode voltage. This scheme experiences neutral point fluctuations, which is characteristic of neutral point clamped topology. The neutral point fluctuation in this scheme can be controlled, by adding additional hardware to balance the neutral point voltage fluctuation [6].

The open-end winding induction motor, fed by two two-level inverters with half the dc-link voltage (compared to the conventional three-level scheme) from both sides, realizes a three-level inverter structure. [7]–[9]. In [7] and [8], isolated power supplies are used to suppress the zero sequence currents in the phase windings of dual inverter fed open end winding induction motor drive. In [10], a space vector based PWM technique is employed to suppress the zero sequence currents in the motor phase windings so that the two two-level inverters can be operated with a single dc-link. The PWM scheme in [10], suppresses the zero sequence currents in the machine phase windings, but does not eliminate the common mode voltage generated by the dual inverter. In the present work, a PWM switching strategy is proposed for the dual-inverter fed open-end winding induction motor drive with single dc-link, such that the two inverters do not generate any alternating common mode voltage. As the alternating common mode voltage is absent in the proposed drive, the possibility of electrostatic coupling and the associated problems are avoided [1]–[4].

The proposed scheme is based on the open-end winding induction motor configuration with conventional two-level inverters and hence does not experience neutral point fluctuations

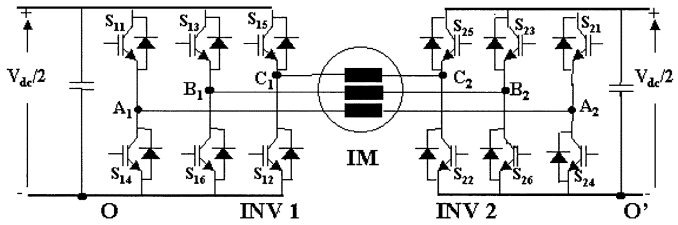


Fig. 1. Schematic of dual inverter fed open end winding induction motor drive with isolated dc-links.

[8], [10]. It does not require the neutral point clamping diodes and has a simple power circuit compared to the conventional three-level inverter based scheme [5]. The proposed scheme uses half the dc-link voltage compared to the neutral point clamped inverter based scheme and has a lesser device count. The present scheme needs an open-end winding configuration for the induction motor which is easily obtained by opening the neutral of the stator windings and does not call for any change in the design or structure of the induction motor.

II. Open-End Winding Induction Motor Drive With a Single dc-Link

Fig. 1 shows the schematic a dual-inverter fed open-end winding induction motor drive, where INV1 and INV2 are conventional two-level inverters [7], [8]. Open-end winding induction motor structure is obtained by opening the neutral point of the conventional cage induction motor and does not require any design change in the motor. A three-level inverter structure is realized, when the open-end winding induction motor is fed by two two-level inverters with half the dc-link voltage $(V_{\rm dc}/2)$, compared to the dc-link voltage of the conventional neutral point clamped three-level inverter.

Each of the two-level inverter in the open-end winding induction motor drive (Fig. 1) can generate voltage space vectors as shown in Fig. 2(a). The active vectors for both inverters have magnitude of $V_{\rm dc}/2$ since the dc-link voltage is $V_{\rm dc}/2$. V_{A1O}, V_{B1O}, and V_{C1O} are the pole voltages of INV1 and V_{A2O}, V_{B2O}, and V_{C2O} are the pole voltages of INV2. Any leg of the two inverters can independently attain levels 0 or $V_{\rm dc}/2$. The voltage across a particular phase winding can be obtained by

$$V_{A1A2} = V_{A1O} - V_{A2O} \tag{1}$$

$$V_{B1B2} = V_{B1O} - V_{B2O} \tag{2}$$

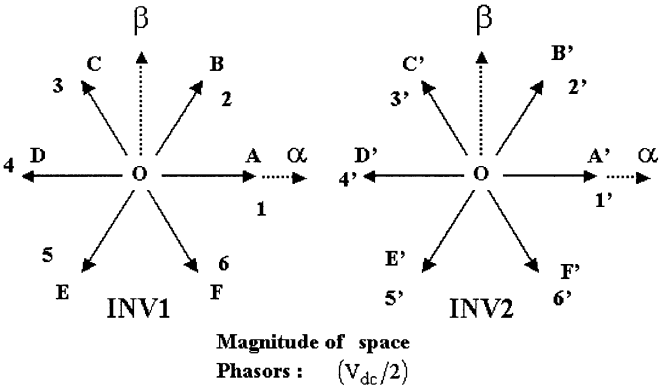
$$V_{C1C2} = V_{C1O} - V_{C2O}. \tag{3}$$

The phase winding can attain one of the levels, $-V_{\rm dc}/2(\text{`}-\text{'}), 0(\text{`}0\text{'})$ or $V_{\rm dc}/2(\text{`}+\text{'})$. The combined effect of the voltages in the three windings can be represented by a voltage space vector V_S as defined by

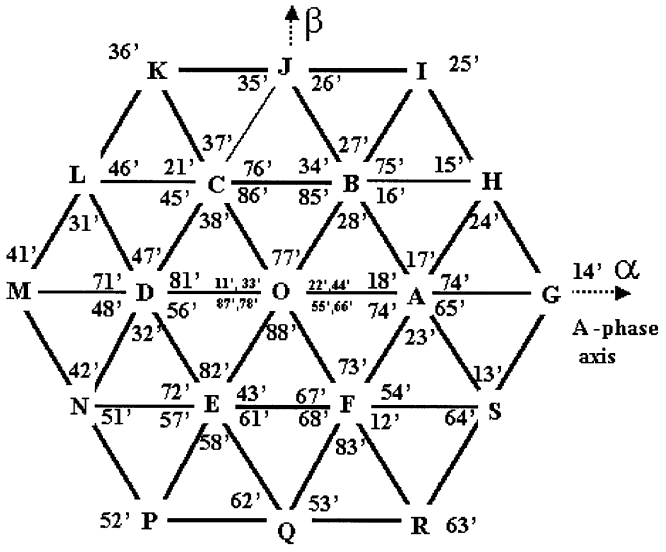
$$V_S = V_{A1A2} + V_{B1B2}e^{j2\pi/3} + V_{C1C2}e^{j4\pi/3}. \tag{4}$$

This voltage space vector can be equivalently represented as the sum of the voltage space vectors generated by the two two-level inverters. If V_{S1} and $\rm V_{S2}$ are the voltage space vectors generated by INV1 and INV2, respectively, the resultant voltage space vector is

$$V_S = V_{S1} + V_{S2}. \tag{5}$$



(a)



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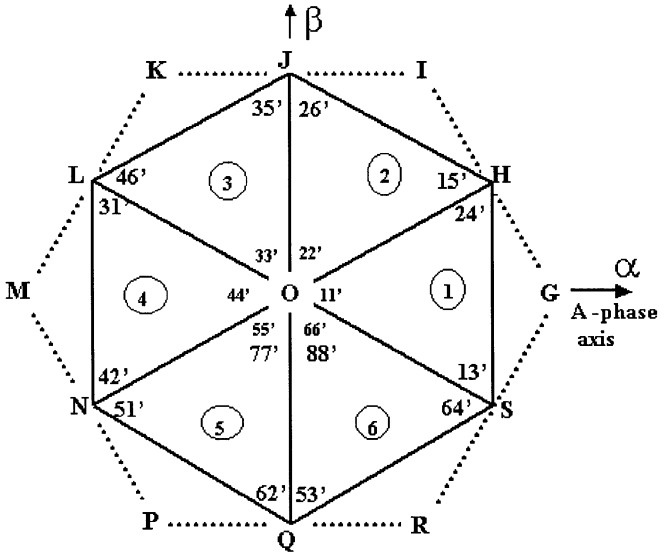


(c)

Fig. 2. (a) Voltage space vectors of the individual inverters. (b) Voltage space vectors and space phasor combinations of the dual inverter. (c) Voltage vectors without triplen contribution.

Fig. 2(a) shows the individual space vectors of the two-level inverters, where the eight states of INV1 are referred as 1, 2–8, and the eight states of INV2 are referred as $1'$, and $2'$–$8'$. Fig.2(b)

TABLE I
VOLTAGE SPACE VECTOR COMBINATIONS PRODUCING ZERO COMMON MODE VOLTAGE IN THE MOTOR PHASE WINDINGS

Vector	Space phasor combinations	Common mode voltage of INV1 (V_{C1})	Common mode voltage of INV2 V_{C2}	Common mode voltage across machine phase (V_{C1} - V_{C2})
OS	13'	$V_{dc}/6$	$V_{dc}/6$	0
	64'	$V_{dc}/3$	$V_{dc}/3$	0
OH	15'	$V_{dc}/6$	$V_{dc}/6$	0
	24'	$V_{dc}/3$	$V_{dc}/3$	0
OJ	35'	$V_{dc}/6$	$V_{dc}/6$	0
	26'	$V_{dc}/3$	$V_{dc}/3$	0
OL	31'	$V_{dc}/6$	$V_{dc}/6$	0
	46'	$V_{dc}/3$	$V_{dc}/3$	0
ON	51'	$V_{dc}/6$	$V_{dc}/6$	0
	42'	$V_{dc}/3$	$V_{dc}/3$	0
OQ	53'	$V_{dc}/6$	$V_{dc}/6$	0
	62'	$V_{dc}/3$	$V_{dc}/3$	0
Zero vector at origin	11',33',55',	$V_{dc}/6$	$V_{dc}/6$	0
	22',44',66',	$V_{dc}/3$	$V_{dc}/3$	0
	77'	$V_{dc}/2$	$V_{dc}/2$	0
	88'	0	0	0

shows the resultant 19 voltage space vectors for all the possible combinations of the states of the individual inverters [8]. It can be verified that, among these 19 voltage vectors, there are seven voltage vectors which do not contribute any common mode voltage in the machine phase windings [10]. These vectors are at the locations H, J, L, N, Q, S, and O [Fig. 2(b)]. For the calculation of the common mode voltage at these locations we assume that points O and O′ in Fig. 1 are connected. For example, the common mode voltage (with respect to the negative rail of dc-link) for the space phasor combination of 13′ for vector OS (Fig. 2(b)) can be calculated as follows. For the space phasor combination 13′ INV1 is in state 1(‘$+--$') and INV2 is in state 3‘$(-+-)$. INV1 and INV2 being two-level with dc-link voltage of $V_{dc}/2$, the pole voltage level ‘+' corresponds to $V_{dc}/2$ and pole voltage level ‘−' corresponds to 0 (when the pole voltages are referred to the negative rail of the dc-link). Therefore common mode voltage generated by INV1 for the combination 13′ is

$$V_{C1(+--)} = (V_{A1O} + V_{B1O} + V_{C1O})/3 = (V_{dc}/2 + 0 + 0)/3 = V_{dc}/6. \quad (6)$$

The common mode voltage generated by INV2 for this combination is

$$V_{C2(-+-)} = (V_{A2O} + V_{B2O} + V_{C2O})/3 = (0 + V_{dc}/2 + 0)/3 = V_{dc}/6. \quad (7)$$

The common mode voltages corresponding to all the seven vectors in Fig. 2(b) are given in Table I From Table I, it can be seen that these vectors do not generate any common mode voltage across the machine winding and hence zero sequence currents will not flow in the machine winding if these vectors are only used for PWM generation [10]. Hence isolated dc-links are not required to suppress zero sequence currents and both the two-level inverters can be operated with the same dc-link. Fig. 3

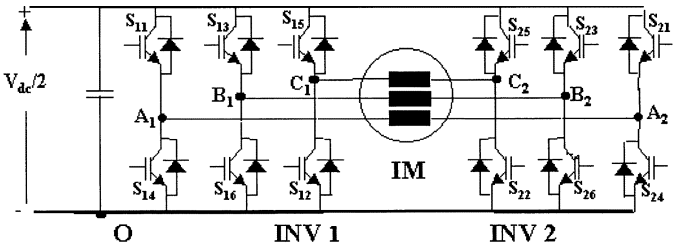


Fig. 3. Schematic of dual inverter fed open end winding induction motor drive with single dc-links.

shows the schematic of the dual inverter fed open end winding induction motor drive with the single power supply [10].

The active vectors which do not produce the common mode voltage across the machine windings form a hexagon as shown in Fig. 2(c), and when they are used for PWM generation, the combined inverter operates as a two-level inverter. Fig. 2(c) also shows the space phasor combinations which would generate these active vectors. Each of the active vector of this resultant two-level inverter can be realized by two different space phasor combinations. In the scheme presented in [10], these active vectors $\mathbf{OS}, \mathbf{OH}, \mathbf{OJ}, \mathbf{OL}, \mathbf{ON}, \mathbf{OQ}$ are generated by using the combinations 13′, 24′, 35′, 46′, 51′, and 62′, respectively. The zero vectors used were 77′ and 88′. When this scheme is adopted, the two-level inverter INV1 will switch through the active vectors 1–6 and INV2 will switch through 1′ through 6′ [10].

As the two-level inverters in this scheme [10], switch individually through the vectors 1–6 and 1′–6′, they generate alternating common mode voltage (with respect to the negative dc link rail) as in the case of any conventional two-level inverters (Table I). These common mode voltages do not cause the zero sequence currents in the machine phase windings, as at every instant the common mode voltages generated by the individual inverters are equal and appear at the opposite ends of the windings. But these common mode voltages generated by the inverters can couple to the stator frame and rotor frame causing undesirable bearing currents and leakage currents as in the case of the conventional PWM inverters [1]–[4]. A PWM scheme is proposed in the present work, to eliminate these common mode voltages generated by the individual inverters.

III. PROPOSED PWM SCHEME TO ELIMINATE COMMON MODE VOLTAGE

In the proposed PWM scheme, the vectors of the individual inverters are selected such that they do not generate any alternating common mode voltage in the system. Each of the active vectors of Fig. 2(c) (the dual inverter operated with single dc link) can be realized by two combinations of individual inverter voltage space phasors. This multiplicity of space phasors is due to the inherent multiplicity available for the ‘0’ level, in the case of open end winding induction motor configuration. It may be observed that, if the combinations for the vectors at H, J, L, N, Q, and S are chosen as 15′, 35′, 31′, 51′, 53′, and 13′ respectively for PWM generation (referred as sequence-1), the individual inverters assume the three states $1(+--), 3(-+-)$ and $5(--+)$ for INV1 and 1′, 3′, and 5′ for INV2. Let us refer

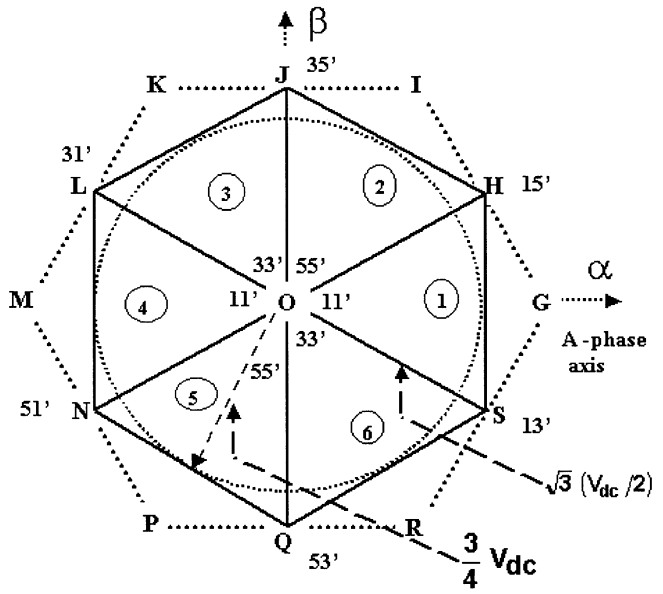


Fig. 4. Space phasor combinations for active vectors and zero vectors used in the present work (for sequence-1).

these combinations as sequence-1. The common mode voltage generated by INV1 (referred to the negative rail of the dc-link, Fig. 3) for the states 1, 3, and 5 can be determined from its pole voltages (Table I) [(6) and (7)].

Therefore, if the individual inverters use only the states (1, 3, and 5), they do not generate any alternating common mode voltage. The zero vector in the dual inverter has eight combinations. Of these, the combinations $11'$, $33'$ or $55'$ are to be used along with sequence-1.

It may be observed that there is one more switching sequence available, which will not generate alternating common mode voltages in the individual inverters. This alternative combinations (referred as sequence-2) for the active vectors H, J, L, N, Q, and S are $64'$, $24'$, $26'$, $46'$ $42'$, and $62'$, respectively. It can be verified that, this sequence also, when used with zero vectors, $22'$, $44'$ or $66'$ do not generate any alternating common mode voltage (Table I). Hence in the present work, the alternating common mode voltage is eliminated by using voltage vectors of sequence-1 or sequence-2.

Hence, with the PWM scheme proposed in the present work, the individual inverters do not generate any alternating common mode voltages in the system, and the possibility of bearing currents and leakage currents due to electrostatic coupling and its associated problems are also avoided. The active vectors and the zero vectors for the dual inverter used in the present work (for sequence-1) are shown in Fig. 4.

From the Fig. 4, it can be noted that a particular individual pole voltage of INV1 and the respective pole voltage in INV2 are at 180° out of phase. Also the pole voltage will not have half wave symmetry as the inverters only switch through vectors 1, 3, or 5 (for sequence-1) or vectors 2, 4, or 6 (sequence-2). The maximum amplitude reference space vector that can be generated by the drive under linear modulation with the proposed PWM is equal to the radius of the circle inscribed in the hexagon in Fig. 4 (shown by the dotted line in Fig. 4). The amplitude of active vectors in the proposed drive is $\sqrt{3}(V_dc/2)$ and the maximum amplitude of reference space vector generated (Fig. 4)

$$|V_{\rm sr}|_{\max} = \sqrt{3}/2 \times \sqrt{3}(V_{\rm dc}/2) = \frac{3}{4}V_{\rm dc}. \tag{8}$$

The corresponding maximum value of peak fundamental phase voltage that can be generated by the drive is then given by

$$(V_{\rm peak,1})_{\max} = 2/3 \times |V_{\rm sr}|_{\max} = 2/3 \times \frac{3}{4}V_{\rm dc} = \frac{V_{\rm dc}}{2}. \tag{9}$$

It may be observed that, this is same as the maximum value of peak fundamental phase voltage generated by the conventional two-level inverter (which has common mode voltages and its associated problems) with Sinusoidal Pulse Width Modulation. This maximum value of peak fundamental phase voltage is 15% less than to the peak fundamental amplitude that can be generated with the space vector based pulse width modulation. This can be compensated with an additional boost in the dc-link voltage. Hence it can be verified that with a dc-link voltage of 0.57 $V_{\rm dc}$ (15% boost over $V_{\rm dc}/2$) the proposed scheme with common mode elimination, can generate the same maximum fundamental amplitude of the phase voltage equivalent to that generated by a conventional two-level inverter which uses a dc-link voltage of $V_{\rm dc}$ (Fig. 4)

$$\begin{aligned}(V_{\rm peak,1})_{\max} &= 2/3 \times |V_{\rm sr}|_{\max} \\ &= 2/3 \times \left[\frac{\sqrt{3}}{2}(\sqrt{3} \times 0.57V_{\rm dc})\right] = 0.57V_{\rm dc}.\end{aligned} \tag{10}$$

A. Principle of the Proposed PWM Scheme

Each of the active vectors of the dual inverter (which do not contribute to common mode voltage variations, Fig. 4) is synthesised from two individual inverter space vectors which are spaced at 120°. As shown in Fig. 5(a), **OS** can be seen as the sum of **OA** from INV1 and **OC′** from INV2 [Fig. 2(a)]. Vector **OH** is the sum of vectors **OB** from INV1 and **OD′** from INV2 [Fig. 2(a)]. All the vectors of the combined inverter can be resolved similarly as sum of two vectors from the individual inverters and Fig. 5(b) shows the active vectors and the corresponding vector pairs.

From Fig. 5(b), it is seen that vector **OA** of INV1 along with vector **OC′** of INV2 is uniquely transformed to **OS**. Vector **OB** of INV1 and **OD′** of INV2 are transformed to **OH** in the dual inverter scheme. Vectors **OS** and **OH** form the sector-1 of the combined inverter (Fig. 4). Vectors **OA** and **OB** of INV1 define the sector-1 of INV1 and **OC′** and **OD′** define the sector-3 of INV2 [Fig. 2(a)]. This means that sector-1 of INV1 and sector-3 of INV2 are mapped to sector-1 of the combined inverter. Similarly each of the sectors in the combined inverter gets mapped to a sector in the individual inverter. Therefore, a reference voltage space vector for the combined inverter also gets mapped to a pair of reference space vectors corresponding to the individual

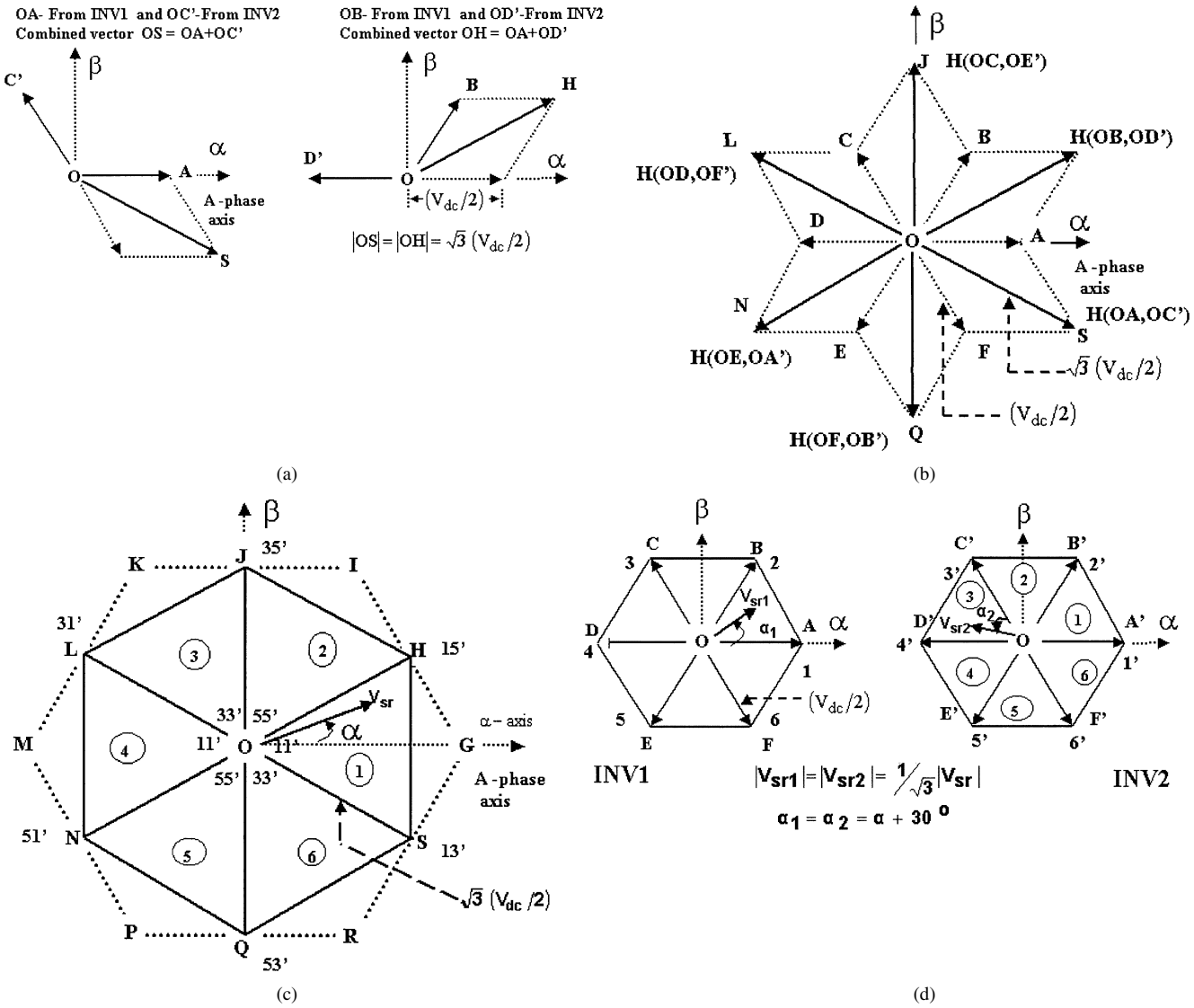


Fig. 5. (a) Synthesis of the combined voltage vectors forming sector-1. (b) The voltage vectors without common mode voltages, and their components. (c) The reference space phasor $V_{\rm sr}$ for the dual inverter. (d) The reference space phasors $V_{\rm sr1}$ and $V_{\rm sr2}$ for the individual inverters.

inverters. Corresponding to a voltage space vector for the combined inverter, a voltage space vector component for the individual inverters can be determined.

If we can generate the inverter voltage vectors and switching times with reference space vector for one of the inverters (say INV1), these vectors generated for INV1 ($\mathbf{OA}, \mathbf{OB}, \mathbf{OC}$ etc.) can be mapped to a unique vector for the dual inverter ($\mathbf{OS}, \mathbf{OH}, \mathbf{OJ}$ etc.). For example, the reference space vector $V_{\rm sr}$ in sector-1 of the dual inverter [Fig. 5(c)] can be mapped to a reference space vector $V_{\rm sr1}$ in sector-1 of INV1 and $V_{\rm sr2}$ in sector-3 of INV2 [Fig. 5(d)]. This mapping is explained in Section III-B. This mapped reference space vector can be realized by switching $\mathbf{OA}$ and $\mathbf{OB}$ along with the zero vector [Fig. 5(c)] and these voltage vectors with respect to INV1 can be generated with a PWM controller using $V_{\rm sr1}$ as the reference space phasor. As we have explained earlier, these vectors are transformed to, active vectors $\mathbf{OS}$ and $\mathbf{OH}$ and the zero vector in the combined inverter. In the proposed work, $\mathbf{OS}$ is realized by the space phasor combination $13'$ and $\mathbf{OH}$ is realized by $15'$ (for sequence-1, Fig. 4). A simple digital logic can be used to translate the vectors generated by the controller with respect to INV1, to the actual vectors of the combined inverter. Whenever the PWM controller for INV1 outputs $\mathbf{OA}$ digital logic maps it to $13'$ and generates the gate signals for the corresponding switches in INV1 and INV2. Whenever the PWM controller output is $\mathbf{OB}$, the digital logic generates the switching signals corresponding to the combination $15'$. The digital logic similarly generates the respective switching signals for the all individual vectors of INV1. Hence, the PWM generation for the proposed work has the following steps:

a) map the reference voltage space vector to the corresponding component for an individual inverter (INV1);
b) generate the switching vectors with respect to INV1 with this mapped reference space vector;
c) translate the switching vectors of INV1 to the actual vectors of the combined vector using a digital logic.

The zero vectors which could be used with sequence-1, are $11'$, $33'$, and $55'$. The zero vector to be applied in any sector is selected such that, while the reference space vector is in a

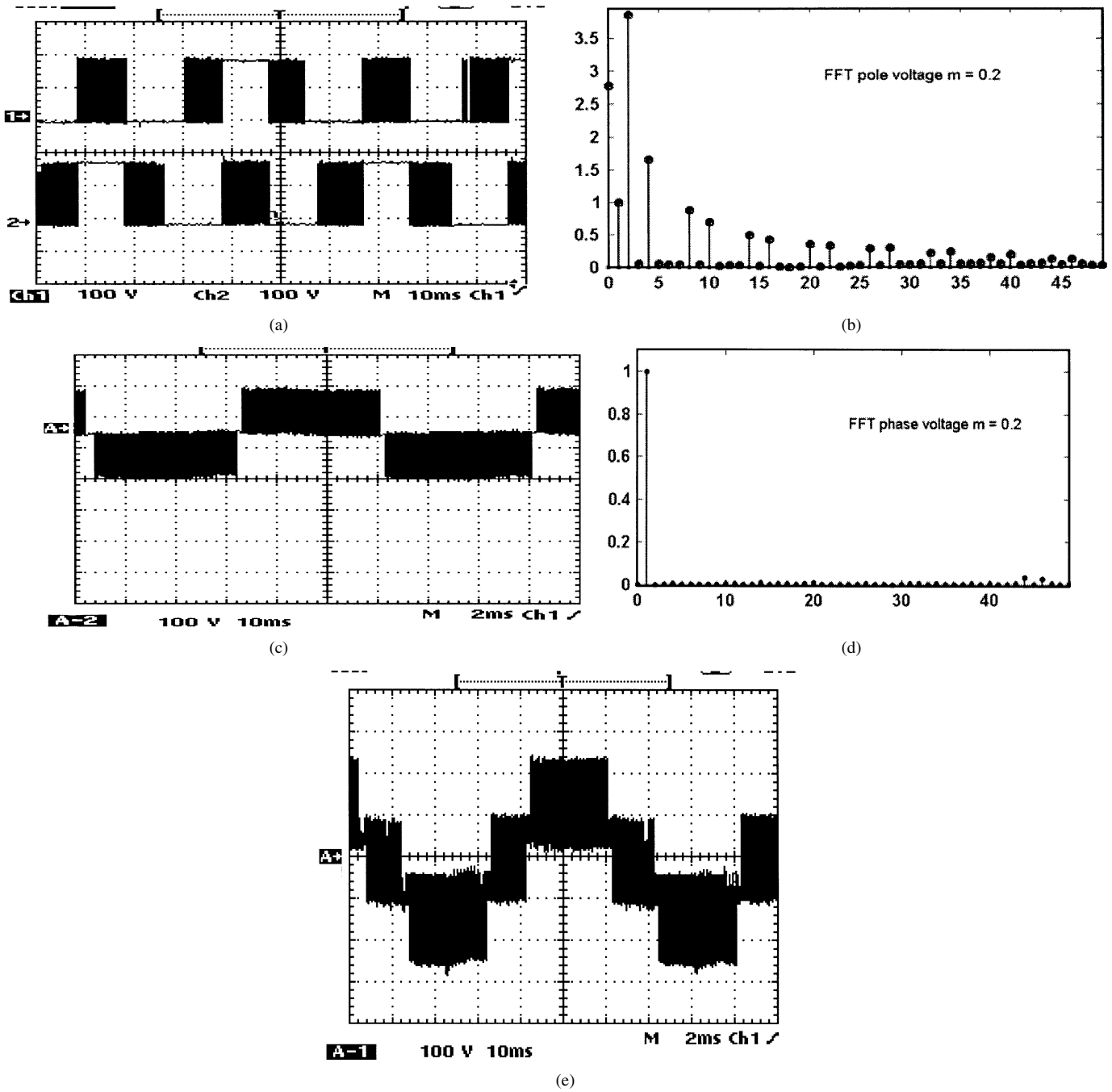
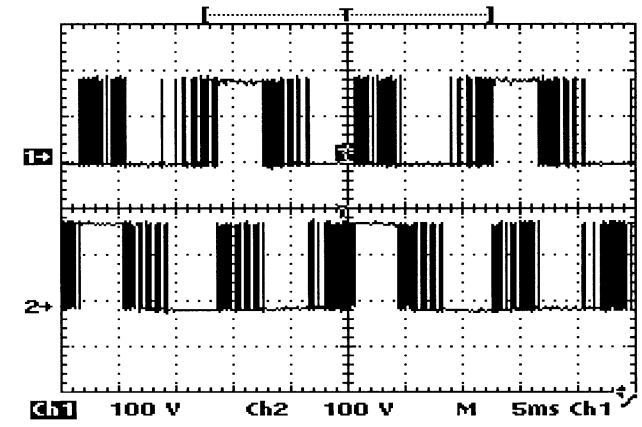


Fig. 6. (a) Pole voltages of INV1 and INV2 for $[m = 0.2]$ ($\mathrm{V_{A10}}$ and $\mathrm{V_{A20}}$) [X-axis 1 div = 10 ms: Y-Axis 1 div = 100 V]. (b) The normalized harmonic spectrum of Pole voltage: $\mathrm{m} = 0.2$. (c) The phase voltages $\mathrm{V_{A1A2}}$ for $[m = 0.2]$ [X-axis 1 div = 10 ms: Y-Axis 1 div = 100 V]. (d) The normalized harmonic spectrum of Phase voltage: $\mathrm{m} = 0.2$. (e) The equivalent line voltage $(\mathrm{V_{A1A2}} - \mathrm{V_{B1B2}})$ for $m = 0.2$ [X-axis 1 div = 10 ms: Y-Axis 1 div = 100 V].

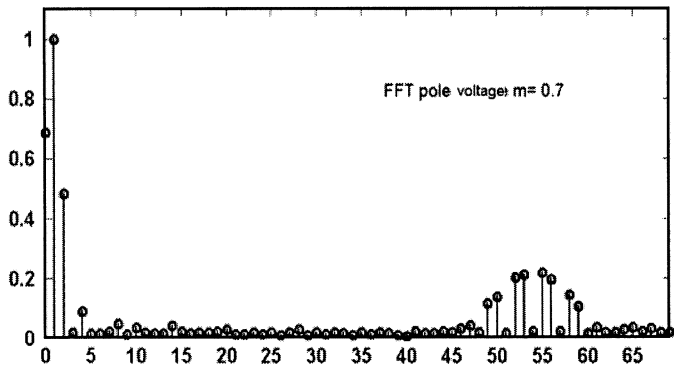
particular sector of the combined inverter, only one of the inverters is switching and the other is clamped to a particular state. Zero vector $11'$ is used for sector-1 and sector-4. With these zero vectors, in sector-1, INV1 is clamped to a state of 1 and INV2 switches amongst $1'$, $3'$, and $5'$. In sector-4 with $11'$ as the zero vector, INV1 switches amongst 1, 3, and 5 while INV2 is clamped to $1'$.

B. Generation of the Reference Space Vector for the PWM Controller

Let V_{sr} be the instantaneous reference space phasor making an angle α with the A-phase axis as shown in Fig. 5(c). This vector has to be realized by switching the vectors **OS** and **OH** along with the zero vectors of the combined inverter as it is in sector-1. This vector can be mapped to corresponding vector with respect to INV1, for which the magnitude and angular relations are to be determined. The ratio of the magnitudes of the reference vector for the combined inverter V_{sr} and the reference vector for the individual inverter will be same as the ratio of the magnitudes of the voltage space vectors of the combined inverter and the individual inverter. The magnitude of the active vector of the individual two-level inverter is $1/\sqrt{3}$ times the magnitude of the active vector in the combined inverter [Fig. 5(c)]. Hence, the magnitude of the instantaneous reference



(a)



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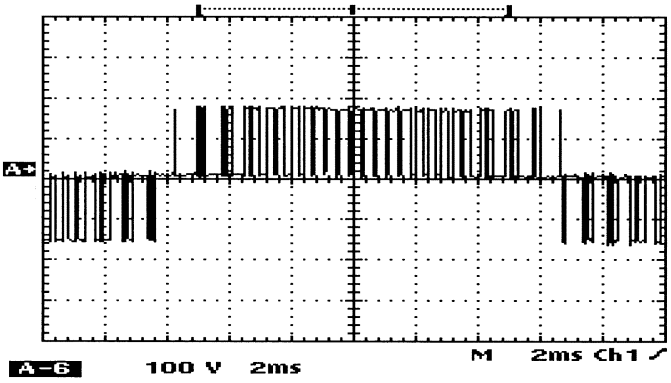

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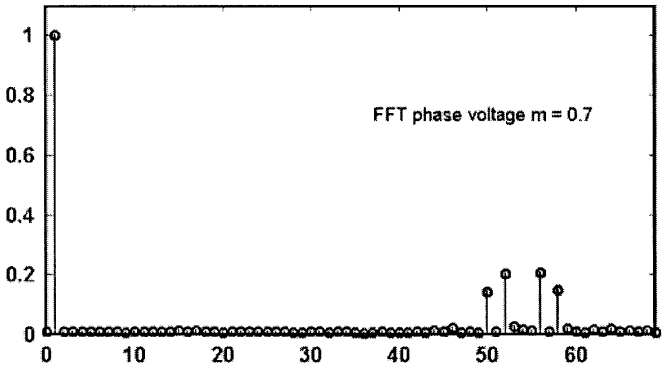

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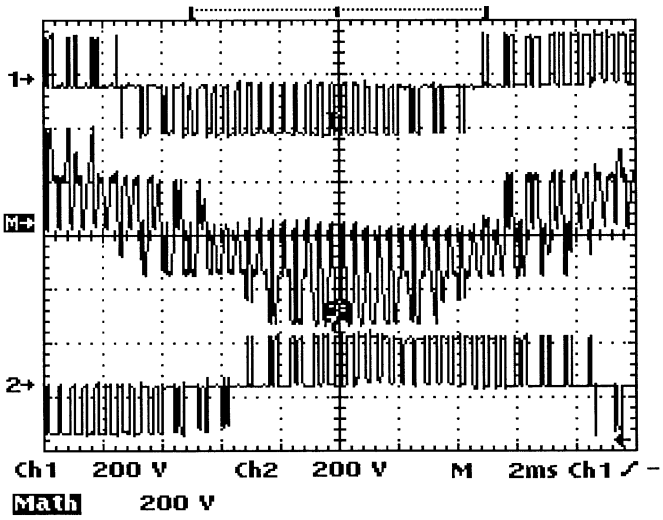


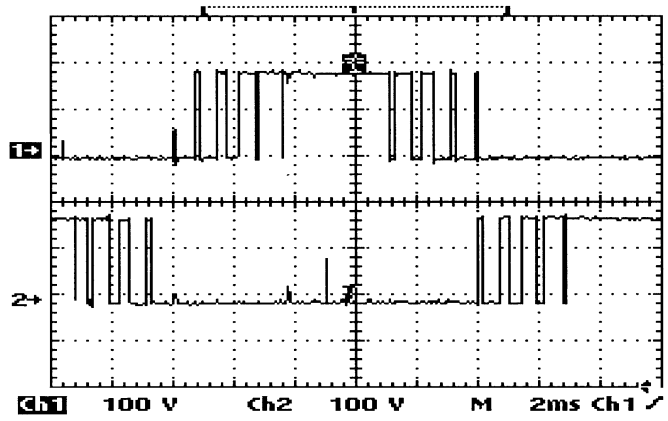
(e)

Fig. 7. (a) Pole voltages of INV1 and INV2 ($\mathrm{V_{A10}}$ and $\mathrm{V_{A20}}$) [for $m = 0.7$ [X-axis 1 div $= 5$ ms: Y-Axis 1 div $= 100$ V]. (b) The normalized harmonic spectrum of the Pole voltage $\mathrm{m} = 0.7$. (c) The phase voltages ($\mathrm{V_{A1A2}}$) for [$m = 0.7$] [X-axis 1 div $= 2$ ms: Y-Axis 1 div $= 100$ V]. (d) The normalized harmonic spectrum of the Phase voltage $\mathrm{m} = 0.7$. (e) The phase voltages (top and bottom) and their difference (line to line voltage) [$m = 0.7$]) [X-axis 1 div $= 2$ ms: Y-Axis 1 div $= 200$ V].

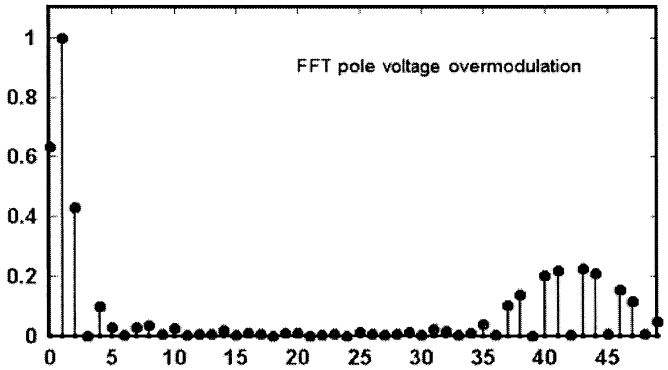
space phasor for INV1 (V_{sr_1}) is $1/\sqrt{3}$ times of the magnitude of the combined reference space phasor, V_{sr}. From Fig. 5(a), the vector **OS** of the dual inverter is transformed to **OA** in INV1 which is leading **OS** by 30°. Similarly **OH** is transformed to **OB** which is leading **OH** by 30°. This can be verified for all the cases, ie the active vector of INV1 leads the respective vector of the combined inverter by 30°. Hence, the transformed instantaneous reference voltage in INV1 also should lead the reference vector of the combined inverter by 30°. Therefore, the mapped reference space phasor in INV1 is given by

$$V_{\mathrm{sr}}(\alpha) = \frac{1}{\sqrt{3}}.V_{\mathrm{sr}}e^{-j30}. \tag{11a}$$

$$V_{\mathrm{sr1}(\alpha)} + jV_{\mathrm{sr1}(\beta)} = \frac{1}{\sqrt{3}}.(V_{\mathrm{sr}(\alpha)} + jV_{\mathrm{sr}(\beta)})e^{-j30}. \tag{11b}$$



(a)



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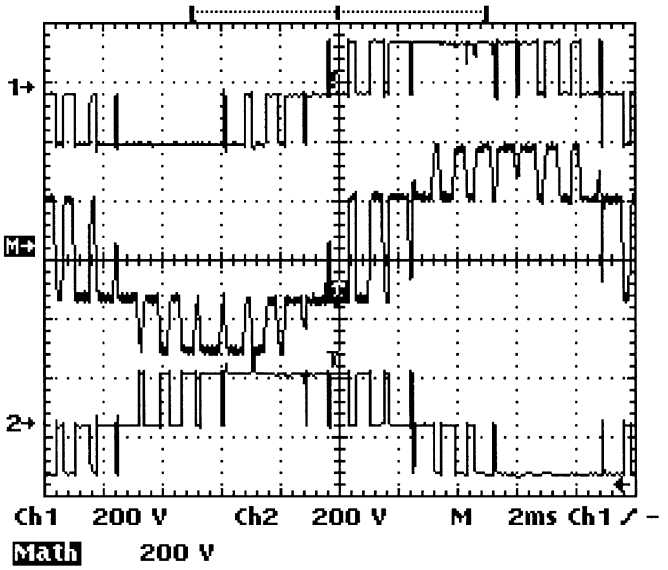

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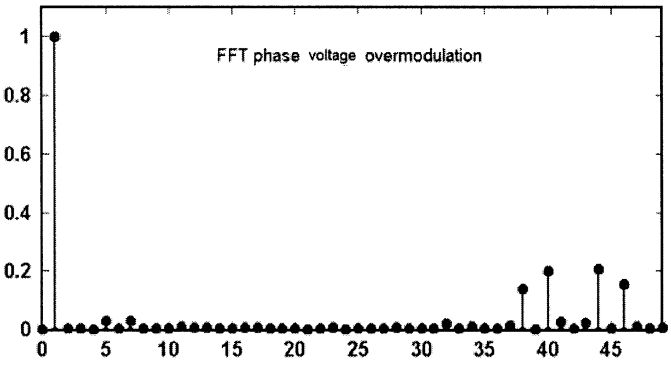


(d)

Fig. 8. (a) Pole voltages of INV1 and INV2 during over-modulation [X-axis 1 div = 2 ms: Y-Axis 1 div = 100 V]. (b) The normalized harmonic spectrum of the Pole voltage during over-modulation. (c) The phase voltages (top and bottom) and their difference (line to line voltage) during over-modulation [X-axis 1 div = 2 ms: Y-Axis 1 div = 200 V]. (d) The normalized harmonic spectrum of the Phase voltage during over-modulation.

If $V_{\rm sr}(\alpha)$ and $V_{\rm sr}(\beta)$ are the components of $V_{\rm sr}$ (for the dual inverter) along the α-β axes, the components of $V_{\rm sr1}$ (corresponding the individual inverter, INV1) along the α-β axes are given by

$$\begin{bmatrix} V_{\rm sr1(\alpha)} \\ V_{\rm sr1(\beta)} \end{bmatrix} = \frac{1}{\sqrt{3}} \begin{bmatrix} \cos 30 & \sin 30 \\ -\sin 30 & \cos 30 \end{bmatrix} \begin{bmatrix} V_{\rm sr(\alpha)} \\ V_{\rm sr(\beta)} \end{bmatrix} = \begin{bmatrix} \frac{1}{2} & \frac{1}{2\sqrt{3}} \\ -\frac{1}{2\sqrt{3}} & \frac{1}{2} \end{bmatrix} \begin{bmatrix} V_{\rm sr(\alpha)} \\ V_{\rm sr(\beta)} \end{bmatrix}. \quad (12)$$

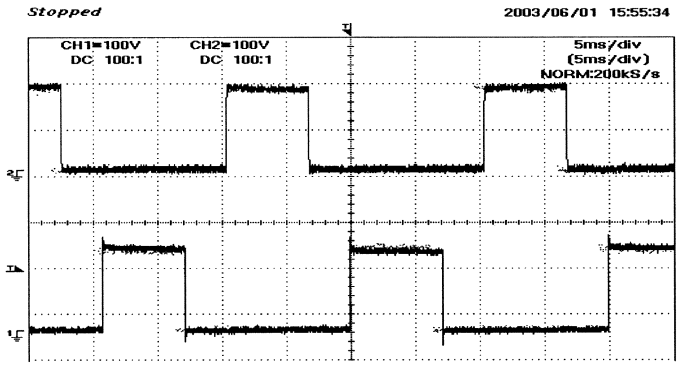
C. Generation of the PWM Signals

The reference space vector obtained with (12) is used by the PWM controller to generate the switching vectors corresponding to INV1. A space vector based PWM with which the switching vectors are directly obtained from the instantaneous reference phase voltages, is used for the present work (The algorithm is given in the Appendix.) [10], [11]. The instantaneous reference phase voltages corresponding to $V_{\rm sr1}(\alpha)$ and $V_{\rm sr1}(\beta)$ are obtained by the transformation (for the individual inverter, INV1)

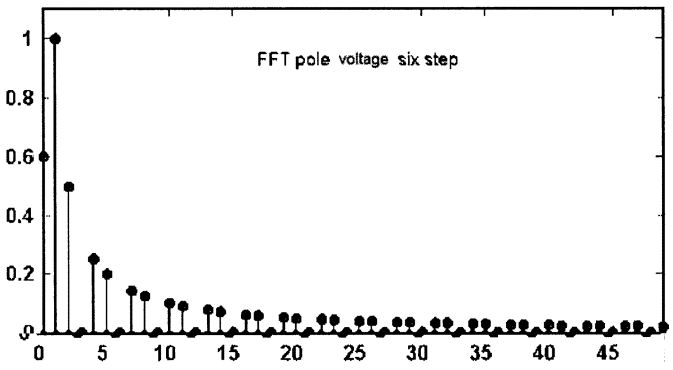
$$\begin{bmatrix} V_{a1} \\ V_{b1} \\ V_{c1} \end{bmatrix} = \begin{bmatrix} \frac{2}{3} & 0 \\ -\frac{1}{3} & \frac{1}{\sqrt{3}} \\ -\frac{1}{3} & -\frac{1}{\sqrt{3}} \end{bmatrix} \begin{bmatrix} V_{\rm sr1(\alpha)} \\ V_{\rm sr1(\beta)} \end{bmatrix}. \quad (13)$$

These instantaneous reference phase voltages are used by the PWM controller to generate the switching vectors of inverter-1 (13), which are then translated to the switching vectors of the combined inverter by deriving the corresponding gate drive signals for INV1 and INV2. Table I shows the logic to translate the active switching vectors generated by the PWM controller (for INV1), to gate drive signals for INV1 and INV2 so that the switching vectors of INV1 are translated to the actual vectors of the dual inverter.

As mentioned earlier, the zero vectors ($11'$, $33'$, and $55'$) are distributed in different sectors such that in any sector one of the inverter is clamped to a particular state. Sector-1 and sector-4 uses $11'$ as zero vector, sector-2 and sector-2 uses $33'$ and sector-3 and sector-6 uses $55'$. These pair of sectors can



(a)



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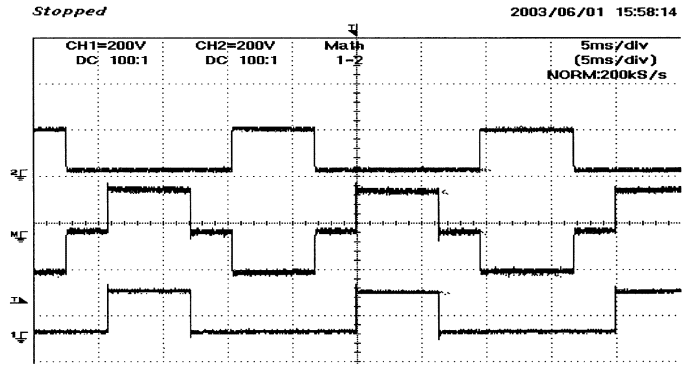

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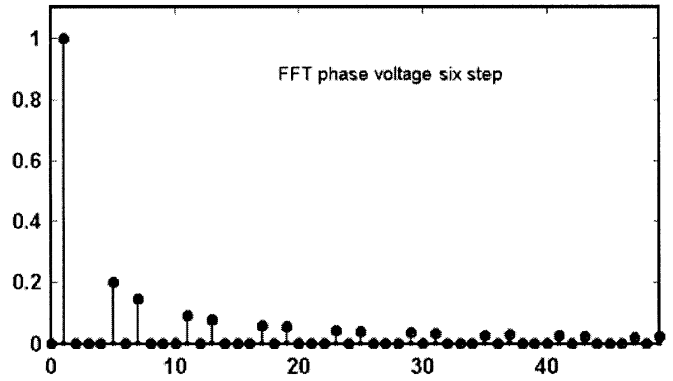

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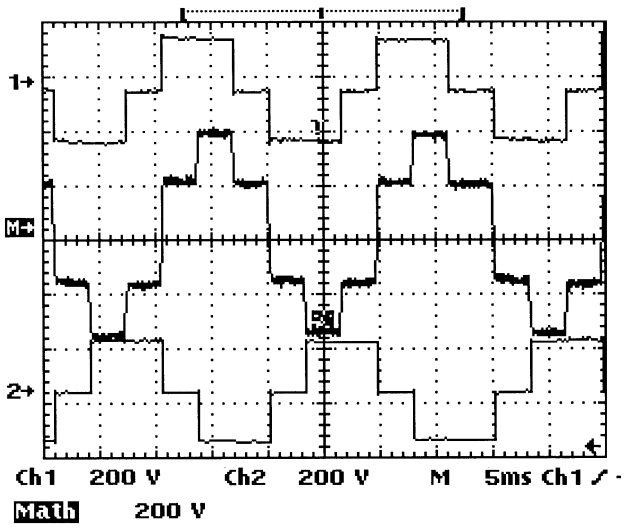

(e)

Fig. 9. (a) Pole voltages of INV1 and INV2 during six-step operation [X-axis 1 div = 5 ms: Y-Axis 1 div = 100 V]. (b) The normalized harmonic spectrum of the Pole voltage during six step operation. (c) The pole voltages (top and bottom) and their difference voltages during six-step operation [X-axis 1 div = 5 ms: Y-Axis 1 div = 200 V]. (d) The normalized harmonic spectrum of the Phase voltage during six step operation. (e) The phase voltages (top and bottom) and their difference (line to line voltage) during six-step operation [X-axis 1 div = 5 ms: Y-Axis 1 div = 200 V].

be identified by checking the phase which has the middle value of the three phase voltage amplitudes. It can be verified that, if the reference space vector is in Sector 1 or 4 B-phase will be the middle phase, in sector-2 or sector-5 A-phase will be the middle phase and if the reference space vector is in sector-3 or sector-6, C-phase will be the middle phase. The PWM controller generates three signals (mid_a, mid_b and mid_c) one of which will be high when a particular phase is the middle phase. The digital logic uses these signals to generate the gate signals during the zero vector duration. Table III shows the part of the logic to generate the gate signal during the zero vectors.

The algorithm for the PWM generation and generation of the actual switching vectors is given in Appendix.

IV. Experimental Results

The proposed PWM scheme is implemented for a 1 kW open end winding induction motor drive with single power supply of

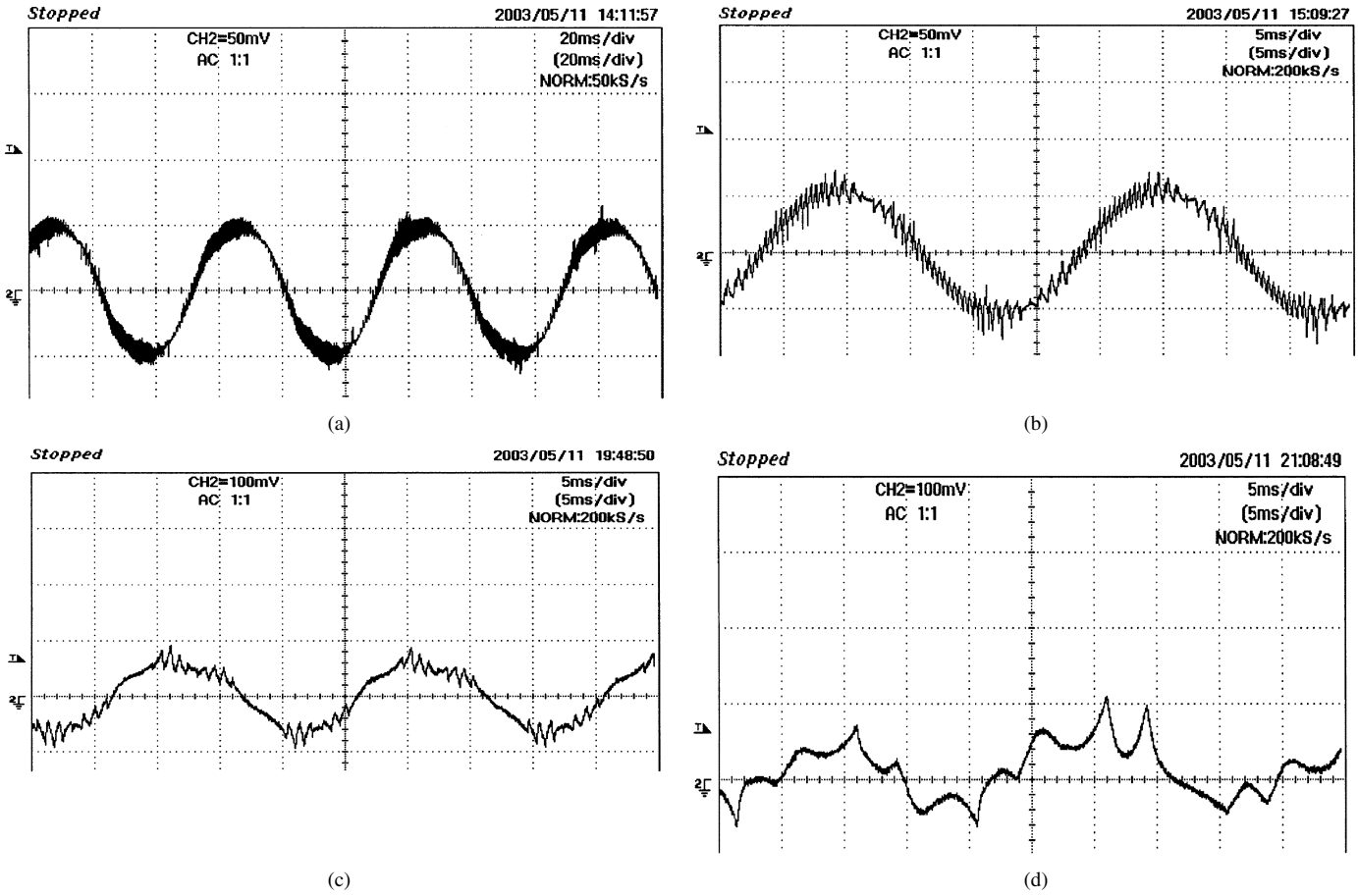

Fig. 10. (a) Motor phase current at no-load for $\mathrm{m} = 0.2$ [X-axis 1 div $= 20$ ms: Y-Axis 1 div $= 1$ Amp]. (b) Motor phase current at no-load for $\mathrm{m} = 0.7$ [X-axis 1 div $= 5$ ms: Y-Axis 1 div $= 1$ Amp]. (c) Motor phase current at no-load during over-modulation [X-axis 1 div $= 5$ ms: Y-Axis 1 div $= 1$ Amp]. (d) Motor phase current at no-load during six-step operation [X-axis 1 div $= 5$ ms: Y-Axis 1 div $= 1$ Amp].

200 V $(V_{\mathrm{dc}}/2)$. The controller is implemented in TMS320F240 DSP platform. The drive was operated under $\mathrm{v/f}$ and was accelerated to the rated speed. The inverter switching frequency is kept constant around 1KHz for the entire speed range. The drive is operated with different set speeds to study the operation under different modulation index and the results are presented. Fig. 6(a) shows the pole voltages of INV1 and INV2 (V_{A10} and V_{A20}) for low speed range $(\mathrm{m} = 0.2)$. The pole voltages are at 180° out of phase as expected and they do not have the half wave symmetry as the inverters are only switching through vectors 1, 3, and 5 (Fig. 4). The pole voltage of INV1 (V_{A10}) is clamped to high level when the reference space phasor is in sector-1 and the pole voltage of INV2 (V_{A20}) is clamped when it is in sector—4.

Fig. 6(b) shows the harmonic spectrum of the pole voltages and it has no triplen components. The pole voltage shows even order harmonics and this is expected as the inverters switch only through the states 1, 3, and 5. The pole voltages from the inverters (at the end of the phase winding) are at 180° out of phase and these even order harmonics get cancelled and the fundamental components get added. Hence, these even order harmonics do not appear in the phase voltage. Fig. 6(c) shows the phase voltage V_{A1A2} and the absence of triplen components in the phase voltage is evident from its harmonic spectrum presented in Fig. 6(d). Fig. 6(e) shows the difference of two phase voltages $(V_{A1A2} - V_{B1B2})$. Since it is the difference between two phase voltages, it is equivalent to the line-to-line voltage as in the case in the conventional single-inverter fed induction motor drive. The line voltage shows the six-step profile, confirming the two-level operation of the dual inverter. Fig. 7(a) shows the pole voltages for the higher speed range $(\mathrm{m} = 0.7)$ and Fig.7(b) shows the corresponding spectrum.

Fig. 7(c) shows the phase voltage for this modulation index $(\mathrm{m} = 0.7)$ and Fig. 7(d) shows the harmonic spectrum of the phase voltages. Two phase voltages and their difference (equivalent line voltage), are presented in Fig. 7(e). The drive is operated in the over modulation region also, where the reference space phasor is forced to trace the hexagonal boundary. Fig.8(a) shows the pole voltages and it does not show the switchings corresponding to the zero vectors as only active vectors are switched while tracing the hexagon. Fig. 8(b) shows the harmonic spectrum of the pole voltage during over-modulation and its shows presence of fifth and seventh harmonic as the reference space vector is now tracing the hexagon. The phase voltage also [Fig. 8(c)] shows reduced switchings and the fifth and seventh harmonic presence is visible in the harmonic spectrum of the phase voltage in Fig. 8(d). Fig. 9(a) shows the pole voltages during six step operation and Fig. 9(b) shows the normalized harmonic spectrum of the pole voltages. The waveforms show that the pole voltages are 180° out of phase and the pole voltages are not symmetric as they switch only through the states of 1, 3, and 5. Fig.9(c) shows pole voltages and the phase voltage during six step operation and Fig. 9(d) presents the harmonic

TABLE II
LOGIC TO TRANSLATE THE ACTIVE VECTORS FOR SEQUENCE-1

Switching vector of INV1(Fig.3)	Actual Active vector of the dual inverter (Fig. 4)	Gate drive for INV1 (Fig.3)			Gate drive for INV2 (Fig.3)		
		S_{11}	S_{13}	S_{15}	S_{21}	S_{23}	S_{25}
1 (+ --)	13'	1	0	0	0	1	0
2 (+ +-)	15'	1	0	0	0	0	1
3 (- + -)	35'	0	1	0	0	0	1
4 (- + +)	31'	0	1	0	1	0	0
5 (- - +)	51'	0	0	1	1	0	0
6 (+ - +)	53'	0	0	1	0	1	0

TABLE III
LOGIC TO TRANSLATE THE ZERO VECTORS

Middle phase (From the Controller)			The zero vector of the dual inverter (Fig.4)	Gating signals for INV1			Gating signals for INV2		
mid_a	mid_b	mid_c		S_{11}	S_{13}	S_{15}	S_{21}	S_{23}	S_{25}
1	0	0	55'	0	0	1	0	0	1
0	1	0	11'	1	0	0	1	0	0
0	0	1	33'	0	1	0	0	1	0

spectrum of the phase voltage which shows the presence of the $6n \pm 1$ order harmonics due to the six step mode of operation. The phase voltages and their difference (equivalent line voltage) are presented in Fig. 9(e). Fig.10(a)–(d) shows the current waveforms at no-load for the different modes of operation.

V. CONCLUSION

1) A space vector based PWM to eliminate alternating common mode voltage in the dual inverter fed open end winding induction motor drive is presented in this paper
2) With the proposed scheme, the zero sequence currents do not flow in the machine phase windings as no common mode voltage exists in the phase windings and the dual inverter can be operated from a single power supply.
3) The individual inverters do not generate any alternating common mode voltage and hence possibility of common mode voltage coupling is avoided.
4) The proposed drive does not experience any neutral point fluctuations compared to the common mode voltage elimination scheme based on conventional neutral point clamped three-level inverter.
5) The proposed drive has a simple power circuit consisting of two standard two-level inverters, and does not require the neutral point clamping diodes.
6) The proposed scheme uses a single dc-link with half the voltage of the common mode elimination scheme based on the conventional three-level inverter.

APPENDIX
ALGORITHM TO GENERATE THE SWITCHING VECTORS OF THE DUAL INVERTER WITH COMMON MODE ELIMINATION

The algorithm employs a space vector based PWM scheme to generates the drive signals for the dual inverter from the instantaneous amplitudes of the reference phase voltages. The principle of this space vector scheme is to achieve centering of the duration of the active vectors within a switching period [10], [11].

1) Read the instantaneous amplitudes of the reference phase voltages for the dual inverter; $V_{a\_\mathrm{ref}}, V_{b\_\mathrm{ref}}, V_{c\_\mathrm{ref}}$. Find the α, β components of the reference space phasor for the dual inverter $V_{\mathrm{sr}}(\alpha)$ and $V_{\mathrm{sr}}(\beta)$ using the following transformation:

$$\begin{bmatrix} V_{\mathrm{sr}(\alpha)} \\ V_{\mathrm{sr}(\beta)} \end{bmatrix} = \begin{bmatrix} 3/2 & 0 & 0 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \end{bmatrix} \begin{bmatrix} V_{a\_\mathrm{ref}} \\ V_{b\_\mathrm{ref}} \\ V_{c\_\mathrm{ref}} \end{bmatrix}.$$

2) Find the α, β components of the reference space phasor with respect to INV1, $V_{\mathrm{sr1}}(\alpha)$ and $V_{\mathrm{sr1}}(\beta)$ using (12).
3) Find the instantaneous amplitudes of the phase voltages (V_{a1}, V_{b1}, V_{c1}) for INV1 using (13).
4) Generate the switching vectors of INV1 using these instantaneous reference amplitudes, as follows.
   a) Convert these voltages to a proportional times by the following equations [10], [11]

$$T_{a\_\mathrm{ref}} = V_{a1} \times \frac{Ts}{(V'_{\mathrm{dc}}/2)}; \quad V'_{\mathrm{dc}} = \frac{\sqrt{3}V_{\mathrm{dc}}}{2}$$
$$T_{b\_\mathrm{ref}} = V_{b1} \times \frac{Ts}{(V'_{\mathrm{dc}}/2)}; \quad \mathrm{T_{c\_ref}} = \mathrm{V_{c1}} \times \frac{\mathrm{Ts}}{(\mathrm{V'_{dc}}/2)}.$$

   b) Sort these times and determine, $\mathrm{T_{max}}, \mathrm{T|}$, and $\mathrm{T_{min}}$.
   c) The duration of the active vector $\mathrm{T_{effective}}$ is given by $\mathrm{T_{effective}} = \mathrm{T_{max}} - \mathrm{T_{min}}$.
      The duration of the zero vector period is given by, $\mathrm{T_{zero=}Ts} - \mathrm{T_{effective}}$.
      The centering of the active vector is achieved by adding a offset time $\mathrm{T_{offset}}$, to the individual times, $T_{a\_\mathrm{ref}}, T_{b\_\mathrm{ref}}, T_{c\_\mathrm{ref}}$. This makes the zero vector durations equal to $\mathrm{Tzero}/2$ each.
      $\mathrm{T_{offset}} = \mathrm{T_{zero/2}} - \mathrm{T_{min}}$.
   d) The inverter leg switching timings (for INV1) $T_{\mathrm{ga}}, T_{\mathrm{gb}}, T_{\mathrm{gc}}$, are obtained by adding this offset value to $T_{a\_\mathrm{ref}}, T_{b\_\mathrm{ref}}, T_{c\_\mathrm{ref}}$. These PWM outputs $(T_{\mathrm{ga}}, T_{\mathrm{gb}}, T_{\mathrm{gc}})$, define the switching vector of INV1 [10], [11].
5) Generate signals mid_a, mid_b, and mid_c, which indicates which of the reference phase voltages for INV1 (V_{a1}, V_{b1}, V_{c1}) is currently the mid phase. If A-phase is the mid phase the signal mid_a is made '1', if B-phase is the mid phase mid_b is made '1' and if C-phase is the mid phase mid_c is made "1."

6) Generate the drive signals for INV1 and INV2 with the logic in Tables II and III using the PWM outputs $T_{\rm ga}, T_{\rm gb}, T_{\rm gc}$ and signals mid_a, mid_b, and mid_c.

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