A Dynamic Power Reduction Technique for Incremental $\Delta\Sigma$ Modulators

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***Abstract*—This paper presents a dynamic power reduction technique for incremental $\Delta\Sigma$ (I-$\Delta\Sigma$) modulators. The technique makes use of the unequal weighting of the digital reconstruction filter. The underlying idea is that the input signal samples are not equally weighted in the higher order reconstruction filter. Thus, it is possible to increase the non-idealities of the I-$\Delta\Sigma$ modulator during the runtime of a single Nyquist conversion, thereby saving power. This principal idea is verified by an example design, where the input-referred noise of the first integrator is dynamically increased, which allows for improved efficiency. The proposed technique is readily applicable to every state-of-the-art I-$\Delta\Sigma$ modulator. Furthermore, it is shown that this property can also be used to switch a single-bit DAC into a multibit DAC during runtime, thereby greatly improving the achievable SQNR without suffering from the DAC non-linearity. The prototype I-$\Delta\Sigma$ modulator is manufactured in a 180 nm CMOS technology and achieves a DR/SNDR = 91.5/86.6 dB for a sampling rate of 200 kS/s while consuming 1.1 mW from a 3 V supply, while the dynamic power reduction method accounts for 30% power savings.**

***Index Terms*—ADC, biomedical, delta sigma, discrete time, dynamic power reduction, slicing**

I. Introduction

In many sensor applications, such as in high-channel count biomedical applications as presented in [1], analog-to-digital converters (ADCs) feature resolutions exceeding 14 bits. These ADCs must be capable of being multiplexed between individual channels without memory and thus without inter-sample interference. Therefore, they need to provide true sample-to-sample conversion at Nyquist-rate. SAR ADCs offer the best efficiency for a huge range of sampling frequencies and resolutions in the recent state of the art. But to achieve high resolution (e.g. ≥ 14 bits) and high linearity (e.g. ≥ 90 dB), almost exclusively noise-shaping and mismatch-error-shaping have been used. However, these techniques introduce memory to the system and thus ADCs making use of these techniques can not be multiplexed. Similarly, freely-running $\Delta\Sigma$ modulators dominate the state of the art in efficiency for high-resolution designs. Again, they use noise-shaping and have memory by their loop and decimation filters and thus can not be multiplexed nor do they offer true Nyquist-rate sample-to-sample conversion. However, there are solutions as presented in [2], [3] using freely-running $\Delta\Sigma$ modulators in multiplexed operation. Still, they come with drawbacks like decreased power efficiency or increased crosstalk and inter-sample interference. Another candidate for high-resolution, yet true Nyquist-rate conversion, is the incremental Delta-Sigma (I-$\Delta\Sigma$) ADC. It still features similar properties like the freely-running $\Delta\Sigma$ ADC, as oversampling and noise-shaping. In contrast, the regular reset of its filters makes true Nyquist-rate operation possible. While offering Nyquist-rate conversion capabilities, I-$\Delta\Sigma$s are less power efficient than freely-running $\Delta\Sigma$ modulators. Although [4] proposes an eighth-order cascaded incremental ADC that can outperform conventional $\Delta\Sigma$s in terms of SQNR for OSRs in the single-digit range, I-$\Delta\Sigma$s usually require higher oversampling for most common modulator architectures. Consequently, all measures to enhance the efficiency of I-$\Delta\Sigma$ ADCs are highly desired.

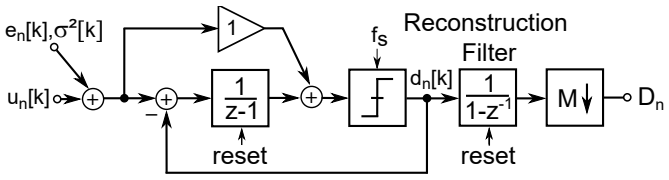

Fig. 1. Block diagram of a 1st order modulator including input-referred noise $e_n[k]$ with variance $\sigma^2[k]$.

This paper proposes a dynamic power reduction scheme as shown in [5], where non-idealities can be successively increased during a single Nyquist-rate conversion. This allows for a successively reduced power during every single conversion step. While it is applicable to all non-idealities within the I-$\Delta\Sigma$ modulator, this paper proves the concept with a dynamically increased input-referred noise of the input stage.

The paper is organized as follows: Section II gives an introduction to the concept of dynamically increased non-idealities in I-$\Delta\Sigma$ ADCs and Section III presents simulation examples. Subsequently, Section IV gives an insight into the circuit-level implementation of this proof of concept. Finally, Section V and VI present measured results of the implemented design and conclude the paper.

II. Theory of Dynamically Increased Non-idealities in I-$\Delta\Sigma$ Modulators

This section provides a mathematical description of the signal behavior of I-$\Delta\Sigma$ ADCs to understand the concept of dynamic power reduction.

A. Weighting Function of the Reconstruction Filter

The considerations of the signal weighting are done in terms of a first order discrete-time I-$\Delta\Sigma$ ADC with feedforward path, also referred to as low-distortion path [6] as shown in

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Fig. 1. Here, k denotes the k-th clock cycle during the n-th Nyquist-rate conversion. The whole structure, comprising the modulator as well as the reconstruction filter, is periodically reset at the end of the M-th clock cycle ($k = M$), where M is the oversampling ratio (OSR). This gives the I-$\Delta\Sigma$ ADC the possibility to be used in multiplexed environments.

Shortly before the reset, only the last value of the output of the digital reconstruction filter D_n is stored. Consequently, every Nyquist-rate conversion consists of M cycles running at the internal sampling rate f_s, whereas the decimated output of the reconstruction filter is only running at Nyquist-rate f_N. Referring again to Fig. 1, the non-idealities are modeled as input-referred error $\mathrm{e}_n[k]$ with variance $\sigma^2[k]$. It will be shown afterwards that this variance can also be made time varying by increasing this input-referred noise during runtime. Extending the findings from [7], the signal content contained in the decimated digital output sample D_n of the reconstruction filter for the n-th Nyquist-rate conversion can be calculated as:

$$\mathrm{D}_n = \sum_{k=1}^{M} \mathrm{d}_n[k] \cdot \mathrm{w}^*[k], \tag{1}$$

where $\mathrm{d}_n[k]$ is the output of the I-$\Delta\Sigma$ modulator during the n-th Nyquist-rate conversion. Here, $\mathrm{w}^*[k]$ are the normalized filter weights for a generic reconstruction filter as a function of cycle k. According to [7], the output of the quantizer $\mathrm{d}_n[k]$ can be determined by the finite length convolution of length M as:

$$\mathrm{d}_n[k] = [(\mathrm{u}_n[k] + \mathrm{e}_n[k]) * stf_\mathrm{mod}[k]]_M + [\mathrm{q}[k] * \mathrm{ntf}_\mathrm{mod}[k]]_M, \tag{2}$$

where $stf_\mathrm{mod}[k]$ and $ntf_\mathrm{mod}[k]$ are the impulse responses of the modulator's signal-and noise transfer functions, respectively. As the error sequence $\mathrm{e}_n[k]$ is already input-referred, it is indistinguishable from the input signal $\mathrm{u}_n[k]$ from the modulator's perspective. The power of the input signal contained in the digital output sample D_n of the n-th Nyquist-rate conversion can be calculated by means of (1) and (2) as linear superposition is applicable.

Referring again to Fig. 1, the decimated output D_n of the n-th Nyquist-rate conversion consists of a signal as well as an input-referred error component and quantization noise. A very common reconstruction filter for I-$\Delta\Sigma$ modulators is the chain-of-integrators (CoI) filter. Without the loss of generality, a CoI filter is used throughout this paper. The filter non-normalized weights $\mathrm{w}_\mathrm{CoI}[k, L, d]$ for a CoI filter of order L with input-to-output delay d, can be calculated as follows:

$$\mathrm{w}_\mathrm{CoI}[k, L, d] = \begin{cases} \frac{1}{(L-1)!} \prod_{i=1}^{L-1} (M-d-k+i) & , 1 \le k \le M-d \\ 0 & , \text{else} \end{cases} \tag{3}$$

Here, d is the input-to-output delay. To remove the scaling due to the reconstruction filter, the filter weights should be divided by the normalization factor N_F that can be obtained as:

$$N_F = \sum_{k=1}^{M} w_\mathrm{CoI}[k, L, d] = w_\mathrm{CoI}[1, L+1, d]. \tag{4}$$

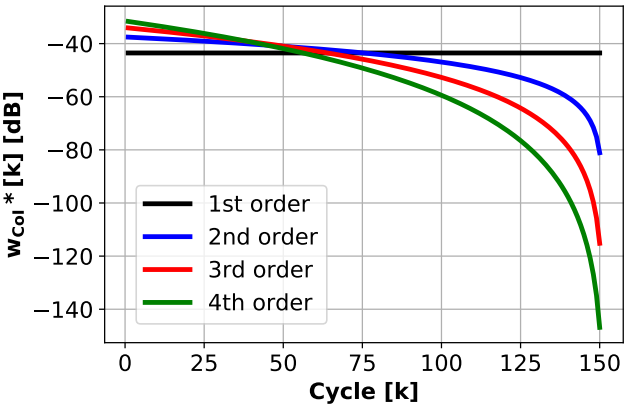


Fig. 2. Logarithmic plot of the normalized filter weight $\mathrm{w}_\mathrm{CoI}*[k]$ for a 1st to 4th order CoI filter.

A logarithmic plot of the normalized weighting ($\mathrm{w}^*_\mathrm{CoI} = \mathrm{w}_\mathrm{CoI}/\mathrm{N}_\mathrm{F}$) of a delay-less CoI filter of first to fourth order, given an exemplary OSR of $M = 150$, is shown in Fig. 2.

It can clearly be observed that a first order filter features equal weighting for all cycles. In contrast, for higher order filters, the signal weighting is shifted more and more towards early cycles. This property can be used to loosen requirements on the modulator non-idealities towards the end of a conversion cycle, thereby possibly saving power without suffering from a radical drop in performance. Before simulating this approach in Section III, in the following the influence of circuit noise on I-$\Delta\Sigma$ ADCs is shortly investigated to be able to compare the analysis with simulations thereafter.

B. Noise Performance of I-$\Delta\Sigma$ Modulators

The noise performance is a decisive factor for the power consumption of any I-$\Delta\Sigma$ modulator. In the following, it is analyzed how non-equal weighting of the reconstruction filter influences the achievable SNR. As a discrete-time I-$\Delta\Sigma$ modulator is realized, the noise of a switched-capacitor (SC) input stage, as depicted in Fig. 3, is investigated. An in-depth analysis of the noise behavior of SC circuits is performed in [8]. In the following, this is slightly extended by also taking the 1/f noise into account and also by adopting the results to discrete-time I-$\Delta\Sigma$ modulators.

Equation (5) shows the input-referred noise of a commonly used stray-insensitive SC integrator. In [8], this is derived from the sampling switch noise and the OTA's input-referred noise during the two operation phases of the SC integrator:

$$\overline{\mathrm{v}^2_\mathrm{Cs}} = \frac{k_B T}{C_s}\left(1 + \frac{2R_{sw}g_m}{1+2R_{sw}g_m}\right) + \underbrace{\frac{\mathrm{S}_\mathrm{OTA,th}}{4\tau_2}}_{\overline{\mathrm{v}^2_\mathrm{OTA,th}}} + \overline{\mathrm{v}^2_\mathrm{OTA,1/f}}, \tag{5}$$

where k_B is the Boltzmann constant, T is the absolute temperature and C_s is the sampling capacitor. R_sw is the on-resistance of the sampling switches. The input impedance seen towards the OTA's virtual ground can be approximated with $1/\mathrm{g}_\mathrm{m}$ derived at hands of the equivalent circuit shown in top

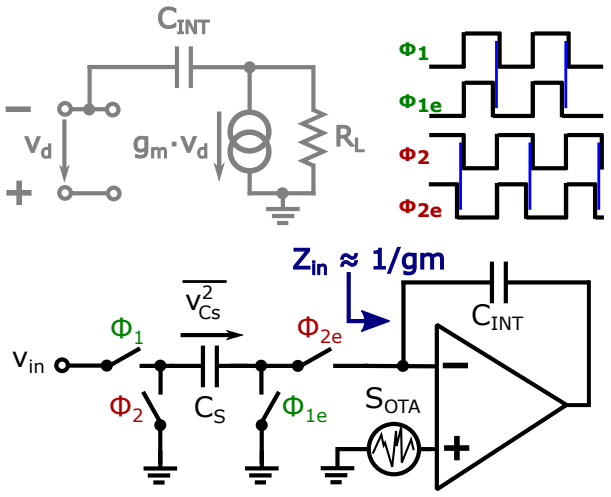


Fig. 3. Schematic of stray-insensitive SC integrator including non-overlapping clocks and equivalent circuit of a single-stage OTA.

left of Fig. 3 under the assumption that R_L is large. $S_{OTA,th}$ is the input-referred power spectral density of the thermal noise of the OTA. The time constant during phase Φ_2, namely τ_2 is given by

$$\tau_2 = (\frac{1}{g_m} + 2R_{sw})C_s. \tag{6}$$

In addition, the input-referred 1/f noise of the OTA $\overline{v^2_{OTA,1/f}}$ has been added to (5), since we later investigate both noise sources using the proposed dynamic increase of non-idealities. While [8] shows that the input-referred thermal noise is filtered by the low-pass characteristic of the OTA, this is not the case for the 1/f noise, if - as usually the case - the 1/f corner frequency is lower than $1/\tau_2$. Therefore, the 1/f noise contribution of the OTA is seen one by one on the sampling capacitor.

Since the dynamic reconfiguration of the I-$\Delta\Sigma$ modulator will have a large impact on the noise contribution in the circuit implementation, in the following the OTA noise is derived and evaluated within the SC integrator and the I-$\Delta\Sigma$ ADC as well. For a simple CMOS OTA, i.e. a differential stage with current mirror load [8], and assuming all devices are identical and operated in strong inversion, the input-referred noise power spectral density becomes:

$$S_{V,tot} \approx \underbrace{\frac{16k_BT}{3g_{m1}}}_{S_{OTA,th}} + \underbrace{\frac{2K_F}{C_{ox}^2 \cdot W_1L_1 \cdot f}}_{S_{OTA,1/f}}, \tag{7}$$

where K_F is a technology dependent factor, C_{ox} denotes the oxide capacitance per area and W_1, L_1 are the width and length of the input transistor pair, respectively. To obtain the 1/f noise power $\overline{v^2_{OTA,1/f}}$, which was introduced in (5), one has to integrate $S_{OTA,1/f}$:

$$\overline{v^2_{OTA,1/f}} = \frac{2K_F \cdot ln(f_2/f_1)}{C_{ox}^2 \cdot W_1L_1}, \tag{8}$$

TABLE I
EXTRACTED THERMAL NOISE PENALTY FACTOR NP

L \ M	25	50	75	100	150	200
1	1.0	1.0	1.0	1.0	1.0	1.0
2	1.3	1.3	1.3	1.3	1.3	1.3
3	1.7	1.8	1.8	1.8	1.8	1.8
4	2.2	2.2	2.2	2.3	2.3	2.3

where f_1 is a chosen lower bound and f_2 can be approximated with f_c, which is the 1/f noise cutoff frequency. Using (5), (6), and (7), $\overline{v^2_{OTA,th}}$ can be obtained as:

$$\overline{v^2_{OTA,th}} = \frac{S_{OTA,th}}{4\tau_2} = \frac{4k_BT}{3C_s}(\frac{1}{1+2R_{sw}g_m}). \tag{9}$$

Plugging this in (5) yields:

$$\overline{v^2_{Cs}} \approx \underbrace{\frac{k_BT}{C_s}(\frac{7/3+4R_{sw}g_m}{1+2R_{sw}g_m})}_{\overline{v^2_{Cs,th}}} + \underbrace{\frac{2K_F \cdot ln(f_c/f_1)}{C_{ox}^2 \cdot W_1L_1}}_{\overline{v^2_{OTA,1/f}}}. \tag{10}$$

As explained later, it is valid to assume a modulator with unity STF, the calculated input-referred noise power of the input stage of the I-$\Delta\Sigma$ modulator $\overline{v^2_{Cs}}$ can directly be transferred to the output of the ADC. Then, the following integral must be solved:

$$\overline{D^2_{noise}} = \frac{\overline{v^2_{Cs,th}}}{fs}\int_{-0.5}^{0.5} |\sum_{k=1}^{M} w^*_{CoI}[k] \cdot e^{-j2\pi fk}|^2 df + \overline{v^2_{OTA,1/f}}$$
$$\approx \frac{np}{M} \cdot \frac{2k_BT}{C_s}(1 + \frac{1/6}{1+2R_{sw}g_m}) + \frac{2K_F \cdot ln(f_c/f_1)}{C_{ox}^2 \cdot W_1L_1}. \tag{11}$$

This can either be done analytically or numerically. The second part of (11) is a simplified version of the analytical solution, where np is called thermal noise penalty factor [7]. The factor np has been calculated for different values of OSR and filter orders. The result are shown in Table I. It can directly be seen that the noise penalty is weakly dependent on the OSR but strongly dependent on the chosen architecture, which sets the filter order L. From (11) it becomes clear that the power of the white noise is reduced by the factor np/M. Thus, it takes advantage of the oversampling nature of the I-$\Delta\Sigma$ ADC, but in contrast to a freely-running one, np corresponds to the penalty for the Nyquist-rate operation. In a proper design, the 1/f noise corner can be assumed to be below the maximum signal bandwidth and therefore it fully contributes to the noise power without being affected by the digital filter. Therefore, it is up to the designer to reduce the effect of 1/f noise to meet the overall noise requirements.

What is used later for the dynamic increase of noise in the I-$\Delta\Sigma$ is the possibility from (11) of scaling the input-referred thermal noise power by linearly scaling the sampling capacitor and the 1/f noise by linearly scaling the input pair of the OTA.

III. SIMULATION EXAMPLE

This section gives simulation examples that investigate different sources of non-idealities. Thereby, we investigate the dynamic increase of noise, for which the analysis in the

TABLE II
SCALING COEFFICIENTS OF THE EXAMPLE MODULATOR

c1	c2	c3	a1	a2	a3
0.2393	0.4309	0.155	9.752	8.942	5.916

previous section gave the circuit level foundation, and which is also being used for the prototype implementation in Section IV. In addition, it is shown that the dynamic increase of non-idealities can also be extended to other error sources. Therefore, also settling errors and DAC non-linearity errors are investigated. The example 3rd order CIFF modulator is depicted in Fig. 4. The used scaling coefficients are shown in Table II. As the feedforward path is not present in this modulator, the freely-running STF would show slight out-of-band peaking. As the resulting out-of-band peaking mainly affects thermal noise, it is of interest how this relates to the digital output. To answer this, Fig. 5 shows a comparison between the transfer function of the reconstruction filter and the STF of the entire ADC before decimation. Having a look at the absolute difference between both curves, as shown in red, it becomes clear that it is valid to assume STF$\approx$1 as the modulator shows very limited influence on the STF. For the following simulations an OSR=150 has been chosen such that the results are clearly not limited by quantization noise. A simulation without noise leads to an SQNR$\approx$99 dB for a sinusoidal input with an amplitude of -6 dBFS.

A. Dynamic Increase in Noise

It is investigated using a Simulink model, how an increase in the noise over runtime affects the performance of the exemplary I-$\Delta\Sigma$ ADC. Therefore, the input-referred noise voltage is increased ($\times$2 or $\times$4, respectively) during runtime and the expected value of the SNR is calculated for comparison using (11). It is worth mentioning that the SQNR remains unaffected by this technique. The power of thermal and 1/f noise have been chosen such that the noise contributed to the digital output is equal for both components: $\overline{\mathrm{v}_{\mathrm{th}}^2} = \overline{\mathrm{v}_{\mathrm{OTA},1/\mathrm{f}}^2}$ to allow for a noise limited SNR$\approx$ 89 dB assuming again a sinusoidal input signal with an amplitude of -6 dBFS. Now, the noise power is increased after a certain amount of cycles during a single Nyquist-rate conversion. Thereby, the SNR of the ADC is affected according to (1), (2), and (11), where the variance of the input-referred noise becomes now time-dependent. However, it can be shown that the resulting PSD of the noise is still white. Fig. 6 shows this effect of increasing the input-referred noise power during runtime. The three shown simulations are with a constant input-referred noise as well as with a doubled and quadrupled input-referred noise after cycle $1 \leq k < M = 150$. Additionally, the expected values from (1), (2), and (11) are indicated. It can be observed that even increasing the noise power by a factor of four towards the end of a conversion does barely affect the SNDR. Furthermore, the matching between theory and simulation is good.

B. Dynamic Increase of Settling Errors

The required settling accuracy of SC integrators for high-resolution applications sets strict requirements on slew-rate (SR) and gain-bandwidth (GBW) of the implemented OTAs. As the non-idealities of the first integrator in the integrator chain are not shaped by a preceding stage, the linearity requirement of this stage has to be approximately the same as the linearity requirement of the entire modulator. Therefore the first integrator stage is usually designed with highly linear switches and an OTA with very high gain, SR and GBW, respectively. As the most dominant power source in this integrator is the OTA, its non-idealities during the settling process shall be discussed in the following.

The settling of the OTA can roughly be divided into three phases. The first settling phase is dominated by the finite SR of the OTA. Here, the output is linearly charged, as the maximum current available is sunk into the integration capacitor. As soon as the settling process due to GBW limitations is slower than the SR limited settling, an exponential settling behavior can be observed. If enough time is given for settling, the integrator will settle to a final value within a certain distance to the ideal value determined by the finite DC gain. As the time for slewing and exponential settling is highly signal-dependent, harmonic distortion may arise from it if SR and GBW are not chosen sufficiently large. According to [9], this error is exponentially dependent on the input of the first integrator consisting of input and feedback signal, respectively. As for any $\Delta\Sigma$ modulator, this signal is the difference between input signal and feedback signal. As it makes calculations cumbersome, simulations are preferred over an analytical expression to investigate the effects of a dynamic increase in settling errors over runtime on the overall accuracy. Fig. 7 depicts the achieved SNDR for a dynamic reduction of SR and GBW of the first integrator during a single Nyquist-rate conversion cycle of the exemplary I-$\Delta\Sigma$ ADC. For this purpose, all circuit-noise sources are turned off. The input amplitude has been chosen as 0.5 FS. The initial SR and GBW have been chosen such as to allow almost ideal SNDR = SQNR, which is shown as a reference in Fig. 7. After a given time instant $k < M$ during a Nyquist-rate conversion, the SR and GBW have been divided by a factor of two and four, respectively. This is shown in the blue and red curves. Even though it can again be seen that a worsening of the SR and GBW towards the end of a conversion cycle has a decreasingly minor effect, it is obvious that the potential savings are limited, since a severe drop in performance can still be seen even when the switch-off instant is rather late. This is due to strong harmonic distortion as well as quantization-noise-folding. Thus, for the proposed dynamic power saving technique, a circuit technique would be required which allows to increase input-referred noise without significantly affecting the SR and GBW specification. This will be solved in Section IV.

C. Dynamic Increase of Non-Linearities of the Feedback DAC

Before going to the prototype implementation of the proposed technique using dynamic noise increase for a dynamic power saving, yet another non-ideality and its behavior for its dynamic increase is investigated.

Even though it is later not used due to fast prototyping reason, we still present it here to show the generality and the

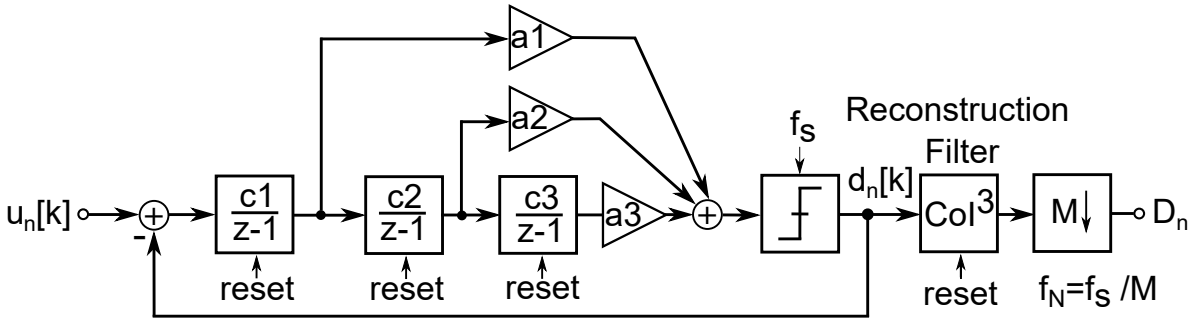


Fig. 4. Block diagram of the implemented 3rd order CIFF architecture with a 3rd order CoI filter.

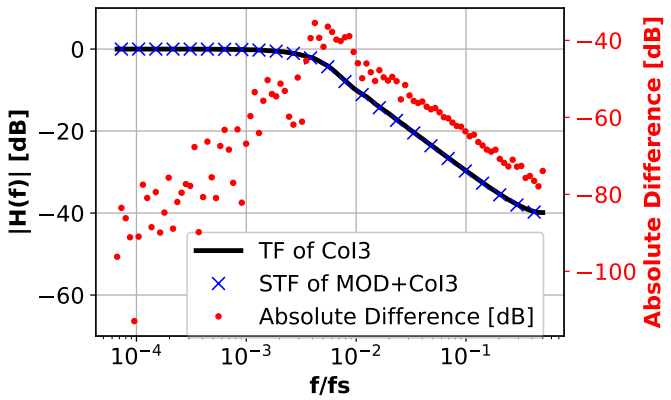


Fig. 5. Comparison of the transfer functions of the reconstruction filter and the STF of the entire ADC (composed of modulator and reconstruction filter) before decimation.

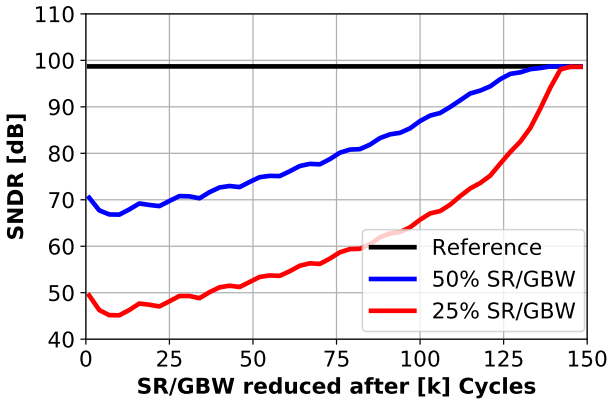


Fig. 7. SNDR for dynamic reduction of SR and GBW to 100% (Reference), 50% and 25%, respectively.

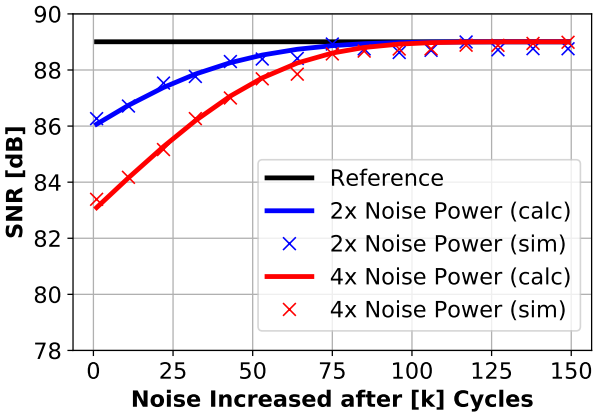


Fig. 6. Calculated (solid) and simulated (crossed) degradation in SNR due to a dynamic increase (×2 or ×4) in thermal noise after cycle k.

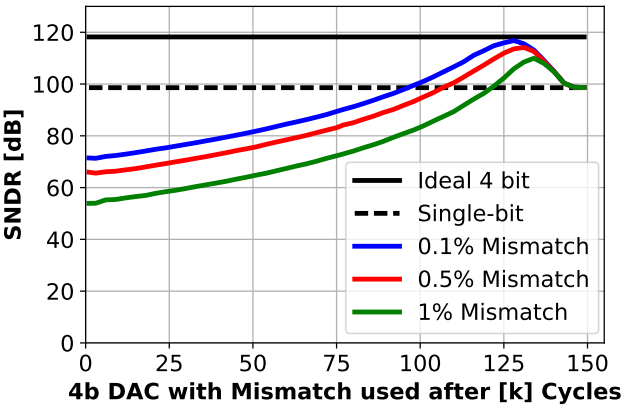


Fig. 8. SNDR for first making use of a single-bit DAC and then after k cycles making use of a 4b DAC with mismatch.

potential of the presented technique. The usage of multibit quantization within ΔΣ modulators is highly beneficial in terms of stability, SQNR and maximum stable amplitude. Besides the higher complexity for the multibit quantizer and feedback DAC, the major drawback of a multibit DAC is the non-linearities that result from component mismatch. Linearization techniques have been used to reduce the influence of harmonic distortion [10], [11], though they are less effective as in freely-running ΔΣ modulators. Therefore, it is proposed here to use the presented dynamic increase of non-idealities in I-ΔΣ ADCs in the context of multibit operation. If the non-linearity of the DAC is only present at later cycles, its influence on the overall SNDR should be minor as compared to when it is present all the time. In

order to allow such a scenario, various possibilities could be approached; in the shown example, a single-bit operation of the exemplary I-$\Delta\Sigma$ modulator is used during the early cycles. Therefore, no harmonic distortion originates in these early cycles. During later cycles, the single-bit operation is changed into a multibit operation, where we left the scaling coefficients (for the sake of simplicity) constant and only dynamically switch in a multibit quantizer and a multibit DAC. The 4b DAC is simulated with a relative component mismatch of 0.1 %, 0.5 %, and 1 %. Very interestingly, it can be seen in Fig. 8, that the high non-linearity severely drops the achievable SNDR of the I-$\Delta\Sigma$, if the multibit operation is started very early. For a late multibit operation, the non-linearity does not affect the output performance anymore, but the better resolution now yields further suppression of the quantization error. Given a certain DAC non-linearity, a sweet spot can be found, which maximizes the achievable SNDR. The earlier the DAC non-linear contribution from the multibit DAC starts, the more it is weighted by the reconstruction filter. This degrades the maximum achievable SNDR by the commonly known harmonic distortion as well as mixing of quantization noise. The later the multibit DAC is switched in, the less effective the residual quantization noise is reduced. Thus, a sweet spot appears. Obviously, the smaller the non-linearity contribution from the multibit DAC, the earlier it is possible to switch in the multibit-DAC without seeing the performance degradation. This moves the sweet spot to earlier switching points, effectively decreases the quantization noise more and thus increases the maximum achievable SNDR. As a reference, the SNDR of an ideal DAC is shown in Fig. 8. It can be seen that for a small mismatch ($\approx$0.1 %) nearly no degradation in performance is visible anymore if the point of multibit activation is chosen to be k = 125. As stated in [12], conventional linearization techniques like DEM/DWA become inefficient in I-$\Delta\Sigma$ ADCs. Therefore, [12] presents an adaptive DEM algorithm, called smart-DEM to solve this shortcoming. However, digital effort is required to linearize the implemented multibit DAC. The implementation proposed in our paper gives the designer the huge advantage, that a non-linear multibit DAC (and a power hungry multibit quantizer) only need to be activated for a short period before the end of every single Nyquist-rate conversion. Moreover, nearly no degradation in the SQNR performance can be observed compared to the case where a multibit DAC is used from the beginning on. Furthermore, significantly worse matching can be allowed for the multibit DAC in this case. Already for relative mismatches between 0.5 % and 0.1 %, the performance is very close to the ideal performance in our case. This means that no calibration techniques are needed. This proves another superior implementation possibility for the proposed technique of dynamic increase of non-idealities in I-$\Delta\Sigma$.

IV. Implementation Example

In this section, a prototype implementation in a 180 nm CMOS process is presented using the dynamic increase of non-idealities and thus the decrease of power. The prototype increases the input-referred noise during every single Nyquist-rate conversion. This has been chosen as the reduction of GBW and SR in the SC I-$\Delta\Sigma$ modulator has a strong impact on the performance, even when the non-ideality is increased late in the conversion cycle as was seen in Fig. 7. A pure single-bit implementation was chosen for rapid prototyping of the design even though a future implementation will surely use the presented approach in Section III-C.

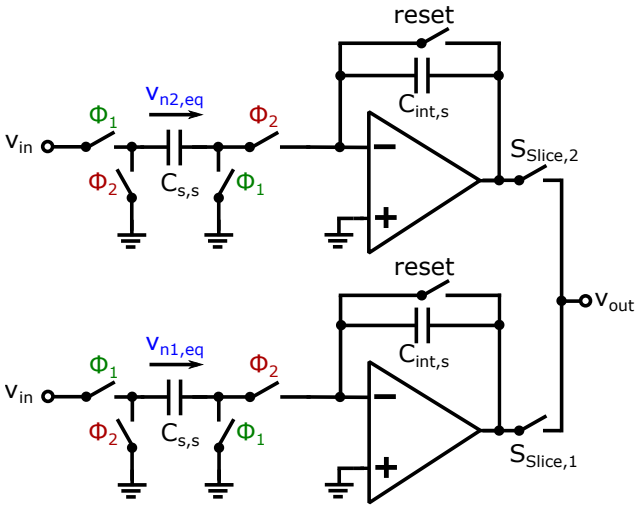


Fig. 9. Slicing technique using two SC integrators.

Looking into (9), this could be achieved by dynamically reducing the tail-current of an OTA in order to reduce its g_m. The drawback of this solution is that also bias points of transistors within the OTA are affected. This sets bounds to the range in which the current can be varied. It would also have a significant impact on SR and GBW, which - according to Section III-B - should be kept rather constantly high. Another way of increasing the noise contribution of an OTA, and thereby saving power, is the so called slicing method as presented in [5]. This technique yields advantages over the switched-biasing technique and is analyzed in the next section.

A. The Integrator Slicing Technique

A schematic illustration of the slicing technique is shown in Fig. 9. Here, the outputs of two SC integrators can be connected by two switches that can be enabled/disabled by the control signal $S_{Slice,1}$ and $S_{Slice,2}$. For now it is assumed that both integrator paths are perfectly matching. During the sampling phase Φ_1, the input voltage v_{in} is sampled to the sliced sampling capacitors denoted by $C_{s,s}$. As already derived in Section II, noise originating from the on-resistance of the switches is sampled to the capacitor $C_{s,s}$. In the integration phase Φ_2, again noise contributed by the switches and the OTA can be modeled as a voltage across the capacitor. Therefore, the rms-noise voltage stored on each capacitor can be calculated from (10). Reviewing this equation, it becomes clear that slicing the integrator into two slices yields an increased noise power of a factor of two for each slice as the sampling capacitor and the widths of all transistors within the amplifier are divided by two, which in turn doubles the effective thermal noise and 1/f noise. It should be noted at this point that all

small-signal properties of the sliced integrator like SR, GBW, and DC-gain are the same as for the original integrator. This is valid, if the assumption that the load of the OTAs are sliced in the same way or that the non-sliced load is negligible holds true. The noise voltage as well as the signal voltage can also be represented by charge stored on the sliced sampling capacitor $\mathrm{C_{s,s}}$. During the integration phase, this charge is transferred to the sliced integration capacitor $\mathrm{C_{int,s}}$. For the following calculation it can be assumed that the negative terminals of both OTAs are shorted. Ideally, there will be no current flowing across this connection as both OTAs provide virtual ground. As the signal charge stored on both capacitors $C_{s,s}$ is strongly correlated, this charge adds up: $\mathrm{Q_{Cs,vin}} = 2 \cdot \mathrm{Q_{vin}}$. Whereas noise charges are strongly uncorrelated as the noise originates from different parts of the circuits and therefore only add up in an rms-sense: $\overline{\mathrm{Q_{Cs,n}}} = \sqrt{2} \cdot \overline{\mathrm{Q_{vcs}}}$. The net charges to be transferred can now be calculated as:

$$\mathrm{Q_{Cs,signal}} = 2 \cdot C_{s,s} \cdot \mathrm{v_{in}} \tag{12}$$

and

$$\mathrm{Q_{Cs,noise}} = C_{s,s} \cdot \sqrt{v_{n1,eq}^2 + \mathrm{v_{n2,eq}^2}} = \sqrt{2} \cdot C_{s,s} \cdot \mathrm{v_{n,eq}} \tag{13}$$

under the assumption that $v_{n1,eq}^2$ = $v_{n2,eq}^2$= $v_{n,eq}^2$. This means, by taking two integrators in parallel instead of one, the overall SNR is increased by a factor of two. This could be extended to an arbitrary number of slices. Every doubling of the number of stages yields 3 dB improvement in SNR. This technique can then be used to dynamically increase the noise power over time. This is achieved by choosing the number of slices such that the normal noise requirements are fulfilled as long as all slices are active, consequently e.g. the summed sampling capacitors $\mathrm{S \cdot C_{s,s}}$ is chosen such that the noise requirements of the overall I-$\Delta\Sigma$ ADC are met with respect to (11) without any dynamic modification. Now the noise power can be increased during run-time by deactivating slices as illustrated in Section IV. Thereby, the OTAs in the deactivated slices are turned off and consequently save power.

While implementing the slicing technique, mismatch between the individual integrator paths needs to be taken into account as cross currents between slices are caused by different voltages at their outputs. A mismatch between capacitors that set the scaling coefficients can be one source of a potentially problematic mismatch error. Another one is a difference in offset between OTA slices. This offset can be modeled as a voltage source at the non-inverting terminal of the OTAs. Therefore, the offset directly refers to the output of the OTAs. If there is a mismatch between the integrators, the OTAs force currents into the output of the other ones. Thus, it must be made sure, that these error sources are small enough to not noticeably affect the performance nor the power consumption.

The switches $\mathrm{S_{Slice,1}}$ and $\mathrm{S_{Slice,2}}$ from Fig. 9 have been added to prohibit any disturbance of the yet active integrators during deactivation of slices. Furthermore, the on-resistance of these switches prohibit an excessive current flow due to offset mismatches between the OTAs. It should be noted that the on-resistance of these switches must not be chosen excessively large as this negatively affects the time constant with which the sampling capacitor of the second stage can be charged. Nevertheless, the requirements on these switches are relaxed. One reason is that the switch is changing its state from on to off only once per Nyquist-rate cycle. This usually happens towards later cycles, where the weighting of the non-idealities is reduced as previously shown. Another reason is that every non-linear contribution as well as noise is suppressed by the preceding integrator.

B. Selection of Slicing Parameters

In the following it is investigated how the slicing parameters can be selected in order to achieve an improvement in the efficiency of the modulator. At this point it is worth mentioning that the benefit of the proposed technique is highly dependent on the properties of the I-$\Delta\Sigma$ modulator. Therefore, a general quantitative statement is not possible as the ADC performance is dependent on many factors like the choice of architecture, quantizer resolution, OSR, the order of the reconstruction filter, design margin as well as the number of slices, only to name a few. An optimization of the whole ADC and its respective parameters including the slicing technique is theoretically possible. However, precise knowledge of the influence of all desired parameters on the ADC performance is necessary. This requires precise modeling of the ADC down to the circuit-level. Therefore, the optimization has been restricted to the slicing instants only, whereas the ADC structure has been readily designed beforehand. Nevertheless, making use of the slicing technique will yield improvement in the modulator's efficiency. However, as the noise in such a sliced integrator can be gradually increased, the degrees of freedom are related to the number of integrator slices and the number of cycles M. If S is the number of integrator slices, the overall power consumption of the sliced integrator $\mathrm{P_{int}}$ during a single Nyquist-rate conversion cycle can be calculated as:

$$\mathrm{P_{int}} = \frac{\mathrm{P_{max}}}{\mathrm{S \cdot M}} \sum_{\mathrm{i=0}}^{\mathrm{S-1}} (\mathrm{S - i}) \cdot \mathrm{k_i}, \tag{14}$$

where P_{max} is the power consumed by the integrator when all slices are active. k_i denotes the number of cycles between two switching actions. k_0 is then the number of cycles, where no slice is deactivated, k_1 the number of cycles, where one of S slices is deactivated, and k_{S-1} is the number of cycles, where only one active slice is left over. Therefore,

$$\sum_{\mathrm{i=0}}^{\mathrm{S-1}} \mathrm{k_i} = \mathrm{M} \tag{15}$$

holds true. The total noise power at the output of the reconstruction filter according to (1) and (2) can be calculated as

$$\mathrm{P_{noise}} = \overline{\mathrm{D_{noise}^2}} \cdot \sum_{\mathrm{i=1}}^{\mathrm{M}} \mathrm{p[i]} \cdot \mathrm{w^*[i]^2} \tag{16}$$

where $\overline{\mathrm{D}^2_{\mathrm{noise}}}$ is the noise power without slicing derived in (11) and

$$p[i] = \left\{ \underbrace{\frac{S}{S}, ..., \frac{S}{S}}_{k_0}, \underbrace{\frac{S}{S-1}, ..., \frac{S}{S-1}}_{k_1}, ..., \underbrace{\frac{S}{1}, ..., \frac{S}{1}}_{k_{S-1}} \right\}, i = 1...M \tag{17}$$

Thus, k_0 cycles long, the noise is as designed, k_1 cycles long, it is dominated by $S-1$ slices, and finally k_{S-1} cycles long the noise originates from only one slice. Note that in (14) and (16) not all slices are necessarily switched off at the same time instant. In contrast to the simplified simulation in Fig. 6, where the noise was being increased in one shot. The time instants for disabling the individual slices can obviously be chosen independently.

In the presented I-$\Delta\Sigma$ ADC prototype, the number of slices has been set to four. This is a compromise of slicing flexibility and thus potential power savings on the one hand and sizing of transistors and switching overhead on the other hand. For instance, the switches used in the input sampling network are implemented as bootstrapped switches as presented in [13]. Already for small sizes of the pass transistor, the circuit overhead is large as the transistors in combination with the capacitor are an area penalty and the size of the additional components is, to a first order, independent of the size of the passing device. This means that slicing the integrator does not keep the same area but will always require more area. Also, every individual slice needs its own control signals which complicates the layout.

Having chosen the number of slices, the number of possible deactivation cycles is still huge. The curve in Fig. 10a shows the expected power savings according to (14). Fig. 10b shows the expected drop in SNR for the same configuration as in Fig. 10a calculated with (16). The crosses in both figures mark measured results for the respective configuration as performed with the protoype that is described lateron. It can be seen that theory matches very closely to the measurement. As the targets like small SNDR penalty and large power savings contradict each other, an optimization criterion has to be found. In this design, the Schreier FoM has been chosen as optimization criterion as it includes both properties:

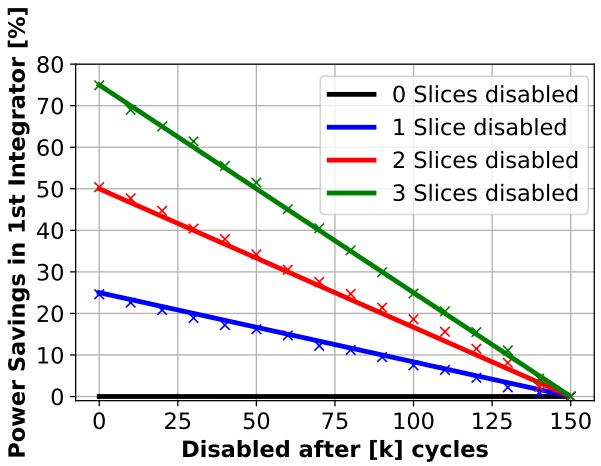
$$\mathrm{FoM_S} = (\mathrm{SN})\mathrm{DR} + 10 \cdot \log_{10}(\frac{\mathrm{BW}}{\mathrm{Power}}). \tag{18}$$

Modifying (18) with the help of (14) and (16), yields an expression for the change in the FoM as a function of the slicing instants:

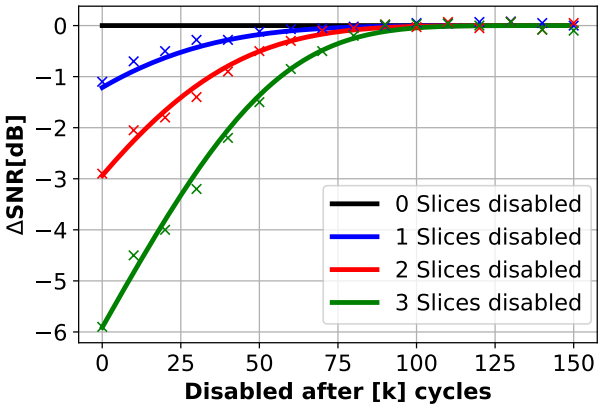
$$\begin{aligned} \Delta FoM = & -10 \cdot log_{10}(\frac{\sum_{i=1}^{M} p[i] \cdot w^*[i]^2}{\sum_{i=1}^{M} w^*[i]^2}) \\ & + 10 \cdot log_{10}(\frac{S \cdot M}{\sum_{j=0}^{S-1}(S-j) \cdot k_j}). \end{aligned} \tag{19}$$

Omitting the constant terms in (19), the following is obtained:

$$\Delta FoM^* = -10 \cdot log_{10}(\sum_{i=1}^{M} p[i] \cdot w^*[i]^2 \cdot \sum_{j=0}^{S-1}(S-j) \cdot k_j) \tag{20}$$



(a) Calculated (solid) and measured (crossed) power savings by disabling 0 to 3 slices during operation according to (14).



(b) Calculated (solid) and measured (crossed) SNR drop by disabling 0...3 slices during operation according to (16).

Fig. 10. Power savings and SNR drop due to the proposed slicing method.

From (20) it can be seen that the maximum improvement of the FoM can be achieved by minimizing the following function:

$$f(M, S, k_{0...S-1}) = \sum_{i=1}^{M} p[i] \cdot w^*[i]^2 \cdot \sum_{j=0}^{S-1}(S-j) \cdot k_j. \tag{21}$$

This can either be achieved by sweeping across all possible switching combinations of k_0 to k_{S-1} and select the set of parameters that minimizes (21) or one can solve this optimization problem analytically by means of the method of Lagrange multipliers [14], for example. This will be explained in the following.

The goal is to minimize $f(M, S, k_{0...S-1})$ under the condition that

$$g(M, k_{0...S-1}) = k_0 + ... + k_{S-1} - M = 0. \tag{22}$$

Using (21) and (22), the Lagrange-function:

$$\mathcal{L}(k_{0...S-1}, \lambda_1) = f(M, S, k_{0...S-1}) + \lambda_1 \cdot g(M, k_{0...S-1}) \tag{23}$$

can be constructed. In the following M and S are assumed to be fixed. Now the partial derivatives of (23) have to be calculated and equated to zero:

$$\nabla_{k_{0\ldots S-1},\lambda_1}\mathcal{L}(k_{0\ldots S-1},\lambda_1) \stackrel{!}{=} 0. \tag{24}$$

The equation system resulting from the operation performed in (24) must be solved to obtain the optimal switching instants. This can be done numerically. In case of multiple solutions to the equation system, the different solutions have to be plugged into (21) and the set of switching instants yielding the minimum has to be chosen. An optimal sequence that maximizes the Schreier FoM for S = 4, L = 3, M = 150 yields an improvement of about 2 dB while the SNR drops by nearly 0.9 dB. It should be noted that distortion remains unaffected by the slicing technique, since GBW, SR and DC gain of the OTA as well as the time-constant of the SC sampling circuit remain unaffected under ideal conditions. For the example design, the following slicing parameters: $k_{0,1,2,3} = 40, 30, 10, 70$ have been chosen.

C. Architectural Decisions

The presented prototype I-$\Delta\Sigma$ ADC is developed for an already existing neural interface [1]. The targeted conversion rate is 200 kS/s to be able to multiplex between multiple electrodes. The conversion speed makes it possible to convert the analog voltage of ten electrodes with a single ADC. As the neural signals are known to have a wide dynamic range, the ADC should accommodate this range. Therefore, the design specifications target a dynamic range of 90 dB. The chosen modulator architecture is depicted in Fig. 4. A simple feed-forward architecture, as in Fig. 4, has been chosen since this reduces the swing of the integrators, thereby increasing linearity. Furthermore, a third order modulator has been selected as it offers a very good tradeoff between maximum stable amplitude (MSA) and achievable SQNR for a given OSR. A discrete-time implementation is used, as the already existing neural recorder is realized in SC technique. The coefficients have been chosen by means of a genetic algorithm as used for www.sigma-delta.de [15]. For a dynamic range of 90 dB an SQNR of at least 100 dB is targeted. This results in a required oversampling ratio of M = 150. Therefore, the internal sampling rate is set to be 30 MHz. A single bit quantizer has been selected due to its inherent linearity. Reconfiguration into a multibit converter as outlined in Section III-C was not implemented to achieve a rapid prototyping. For the sake of simplicity, the reconstruction filter is a 3rd order CoI (CoI^3) filter.

A simplified circuit-level diagram of the implemented modulator is depicted in Fig. 11. As the SC sampling network is located at the input of the modulator, all errors directly affect the performance of the overall system. This means there are tight constraints in terms of noise and linearity on this network. Therefore, bottom-plate sampling has been employed as shown in Fig. 11 to mitigate the influence of signal-dependent charge injection that can cause harmonic distortion as well as an increased noise floor. As for all recent publications on low-to-medium speed, high-resolution $\Delta\Sigma$ ADCs, the most dominant power consumer is the first integrator stage. This is because constraints like linearity and noise performance are tightest there. Thus, it is expected that approximately 80% of the overall power are consumed in this stage. Later stages benefit from the noise-shaping property of the previous stages and thus are relaxed in terms of power consumption.

Therefore, the slicing technique has only been applied to the first integrator as depicted in Fig. 11. The loading due to the second integrator and the SC adder is negligible even for the case of a single slice being active. A number of four slices has been selected as a compromise between area efficiency and power savings. On the bottom of Fig. 11 the non-overlapping clock phases as well as the control signals for enabling/disabling the individual integrator slices 1a-d are shown. It should be noted that the original non-sliced integrator has been designed for the overall noise requirements and has only then been sliced into four integrators with quartered component sizes. Also the size of the input sampling capacitors $\mathrm{C_{s,s}}$ per slice has been reduced by a factor of four as compared to the original integrator. To not alter the integrator scaling coefficients, also the feedback capacitors $\mathrm{C_{int,s}}$ have been sliced by four. The OTA has been split as well. To achieve this, the width of every single transistor has been reduced to a quarter of the previous size.

D. Circuit Design

A dominant source of harmonic distortion is the signal-dependent variation of on-resistance of the sampling switches. To linearize the switches, the gate-source voltage of the switches is made independent of the input signal by bootstrapping. The implementation used for the bootstrapped switches is the one presented in [13]. As the second and third stages are relaxed in terms of linearity due to the shaping of the first stage, simple transmission gates are used here. Furthermore, bottom-plate sampling is used in all integrator stages to reduce sensitivity towards parasitic capacities and to further mitigate signal-dependent charge injection. Unfortunately, many transistors are already minimum size after optimization of the original bootstrapped switch. Therefore, it has not been possible to split every single component of the switches, leading to an overhead in chip area.

A folded-cascode with SR enhancement has been chosen for the first OTA. A simplified schematic of a single amplifier slice is depicted in Fig. 12. The continuous-time common-mode feedback circuit is not shown for the sake of simplicity. Additionally, the control signals a and $\overline{a}$, as shown in Fig. 11, for disabling the sliced amplifier are denoted. For accurate settling, the required GBW as well as the SR of the OTA must be chosen carefully. The modeling as well as effects on the performance are described in [9]. Extensive simulations have shown that a large SR is beneficial for improved settling and thereby reduces harmonic distortion. Furthermore, a high SR can even be traded in for GBW. A folded-cascode which is similar to the one presented in [16] has been selected due to the high SR as well as for its simplistic structure that leads to a very efficient performance. However, to additionally boost the SR, a modification on the original structure has been carried

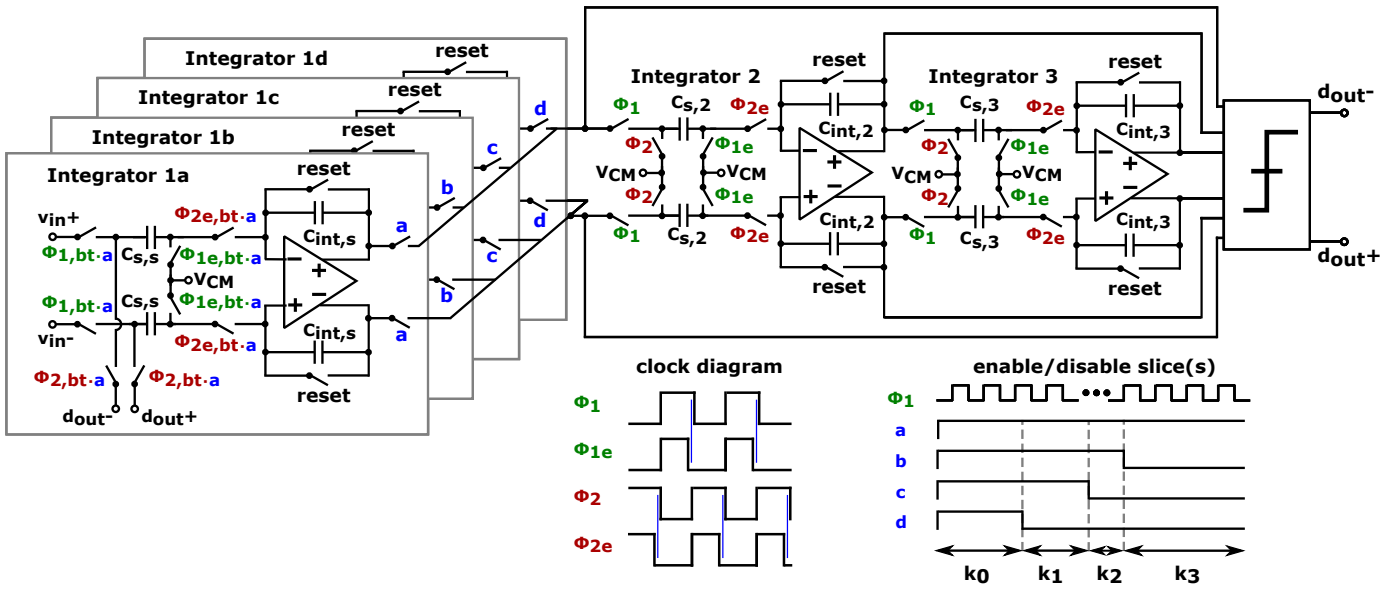


Fig. 11. Overview over the implemented modulator including integrator slicing.

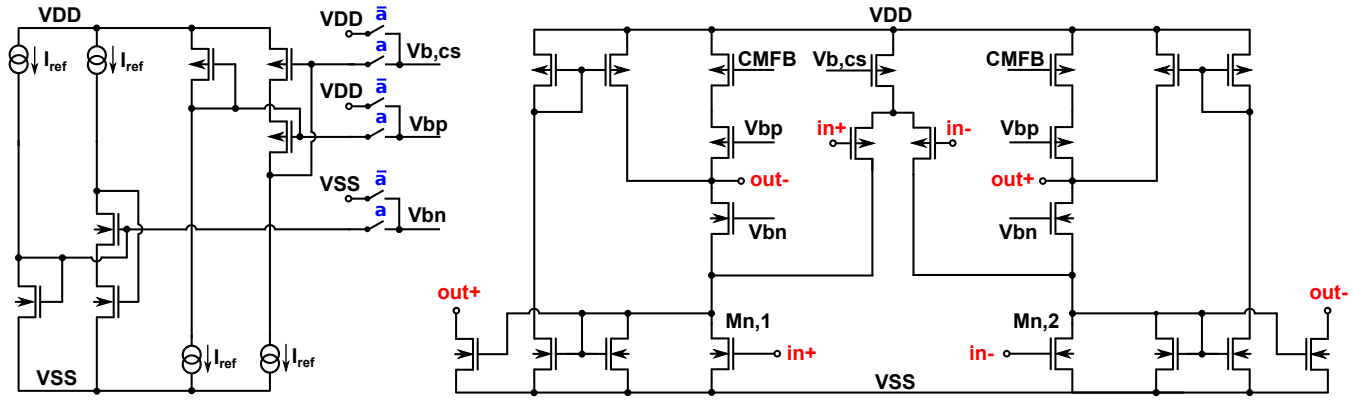


Fig. 12. Implemented folded-cascode amplifier with SR enhancement. The switchable biasing is shown for slice 1a (cf. Fig. 11). The continuous-time common-mode feedback is not shown for the sake of simplicity.

out as can be seen in Fig. 12. In addition to the original structure the tail current sources have been replaced by $M_{n,1}$ and $M_{n,2}$. The gates of these transistors are now driven with the input signal. Though, it must be made sure in the design that these devices are chosen small enough to achieve a small quiescent current in the settling point. The achieved DC gain of the folded-cascode is 70 dB. The GBW at an effective load of 400 fF during integration phase is 210 MHz while maintaining a phase margin of 70°, respectively. The maximum achievable SR for a full-scale input is up to 2700 V/μs, respectively. The second and third integrators are realized as telescopic amplifiers. The requirements in terms of load, swing, GBW, SR and noise performance are relaxed thanks to the noise-shaping property of the previous stages. The second OTA yields a DC gain of 70 dB with a GBW of 150 MHz with an an effective load of 30 fF. The OTA of the last integrator achieves the same DC gain with a GBW of 100 MHz and an effective load of 38 fF. The summer stage is realized by a passive SC adder network. The capacitors are chosen close to minimum

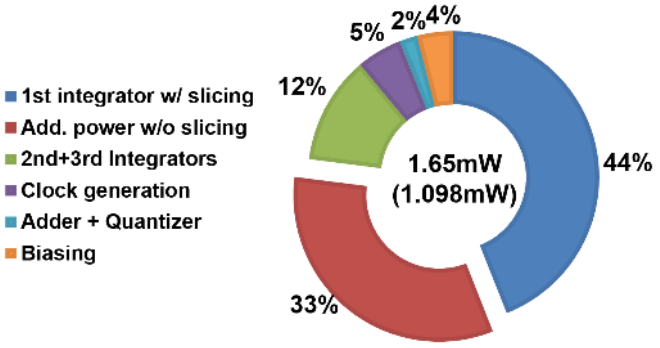


Fig. 13. Power distribution of the individual components of the modulator.

size in order to form a small load for the OTAs. The single-bit decision is performed by means of a strong-arm latch. The power distribution of the overall system is depicted in Fig. 13. The overall power consumption of the system without slicing is 1.65 mW. The power consumption of the 2nd and 3rd inte-

grator including sampling networks as well as the OTAs sums up to approximately 200 μW. The clocking network including the generation of the non-overlapping clocks consumes 5% of the overall power, meaning 82.5 μW. Quantizer, adder and reference generation for the first integrator contribute another 100 μW. This leaves 1.27 mW of power consumption for the first integrator. Employing the slicing technique using the set of parameters $k_{0,1,2,3}$ = 40, 30, 10, 70 the power consumed in the first integrator can be cut down by 43% which is equivalent to a power saving in the entire modulator of 33% as shown in red. The expected SNR and SNDR from simulation without making use of the slicing technique are 89.2 dB and 89 dB, respectively. The simulated SFDR is dominated by the third harmonic and equals 105.2 dB.

V. Measurement Results

The presented design was fabricated in a 180 nm CMOS technology. A photograph of the chip can be seen in Fig. 14. Without making use of the slicing technique, the modulator consumes 1.65mW from a 3V supply. The CoI^3 filter is implemented on an FPGA that has been used to control the slices, the reset as well as to perform the readout. Choosing the slicing parameters ($k_{0,1,2,3}$ = 40, 30, 10, 70), the power consumption can be reduced to 1.098 mW, while only 0.7 dB and 0.8 dB loss in SNR and SNDR (respectively) are measured. The measured spectra with and without slicing are shown in Fig. 15a and 15b, respectively. Though, it has previously been stated that no changes in the spectrum except for the noise floor are expected by making use of the slicing technique, a change in the harmonics can be observed on (absolutely) low level. It could not be clarified what the origin of this change is. However, the drop in SNR is in perfect agreement with the theoretical expectation whereas the superior linearity is barely affected. Furthermore, it can be seen that the noise floor is dominated by the 1/f noise of the modulator. Techniques like CDS or chopping were not implemented in this proof-of-concept IC. The MSA, measured for a 13 kHz sinusoid, is shown in Fig. 16 with the same slicing configuration. The achieved SNR/SNDR/DR are 88.2/86.6/91.5 dB. The measured SFDR exceeds 97 dB over the complete inband. At frequencies close to the Nyquist-frequency, the SFDR is assumed to be limited by the used signal source [5], by comparing it to reference measurements of a commercial 24-bit ADC. Though, the modulator is intended to be used for multiplexed input signals, which furthermore reduces the maximum allowable input frequency per channel, consequently improving the SFDR to almost 105 dB at low frequencies. The presented IC achieves a Schreier FOM of 171.1 dB. Table III summarizes this work and gives a comparison to state-of-the-art designs. Considering efficiency, Nyquist-rate capability, measured performance at Nyquist-frequency as well as area consumption, the presented design competes well with the state of the art.

VI. Conclusion

This paper describes an I-$\Delta\Sigma$ ADC, which makes use of a dynamic power saving scheme, the so-called "slicing technique", which provides a superior performance in terms

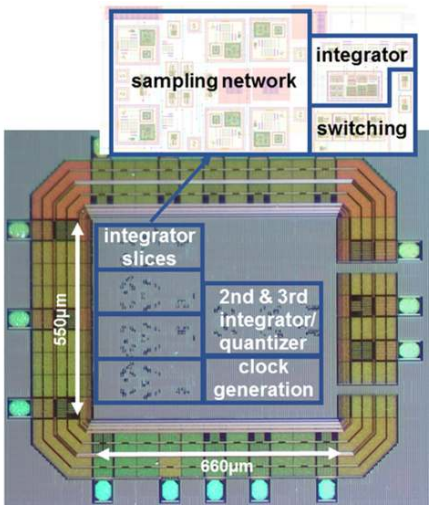
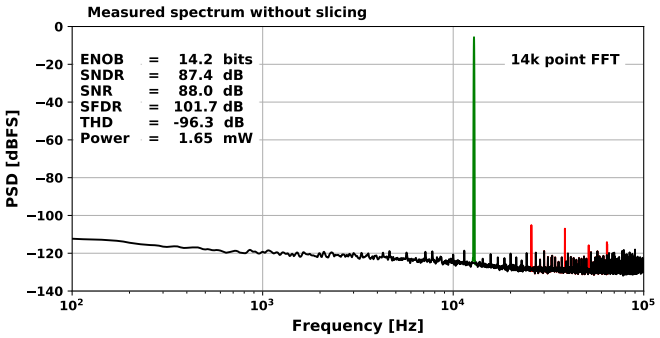
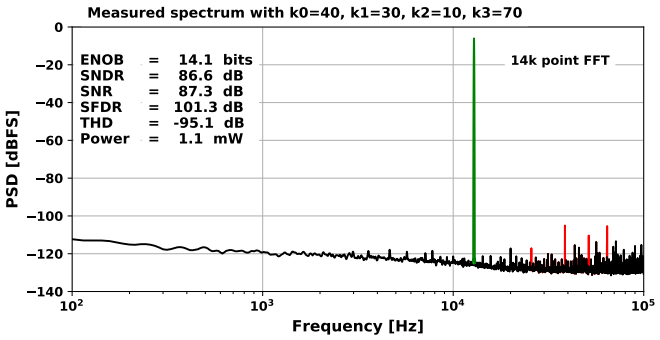


Fig. 14. Chip photograph of the prototype IC [5].



(a) Measured spectrum **without** the use of the slicing technique.



(b) Measured spectrum **with** the use of the slicing technique.

Fig. 15. Measured spectra with and without the use of the slicing technique using 14 k samples averaged across 50 measurements with an input signal of -4 dBFS at 13 kHz [5].

of the Schreier FoM. This technique can be applied to any state-of-the-art I-$\Delta\Sigma$ modulator. This technique is especially suitable for discrete-time modulators. A test chip implemented in a 180 nm CMOS technology node achieves a DR of 91.5 dB and an SNDR of 86.6 dB while making use of the slicing technique, thereby consuming 1.1 mW leading to a state-of-the-art Schreier FoM of 171.1/166.2 dB, respectively.

Acknowledgment

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TABLE III
COMPARISON TO THE STATE OF THE ART

	[17]	[18]	[19]	[20]	[21]	[22]	[23]	This work
Architecture	SAR	SAR	CT $\Delta\Sigma$	Zoom	Zoom	I-$\Delta\Sigma$	I-$\Delta\Sigma$	I-$\Delta\Sigma$
Nyquist-rate capability	√	√	X	√	X	√	√	√
Technology[nm]	40	180	40	160	160	160	180	180
Resolution[bits]	16	18	16	20	20	14	16	15
Total sampling capacitance[pF]	2x16	-	-	2x10.2	2x13.5	1x0.5	2x3.2	2x0.35
Area[mm^2]	0.074	3.87	0.053	0.375	0.25	0.45	0.5	0.363
Power Supply[V]	2.5/1.1	5/1.8	1.2	1.8	1.8	1	1.5	3
Power [μW]	101	30520	4.5	6.3	280	20	34.6	1098
$f_{s,nyq}$ [kS/s]	80	5000	10	0.025	2	1.334	2	200
SNDR [dB]	84.8	100	93.5	119.8	118.1	81.9	96.8	86.6
SFDR [dB]	107	-	102.5	-	120.3	-	-	101.3
FOM_s [dB]	170.8	179.9	184/187	182.7	185.8	157.1	174.6	171.1

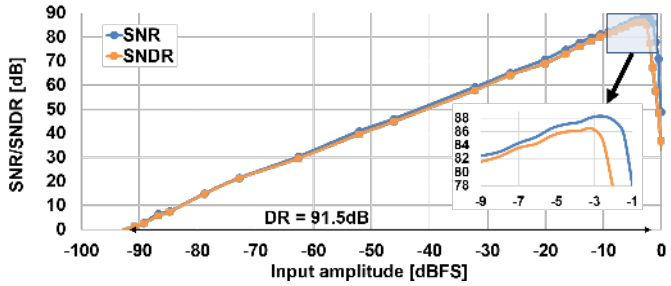

Fig. 16. Measured SNR/SNDR of the I-$\Delta\Sigma$ as a function of the input amplitude [5].

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