A Dynamic Test Method for High-Resolution A/D Converters

T. MICHAEL SOUDERS, MEMBER, IEEE

Abstract—**A dynamic test method is described for A/D converters having up to 16 bits of resolution. The technique exercises the test converter with stepped input changes, simulating the output of an S/H amplifier. Dynamic errors as low as 4 ppm can be measured within 4 μs following a step change as large as 20 V.**

DYNAMIC analog-to-digital (A/D) converter errors can be defined as any deviations from the static transfer characteristic resulting from prior exercise, i.e., previous change of input. Since high-speed converters are typically preceded by a sample/hold (S/H) amplifier in a data-acquisition system, it is most appropriate to characterize the response of A/D converters to stepped input changes, such as are normally presented from an S/H amplifier output. Among the potential sources of response error are input buffer settling limitations, the response time of the internal analog comparator, and errors related to thermal disequilibrium caused by changes in input amplitude, conversion rate, etc. To satisfactorily simulate the dynamic output of an ideal S/H amplifier and measure the resultant dynamic converter errors, four conditions must be met:

1) A signal must be generated which is capable of rapidly stepping in either direction between any pair of levels in the defined range of the converter under test.

2) The transitions must settle within an acceptably small error band of the new level in a time consistent with the performance (determined primarily by the acquisition time) of the equivalent S/H amplifier. An error band of $\frac{1}{4}$ least significant bit (LSB) has been selected for this work.

3) The signal generator must be capable of driving the input impedances of unbuffered converters which range as low as 2 kΩ.

4) To achieve resolution of better than 1 LSB and conform to the stated definition of dynamic errors, the response measurements must be made with respect to well-defined reference points for which the static transfer errors are established. Code transition levels are the most commonly used reference points for static characterization.

Condition 1) could be achieved in a number of ways. As illustrated in Fig. 1(a)-(c), these include using (a) a D/A converter, or (b) an analog multiplexer, or (c) summing a static level with a rectangular pulse using a summing amplifier.

Manuscript received September 24, 1981; revised October 30, 1981.
The author is with the Electrosystems Division, National Bureau of Standards, Washington, DC 20234.

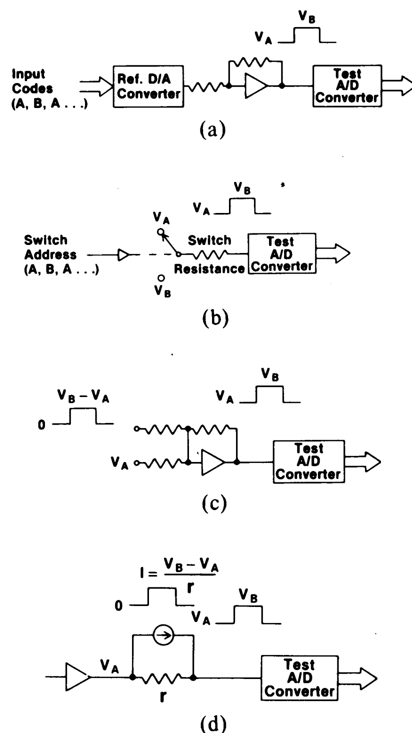

Fig. 1. Techniques for generating voltage steps required in dynamic A/D converter testing. (a)-(c) Alternative techniques. (d) Preferred technique.

Conditions 2)-4), however, place restrictions on these methods. Amplifiers, used either as the output stage of a D/A converter (a) or as a summing amplifier (c), suffer from settling time limitations for high resolution, and multiplexers (b) are limited by their ON resistance and settling time, particularly when driving significant loads.

In the approach described here and illustrated in Fig. 1(d), conditions 1)-3) are satisfied by superimposing a voltage pulse on a quasi-static level maintained at the output of an operational amplifier. The voltage pulse is created by switching on a programmable current through a relatively low-value (200-Ω) resistor in series with the amplifier's output to produce the voltage step, and switching the current off to return to the original voltage. To illustrate the concept, the step generator is shown as a simple combination of a current source and a resistor; the actual circuit is discussed later. Note that for the second transition in which the voltage returns to its original level, the settling time is largely determined by the speed with which the current can be switched off. Furthermore, after the

U.S. Government work not protected by U.S. copyright

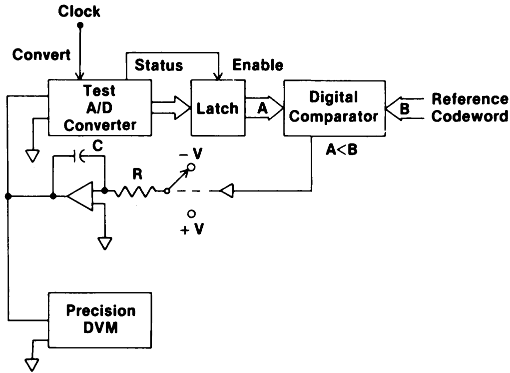

Fig. 2. Transition-locking feedback loop employed in static A/D converter testing.

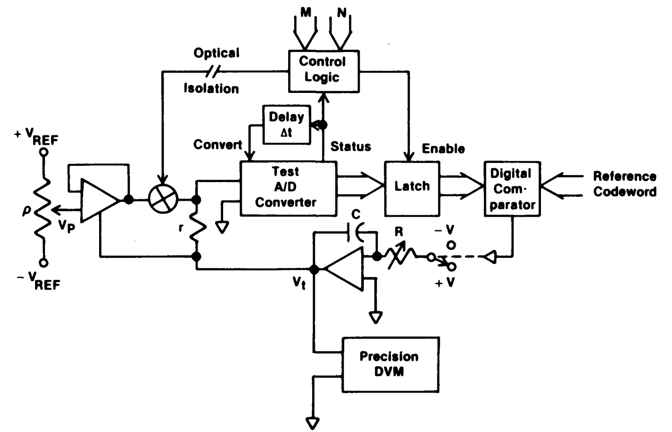

Fig. 3. Circuit for dynamic A/D converter testing: transition-locking feedback loop in conjunction with dynamic step generator (at left).

current is switched off, the ON impedance of the current switch is no longer included in the input circuit, so that the second transition is immune to the ON resistance instability limitations inherent in example of Fig. 1(b). Fortunately, no voltage change is required of the amplifier during either transition but only the ability to quickly supply current to the resulting dynamic load. Thus the amplifier's settling time requirements are relaxed. This is easily verfied by monitoring the amplifier's output voltage during current switching. While the current pulse through the resistor is as large as 100 mA for a 20-V step, the amplifier must only supply a current change of 10 mA maximum, or V_p/R_{in}, where V_p is the pulse voltage equivalent to $V_B - V_A$ in the figure, and R_{in} is the input resistance of the test converter (generally ≥ 2 kΩ).

To measure the dynamic response of a converter to these steps and thereby satisfy condition 4), the resulting step generator is applied in a manner suggested by the transition-locking feedback loop employed in an NBS static test set for A/D converters [1]. This circuit, shown in Fig. 2, uses discrete time (versus continuous) feedback to precisely locate and measure the static code transition levels. These are the input levels at which the digital output transitions between adjacent codes occur. Each transition is defined by the reference codeword applied to the digital comparator. In operation, the input voltage to the test converter oscillates with a triangular waveform about the transition level. The dither amplitude ΔV can be set arbitrarily low, e.g., a small fraction of a least significant bit, by appropriate choice of integrator time constant, conversion rate, and integrator input voltage. Once locking has occurred, this transition voltage is easily measured using, for example, a high-resolution digital voltmeter, as shown.

The time intervals between data samples latched from the test converter represent periods of open-loop operation, and thus afford the opportunity of rapidly stepping the input voltage to different levels and back without disturbing the normal transition-locking feedback cycle. This dynamic exercise is accomplished by superimposing a voltage step on the integrator's output as described above and illustrated in Fig. 3. The step changes are made in between conversions with time allowed for settling. While the unit under test converts when the input is both at the pulse level as well as at the transition level, the feedback samples are latched only following conversions made at the transition level. If the superimposed voltage is switched off prior to the next feedback sample, locking at the reference level can be maintained. Referring to the timing diagram of Fig. 4, note that the feedback voltage represented by dashed lines changes only slowly during open-loop periods due to the long integration time constant. This change is given by

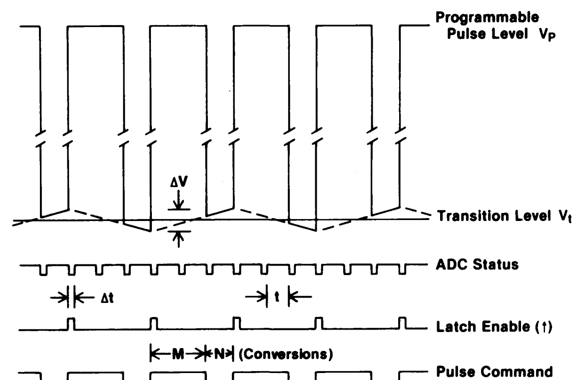

Fig. 4. Timing diagrams showing timing relationships between test set control signals and input voltage to test converter. *Notes:* 1) A low level for ADC status output indicates conversion is complete and data are valid. The falling edge of this signal initiates the next conversion following delay Δt. 2) A high level pulse command turns pulse current switch ON.

$$\Delta V = (V/RC)(M + N)(t + \Delta t)$$

where

- V input voltage to integrator
- M number of conversions made with input at pulse level
- N number of conversions made with input at transition level
- t conversion duration of test unit
- Δt time delay to allow for pulse to return to zero
- RC time constant of integrator.

Any dynamic response error due to this superimposed step change will be manifested as a change in the code transition level maintained by the feedback loop. For example, the static level of the major transition (from binary code 01111... to 100000...) may shift as a result of thermal changes arising when the input is stepped periodically to full scale and back.

Fortunately, thermal changes in the integrator have no effect on the level maintained by the feedback loop, since this level is controlled entirely by the test converter. If the feedback and step voltages are summed with negligible interaction, then the transition voltage can be measured and its changes monitored quite simply at the integrator's output with the DVM. The dynamic measurement can, in other words, be transformed to a static one.

A manually operated test set has been built following these design principles. A 16-bit reference codeword is entered via a toggle register, and pulse voltage V_p is set via potentiometer ρ. The ON and OFF durations of the pulse are entered from *BCD* switches whose settings M and N control the number of conversions made, respectively, at the pulse level and at the transition level determined by the reference codeword. For $N > 1$, the converter is permitted two or more conversions to reach the final decision which controls the feedback loop. Alternatively, delay Δt can be changed in smaller increments to determine an optimum recovery time.

The pulse current is driven from a follower amplifier having high-output drive capability, and is switched ON and OFF through resistor r via a junction FET having very low ($\leq$2-Ω) ON resistance and >30-V breakdown voltage. Since this ON resistance is in series with resistor r when the switch is on, it causes an uncertainty in the value of the pulse level given by $R_{on}/(r + R_{on}) \leq 1$ percent. The amplifier and switching transistor drive circuitry are all powered by a modular supply whose common terminal is connected to the integrator's output, and is thus held at the transition level.

The settling time of the pulse (returning to the transition level) has been measured at the test converter's input using a modification of the "viewing circuit" described by Schoenwetter in [2]. The pulse was found to return to within 4 ppm (full-scale range) of the transition level in under 4 μs following a step change of 20 V. Additional observations at the integrator's output during pulse switching revealed that the switching transients and level changes were insignificant, affecting the average value by no more than 1 ppm.

With this test set, each of the four conditions initially stated can be met. Any of the 2^n levels in the defined range of the converter under test can be selected as the reference transition level, and any other level may be independently selected as the pulse level. While the pulse levels are not known to better than 1 percent, the transition levels are precisely defined, and any step can be accurately generated in terms of a return from a pulse level to a transition level. Since these steps do not appreciably exercise any critical amplifiers, the settling time is kept short and the error band small. In addition, by excluding the switch resistance from the input circuit after the step is made, errors due to resistance instability in the equivalent input circuit are eliminated. Accordingly, converters having relatively low input impedances can be tested without incurring proportionately greater errors due to switch resistance changes. Finally, with this method, dynamic errors are explicitly measured in terms of resulting deviations of the reference (code-transition) levels from their static values. These characteristics make the test set suitable for measuring the dynamic performance of converters having resolution as high as 16 bits. At resolutions of greater than 12 bits, the test set can simulate an S/H amplifier having better dynamic response than any commercial products presently available. Furthermore, it seems possible that improvements in the switching circuit can lead to even shorter settling time. This, in addition to tradeoffs with accuracy, could extend the applicability to faster converters of less resolution.

REFERENCES

[1] T. M. Souders and D. R. Flach, "An automated test set for high resolution analog-to-digital and digital-to-analog converters," *IEEE Trans. Instrum. Meas.*, vol. IM-28, no. 4, pp. 239–244, Dec. 1979.

[2] H. K. Schoenwetter, "A high-speed low-noise 18-bit digital-to-analog converter," *IEEE Trans. Instrum. Meas.*, vol. IM-27, no. 4, Dec. 1978.