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A Family of Binary Memristor-Based Low-Pass Filters With Controllable Cut-Off Frequency

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ABSTRACT The nanoscale size and controllable memristance of Memristor (MR) have shown evident superiorities for structuring new integrated circuits with different functions. With regards to the reported MR based filters, their cut-off frequencies could be hardly hot-line controlled on purposes. In this paper, by using the boundary values of memristance, a method for hot-line adjusting cut-off frequencies is newly proposed by inputting a preset DC voltage together with the to-be-filtered signal, without the requirement of extra memristance write circuits, which is hence beneficial for integrated implementation. The floating MR emulator is firstly presented and the saturation operation of its memristance is interpreted. A family of MR based low-pass filters with controllable cut-off frequency are proposed by combining the connection nodes of a memristive circuit network Z with the op amp. Two circuits of the low-pass filter family are chosen for demonstration, and the cut-off frequency and passband gain are calculated. Square and sinusoidal voltage signals are used to test the performance of the proposed low-pass filter family. Both the simulation and experimental results show that the proposed filters can achieve cut-off frequency adjustment with good filtering performance.

INDEX TERMS Memristor, low-pass filter, controllable cut-off frequency, emulator.

I. INTRODUCTION

The MR was envisioned by professor L.O. Chua as a two-terminal electrical element in 1971 and physically fabricated by HP Lab in 2008 [1], [2]. Due to the unique characteristics of nanoscale size and controllable memristance, tremendous research attentions have been attracted to widen the potential applications of MRs, especially in the fields of integrated circuits with the functions of data storage, neural network computation, programmable logic, signal processing, etc. [3]–[11].

Before the physical MRs are commercially popularized, various simulation models have been established beforehand to display the dynamic characteristics of MR based circuits. Behavioral models for emulating TiO_2 MRs of HP Lab are presented in [12] and [13], and these simulation models require physical constitutive relation equations. A MR emulator by making use of a digitally controlled potentiometer and a microcontroller is proposed in [14] and programmed to mimic the characteristics of the HP memristor. Also, MR emulators implemented by the hardware circuits also are reported for experimental investigations, based on the electronic devices with controllable resistance, such as light dependent diodes and resistors [15], junction field effect transistors [16], programmable potentiometers [17], etc. These emulators show high effectiveness and have made great contributions for the beforehand investigation of MR based circuits. Note that, the memristance variation of MR is decided by the instantaneous charge or flux going through its two terminals, hence as an MR connected into the hardware circuit, the memristance will be instantaneously varied but only dependent on the inside operation states of the MR based circuit. Therefore, MR read/write circuits have to be employed for timely sampling memristance and synchronously controlling the memristance to the required target values [18], [19].

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The memristive filters have been emerging as an interesting research topic in consideration of the new characteristics brought by nanoscale MRs. By using MRs to replace the resistors in traditional filter circuits, a group of active filters are studied in [20]. The transfer function, cut-off frequency, and Bode plot are demonstrated to show the different dynamic responses of these MR based filters. In [21], an ultralow-voltage and -power DTMOS-based MR is designed by using CMOS 0.18 μm process technology, and the MR is then used to build a second order Sallen-Key band-pass filter for processing the real electroencephalogram data. The TiO_2 MR based low-pass and high-pass Sallen Key filters are discussed in [22], which presents the frequency operation criterion for preventing the output distortion caused by the memristance saturation. These research works have evidently shown the interesting particularities observed from the MR based filters. MRs are also employed to design functional circuits which can be indirectly utilized for building analog filters. In [23], a 15-tap CT finite impulse response Savitzky-Golay filter was designed by using the MR-based delay blocks for smoothening the electrocardiographic signals accompanied with the high-frequency noises. A mixed-signal implementation of complex-valued FIR filter bank using a MR-based approximate multiplier is designed in [24] for accelerating the digital signal processing. However, the cut-off frequency of these MR based filters can be hardly hot-line adjusted on purpose since the memristance variation only relies on the inside states of the filter circuits.

In order to control the cut-off frequency of MR based filters, extra writing circuits are normally adopted to timely control the memristance [25], [26]. By using the resistance switching characteristics of MR, the novel printed MR-capacitor based low pass and high pass filters for analog circuits to achieve tunable cut-off frequencies and bandwidth are proposed in [25], of which the cut-off frequencies can be controlled by switching the state of MR. In [26], a programmable MR potentiometer with simple structure and small volume is designed and utilized for structuring an active MR-filter with adjustable cut-off frequency and phase. However, although the cut-off frequency could be controlled by using the memristance writing circuits, the complexity and volume of the hardware implementation of these filters will be greatly increased, which could degrade the integrated fabrication.

In this paper, the operation principle of a floating MR emulator is introduced and then applied to the design of the low-pass filter family. By utilizing the MR with binary operation to replace one of the resistors inside a *RC* network, a family of low-pass filters with controllable cut-off frequency is newly proposed and investigated. Differently from those earlier reported MR-based filters, the cut-off frequency can be controlled between two values by only inputting a DC control voltage together with the signal to be filtered. Two filter circuits of this low-pass family are selected for comprehensive study, and both simulation and experimental results are given for validation.

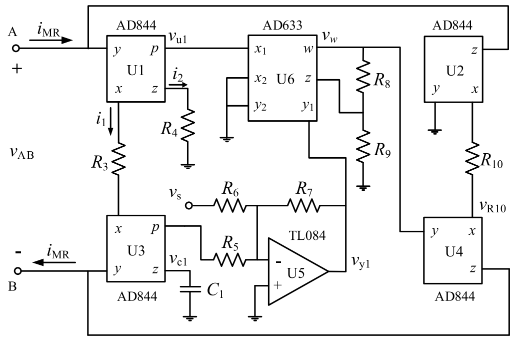

FIGURE 1. Circuit schematic of floating MR emulator.

II. REALIZATION OF BINARY MR

In order to investigate this MR based filter family, an MR emulator with floating terminals previously proposed in [27] is newly modified for mimicking the binary MR behaviors. The circuit schematic of the floating MR emulator is shown in Fig. 1, where four current conveyors AD844(U1∼U4), one op amp TL084 (U5), one multiplier AD633(U6), one capacitor C_1 and several resistors are required. The expression of the equivalent memristance can be written by

$$R_{\rm m} = \frac{1}{W(\varphi_{\rm AB})} = \frac{1}{\alpha\varphi_{\rm AB} + \beta}, \tag{1}$$

where $R_{\rm m}$ represents the memristance, W denotes the memductance, and $\varphi_{\rm AB}$ is the time integral of the terminal voltage $v_{\rm AB}$. α and β are two constants and decided by the values of normal resistors and capacitors in the emulator circuit, and we have

$$\alpha = \frac{R_4R_7(R_8+R_9)}{10R_3^2R_5C_1R_8R_9}, \quad \beta = -\frac{R_4R_7(R_8+R_9)}{10R_3R_6R_8R_{10}}.$$

The charge going through capacitor C_1 can be expressed by the voltage v_{c1} across, namely

$$q_1 = \frac{\varphi_{AB}}{R_3} = -C_1v_{c1}. \tag{2}$$

The operational amplifier U5 and the resistors R_5, R_6, and R_7 are combined together to form an inverting adder, and the output voltage of U5 is

$$v_{y1} = -(\frac{R_7}{R_5}v_{c1} + \frac{R_7}{R_6}v_s), \tag{3}$$

where $v_{\rm s}$ is the terminal voltage of the voltage source in serial connection with R_6.

By substituting (2) into (3), we can get the mathematical expression of $\varphi_{\rm AB}$, namely

$$\varphi_{\rm AB} = \frac{R_3R_5C_1}{R_7}(v_{y1} + \frac{R_7}{R_6}v_s). \tag{4}$$

According to the datasheet of the multiplier U6, its output voltage $v_{\rm w}$ can be obtained by

$$v_{\rm w} = \frac{R_4(R_8+R_9)}{10R_3R_8}v_{\rm AB}v_{y1}. \tag{5}$$

Note that the current going through the resistor R_{10} is equal to the current inputting into terminal A, hence the current of the MR can be calculated by

$$i_{\mathrm{MR}} = \frac{v_{R_{10}}}{R_{10}} = \frac{v_{\mathrm{w}}}{R_{10}}. \tag{6}$$

Therefore, the memristance can be now rewritten by

$$R_{\mathrm{m}} = \frac{V_{\mathrm{AB}}}{i_{\mathrm{MR}}} = \frac{V_{\mathrm{AB}} R_{10}}{v_{\mathrm{w}}}. \tag{7}$$

It can be observed from (1) and (4) that the memristance value can be influenced by the output voltage of operational amplifier U5. Note that, U3 is employed for integral operation to obtain the equivalent flux φ_{AB}. When input voltage across terminals A and B is periodic AC voltage without DC component, the equivalent flux φ_{AB} measured from U3 is also an AC voltage. However, when a DC voltage is inputted together with the AC signal, output voltage of U3 will be increased until reach saturation, and this saturation voltage could be delivered to adder circuit and also results in output saturation of U5. Hence, the equivalent memristance of MR shown in Fig. 1 could be maintained at its boundary value by the saturation of U5.

Generally, the output saturation voltage is decided by the power sources connected to active chips U1∼U6. Note that, values of memristance or memductance of a real MR must be greater than zero. Hence, in order to guarantee validity of the MR emulator, output voltage of U5 is supposed to be positive. To achieve this purpose, U5 is only powered by unipolar power supply with positive output voltages.

When the applied DC control voltage $v_{\mathrm{DC}} > 0$, operational amplifier U5 can be increased to the upper saturation voltage, and in this case memristance will reach its lower boundary value. By denoting $v_{y1\mathrm{H}}$ as the upper output saturation voltage of U5, based on (5) and (6), the expression of lower boundary value of the memristance R_{on} can be written by

$$R_{\mathrm{on}} = \frac{10 R_3 R_8 R_{10}}{R_4 (R_8 + R_9) v_{y_{1\mathrm{H}}}}. \tag{8a}$$

To achieve the upper saturation of U5, the output voltage of U3 v_{c1} must be negative and satisfying the following condition,

$$v_{\mathrm{c}1} \le -\frac{R_5}{R_7}\left(v_{y_{1\mathrm{H}}} + \frac{R_7}{R_6} v_s\right). \tag{8b}$$

Likewise, as the applied DC control voltage $v_{\mathrm{DC}} < 0$, the output of U5 will be decreased to the lower saturation voltage, and the memristance will be thereby forced to its upper boundary value. By denoting $v_{y1\mathrm{L}}$ as the lower output saturation voltage of U5, the expression of upper boundary value of the memristance R_{off} can be obtained by

$$R_{\mathrm{off}} = \frac{10 R_3 R_8 R_{10}}{R_4 (R_8 + R_9) v_{y_{1\mathrm{L}}}}. \tag{9a}$$

Also, to achieve the lower saturation of U5, the output voltage of U3 must be positive and satisfying the following condition,

$$v_{\mathrm{c}1} \ge -\frac{R_5}{R_7}\left(v_{y_{1\mathrm{L}}} + \frac{R_7}{R_6} v_s\right). \tag{9b}$$

It can be seen from that, by inputting proper DC control voltage, the output voltage of U3 can be altered to satisfy (8b) and (9b), and hence the equivalent upper as well as lower memristance boundaries can be reached. Therefore, the binary operation can be achieved by properly configuring the emulator circuit parameters. It is worth noting that, the output voltage of U6 must be prevented from saturation during the usage of this emulator. It can be evidently observed from (10) that, as the output voltage v_w of U6 is saturated, the current i_{MR} going through the MR emulator will be constant independently of the input voltage v_{AB}, hence in this case this emulator will be no longer performed as an MR.

III. THE PROPOSED FILTER FAMILY BASED ON MR

The general topologies of the proposed low-pass filter circuit are shown in Fig. 2(a). This topology could be clearly divided into three parts. The first part is the feedback network including two resistors R_{a} and R_{b}, as enclosed by blue dotted frame. This feedback network can be used to adjust the output gain of the filter. The second part is a network consisting of the four-terminal network Z and two resistors R_1 and R_2. There are four ports inside this network, namely ports 1, 2, 3, and 4. Port 1 is directly connected to the input terminal. The port 2 is shorted to the non-inverting input terminal, while the port 3 is connected to the output terminal of the operational amplifier via resistor R_1. The port 4 is connected to resistor R_2. The third part is the single operational amplifier. It can be deduced from Fig. 2(a) that, there are many options to design different filters by modifying the inside circuit of network Z.

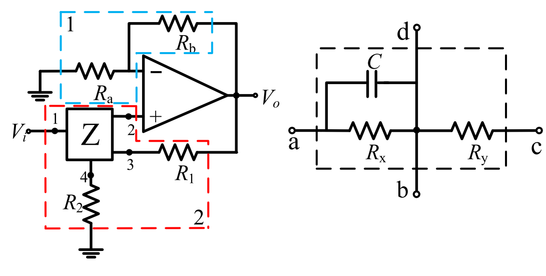

FIGURE 2. **The proposed filter family (a) Circuit of the low-pass filter; (b) Network Z.**

However, in order to simplify the theoretical calculation, only first-order RC network is taken for design the low-pass filter. As shown in Fig. 2(b), the network Z is structured only by two resistors R_{x} and R_{y}, and one capacitor C, and possess four connect nodes a, b, c, and d (b and d are shorted). Also, the filter topology can be changed by differently changing the connection combinations of the four ports and the four connection nodes of RC network Z.

For example, by connecting node a to 4, nodes b and d together to 2 and 3, node c to 1, a low-pass filter circuit

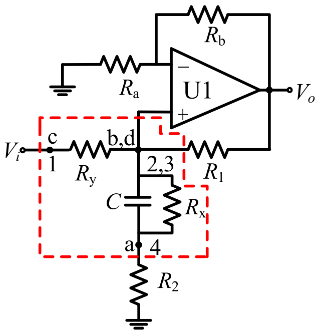

FIGURE 3. Low-pass filter by connecting node a to 4, nodes b and d together to 2 and 3, node c to 1.

can be get, as shown in Fig. 3. Note that, the low-pass filter performance is also dependent on the parameter values of the four resistors R_1, R_2, R_x and R_y. By carefully evaluating the frequency and amplitude response, 8 low-pass filters are suggested and listed in Tab. 1 by comprehensively considering the filtering performance, where "∞" and "0" represent open circuit and short circuit, respectively.

By taking the first case in Tab. 1 for demonstration, namely $R_2 = 0$, the transfer function of this filter can be obtained by

$$H = A\frac{\omega_c}{s+\omega_c}, \tag{10}$$

where ω_c is cut-off angular frequency and A is a constant, which can be expressed by

$$\omega_c = \frac{R_x+R_y}{R_xR_yC} - \frac{R_b}{R_1R_aC}, \quad A = \frac{R_1R_x(R_a+R_b)}{R_1R_a(R_x+R_y)-R_bR_xR_y}.$$

Hence, the cut-off frequency can be calculated by

$$f_c = \frac{\omega_c}{2\pi} = \frac{1}{2\pi C}\left(\frac{R_x+R_y}{R_xR_y} - \frac{R_b}{R_1R_a}\right). \tag{11}$$

The passband gain is

$$A_v = A = \frac{R_1R_x(R_a+R_b)}{R_1R_a(R_x+R_y)-R_bR_xR_y}. \tag{12}$$

It can be seen from (11) that, the cut-off frequency is in fact dependent on the values of R_x and R_y of network Z. Hence, in order to obtain the filters with controllable cut-off frequency by using the memristance variation of MR, one of the resistors inside the network Z, R_x or R_y, is replaced by a MR to rebuild the filter. Since only R_y is not allowed to be operated under open circuit or short circuit, the case of replacing R_y is chosen for study in this paper.

Likewise, by differently combining the connection nodes of the network Z together with ports 1, 2, 3, and 4, the low-pass filter circuits can be obtained, as shown in Tab. 2. Also, the resistor R_y could be replaced by MR for implementing the low-pass filter with controllable cut-off frequency. The filter circuits configured with MR as listed in Tab. 1 and Tab. 2 are together structuring a family of MR based low-pass filters.

TABLE 1. A family of mr based low-pass filters of the first case of connection combination.

Connection combinations	Configuration of the resistors			
	R_1	R_2	R_x	R_y
a↔4 b,d↔2,3 c↔1	R_1	0	R_x	$R_y \to R_M$
	R_1	0	∞	$R_y \to R_M$
	R_1	R_2	R_x	$R_y \to R_M$
	R_1	R_2	∞	$R_y \to R_M$
	∞	0	R_x	$R_y \to R_M$
	∞	0	∞	$R_y \to R_M$
	∞	R_2	R_x	$R_y \to R_M$
	∞	R_2	∞	$R_y \to R_M$

TABLE 2. A family of low-pass filters of the other three cases of connection combination.

Connect combinations	Configuration of the resistors			
	R_1	R_2	R_x	R_y
a↔3,4 b,d↔2 c↔1	0	R_2	R_x	R_y
	0	R_2	∞	R_y
	0	∞	R_x	R_y
	0	∞	∞	R_y
	R_1	∞	R_x	R_y
	R_1	∞	∞	R_y
a↔3 b,d↔2 c↔1,4	0	R_2	R_x	R_y
	0	R_2	∞	R_y
	R_1	R_2	R_x	R_y
	R_1	R_2	∞	R_y
a↔3 b,d↔2,4 c↔1	0	R_2	R_x	R_y
	0	R_2	∞	R_y
	R_1	R_2	R_x	R_y
	R_1	R_2	∞	R_y
a↔4 b,d↔2 c↔1,3	R_1	0	R_x	R_y
	R_1	0	∞	R_y

IV. CASE STUDY

In order to theoretically show the detailed characteristics of this family of MR based low-pass filters, two topologies are demonstratively selected for further studies.

A. TOPOLOGY A

By setting $R_2 = 0$ (short circuit) and replacing the resistor R_y by MR R_m, the low-pass filter with positive feedback loop named topology A in this section can be obtained, as shown in Fig. 4(a). The voltage V_C is the voltage of the non-inverting input of the op amp U1, which is also the voltage across capacitor C. In order to testing this filter, a voltage V_i of square wave with high level V_{OH} and low level V_{OL} is chosen as the input voltage to be filtered. The period of the input voltage is configured as T, and the pulse width is $t_h = t_l = T/2$. The waveforms of the input and output voltage of the filter topology A and the capacitor voltage are presented in Fig. 4(b), of which the black curve is the input voltage V_i. Note that, V_i is in fact the sum of V_{i1} and V_{p1}, where V_{i1} is the to be filtered signal with average value of zero during each period. The red curve is the voltage V_C, and the green curve is the output voltage V_o.

During the time interval of $[0, T/2]$, the capacitor C is charged by the input voltage until its terminal voltage reaches the steady state V_{OH1}. According to Kirchhoff's voltage law,

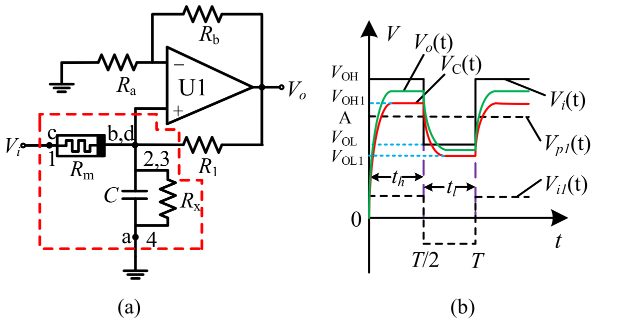

FIGURE 4. Filter with topology A (a) Circuit topology; (b) Key curves.

we have

$$\frac{V_{OH}-V_C}{R_m}=C\frac{dV_C}{dt}+\frac{V_C}{R_x}-\frac{R_b}{R_1R_a}V_C, \quad V_C(0)=0. \tag{13}$$

Thus, the voltage across the capacitor C can be resolved,

$$V_C=\frac{P}{Q}V_{OH}(1-e^{-\frac{Q}{PR_mC}t}). \tag{14}$$

During the time interval of $[T/2, T]$, the input voltage V_i is altered from the high level V_{OH} to the low level V_{OL} at the moment $T/2$. The voltage across capacitor C cannot be abruptly changed, and the capacitor C will be discharged from $T/2$ until the capacitor reaches its steady state voltage V_{OL1}. According to Kirchhoff's voltage law, the following equations hold,

$$\frac{V_{OL}-V_C}{R_m}=C\frac{dV_C}{dt}+\frac{V_C}{R_x}-\frac{R_b}{R_1R_a}V_C, V_C(\frac{T}{2})=V_{OH1}. \tag{15}$$

Thus, the voltage across the capacitor C can be obtained,

$$V_C=\frac{P}{Q}V_{OL}+(V_{OH1}-\frac{P}{Q}V_{OL})e^{-\frac{Qt}{PR_mC}}. \tag{16}$$

Then, the output voltage of topology A can be calculated by

$$V_o=(1+\frac{R_b}{R_a})V_C, \tag{17}$$

Starting from $t = T$, the voltage V_C across the capacitor will be periodically charged and discharged as the input square wave voltage exchanging between high and low levels.

The cut-off frequency of the topology A can be calculated by

$$f_c=\frac{Q}{2\pi R_mPC}. \tag{18}$$

The passband gain of the topology A can be resolved by

$$A_v=\frac{P+R_1R_xR_b}{Q}, \tag{19}$$

where P and Q are two constants and can be expressed by

$$P=R_1R_aR_x, \quad Q=R_1R_a(R_m+R_x)-R_bR_mR_x.$$

B. TOPOLOGY B

By setting $R_1 = \infty$ and $R_2 = 0$, and replacing the common resistor R_y by MR with memristance R_m, the low-pass filter without positive feedback loop can be obtained and named by topology B, as shown in Fig. 5(a). V_C is the voltage across the capacitor C and the resistor R_x, which is also the voltage of the non-inverting input terminal of the op amp U1. A square waveform is also adopted as the input voltage V_i for testing.

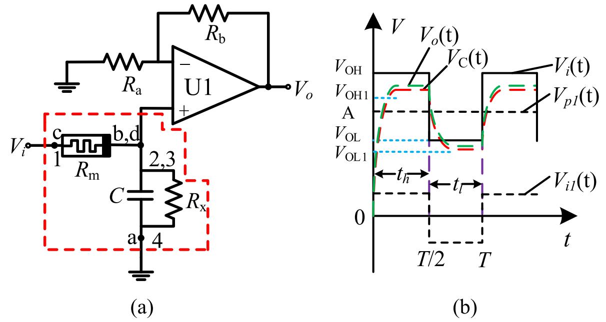

FIGURE 5. Filter with topology B (a) Circuit topology; (b) Key curves.

During the time interval $[0, T/2]$, the capacitor C is charged until the steady state voltage V_{OH1} is reached. According to Kirchhoff's voltage law, we have

$$V_C+R_m(C\frac{dV_C}{dt}+\frac{V_C}{R_x})=V_{OH}, \quad V_C(0)=0. \tag{20}$$

Thus, the voltage across the capacitor is

$$V_C=\frac{R_xV_{OH}}{R_m+R_x}(1-e^{-\frac{t(R_m+R_x)}{CR_mR_x}}). \tag{21}$$

During the interval $[T/2, T]$, the input voltage V_i is jumped from the high level V_{OH} to the low level V_{OL} at the moment $T/2$. Since the voltage across the capacitor C cannot be abruptly changed, the capacitor C will be discharged from $T/2$ until reaching the steady state V_{OL1}. According to Kirchhoff's voltage law, the following can be obtained,

$$V_C+R_m(C\frac{dV_C}{dt}+\frac{V_C}{R_x})=V_{OL}, \quad V_C(\frac{T}{2})=V_{OH1} \tag{22}$$

The voltage across the capacitor C can be got by solving (22), namely,

$$V_C=\frac{R_xV_{OL}}{R_m+R_x}+(V_{OH1}-\frac{R_xV_{OL}}{R_m+R_x})e^{-\frac{t(R_m+R_x)}{R_mR_xC}}. \tag{23}$$

The output voltage of the filter with topology B can be expressed by,

$$V_o=(1+\frac{R_b}{R_a})V_C. \tag{24}$$

The capacitor voltage V_C can be periodically charged and discharged as the input square wave voltage changed between high and low levels.

The cut-off frequency of the topology B can be calculated by

$$f_c=\frac{R_m+R_x}{2\pi R_xR_mC}. \tag{25}$$

The passband gain of the topology B can be then written by

$$A_{\mathrm{v}} = \frac{R_{\mathrm{x}}(R_{\mathrm{a}} + R_{\mathrm{b}})}{R_{\mathrm{a}}(R_{\mathrm{m}} + R_{\mathrm{x}})}. \tag{26}$$

The calculation results of (18) and (25) show that, the cut-off frequency of these two filters could be altered by the value of memristance R_{m}.

V. SIMULATION VERIFICATION

In order to confirm the validation of these low-pass filters with controllable cut-off frequency, simulations based on Pspice software are carried out in this section.

A. TOPOLOGY A

In order to achieve the binary operation of the MR emulator, the parameters in Fig. 1 are configured as $R_3 = 10\mathrm{k}\Omega$, $R_4 = 5\mathrm{k}\Omega$, $R_5 = 10\mathrm{k}\Omega$, $R_6 = 25\mathrm{k}\Omega$, $R_7 = 15\mathrm{k}\Omega$, $R_8 = 10\mathrm{k}\Omega$, $R_9 = 50\mathrm{k}\Omega$, $R_{10} = 1\mathrm{k}\Omega$, $C_1 = 150\mathrm{nF}$, and $v_s = -15\mathrm{V}$. According to the TL084 datasheet, the upper and lower output saturation voltages of U5 are 13.5V and 1.5V, respectively. According to (8) and (9), the maximal memristance value R_{off} of MR is 2.22kΩ, and the lower boundary memristance value R_{on} is 246.91 Ω. In order to verify the filtering performance of the chosen filter A, the simulation verification is performed in Pspice software and then imported into the Origin software for curve plotting, as shown in Fig. 6. The input voltage V_i is a square waveform, which has the high voltage level of $V_{\mathrm{OH}} = 1\mathrm{V}$ and the low voltage level of $V_{\mathrm{OL}} = -1\mathrm{V}$. The pulse period is $T = 0.2\mathrm{s}$, and the high level duration t_h and low level duration t_l are both equal to 0.1s. A positive DC control voltage V_{p1} with amplitude 2V is imposed together with the input signal for adjusting the cut-off frequency. The two resistors inside the feedback network 1 have the resistances $R_{\mathrm{a}} = 5\mathrm{k}\Omega$ and $R_{\mathrm{b}} = 1\mathrm{k}\Omega$. The resistor $R_1 = 1\mathrm{k}\Omega$, the filter capacitor is $C = 15\mu\mathrm{F}$ and the resister in parallel with the capacitor is $R_{\mathrm{x}} = 1\mathrm{k}\Omega$.

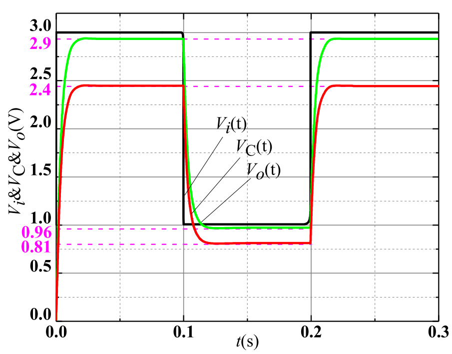

FIGURE 6. Simulation results of topology A under square waveform excitation.

As shown in Fig. 6, the black curve is the input voltage V_i, the red curve is the capacitor voltage V_{C}, and the green curve is the output voltage V_o. The input voltage levels V_{OH} and V_{OL} are both greater than 0 due to the added control voltage. The memristance of the MR can be forced to reach its lower boundary value R_{on} by this control voltage. Inside [0, 0.1]s, the input voltage is high level V_{OH}, the capacitor C is charged from $t = 0$, and the voltage V_{C} is increased from 0 to its steady state voltage of 2.4V, as shown by the red curve in Fig. 6. According to (17), the output voltage V_o is 1.2 times higher than the capacitor voltage V_{C}, as shown by the green curve.

When the memristance reaches the lower boundary value R_{on}, according to (18), the cut-off frequency of the filter A is $f_{\mathrm{c}} = 51.46\mathrm{Hz}$. Based on the Fourier transformation, the standard square wave can be decomposed by the sum of multiple sine waves. When the input voltage V_i is a standard square waveform, after the filtering operation of the low-pass filter, the input harmonics with frequency greater than the cut-off frequency can be filtered out, and hence the output voltage V_o is distorted and no longer a standard square waveform, as shown in Fig. 6. This simulation result show that the low-pass filter A designed in this paper can achieve low-pass filtering. Likewise, as the input signal is mixed with high frequency sinusoidal signal with the frequency greater than the cut-off frequency, the low pass filter will only outputs sinusoidal signal with the frequency less than the cut-off frequency. In order to verify this performance, the sinusoidal voltages $V_1 = 1\sin(20\pi t)$ and $V_2 = 1\sin(1400\pi t)$ are inputted together into the filter for testing. Also, in order to test the controllability of the filter cut-off frequency, a DC control voltage V_{p1} with the amplitude of 3V or -3V is also inputted along with the testing sinusoidal signals. The control voltage with positive value will drive the MR memristance to reach its lower boundary value, and the negative level will enforce the memristance to reach the upper boundary value. Hence, the cut-off frequency of the filter can be adjusted by the input DC control voltage V_{p1}. By changing the filter capacitance to $1\mu\mathrm{F}$ and maintaining the parameters of other components unchanged, the input and output waveforms are numerically simulated and shown in Fig. 7.

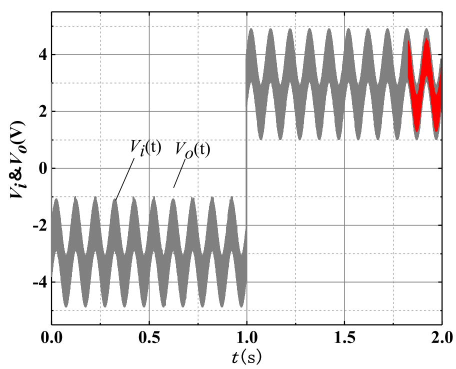

FIGURE 7. The waveforms of the input and output of the filter A under sinusoidal signal.

In Fig. 7, the grey curve is the input voltage V_i, and the red curve is the output voltage V_o. During the interval of

[0, 1]s, V_{p1} is negative and the memristance of the MR reaches the upper value R_{off}. According to (18), the cut-off frequency is now 198.94Hz, and the frequency of signal V_1 is lower than this cut-off frequency. Therefore, the signal V_1 inside the input signal can be transferred through the filter without attenuation, while the signal V_2 with frequency higher than 198.94Hz is filtered out. During the time interval [1, 2]s, the value of V_{p1} is positive, the memristance of the MR is changed to lower boundary value. The cut-off frequency of the low pass filter A is then switched from 198.94 Hz to 771.90Hz, and hence the input signals V_1 and V_2 can together pass through the filter, as shown in Fig. 7. These results confirm that the low-pass filter A can achieve good filtering performance with controllable cut-off frequency, and the cut-off frequency of this low-pass filter A can be adjusted by directly adding a proper DC control signal together with the input signal, without requirement of changing the circuit structure and parameters.

In order to comprehensively test the controllability of this filter, a voltage signal V_1 with the amplitude of 1 V and low frequency of 1Hz is inputted into the filter A. Another voltage signal V_2 with the amplitude of 1 V also but relatively high frequency is together inputted for further testing. These high frequencies are chosen as 0.1 kHz, 0.4 kHz, 0.7 kHz, 1.4 kHz, 2.8 kHz, and 5.6 kHz, respectively. When the MR reaches its lower or upper boundary values, the output amplitudes of V_1 and V_2 are measured, and together listed in Tab. 3.

TABLE 3. The amplitude testing of filter.

Frequencies of V_2	$R_M = R_{off}$		$R_M = R_{on}$	
	V_1	V_2	V_1	V_2
0.1kHz	0.41V	0.35V	0.98V	0.94V
0.2kHz	0.41V	0.27V	0.98V	0.89V
0.7kHz	0.41V	0.10V	0.98V	0.63V
1.4kHz	0.41V	0.05V	0.98V	0.40V
2.8kHz	0.41V	0.03V	0.97V	0.21V
5.6kHz	0.41V	0.01V	0.97V	0.11V

It can be seen that, regardless of memristance, the amplitude of the high-frequency signal V_2 can be gradually attenuated as the frequency is increased. For the case of $R_M = R_{\text{off}}$, when the high frequency is changed from 0.7 kHz to 1.4 kHz, the attenuation of the input signal V_2 is increased. In similarity, when R_M reaches R_{on}, the frequency is changed from 0.2 kHz to 0.7kHz, and the amplitude attenuation of the high frequency is also increased. These results evidently show that the signals with the frequency greater than the cut-off frequency can be attenuated by the low-pass filter.

B. TOPOLOGY B

The parameters of the MR emulator are configured as the same with that used by testing filter topology A. Thus, the two boundary values of the memristance are $R_{\text{off}} = 2.22\text{k}\Omega$ and $R_{\text{on}} = 246.91\Omega$. In similarity with the low-pass filter A, the filtering performance with input signal of square waveform is validated by setting the input square voltage V_i with the parameters as $V_{\text{OH}} = 3\text{V}$, $V_{\text{OL}} = 1\text{V}$, $T = 0.2\text{s}$ and $t_h = t_l = 0.1\text{s}$. In the negative feedback network, the resistance $R_a = 5\text{k}\Omega$ and $R_b = 1\text{k}\Omega$, while the filter capacitor $C = 15\mu\text{F}$ and $R_x = 1\text{k}\Omega$. The filter B is simulated also by the Pspice software and the sampled curve are replotted by using the Origin software. The results are shown in Fig. 8.

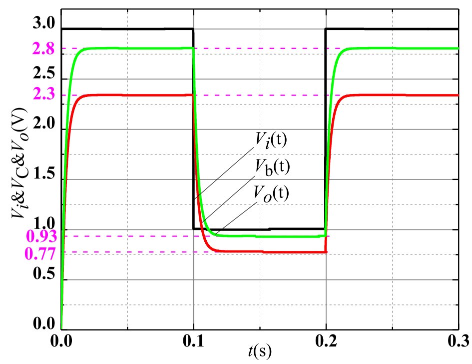

FIGURE 8. Simulation results of topology B under square wave signal.

As shown in Fig. 8, the black curve is the input signal V_i, the red curve is the capacitor voltage V_b, and the green curve is the output voltage V_o. Since the input control voltage $V_i > 0$, the memristance can reach the lower boundary value R_{on}. During the interval [0, 0.1]s, the input signal is remained at the high level V_{OH}, the capacitor C is charged and the capacitor voltage V_b is raised until the capacitor is reached the steady state. During [0.1,0.2]s, the input voltage V_i is altered from the high level to the low level. The capacitor is now discharged from the time $t = 0.1$ until steady state, and the capacitor voltage V_b is decreased from the stable state of $V_{\text{OH1}} = 2.3\text{V}$ to $V_{\text{OL1}} = 0.77\text{V}$.

When input signal is square waveform, according to (25), the cut-off frequency of filter B is $f_c = 53.58\text{Hz}$ as $R_M = R_{\text{on}}$. After filtered by the low-pass filter B, the higher harmonics of square waveform signal with the frequency greater than cut-off frequency f_c can be removed, and the output is no longer a standard square waveform. Therefore, the low-pass filtering can be realized even when the signal is a sinusoidal wave. Then, the control voltage signal V_{p1} is inputted together with the sinusoidal signal V_i for tuning the cut-off frequency. V_i is the superposition of two sinusoidal signals V_1 and V_2, where $V_1 = 1\sin(20\pi t)$ and $V_2 = 1\sin(1400\pi t)$. In the feedback network, the resistances are $R_a = 5\text{k}\Omega$ and $R_b = 1\text{k}\Omega$, while the filter capacitance $C = 1\mu\text{F}$ and $R_x = 1\text{k}\Omega$. The input and output waveforms are simulated and shown in Fig. 9, where the grey curve is input voltage V_i, and the green curve is output voltage V_o. In order to test the adjustment ability of cut-off frequency, control signal V_{p1} is first set to be negative of -3V during the interval of [0, 1]s, and then positive of 3V during the time interval [1, 2]s. Under excitation of negative voltage V_{p1}, the memristance could rapidly reach the upper value R_{off}; while the value of V_{p1} is positive, the

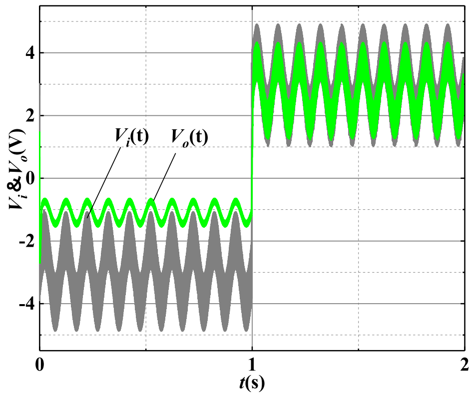

FIGURE 9. The waveforms of the input and output of the filter B under sinusoidal excitation.

TABLE 4. The amplitude testing of filter B.

Frequencies of V_2	$R_M = R_{off}$		$R_M = R_{on}$	
	V_1	V_2	V_1	V_2
0.1kHz	0.35V	0.30V	0.94V	0.88V
0.2kHz	0.35V	0.24V	0.94V	0.86V
0.7kHz	0.35V	0.10V	0.94V	0.62V
1.4kHz	0.35V	0.05V	0.94V	0.39V
2.8kHz	0.35V	0.03V	0.94V	0.21V
5.6kHz	0.35V	0.01V	0.94V	0.11V

memristance is forced to approach lower boundary value. According to (25), the cut-off frequencies of filter B corresponding to the lower and upper boundary values can be calculated as $f_{cl} = 230.8$Hz and $f_{ch} = 803.7$Hz, respectively. Therefore, only V_1 with frequency 10Hz can pass through the filter during time [0, 1]s.

During the time interval [1, 2]s, the cut-off frequency is increased to 803.7Hz by negative control voltage, and hence the input signals V_1 and V_2 can together pass through the filter. This result shows that the cut-off frequency of the low-pass filter B can be also adjusted by inputting a proper DC control voltage together with the input signal, and hence possesses the attractive advantages without requirement of adding extra circuit components as well as changing the circuit structure and parameters.

In order to comprehensively verify the filtering performance of the filter B, the amplitude of the V_1 is set to 1V with the frequency of 10 Hz. The frequencies of V_2 are configured to 0.1 kHz, 0.2 kHz, 0.7 kHz, 1.4 kHz, 2.8 kHz, and 5.6 kHz, respectively. The output amplitudes of V_1 and V_2 after passing through the filter are sampled and shown in Table 4. Evidently, regardless of the memristance, as the frequency of V_2 is increased, the output amplitude is correspondingly decreased. When the frequency of V_2 is greater than the cut-off frequency of the low-pass filter, the amplitude attenuation is very large, which also shows the low-pass performance of this MR based filters.

VI. EXPERIMENTAL VERIFICATION

A. TOPOLOGY A

In order to verify the filtering performance of the filter A, the parameters of the MR emulator are configured as $R_3 = 10\text{k}\Omega$, $R_4 = 5\text{k}\Omega$, $R_5 = 10\text{k}\Omega$, $R_6 = 25\text{k}\Omega$, $R_7 = 15\text{k}\Omega$, $R_8 = 10\text{k}\Omega$, $R_9 = 50\text{k}\Omega$, $R_{10} = 1\text{k}\Omega$, $C_1 = 150$nF and, $v_s = -15$V. The resistances in the feedback circuit are $R_a = 5\text{k}\Omega$ and $R_b = 1\text{k}\Omega$. The filter capacitor $C = 15\mu$F, the resistor $R_1 = 1\text{k}\Omega$, and the resistor $R_x = 1\text{k}\Omega$. The input signal V_i is a square waveform with high level of 3V and low level of 1V. The experimental result is shown in Fig. 10, of which the CH1 channel is the iutput signal V_i, and the CH2 channel is the output signal V_o. It can be seen from Fig. 10 that corresponding to the input signal V_i going through the filter A, the output signal V_o is no longer a standard square wave, which is consistent with the simulation results. According to (19), the passband gain of the filter A is $A_V = 1.00$, and this amplitude of the output signal V_o is substantially in good agreement with the theoretical calculation.

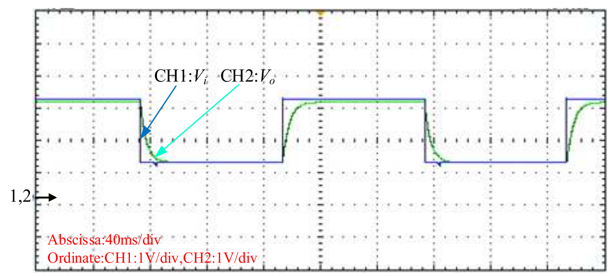

FIGURE 10. Experimental waveforms of input and output signals of filter A as the input is square waveform.

The magnitude-frequency characteristic for topology A is shown in Fig. 12. The black curve is the scenario when the memristance is R_{on}, and the red curve corresponds to the case when the memristance is R_{off}. It can be seen from the figure that the cut-off frequency of topology A in the Bode plot is consistent with the calculation result.

For further testing, the resistances in the feedback network 1 are configured as $R_a = 5\text{k}\Omega$ and $R_b = 1\text{k}\Omega$, the capacitance is $C = 1\mu$F, and the resistances $R_x = R_1 = 1\text{k}\Omega$. The input signal V_i is the superposition of V_1 and V_2, and the control voltage V_{p1} is set in equivalence to that of simulation, and the experimental results are shown in Fig. 11. During the time interval t_l, the input control voltage V_{p1} is negative with low voltage level, and is positive with high level during the time interval t_h. Therefore, the lower cut-off frequency f_{cl} of the filter is 198.94 Hz during the time t_l interval and the higher cut-off frequency f_{ch} is 771.91Hz for the time interval t_h. Therefore, the high frequency signal V_2 can be filtered out during the time interval t_l. When V_{p1} is positive, the frequencies of the input signals V_1 and V_2 are both smaller than cut-off frequency f_{ch}, and hence the input signal V_i can be passed through the filter.

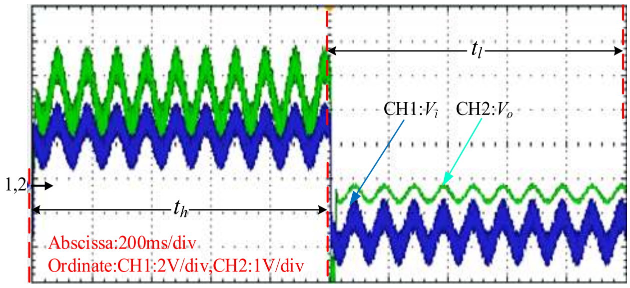

FIGURE 11. Experimental waveforms of input and output signals of filter A as the input is sinusoidal waveform.

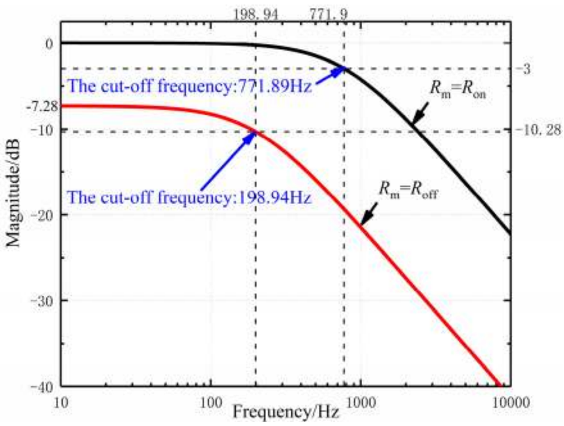

FIGURE 12. Magnitude-frequency characteristic of topology A.

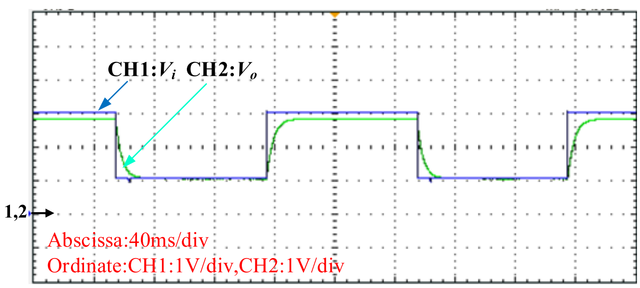

FIGURE 13. Experimental waveforms of input and output signals of filter B as the input is square waveform.

B. TOPOLOGY B

The parameters of the MR emulator circuit are configured as $R_3 = 10\text{k}\Omega$, $R_4 = 5\text{k}\Omega$, $R_5 = 10\text{k}\Omega$, $R_6 = 25\text{k}\Omega$, $R_7 = 15\text{k}\Omega$, $R_8 = 10\text{k}\Omega$, $R_9 = 50\text{k}\Omega$, $R_{10} = 1\text{k}\Omega$, $C_1 = 150\text{nF}$ and $v_s = -15\text{V}$. The resistances of the feedback network are $R_\text{a} = 5\text{k}\Omega$, $R_\text{b} = 1\text{k}\Omega$, the filter capacitor $C = 15\mu\text{F}$, and the resistor $R_\text{x} = 1\text{k}\Omega$. The input signal V_i is a square waveform with high level of 3V and the low level of 1V. The experimental results are shown in Fig. 13. In Fig. 13, the CH1 channel is the input signal V_i, and the CH2 channel is the output signal V_o. It can be seen from Fig. 13, the output signal V_o is no longer a standard square wave, due to the operation of filter B, and the harmonics with the frequency greater than the cut-off frequency can be greatly attenuated. It can be also confirmed that, the experimentally measured amplitudes of the output signal V_o are also consistent with the theoretical calculation and simulation.

For the testing case that the input signal V_i is structured by sinusoidal signals, the parameters of the filter are configured as $R_\text{a} = 5\text{k}\Omega$, $R_\text{b} = 1\text{k}\Omega$, $R_\text{x} = 1\text{k}\Omega$, and $C = 1\mu\text{F}$. The amplitude and frequency of the input signal V_1 are 1V and 10Hz, respectively. Also, the amplitude of the input signal V_2 with higher frequency of 700Hz is 1V. The experimental results are shown in Fig. 14.

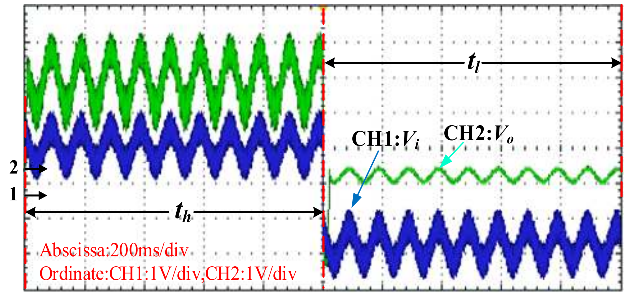

FIGURE 14. Experimental waveforms of input and output signals of filter B as the input is sinusoidal waveform.

In similarity to topology A, during the time interval t_l, the input control voltage V_{p1} is negative, and the memristance is reached the maximum value to obtain the cut-off frequency of 230.8 Hz. During the time interval t_h, the input control voltage V_{p1} is positive, the cut-off frequency of filter B can be measured as 803.7 Hz. Therefore, the high frequency signal V_2 can be filtered out during the time interval t_l. During the time interval t_h, the input signal V_i can be passed through the filter.

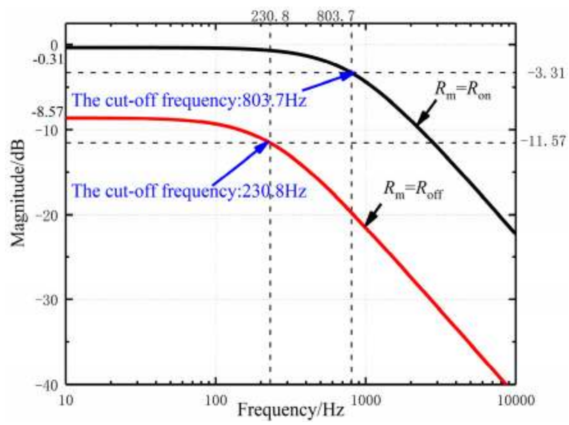

FIGURE 15. Magnitude-frequency characteristic of topology B.

The magnitude-frequency characteristic for topology B is shown in Fig. 15. The black curve is the scenario when the memristance is R_on, and the red curve corresponds to the case when the memristance is R_off. It can be seen from the figure that the cut-off frequency of topology A in the Bode plot is consistent with the calculation result.

These results evidently show that the proposed MR based low-pass filters could offer good filtering performance with controllable cut-off frequency by inputting a DC control voltage. Also note that, this added DC control voltage could be easily removed at the output side if necessary.

VII. CONCLUSION

A family of low-pass filters is proposed by combining the connection nodes of network Z with the ports of filter op amp. In order to achieve the tunable cut-off frequency, the MR is adopted to replace the resistor inside the network Z of the low-pass filter family. By properly configuring the filter circuit parameters and the input control voltages, the cut-off frequency of the low-pass filters can be easily tuned hot-line. The most attractive advantage of the proposed low-pass filters is the cut-off frequency can be controlled without the requirement of adding extra memristance writing circuits or topology reconstruction, which is propitious to integrated circuit implementation together with the nanoscale size of MR. These research results could provide beneficial and reliable references for further investigation of MR application in integrated circuits.

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