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A Family of Memristor-Based Reactance-Less Oscillators

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SUMMARY

In this paper, we present for the first time a family of memristor-based reactance-less oscillators (MRLOs). The proposed oscillators require no reactive components, i.e., inductors or capacitors, rather, the “resistance-storage” property of memristor is exploited to generate the oscillation. Different types of MRLO family are presented and for each type, closed form expressions are derived for the oscillation condition, oscillation frequency, and range of oscillation. Derived equations are further verified using transient circuit simulations. A comparison between different MRLO types is also discussed. In addition, detailed fabrication steps of a memristor device and experimental results for the first MRLO physical realization are presented.

KEYWORDS: memristors; reactance-less oscillator; voltage-controlled oscillator

1. INTRODUCTION

The memristor is a nonlinear resistor that changes its state depending on the charge passing through it. The existence of the memristor was first postulated by Leon Chua in 1971 [1] and later generalized in 1976 [2]. Recently, it has been shown that resistive devices with pinched hysteresis behavior have been around for a couple of hundred years [3] and have been demonstrated experimentally by multiple research groups and labs [4–6]. However, it was not until 2008 when a passive two terminal physical implementation was directly related to the theory [7]. Since then, memristors have received intensive attention from researchers in many different fields. Due to its unique characteristics, the memristor is expected to play an important role in many applications [8, 9] including chaotic circuits [10, 11], non-volatile memory [12–15], pattern recognition [16, 17], neural networks [18], cryptography [19], reconfigurable logic [20], and circuit modeling [21]. In addition, memristors can be used to build programmable analog circuits and novel circuit architectures [22–24].

Oscillators are key components in electronic systems since there is always a need for a repetitive signal with a given frequency and waveform for timing, modulation, and test and measurement applications. Oscillators can be classified as sinusoidal or relaxation oscillators. Sinusoidal oscillators are based on positive feedback, where a frequency selective network is used to determine the frequency of oscillation of the sinusoidal output [25]. Relaxation oscillators generate square or triangular waveforms based on astable multivibrators [26]. Both oscillators depend on reactive elements (i.e., capacitors and inductors) to realize the oscillator function. It should be noted that even ring oscillators depend on the delay introduced by the intrinsic and extrinsic capacitance at every node in the chain, where the intrinsic

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capacitance is the parasitic capacitance of the transistor device while the extrinsic capacitance is an intentionally added one [27].

Memristors were previously used to replace resistors in Wien and phase shift oscillators [28, 29], where it was shown that although the poles of the system oscillate, sustained oscillation is maintained owing to the properties of the memristors [30]. However, reactive elements were still required to build the oscillator. In this paper, we present thorough mathematical derivation describing a complete family of memristor-based reactance-less oscillators (MRLOs) alongside a physical realization of an MRLO for the first time. In addition, we present the detailed fabrication steps of a memristor device. The charging and discharging of a reactive element is replaced by the increase and decrease of the memristor resistance. Instead of having an energy storing reactive element, memristors are used as a “resistance-storing” element. The inherent delay in the memristor response due to the finite dopant drift mobility is exploited to realize the oscillator function.

It should be noted that the switching speed for all types of MRLO depends on the dopant drift mobility (μ_v). For the μ_v value reported in [7], the proposed oscillator is suitable for low frequency applications. The applications of low frequency oscillators include biomedical circuits and embedded systems though off-chip components are usually used because large capacitors are required [31,32]. The implementation utilizing memristors proposed in this paper eliminates the need for capacitors or inductors allowing a fully integrated implementation in a very small area. However, the introduced concept is general and can be extended to higher frequencies given that technology advancement improves the response speed. For instance, memristors with fast sub-nanosecond switching time have recently been reported [33–35].

Several models for memristors have been introduced including mathematical and behavioral modeling [36–39], circuit modeling based on the dopant drift concept using a window function [40–42] or boundary conditions [43,44], and quantum effect models [45,46]. For this work, we use the dopant drift model of Hewlett Packard (HP) memristor in [36] due to its simplicity and to provide an insight into the operation of the circuits presented. In addition, the dopant-drift model for the memristor is the most widely used. However, the introduced circuits are general to any memristor implementation or model, since the required device property is the pinched i - v hysteresis.

The rest of the paper is organized as follows. Section 2 discusses the general architecture of the MRLO. In Section 3, the general circuit analysis for the proposed oscillator family is presented. Sections 4, 5, and 6 present three special cases of the oscillator and their governing equations. Comparisons and discussions are presented in Section 7. Finally, we introduce the experimental results of the oscillator circuit using one of our fabricated memristor devices in Section 8.

2. GENERAL ARCHITECTURE

The general architecture of the proposed oscillator is shown in Figure 1a. The oscillator is composed of two basic elements (E_1 and E_2) forming a voltage divider and a transfer function ($F(V_i)$). E_1 and E_2 can be a memristor or a resistor, where at least one element is a memristor. The voltage on E_2 is given by

$$V_i(t) = V_o(t) \frac{R(E_2)}{R(E_1) + R(E_2)}, \quad (1)$$

where $R(E_x)$ is the resistance of element E_x . For the sake of simplicity, $F(V_i)$ is assumed to have infinite input impedance.

The type of oscillator is determined according to the type of the two basic elements (E_1 and E_2). E_1 and E_2 can be two memristors, a floating memristor and a grounded resistor, or a floating resistor and a grounded memristor. For each type, the memristor(s) can be connected such that the magnitude of V_i increases when V_o is positive and decreases when V_o is negative, which we will refer to as the positive configuration. The schematics of the three types of MRLO connected in the positive configuration are shown in Figure 1. Alternatively, the memristor(s) can be connected such that the magnitude of V_i decreases when V_o is positive and increases when V_o is negative. This will be referred to as the negative configuration. The analysis and performance of the positive and negative configurations of each type of

MRLO is very similar, except that $F(V_i)$ is different. The transfer functions of $F(V_i)$ for both positive and negative configurations are shown in Figure 2. The threshold voltages V_p and V_n should be selected such that $V_n < 0 < V_p$. A simple implementation of $F(V_i)$ using two comparators and basic gates is also shown in Figure 2. It should be noted that other implementations for $F(V_i)$ are also possible.

For E_1 and E_2 being memristors, their resistances increase or decrease according to the direction of current flowing through them. Using the mathematical model of HP memristor in [36], the memristor resistance as a function of time can be described by

$$R_m^2(t) = R_i^2 + 2k' \int_0^t V_m(\tau) d\tau, \quad (2)$$

where R_m is the memristor resistance, R_i is the initial resistance of the memristor, V_m is the voltage across the memristor, and k' is the memristor constant given by

$$k' = \alpha \mu_v R_{on} (R_{off} - R_{on}) / d^2, \quad (3)$$

where μ_v is the dopant drift mobility, R_{on} and R_{off} are the minimum and maximum memristor resistances respectively, and d is the length of the device. The dopant drift mobility is the physical limit that determines the response time of the memristor whereas the polarity indicated by $\alpha = -1$ or 1 describes how it is connected in the circuit. The suitable polarity configuration, positive or negative, and the oscillation conditions depend on k'_1 and k'_2 , where k'_x is memristor constant of the device 'x'. Resistors are treated by setting their k' to zero, where $k'_1 = 0$ when a resistor (R_a) is used as E_1 and $k'_2 = 0$ when a resistor (R_b) is used as E_2 . It is useful to define the relation between the constants of the two devices as,

$$k_r = \frac{k'_1}{k'_2}. \quad (4)$$

For oscillation to occur, k_r must have any defined value other than unity, given that the proper configuration is used. Hence, no oscillation will occur in the case of two resistors or two memristors with the same memristor constant ($k_r = 1$). In this case, the transfer function input voltage (V_i), given in (1), will be constant with time, thus, no change will occur at the circuit output. Table 1 shows the suitable configuration for each of the possible combinations of k'_x . These combinations of device polarity and their speed determine whether V_i increases or decrease with positive V_o and vice versa. According to (3), the device speed can be adjusted by changing the device length (d) or the limit resistances (R_{on} and R_{off}). The values of R_{on} and R_{off} can be controlled by changing the device area.

3. CIRCUIT OPERATION

In this section the circuit operation for a circuit with two memristors connected in the same polarity is described. However, the circuit tracing is general and can be used for all the other cases.

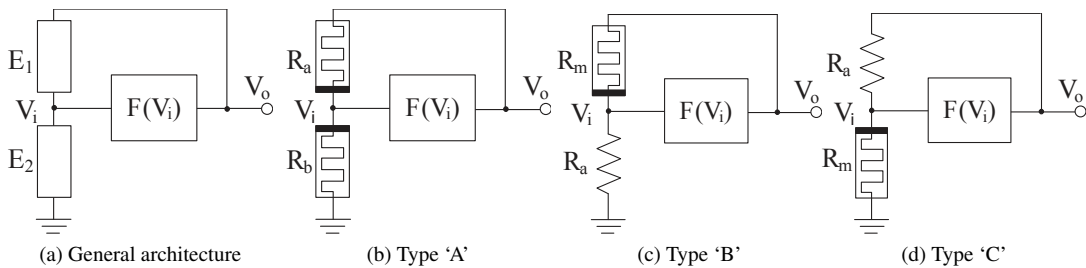


Figure 1: (a) General schematic of the MRLO family. (b-d) Schematic of different sub-types of MRLO family connected in the positive configuration. For type 'A' two identical memristors connected in opposite polarities are used.

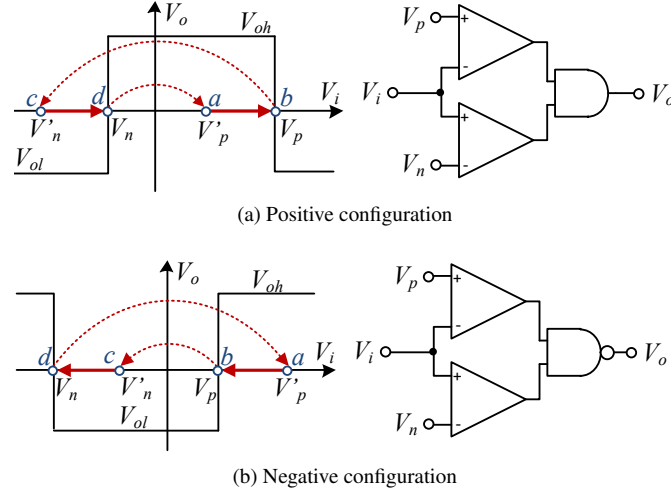


Figure 2: Transfer function of $F(V_i)$ showing transitions between different operating points, in addition to possible circuit implementations for positive and negative configurations. The circuit is made of two comparators and (a) AND gate (b) NAND gate.

The two memristors are connected such that their resistances increase with positive V_o and decrease for negative one as shown by the top-most M-M circuit in Table 1. For proper operation, E_2 must be faster than E_1 such that $k_r < 1$. The operation of the oscillator can be traced as follows, assuming that we start at 'a':

a \rightarrow b: At 'a', V_o is positive and is equal to V_{oh} . Both R_a and R_b will increase, but R_b will increase in a faster speed. Therefore, V_i will increase until the operating point reaches 'b'.

b \rightarrow c: At 'b', the value of V_i will just cross V_p , thus V_o will switch to V_{ol} , and the operating point will jump to 'c'.

c \rightarrow d: At 'c', the resistances of the two memristors will decrease as V_o is negative ($V_o = V_{ol}$), but R_b will decrease faster. Thus, $|V_i|$ will decrease and the operating point will move to 'd'.

d \rightarrow a: At 'd', when V_i just crosses V_n , V_o will switch from V_{ol} to V_{oh} . Consequently, the operating point will instantly move to 'a'. And the oscillation will continue.

It should be noted that the location of the operating points depends on the memristor speed, initial condition, and the values of the voltages used.

3.1. Oscillation Conditions

From (2), the relation between R_a and R_b and the voltage across them can be written as

$$R_a dR_a = k'_a (V_o - V_i) dt, \text{ and} \quad (5a)$$

$$R_b dR_b = k'_b V_i dt. \quad (5b)$$

Given that the same current flows through the two memristors, the relation between the two memristor resistances is given by

$$\frac{1}{k'_a} dR_a = \frac{1}{k'_b} dR_b. \quad (6)$$

By integrating both sides, the relation between R_a and R_b and their initial values is given by

$$R_a - R_{ai} = k_r (R_b - R_{bi}), \quad (7)$$

Table 1: All possible combinations for memristor constants and suitable configuration (positive or negative) for each. M abbreviates memristor and R abbreviates resistor.

Elements	Condition 1	Condition 2	Configuration	Circuit
M-R	$k_r = \infty$	$k'_1 < 0$	+ve	
		$k'_1 > 0$	-ve	
M-M	$1 < k_r < \infty$	$k'_1 < 0$	+ve	
		$k'_1 > 0$	-ve	
	$k_r = 1$	-	none	none
	$0 < k_r < 1$	$k'_1 > 0$	+ve	
		$k'_1 < 0$	-ve	
	$-\infty < k_r < 0$	$k'_1 < 0$	+ve	
$k'_1 > 0$		-ve		
R-M	$k_r = 0$	$k'_2 > 0$	+ve	
		$k'_2 < 0$	-ve	

where R_{ai} and R_{bi} are the initial resistances of R_a and R_b respectively. From (1) and by using (7), the transition resistances at $V_i = V_p$ are given by

$$R_{ap} = \frac{R_{bi}k_r - R_{ai}}{\left(\frac{V_p}{V_{oh}-V_p}\right)k_r - 1}, \text{ and} \quad (8a)$$

$$R_{bp} = \frac{R_{ai} - R_{bi}k_r}{\left(\frac{V_{oh}-V_p}{V_p}\right) - k_r}, \quad (8b)$$

where R_{ap} and R_{bp} are the values of R_a and R_b at the transition point ($V_i = V_p$) respectively. Similarly, the transition resistances at $V_i = V_n$ are given by

$$R_{an} = \frac{R_{bi}k_r - R_{ai}}{\left(\frac{V_n}{V_{ol}-V_n}\right)k_r - 1}, \text{ and} \quad (9a)$$

$$R_{bn} = \frac{R_{ai} - R_{bi}k_r}{\left(\frac{V_{ol}-V_n}{V_n}\right) - k_r}, \quad (9b)$$

where R_{an} and R_{bn} are the values of R_a and R_b at the transition point ($V_i = V_n$) respectively.

Beside the necessary conditions for k_r given in Table 1, the memristor resistances must not reach saturation in order to sustain oscillation.

$$R_{on,a} < R_a < R_{off,a}, \text{ and} \quad (10a)$$

$$R_{on,b} < R_b < R_{off,b}, \quad (10b)$$

where $R_{on,a}$ and $R_{off,a}$ are the ON and the OFF values of R_a , and $R_{on,b}$ and $R_{off,b}$ are the ON and the OFF values of R_b . By substituting (10a) and (10b) in (8a), (8b), (9a), and (9b), the oscillation condition can be given as

$$R_{bi}k_r - R_{ai} < \min \begin{cases} R_{off,a} \left[\left(\frac{V_p}{V_{oh}-V_p} \right) k_r - 1 \right] \\ R_{off,b} \left[k_r - \left(\frac{V_{oh}-V_p}{V_p} \right) \right] \end{cases}, \text{ and} \quad (11a)$$

$$R_{bi}k_r - R_{ai} > \max \begin{cases} R_{on,a} \left[\left(\frac{V_n}{V_{ol}-V_n} \right) k_r - 1 \right] \\ R_{on,b} \left[k_r - \left(\frac{V_{ol}-V_n}{V_n} \right) \right] \end{cases}. \quad (11b)$$

3.2. Oscillation Frequency

The oscillation frequency can be calculated by rewriting (5a) and (5b) as

$$dt = \frac{1}{V_o k'_a} R_a dR_a + \frac{1}{V_o k'_b} R_b dR_b. \quad (12)$$

By integrating (12) from $V_i = V_n$ to $V_i = V_p$, the time of the positive half cycle is given by

$$T_H = \frac{1}{2V_{oh}k'_a} (R_{ap}^2 - R_{an}^2) + \frac{1}{2V_{oh}k'_b} (R_{bp}^2 - R_{bn}^2). \quad (13)$$

Similarly, the negative half cycle can be calculated by integrating (12) from $V_i = V_p$ to $V_i = V_n$

$$T_L = \frac{1}{2V_{ol}k'_a} (R_{an}^2 - R_{ap}^2) + \frac{1}{2V_{ol}k'_b} (R_{bn}^2 - R_{bp}^2). \quad (14)$$

Therefore, the oscillation frequency is given by

$$f = \frac{2V_{oh}V_{ol} (k'_a V_n + k'_b V_n - k'_b V_{ol})^2 (k'_a V_p + k'_b V_p - k'_b V_{oh})^2}{(V_{oh} - V_{ol}) (V_n V_{oh} - V_{ol} V_p) (k'_b R_{ai} - k'_a R_{bi})^2 [(V_n V_{oh} + V_p V_{ol}) (k'_a + k'_b) - 2k'_b V_{oh} V_{ol}]}. \quad (15)$$

This expression is the general case for all the possible values of k_r except $k_r = 1$, since no oscillation occurs at the unity value. Equation (15) can be simplified for $V_{ol} = -V_{oh}$,

$$f = \frac{(k'_a V_n + k'_b V_n + k'_b V_{oh})^2 (k'_a V_p + k'_b V_p - k'_b V_{oh})^2}{V_{oh} (V_p + V_n) (k'_a R_{bi} - k'_b R_{ai})^2 [(V_n - V_p) (k'_a + k'_b) + 2k'_b V_{oh}]}. \quad (16)$$

The minimum and the maximum frequencies of the system can be calculated by substituting (11a) and (11b) in (15). The derived frequency equations are general and hold for any type of proposed MRLOs introduced in the next sections.

3.3. Validation

In order to verify memristor-based circuits, researchers utilize SPICE, Verilog-A, and/or Matlab models [39, 40, 46, 47], or emulate the memristor model using active circuitry [22, 24]. The proposed circuit was verified using Cadence Virtuoso 6 Spectre transient circuit simulations employing the memristor model given in [36]. The parameters R_{on} , R_{off} , d , and μ_v were selected to be 100Ω , $38k\Omega$, $10nm$, and $10^{-10}cm^2s^{-1}V^{-1}$ respectively, which are the same values reported by HP Labs in [7]. The circuit was simulated for $V_{oh} = 1V$, $V_{ol} = -1V$, $V_p = 0.75V$, and $V_n = -0.5V$. Figure 3 compares frequency of oscillation from transient simulation with the derived expression as R_{bi} is swept from $1k\Omega$ to $12k\Omega$. For ($k_r < 1$), the circuit oscillates faster as the ratio k_r decreases, i.e., for larger difference in the speeds of the two memristors.

In the following subsections, three special types of the MRLO are given. These oscillators are easier to tune and have simpler governing equations. In Section 7, a comparison between these types is introduced.

4. MRLO TYPE 'A': TWO OPPOSITE MEMRISTORS ($K_R = -1$)

MRLO type 'A' is a special case where both E_1 and E_2 are two identical memristors of opposite polarities. Thus, there will be two oppositely varying resistances.

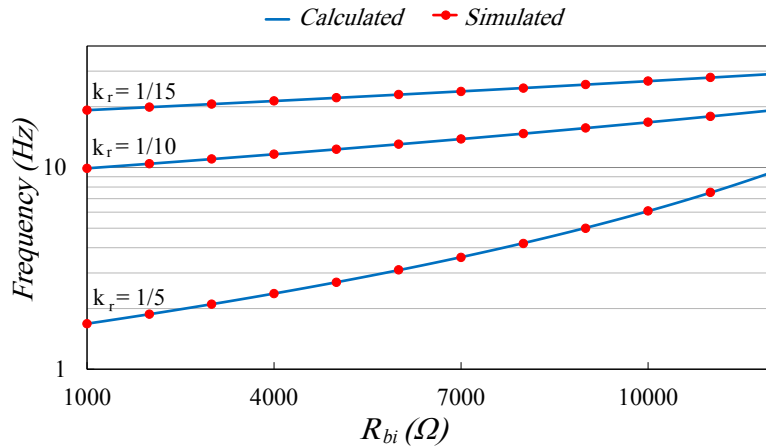


Figure 3: Tuning curve for the oscillation frequency using (15) and circuit simulation on Cadence Spectre for different values of k_r . where $R_{on} = 100\Omega$, $R_{off} = 38k\Omega$, $d = 10nm$, $\mu_v = 10^{-10}cm^2s^{-1}V^{-1}$, $R_{ai} = 4k\Omega$, $V_{oh} = 1V$, $V_{ol} = -1V$, $V_p = 0.75V$, $V_n = -0.5V$, $k'_1 = -3.79 \times 10^8$ and $k'_2 = 3.79 \times 10^8$.

The analysis will be done for the positive configuration shown in Figure 1, noting that the analysis of the negative configuration is similar. The memristors are connected in a polarity such that R_a decreases for positive V_o and increases for negative V_o and the opposite applies for R_b . It should be noted that V_o and V_i always have the same polarity and the magnitude of V_o is always higher than the magnitude of V_i .

4.1. Mathematical Analysis

From (2), the relation between R_a and the voltage across it can be written as

$$R_a dR_a = k' (V_i - V_o) dt. \quad (17)$$

Thus the current flowing through R_a can be written as

$$i_a = -\frac{1}{k'} \frac{dR_a}{dt}. \quad (18)$$

Similarly, the relation between R_b and the voltage across it is given by

$$R_b dR_b = k' V_i dt, \quad (19)$$

and the current flowing through R_b is

$$i_b = \frac{1}{k'} \frac{dR_b}{dt}. \quad (20)$$

We assume that $F(V_i)$ has infinite input resistance. Thus, from (18) and (20)

$$\frac{dR_a}{dt} = -\frac{dR_b}{dt}. \quad (21)$$

By integrating both sides

$$\int_{R_{ai}}^{R_a} dR_a = -\int_{R_{bi}}^{R_b} dR_b, \quad (22)$$

where R_{ai} and R_{bi} are the initial values of R_a and R_b respectively. Thus, the relation between R_a and R_b and their initial values is given by

$$R_a + R_b = R_{ai} + R_{bi}. \quad (23)$$

To derive the oscillation condition we need to write the expressions of R_a and R_b at the transition points, i.e., $V_i = V_p$ and $V_i = V_n$. From (1), the transition resistances are given by

$$R_{ap} = \frac{V_{oh} - V_p}{V_{oh}} (R_{ai} + R_{bi}), \quad (24a)$$

$$R_{bp} = \frac{V_p}{V_{oh}} (R_{ai} + R_{bi}), \quad (24b)$$

$$R_{an} = \frac{V_{ol} - V_n}{V_{ol}} (R_{ai} + R_{bi}), \text{ and} \quad (24c)$$

$$R_{bn} = \frac{V_n}{V_{ol}} (R_{ai} + R_{bi}), \quad (24d)$$

where R_{ap} , R_{bp} , R_{an} , and R_{bn} are the values of R_a and R_b at the transition points $V_i = V_p$ and $V_i = V_n$ respectively. The transition resistances depend on the sum of the initial memristor resistances, thus the oscillation period will also depend on this sum. The memristor resistance oscillates in the time domain between the transition resistances, and as the rails of oscillation change, the oscillation period will also change.

Based on the circuit tracing given in the previous section, the oscillation will occur if V_p and V_n are selected such that

$$V_p > V_n \frac{V_{oh}}{V_{ol}}. \quad (25)$$

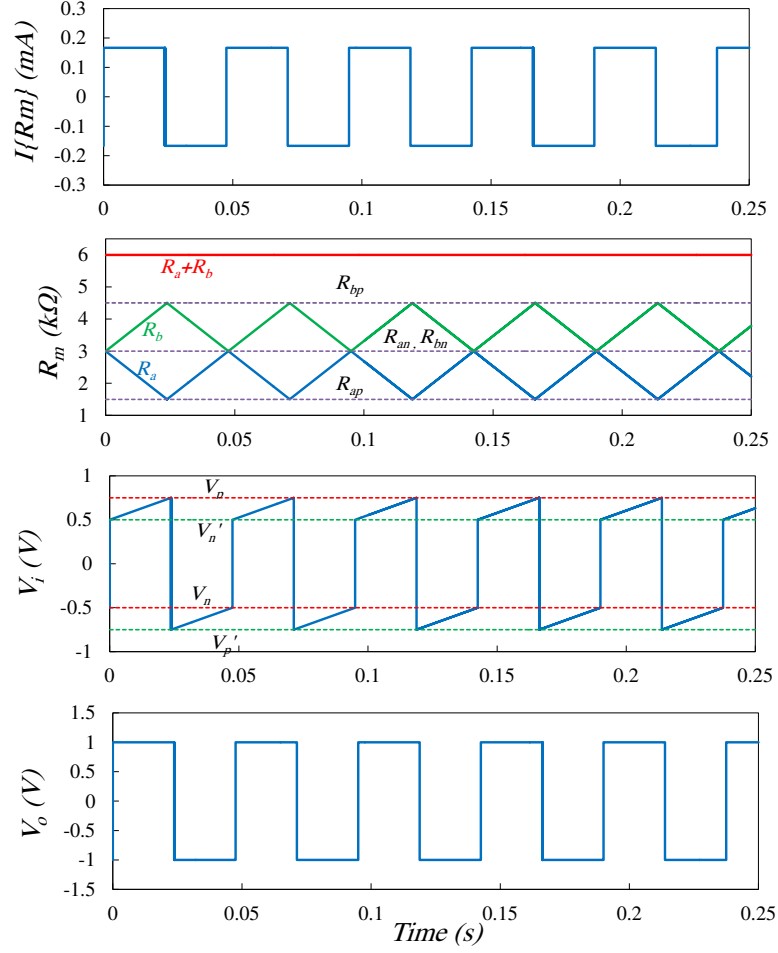


Figure 4: Spectre transient simulation results for $I\{R_m\}$, R_m , V_i , and V_o respectively for $R_{ai} = R_{bi} = 3 \text{ k}\Omega$ and other parameters are the same as Figure 3.

The transition resistances should fall within the minimum and maximum memristor resistances

$$R_{on} < \{R_{an}, R_{ap}, R_{bn}, R_{bp}\} < R_{off}. \quad (26)$$

By substituting with the formulas of the transition resistances given in (24a), (24b), (24c), and (24d) the oscillation condition can be rewritten as

$$(R_{ai} + R_{bi}) > \max\left(\frac{V_{ol}}{V_n}, \frac{V_{oh}}{V_{oh} - V_p}\right) R_{on}, \text{ and} \quad (27)$$

$$(R_{ai} + R_{bi}) < \min\left(\frac{V_{oh}}{V_p}, \frac{V_{ol}}{V_{ol} - V_n}\right) R_{off}. \quad (28)$$

To derive an expression for the oscillation frequency, from (17) and (19), we can write the time differential as

$$dt = \frac{1}{k'V_o} (R_b dR_b - R_a dR_a). \quad (29)$$

Oscillation frequency can be derived in the same technique shown in the previous section. However,

the same equation can be given by substituting ($k'_2 = -k'_1 = k'$) in (15),

$$f = \frac{k'V_{ol}^2V_{oh}^2}{(V_{oh} - V_{ol})(V_nV_{oh} - V_pV_{ol})(R_{ai} + R_{bi})^2}. \quad (30)$$

At $V_{ol} = -V_{oh}$, the expression of the oscillation frequency can be further simplified to be

$$f = \frac{k'V_{oh}^2}{2(V_p + V_n)(R_{ai} + R_{bi})^2}. \quad (31)$$

The frequency of oscillation depends on the memristor constant k' , the sum of the initial resistances of the memristors, and the values of V_{oh} , V_{ol} , V_p , and V_n . The valid range for the oscillation frequency can be derived by substituting the oscillation condition given in (27) and (28) into (31). Substituting, the minimum and maximum oscillation frequencies are given by

$$f_{min} = \frac{k' \max(V_p^2, (V_{oh} + V_n)^2)}{2R_{off}^2(V_p + V_n)}, \text{ and} \quad (32a)$$

$$f_{max} = \frac{k' \min(V_n^2, (V_{oh} - V_p)^2)}{2R_{on}^2(V_p + V_n)}. \quad (32b)$$

4.2. Validation

The two memristor resistances change in a linear fashion in opposite directions and their sum is always constant. The transition resistances depend on the sum of the initial resistances and define the frequency of oscillation. By substituting the circuit parameters into (24a), (24b), (24c), (24d), and (31): $R_{ap} = 1.5 k\Omega$, $R_{bp} = 4.5 k\Omega$, $R_{an} = 3 k\Omega$, $R_{bn} = 3 k\Omega$, and $f = 21.06 Hz$, which shows excellent match to the simulation results (see Figure 4). For further verification of the mathematical analysis presented, the oscillation frequency was tuned by sweeping R_{bi} from $1 k\Omega$ to $12 k\Omega$ (see Figure 5). Figure 4 shows transient simulation results for ($k_r = -1$) description for the model given in [36] running on Cadence Virtuoso 6 Spectre, where $R_{ai} = 4 k\Omega$ and $R_{bi} = 3 k\Omega$. A comparison between simulation results and the derived expression is shown in Figure 5. The comparison shows excellent match between simulation results and the derived expression, with maximum error less than 0.16%.

For the negative configuration, the analysis is similar. But it should be noted that for this case, the oscillation will occur when V_p and V_n are selected such that

$$V_p < V_n \frac{V_{oh}}{V_{ol}}. \quad (33)$$

Thus an additional negative sign will appear in the expressions of oscillation frequency and frequency range, such that the overall expression is positive.

5. MRLO TYPE 'B': FLOATING MEMRISTOR ($K_R = \infty$)

For MRLO type 'B', E_1 and E_2 are a memristor and a resistor respectively. The memristor is connected between V_o and V_i nodes, where both have varying voltage. For the positive configuration shown in Figure 1c, the memristor is connected such that its resistance decreases when V_o is positive and increases when V_o is negative.

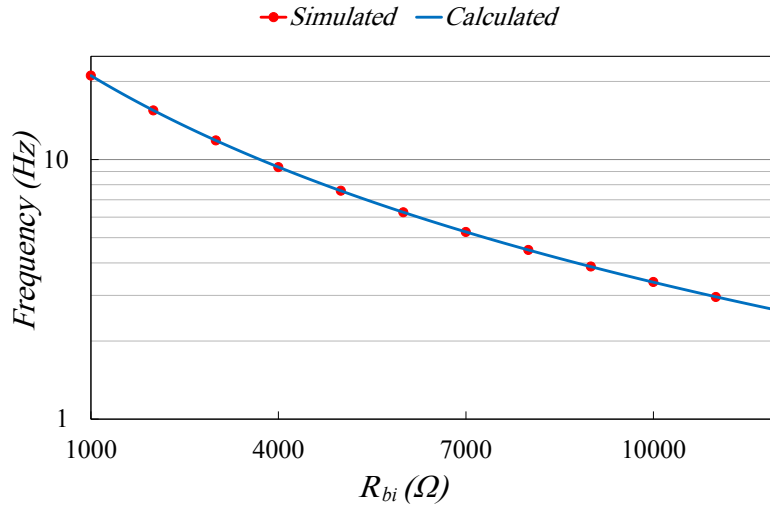


Figure 5: Tuning curve for the oscillation frequency of type 'A' using (31) and circuit simulation on Cadence Spectre for $R_{ai} = 5\text{ k}\Omega$. Other parameters are the same as in Figure 3.

5.1. Mathematical Analysis

From (1), the transition resistances at $V_i = V_p$ and $V_i = V_n$ are given by

$$R_{mp} = R_a \frac{V_{oh} - V_p}{V_p}, \text{ and} \quad (34a)$$

$$R_{mn} = R_a \frac{V_{ol} - V_n}{V_n}. \quad (34b)$$

The transition resistances do not depend on the memristor initial resistance. From the previous circuit tracing, the oscillation will occur if V_p and V_n are selected such that

$$V_p > V_n \frac{V_{oh}}{V_{ol}}. \quad (35)$$

The transition resistances have to satisfy

$$R_{on} < \{R_{mn}, R_{mp}\} < R_{off}. \quad (36)$$

By substituting with (34a) and (34b) into (36), the oscillation condition can be rewritten as

$$R_{on} \left(\frac{V_p}{V_{oh} - V_p} \right) < R_a < R_{off} \left(\frac{V_n}{V_{ol} - V_n} \right). \quad (37)$$

The frequency can be calculated by taking the limit ($k'_2 = k'_b \rightarrow 0$) of (15). This yields

$$f = \frac{2k'V_n^2V_p^2V_{ol}V_{oh}}{R_a^2(V_n^2V_{oh}^2 - V_p^2V_{ol}^2)(V_{oh} - V_{ol})}. \quad (38)$$

It should be noted that (15) is the general case for all possible values of k_r except $k_r = 1$. For the case $V_{ol} = -V_{oh}$, the expression of the frequency of oscillation is simplified to be

$$f = \frac{k'V_n^2V_p^2}{R_a^2V_{oh}(V_p^2 - V_n^2)}. \quad (39)$$

The frequency of oscillation depends on the memristor constant k' and the values of V_{oh} , V_{ol} , V_p , V_n , and R_a . The most direct way to tune the frequency of oscillation is varying the resistance R_a . By substituting the simplified frequency expression into the oscillation condition, the minimum and maximum oscillation frequencies are given by

$$f_{min} = \frac{k'V_p^2 (V_{oh} + V_n)^2}{R_{off}^2 V_{oh} (V_p^2 - V_n^2)}, \text{ and} \quad (40a)$$

$$f_{max} = \frac{k'V_n^2 (V_{oh} - V_p)^2}{R_{on}^2 V_{oh} (V_p^2 - V_n^2)}. \quad (40b)$$

5.2. Validation

Using $R_a = 3k\Omega$ and the same parameters used in validation of type 'A', the derived expressions were compared to transient simulation results. Figure 6 shows transient simulation results. The memristor resistance changes non-linearly and oscillates between two fixed rails which do not depend on the memristor initial state. By substituting parameter values in (34a), (34b) and (39), the memristor resistance oscillates between $R_{mp} = 1k\Omega$ and $R_{mn} = 3k\Omega$ and $f_o = 18.95Hz$, which matches the simulation results.

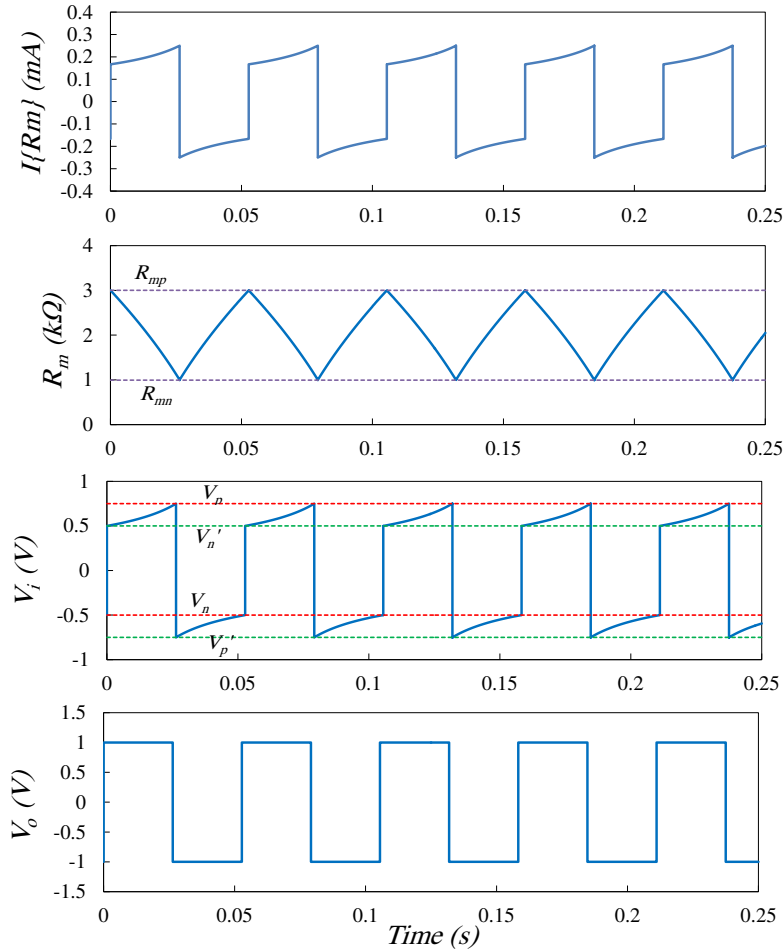


Figure 6: Type 'B' Spectre transient simulation results for $I\{R_m\}$, R_m , V_i , and V_o respectively for $R_a = 3k\Omega$. Other parameters are the same as in Figure 3.

The frequency of oscillation tuning curve using R_a as a parameter is plotted against simulation results in Figure 7, showing excellent match between simulation and analysis.

6. MRLO TYPE 'C': SINGLE GROUNDED MEMRISTOR ($K_R = 0$)

In MRLO type 'C', E_1 is a resistor and E_2 is a memristor. The positive configuration of this type, shown in Figure 1d, was recently presented by the authors in [48]. Slight variations to the original circuit presented in [48] provide higher frequency of operation and a wider range of allowable resistances [49, 50] and could be easily applied to the family of circuits presented. The effect of the linear and non linear models on the oscillation frequency and condition of oscillation on the original circuit presented in [48] have been presented in [51]. The same analysis can be easily applied to the family of circuits presented in this paper but was omitted for simplicity.

Using similar analysis to type 'B', it can be shown that the transition resistances at $V_i = V_p$ and $V_i = V_n$ are

$$R_{mp} = R_a \frac{V_p}{V_{oh} - V_p}, \text{ and} \quad (41a)$$

$$R_{mn} = R_a \frac{V_n}{V_{ol} - V_n}. \quad (41b)$$

The oscillation condition in terms of design parameters is given by

$$R_{on} \left(\frac{V_{ol} - V_n}{V_n} \right) < R_a < R_{off} \left(\frac{V_{oh} - V_p}{V_p} \right). \quad (42)$$

The frequency can be calculated by taking the limit ($k'_1 = k'_a \rightarrow 0$) of (15). This yields:

$$f = \frac{-2k'V_{ol}V_{oh}(V_{oh} - V_p)^2(V_n - V_{ol})^2}{R_a^2(V_{oh} - V_{ol})(V_pV_{ol} - V_nV_{oh})(2V_{oh}V_{ol} - V_{ol}V_p - V_{oh}V_n)}. \quad (43)$$

It should be noted that (15) is the general case for all possible values of k_r except $k_r = 1$. For ($V_{oh} = -V_{ol}$), the oscillation frequency can be further simplified to

$$f = \frac{k'(V_{oh} - V_p)^2(V_{oh} + V_n)^2}{R_a^2V_{oh}(V_p + V_n)(2V_{oh} - V_p + V_n)}. \quad (44)$$

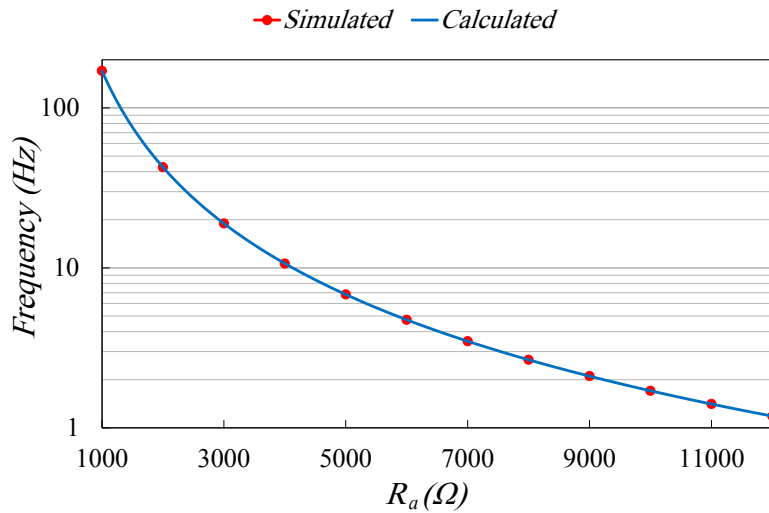


Figure 7: Tuning curve for the oscillation frequency of type 'B' using (39) and circuit simulation on Cadence Spectre. Parameters used are the same as in Figure 3.

The valid range for the oscillation frequency can be derived by substituting the oscillation condition given in (42) into (44). The minimum and maximum oscillation frequencies are

$$f_{min} = \frac{k'V_p^2 (V_{oh} + V_n)^2}{R_{off}^2 V_{oh} (V_p + V_n) (2V_{oh} - V_p + V_n)}, \text{ and} \quad (45a)$$

$$f_{max} = \frac{k'V_n^2 (V_{oh} - V_p)^2}{R_{on}^2 V_{oh} (V_p + V_n) (2V_{oh} - V_p + V_n)}. \quad (45b)$$

Using same parameters as type ‘B’, the oscillator was simulated using SPICE and Verilog-A models, both giving similar results. For further verification of the derived formulas, the oscillation frequency was tuned by sweeping R_a from $1\text{ k}\Omega$ to $12\text{ k}\Omega$. Both simulation results and the derived expression are plotted in Figure 8.

7. COMPARISON AND DISCUSSION

Table 2 shows a comparison between the three types of MRLO. For each type, two configurations that yield identical performance are possible, except that a different transfer function ($F(V_i)$) is required. The transfer function that has simpler implementation will determine the configuration of choice. For type ‘B’ and type ‘C’, the transition resistances do not depend on the initial state of the memristor, thus the oscillation condition and the oscillation frequency are independent of the memristor initial resistance. However, for type ‘A’ the transition resistances, and consequently the oscillation frequency, depend on the sum of memristor initial resistances. Dependence on initial resistances may be considered as a disadvantage. However, this can also be considered as an additional degree of freedom to control the frequency of oscillation. An external circuit can be used to adjust the initial resistances of the memristors and thus tune the oscillation frequency. One important note for type ‘A’ is that the sum of the two memristor resistances is always constant. Thus, the magnitude of the current flowing through them is constant as well, while its polarity depends on the output voltage. This can be an advantage while designing $F(V_i)$ on the circuit level.

In addition to tuning the frequency of oscillation, the oscillation range can be also tuned. Figure 9 shows a comparison of the minimum and maximum oscillation frequencies for the three types of MRLO using V_p as a tuning parameter. For the values of V_p and V_n used in this comparison, type ‘A’ provides

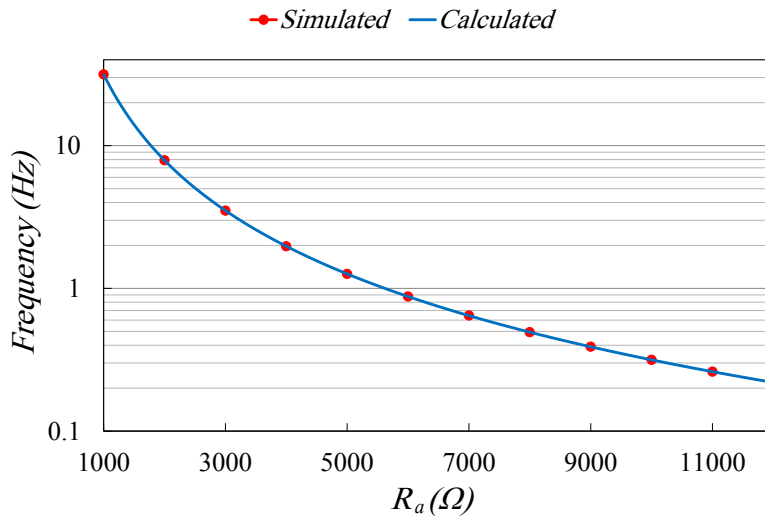


Figure 8: Tuning curve for the oscillation frequency of type ‘C’ using (44) and circuit simulation on Cadence Spectre. Parameters used are the same as in Figure 3

Table 2: Comparison between the different types of MRLOs family.

	Type A	Type B	Type C
First element (E_1)	<i>Memristor</i>	<i>Memristor</i>	<i>Resistor</i>
Second element (E_2)	<i>Memristor</i>	<i>Resistor</i>	<i>Memristor</i>
Depends on initial condition	<i>Yes</i>	<i>No</i>	<i>No</i>
Constant current	<i>Yes</i>	<i>No</i>	<i>No</i>
Oscillation frequency	$\frac{k'V_{oh}^2}{2(V_p+V_n)(R_{ai}+R_{bi})^2}$	$\frac{k'V_n^2V_p^2}{R_a^2V_{oh}(V_p^2-V_n^2)}$	$\frac{k'(V_{oh}-V_p)^2(V_{oh}+V_n)^2}{R_a^2V_{oh}(V_p+V_n)(2V_{oh}-V_p+V_n)}$
Minimum frequency	$\frac{k'\max(V_p^2,(V_{oh}+V_n)^2)}{2R_{off}^2(V_p+V_n)}$	$\frac{k'V_p^2(V_{oh}+V_n)^2}{R_{off}^2V_{oh}(V_p^2-V_n^2)}$	$\frac{k'V_p^2(V_{oh}+V_n)^2}{R_{off}^2V_{oh}(V_p+V_n)(2V_{oh}-V_p+V_n)}$
Maximum frequency	$\frac{k'\min(V_n^2,(V_{oh}-V_p)^2)}{2R_{on}^2(V_p+V_n)}$	$\frac{k'V_n^2(V_{oh}-V_p)^2}{R_{on}^2V_{oh}(V_p^2-V_n^2)}$	$\frac{k'V_n^2(V_{oh}-V_p)^2}{R_{on}^2V_{oh}(V_p+V_n)(2V_{oh}-V_p+V_n)}$
Oscillation condition 1	$R_{on,i} < R_{m,i} < R_{off,i}$		
Oscillation condition 2*	$(-1)^l V_p V_{ol} > (-1)^l V_n V_{oh}$		

* l equals '1' for positive transfer function and '-1' for negative transfer function.

the highest maximum frequency. This is not always the case, as the speed of the oscillator depends on the rate of change of the memristor resistance, which in turn depends on the voltage drop across the memristor. The voltage drop across the memristor depends on the choice of V_p and V_n and the circuit configuration. To further illustrate the effect of V_p and V_n , a plot showing the type of MRLO giving the highest oscillation frequency in the $(V_p, |V_n|)$ plane is shown in Figure 10, where positive configuration

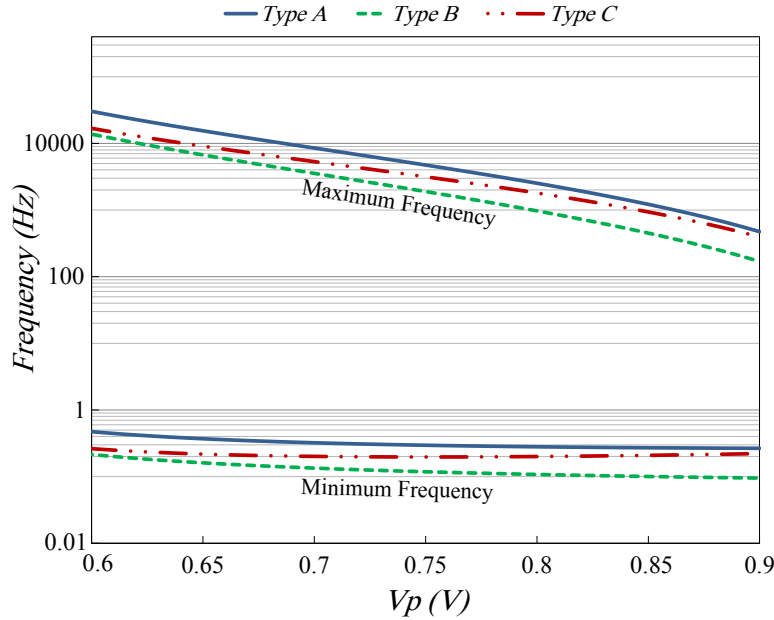


Figure 9: A Comparison of the maximum and minimum frequencies of the three types of MRLO family. Where $R_{ai} = R_{bi} = 3k\Omega$ and other device and circuit parameters are the same as in Figure 3. For type 'B' and type 'C', R_a is selected to be equal to $(R_{ai}+R_{bi})/2$ of type 'A'.

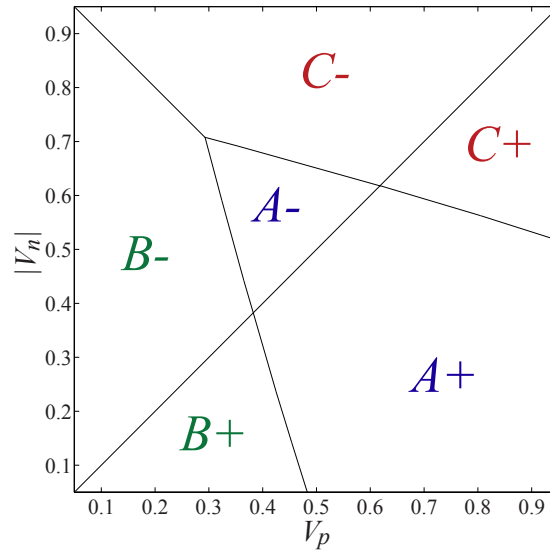


Figure 10: A plot showing regions of operation where each type of MRLO can provide the highest maximum oscillation frequency, where the ‘+’ and ‘-’ subscripts refer to positive and negative configurations respectively.

is used for the area of $V_p > |V_n|$ while the negative one is used elsewhere. The three presented types of MRLO can be used as a voltage controlled oscillator (VCO). The control voltage can be directly applied to one of the voltage parameters that control the oscillation frequency, e.g., V_p and V_n . Alternatively, the resistance R_a can be implemented as a voltage controlled resistance (VCR) for types ‘B’ and ‘C’.

The other main parameter controlling the oscillation frequency is the speed of the memristor device itself, which is modeled by the memristor constant k' . Figure 11 shows that the oscillation frequency increases linearly as the memristor constant increases. Very High oscillation frequencies can be achieved using recently introduced fast memristors [33–35]. However, slower memristors have their useful domain of applications as mentioned in Section 1.

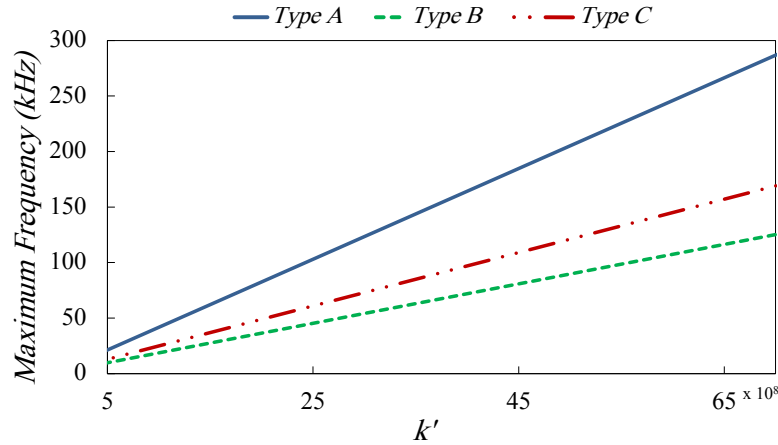


Figure 11: Maximum frequency of the three types of MRLO versus the memristor constant (k') at $V_p = 0.65$. Where $R_{ai} = R_{bi} = 3 \text{ k}\Omega$ and other device and circuit parameters are the same as in Figure 3. For type ‘B’ and type ‘C’, R_a is selected to be equal to $(R_{ai} + R_{bi})/2$ of type ‘A’.

8. EXPERIMENTAL RESULTS

In this section, we present experimental results for the MRLO circuit. The circuit uses a memristor device which was recently fabricated in KAUST local nanofabrication facility. The fabricated device is faster than the original HP device used in our simulations and hence, we are achieving faster oscillation frequencies compared to the simulated circuit. Despite our device's superior performance, we have consistently used the HP device model in this paper since full parameter extraction and model generation for our newly fabricated devices are not complete at the time of submission of this manuscript.

Our memristor devices were fabricated on n-type $\langle 100 \rangle$ silicon wafers with resistivity 10-20 Ohm-cm. After thermal oxidation of the wafer for electrical isolation, the bottom electrode stack of 200 Å Ti/1000 Å Pt was deposited via physical vapor deposition (PVD) and patterned with conventional contact lithography using heated aqua regia based wet etch. Photoresist strip and dilute HF surface treatment preceded 130 Å TiO_2 dielectric deposition in an Oxford FlexAL atomic layer deposition (ALD) reactor using Titanium Isopropoxide precursor and remote Oxygen plasma. Contact lithography was again employed to create a 200 Å Ti/1000 Å Pt top electrode via liftoff. Figures 12a and 12b Show SEM (Scanning Electron Microscope) photos for one of the fabricated memristor devices and its cross section respectively. The active layer of the device (TiO_2) is sandwiched between the two platinum electrodes at their intersection, as marked in the figures. A brief etch in HF diluted 50:1 in water was used to highlight the TiO_2 layer and other interfaces in the cross section SEM. Top and bottom platinum electrodes have intersecting fingers of $100 \mu m$ width. The fabricated devices were screened using a Keithley SCS-4200 parameter analyzer without any additional anneals or forming steps. Figure 12c shows the measured hysteresis of the device using a DC dual voltage sweep from 2 V to -2 V and back with 10 mA compliance current.

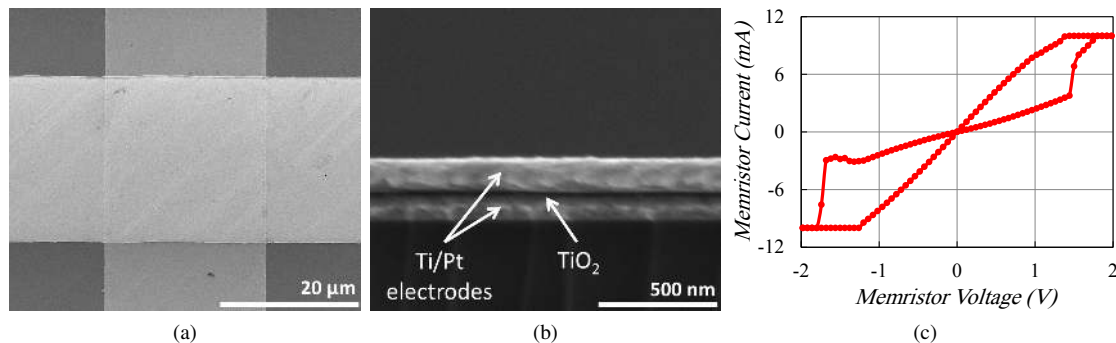


Figure 12: Fabricated memristor device (a) SEM, (b) cross-section SEM, and (c) I-V hysteresis.

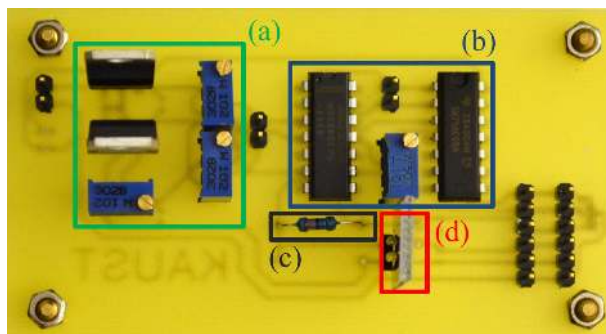


Figure 13: Snapshot of the oscillator PCB. (a) Voltage regulators and voltage dividers. (b) Window function circuit made of two comparators and an AND gate. (c) Resistor $R_b = 560k\Omega$. (d) Memristor die connected to the PCB.

MRLO Type ‘C’ circuit was built using off-the-shelf discrete electronic components mounted on a PCB, as shown in Figure 13. The window comparator is built using two comparators and an AND gate. We used voltage regulators to supply $V_{oh} = 2.5V$ and $V_{ol} = -2.5V$. V_p and V_n were set using voltage dividers since they are not driving any loads. The same circuit can be used to build any of the MRLO family members.

Figure 14a shows the measured response of the window transfer function to a ramp waveform. The transfer function is tested with a ramp of $200kHz$, which is in the same order of the oscillation frequency we got from the circuit. The measured square wave output of the oscillator is shown in Figure 14. The oscilloscope snapshot shows that the circuit frequency of oscillation $\approx 151kHz$. This frequency is achieved at $V_p = V_{REF} + 0.9V$ and $V_n = V_{REF} - 0.6V$.

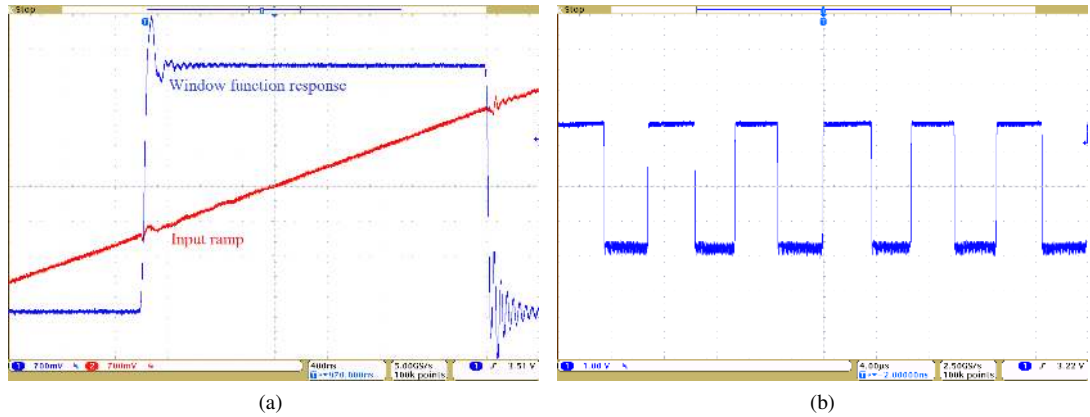


Figure 14: Measurement results of (a) the window function circuit response to a ramp input and (b) square wave output of the implemented MRLO circuit.

9. CONCLUSION

A family of MRLO oscillators that can be implemented without capacitors or inductors was presented. The proposed oscillators use one or two memristors instead of reactive elements. Types ‘A’, ‘B’, and ‘C’ of the MRLO family were analyzed and simulated. Comparison between derived expressions and simulation results shows an excellent match. Type ‘A’ has a constant current magnitude advantage, but it depends on the initial state of the memristors. Types ‘B’ and ‘C’ do not depend on the initial conditions, but a resistor is required. The three types can be used as a VCO and can offer a substantial area advantage over traditional oscillators in the low frequency range. The physical realization and measurement results of a type ‘C’ MRLO was also introduced. Advancement and research in the memristor area will allow more applications with improved performance.

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References

- [1] L. Chua, “Memristor-the missing circuit element,” *IEEE Transactions on Circuit Theory*, vol. 18, no. 5, pp. 507–519, 1971.

- [2] L. Chua and S. M. Kang, "Memristive devices and systems," *Proceedings of the IEEE*, vol. 64, no. 2, pp. 209–223, 1976.
- [3] T. Prodromakis, C. Toumazou, and L. Chua, "Two centuries of memristors," *Nature Materials*, vol. 11, no. 6, pp. 478–481, 2012.
- [4] A. Beck, J. Bednorz, C. Gerber, C. Rossel, and D. Widmer, "Reproducible switching effect in thin oxide films for memory applications," *Applied Physics Letters*, vol. 77, no. 1, pp. 139–141, 2000.
- [5] J. Kriegerand and S. Spitzer, "Non-traditional, non-volatile memory based on switching and retention phenomena in polymeric thin films," in *Non-Volatile Memory Technology Symposium*, 2004, pp. 121–124.
- [6] S. Genrikh, C. Cho, I. Yoo, E. Lee, S. Cho, C. Moon *et al.*, "Electrode structure having at least two oxide layers and non-volatile memory device having the same," *US Patent 7,417,271*, 2008.
- [7] D. B. Strukov, G. S. Snider, D. R. Stewart, and R. S. Williams, "The missing memristor found," *Nature*, vol. 435, pp. 80–83, 2008.
- [8] R. Tetzlaff and T. Schmidt, "Memristors and memristive circuits-an overview," in *IEEE International Symposium on Circuits and Systems (ISCAS'12)*, 2012, pp. 1590–1595.
- [9] P. Mazumder, S. Kang, and R. Waser, "Memristors: Devices, models, and applications," *Proceedings of the IEEE*, vol. 100, no. 6, pp. 1911–1919, 2012.
- [10] F. Corinto, A. Ascoli, and M. Gilli, "Nonlinear dynamics of memristor oscillators," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 58, no. 6, pp. 1323–1336, 2011.
- [11] —, "Memristive based oscillatory associative and dynamic memories," in *International Workshop on Cellular Nanoscale Networks and Their Applications (CNNA'12)*, 2010, pp. 1–6.
- [12] Y. Ho, G. Huang, and P. Li, "Dynamical properties and design analysis for nonvolatile memristor memories," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 58, no. 4, pp. 724–736, 2011.
- [13] S. H. Jo, K.-H. Kim, and W. Lu, "High-density crossbar arrays based on a si memristive system," *Nano Letters*, vol. 9, no. 2, pp. 870–874, 2009.
- [14] M. A. Zidan, H. A. H. Fahmy, M. M. Hussain, and K. N. Salama, "Memristor-based memory: The sneak paths problem and solutions," *Microelectronics Journal*, vol. 44, no. 2, pp. 176–183, 2012.
- [15] K. Eshraghian, K. Cho, O. Kavehei, S. Kang, D. Abbott, and S. Kang, "Memristor MOS content addressable memory (MCAM): hybrid architecture for future high performance search engines," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 19, no. 8, pp. 1407–1417, 2011.
- [16] F. Corinto, A. Ascoli, and M. Gilli, "Analysis of current-voltage characteristics for memristive elements in pattern recognition systems," *International Journal of Circuit Theory and Applications*, 2012, <http://dx.doi.org/10.1002/cta.1804>.
- [17] —, "Class of all iv dynamics for memristive elements in pattern recognition systems," in *The International Joint Conference on Neural Networks (IJCNN'11)*, 2011, pp. 2289–2296.
- [18] Y. V. Pershin and M. Di Ventra, "Solving mazes with memristors: A massively parallel approach," *Physical Review E*, vol. 84, p. 046703, 2011.
- [19] P. Lugli, A. Mahmoud, G. Csaba, M. Algasinger, M. Stutzmann, and U. Rührmair, "Physical unclonable functions based on crossbar arrays for cryptographic applications," *International Journal of Circuit Theory and Applications*, 2012, <http://dx.doi.org/10.1002/cta.1825>.

- [20] Q. Xia, W. Robinett, M. W. Cumbie, N. Banerjee, T. J. Cardinali, J. J. Yang, W. Wu, X. Li, W. M. Tong, D. B. Strukov, G. S. Snider, G. Medeiros-Ribeiro, and R. S. Williams, "Memristor-cmos hybrid integrated circuits for reconfigurable logic," *Nano Letters*, vol. 9, no. 10, pp. 3640–3645, 2009.
- [21] L. O. Chua and C.-W. Tseng, "A memristive circuit model for p-n junction diodes," *International Journal of Circuit Theory and Applications*, vol. 2, no. 4, pp. 367–389, 1974.
- [22] Y. Pershin and M. Di Ventra, "Practical approach to programmable analog circuits with memristors," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 57, no. 8, pp. 1857–1864, 2010.
- [23] S. Shin, K. Kim, and S. M. Kang, "Memristor applications for programmable analog ICs," *IEEE Transactions on Nanotechnology*, vol. 10, no. 2, pp. 266–274, 2011.
- [24] Y. Pershin and M. Di Ventra, "Memristive circuits simulate memcapacitors and meminductors," *Electronics Letters*, vol. 46, no. 7, pp. 517–518, 2010.
- [25] A. Sedra and K. Smith, *Microelectronic Circuits*. Oxford University Press, USA, 1997.
- [26] D. Chattopadhyay, *Electronics (fundamentals And Applications)*. New Age International, 2006.
- [27] A. Hajimiri, S. Limotyrakis, and T. Lee, "Jitter and phase noise in ring oscillators," *IEEE Journal of Solid-State Circuits*, vol. 34, no. 6, pp. 790–804, 1999.
- [28] A. Talukdar, A. G. Radwan, and K. N. Salama, "Generalized model for memristor-based wien family oscillators," *Microelectronics Journal*, vol. 42, no. 9, pp. 1032–1038, 2011.
- [29] —, "Non linear dynamics of memristor based 3rd order oscillatory system," *Microelectronics Journal*, vol. 43, no. 3, pp. 169–175, 2012.
- [30] —, "Time domain oscillating poles: Stability redefined in memristor based wien-oscillators," *IEEE International Conference on Microelectronics (ICM'10)*, pp. 288–291, December 2010.
- [31] A. Elwakil and S. Ozoguz, "A low frequency oscillator structure," in *European Conference on Circuit Theory and Design (ECCTD'09)*, August 2009, pp. 588–590.
- [32] C. Hwang, S. Bibyk, M. Ismail, and B. Lohiser, "A very low frequency, micropower, low voltage CMOS oscillator for noncardiac pacemakers," *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications*, vol. 42, no. 11, pp. 962–966, 1995.
- [33] A. Torrezan, J. Strachan, G. Medeiros-Ribeiro, and R. Williams, "Sub-nanosecond switching of a tantalum oxide memristor," *Nanotechnology*, vol. 22, no. 48, p. 485203, 2011.
- [34] J. Strachan, A. Torrezan, G. Medeiros-Ribeiro, and R. Williams, "Measuring the switching dynamics and energy efficiency of tantalum oxide memristors," *Nanotechnology*, vol. 22, no. 50, p. 505402, 2011.
- [35] F. Miao, J. Strachan, J. Yang, M. Zhang, I. Goldfarb, A. Torrezan, P. Eschbach, R. Kelley, G. Medeiros-Ribeiro, and R. Williams, "Anatomy of a nanoscale conduction channel reveals the mechanism of a high-performance memristor," *Advanced Materials*, vol. 23, no. 47, pp. 5633–5640, 2011.
- [36] A. G. Radwan, M. A. Zidan, and K. N. Salama, "HP memristor mathematical model for periodic signals and DC," in *IEEE International Midwest Symposium on Circuits and Systems (MWS-CAS'10)*, August 2010, pp. 861–864.

- [37] F. Corinto, A. Ascoli, and M. Gilli, "Mathematical models and circuit implementations of memristive systems," in *13th International Workshop on Cellular Nanoscale Networks and Their Applications (CNNA'12)*, 2012, pp. 1–6.
- [38] A. G. Radwan, M. A. Zidan, and K. N. Salama, "On the mathematical modeling of memristors," in *IEEE International Conference on Microelectronics (ICM'10)*, 2010, pp. 284–287.
- [39] K.-H. Jo, C.-M. Jung, K.-S. Min, and S.-M. Kang, "Self-adaptive write circuit for low-power and variation-tolerant memristors," *IEEE Transactions on Nanotechnology*, vol. 9, no. 6, pp. 675–678, 2010.
- [40] Z. Biolek, D. Biolek, and V. Biolkova, "Spice model of memristor with nonlinear dopant drift," *Radioengineering*, vol. 18, no. 2, pp. 210–214, 2009.
- [41] J. Valsa, D. Biolek, and Z. Biolek, "An analogue model of the memristor," *International Journal of Numerical Modelling: Electronic Networks, Devices and Fields*, vol. 24, no. 4, pp. 400–408, 2011.
- [42] T. Prodromakis, B. Peh, C. Papavassiliou, and C. Toumazou, "A versatile memristor model with nonlinear dopant kinetics," *IEEE transactions on electron devices*, vol. 58, no. 9, pp. 3099–3105, 2011.
- [43] F. Corinto and A. Ascoli, "A boundary condition-based approach to the modeling of memristor nanostructures," *IEEE Transactions on Circuits and Systems I*, vol. 59, no. 11, pp. 2713–2726, 2012.
- [44] F. Corinto, A. Ascoli, and M. Gilli, "Modeling dynamics of memristive nano-structures," in *EEE International Symposium on Circuits and Systems (ISCAS'12)*, 2012, pp. 1600–1603.
- [45] H. Abdalla and M. Pickett, "Spice modeling of memristors," in *IEEE International Symposium on Circuits and Systems (ISCAS'11)*, 2011, pp. 1832–1835.
- [46] S. Kvatinsky, E. Friedman, A. Kolodny, and U. Weiser, "Team: Threshold adaptive memristor model," *submitted to IEEE Transactions on Circuits and Systems I: Regular Papers*, 2012.
- [47] M. A. Zidan, A. G. Radwan, and K. N. Salama, "Memristor model," *Matlab Central*, May 2011. [Online]. Available: <http://www.mathworks.com/matlabcentral/fileexchange/31530>
- [48] M. A. Zidan, H. Omran, A. G. Radwan, and K. N. Salama, "Memristor-based reactance-less oscillator," *Electronics Letters*, vol. 47, no. 22, pp. 1220–1221, 2011.
- [49] M. A. Khatib, M. E. Fouda, A. G. Mosad, K. N. Salama, and A. G. Radwan, "Memristor-based relaxation oscillators using digital gates," in *Seventh International Conference on Computer Engineering & Systems (ICCES'12)*, 2012, pp. 98–102.
- [50] A. G. Mosad, M. E. Fouda, M. A. Khatib, K. N. Salama, and A. G. Radwan, "Improved memristor-based relaxation oscillator," *Microelectronics Journal*, 2013.
- [51] M. E. Fouda, A. G. Radwan, and K. N. Salama, "Effect of boundary on controlled memristor-based oscillator," in *International Conference on Engineering and Technology (ICET'12)*, 2012, pp. 1–5.