A Family of Neutral Point Clamped Full-Bridge Topologies for Transformerless Photovoltaic Grid-Tied Inverters

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***Abstract*—Transformerless inverter topologies have attracted more attentions in photovoltaic (PV) generation system since they feature high efficiency and low cost. In order to meet the safety requirement for transformerless grid-tied PV inverters, the leakage current has to be tackled carefully. Neutral point clamped (NPC) topology is an effective way to eliminate the leakage current. In this paper, two types of basic switching cells, the positive neutral point clamped cell and the negative neutral point clamped cell, are proposed to build NPC topologies, with a systematic method of topology generation given. A family of single-phase transformerless full-bridge topologies with low-leakage current for PV grid-tied NPC inverters is derived including the existing oH5 and some new topologies. A novel positive–negative NPC (PN-NPC) topology is analyzed in detail with operational modes and modulation strategy given. The power losses are compared among the oH5, the full-bridge inverter with dc bypass (FB-DCBP) topology, and the proposed PN-NPC topologies. A universal prototype for these three NPC-type topologies mentioned is built to evaluate the topologies at conversion efficiency and the leakage current characteristic. The PN-NPC topology proposed exhibits similar leakage current with the FB-DCBP, which is lower than that of the oH5 topology, and features higher efficiency than both the oH5 and the FB-DCBP topologies.**

***Index Terms*—Common-mode voltage, grid-tied inverter, leakage current, neutral point clamped inverter, photovoltaic (PV) generation system.**

I. Introduction

THE initial investment and generation cost of PV generation system are still too high compared with other renewable energy sources; thus, the efficiency improvement of grid-tied inverters is a significant effort to shorten the payback time and gain the economic benefits faster [1]–[6]. Transformerless grid-tied inverters, such as a full-bridge topology as shown in Fig. 1, have many advantages, e.g., higher efficiency, lower cost, smaller size, and weight. However, the common-mode voltage of v_{AN} and v_{BN} may induce a leakage current i_{Leakage} flowing through the loop consisting of the parasitic capacitors (C_{PV1} and C_{PV2}), the filters, the bridge, and the utility grid [7], [8]. In an isolated topology, the loop for the leakage current is broken by the transformer, and the leakage current is very low. But in a transformerless topology, the leakage current may be too high to induce serious safety [9] and radiated interference issues [8], [10]. Therefore, the leakage current must be limited within a reasonable margin.

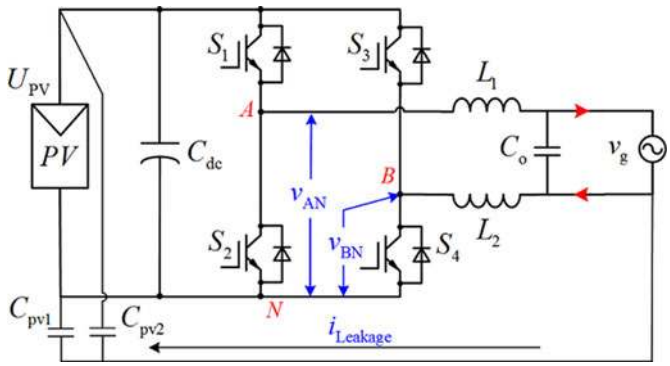

Fig. 1. Leakage current in a transfomerless grid-tied PV inverter.

The instantaneous common-mode voltage v_{CM} in the full-bridge topology shown in Fig. 1 is represented as follows [7], [10]–[12]:

$$v_{\mathrm{CM}} = 0.5(v_{AN} + v_{BN}) \tag{1}$$

where v_{AN} and v_{BN} are voltages from mid-point *A* and *B* of the bridge leg to terminal *N*, respectively.

In order to eliminate the leakage current, the common-mode voltage v_{CM} must be kept constant during all operation modes and many solutions have been proposed [7], [8], [10]–[22] as follows:

1) *Bipolar sinusoidal pulse width modulated (SPWM) full-bridge type inverter topologies.* The common-mode voltage of this inverter is kept constant during all operating modes [7], [13]. Thus, it features excellent leakage-current characteristics. However, both of the current ripples across the filter inductors and the switching losses are large.

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Therefore, the unipolar SPWM full-bridge inverters are attractive for its excellent differential mode characteristics such as higher dc-voltage utilization, smaller inductor current ripple and higher power efficiency.

2) *Improved unipolar SPWM full-bridge inverters.* The conventional unipolar SPWM full-bridge inverter is shown in Fig. 1. In the active modes, the common-mode voltage $v_{\rm CM}$ is equal to $0.5U_{\rm PV}$. In the freewheeling modes, $v_{\rm CM}$ is equal to $U_{\rm PV}$ or zero depending on the leg midpoints (point *A* and *B*) connected to the positive or negative terminal of the input. Therefore, the common-mode voltage of conventional unipolar SPWM full-bridge inverter varies at switching frequency, which leads to high-leakage current [7], [13].

To solve this problem, new freewheeling paths need to be built, and they should separate the PV array from the utility grid in freewheeling modes [10]. A solution named highly efficient and reliable inverter concept (HERIC) topology is proposed in [14]. In the freewheeling modes of HERIC inverter, the inductor current flowing through S_5 and S_6; thus, PV array is disconnected from the utility grid. And two extended HERIC topologies are proposed in [15] and [16], respectively. The disconnection can also be located on the dc side of the inverter, such as the H5 topology [17]. Although these topologies mentioned earlier feature the simple circuit structure, the common-mode voltage depends on both of the parasitic parameters of the leakage current loop and the voltage amplitude of the utility grid [18], which is not good for the leakage current reduction.

To eliminate the leakage current completely, the common-mode voltage $v_{\rm CM}$ should be clamped to half of the input voltage in the freewheeling mode to keep $v_{\rm CM}$ always constant [12], [19]. An example solution is oH5 topology [18], as shown in Fig. 2(a). A switch S_6 and a capacitor leg employed and S_6 turns on to let $v_{\rm CM} = 0.5U_{\rm PV}$ in the freewheeling mode. Unfortunately, there must be a dead time between the gate signals of S_5 and S_6 to prevent the input split capacitor $\rm C_{dc1}$ from shortcircuit. As a result, $v_{\rm CM}$ varies in the dead time, which still induces leakage current [18].

Full-bridge inverter with dc bypass (FB-DCBP) topology proposed in [7] is another solution, as given in Fig. 2(b). It exhibits no dead-time issue mentioned, and the leakage current suppression effect only depends on the turn-on speed of the independent diodes. But FB-DCBP suffers more conduction losses from the inductor current flowing through four switches in the active mode.

On the other hand, many power converters, such as dc–dc converters, voltage-source inverters, current-source inverters and multilevel inverters, have been investigated from the basic switching cells to constructing the topology [23]–[28]. Both of the oH5 topology and the FB-DCBP topology can be regarded as the transformerless gird-tied inverters with the same feature of neutral point clamped (NPC). However, these topologies have not yet been analyzed from the view of topological relationships and switching cells.

In this paper, a systematic method is proposed to generate transformerless grid-tied NPC inverter topologies from two basic switching cells based on the arrangement of the freewheeling routes. And a family of novel NPC inverters is derived with high efficiency and excellent leakage current performance. The paper is organized as follows. In Section II, an NPC switching cell concept is proposed with two basic cells, a positive neutral point clamped cell (P-NPCC) and a negative neutral point clamped cell (N-NPCC), respectively. A family of NPC topologies is generated from the two basic switching cells in Section III. In Section IV, one of the new topologies is analyzed in detail with operational principle, modulation strategy, and power loss comparison with oH5 and FB-DCBP given. Experimental results are presented in Section V, and Section VI concludes the paper.

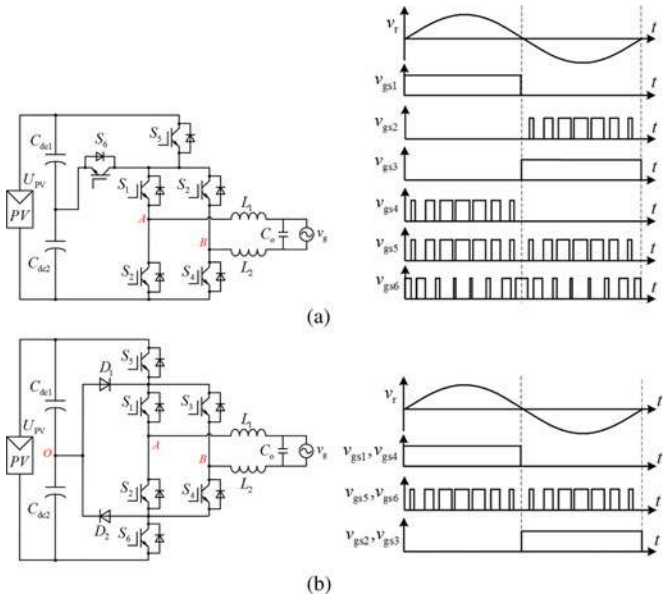

Fig. 2. Some of existing transformerless full-bridge inverter topologies. (a) oH5 [18]. (b) FB-DCBP [7].

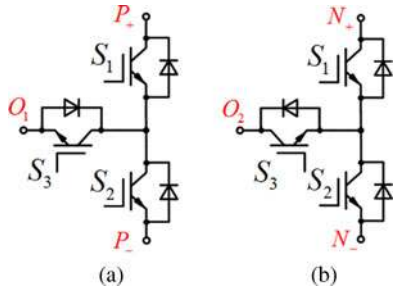

Fig. 3. Two basic NPC switching cells. (a) P-NPCC. (b) N-NPCC.

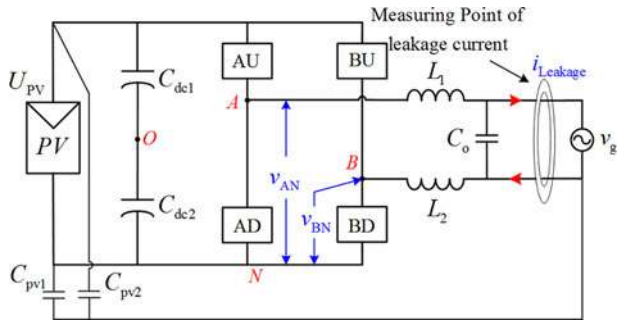

Fig. 4. Universal topology structure of single-phase transformerless full-bridge inverter.

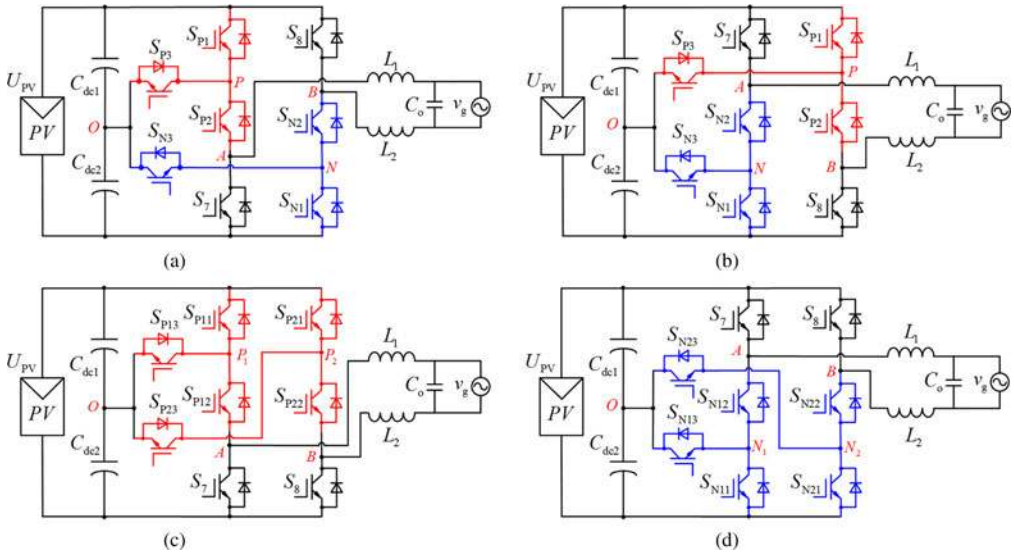

Fig. 5. A family of transformerless full-bridge NPC inverter topologies. (a) PN-NPC. (b) NP-NPC. (c) DP-NPC. (d) DN-NPC.

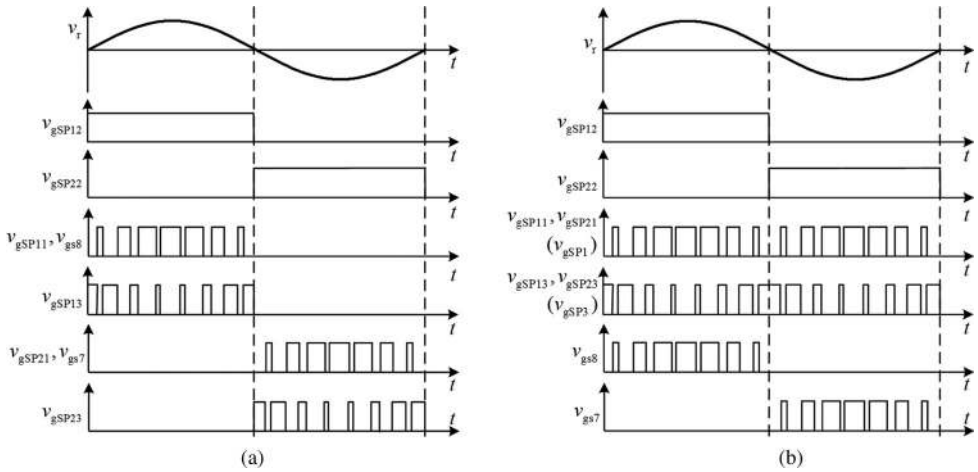

Fig. 6. Modulation strategies for DP-NPC. (a) Primary modulation according to the NPCC switching principle. (b) Improved modulation.

II. Idea of the NPCC

Based on the survey and analysis in Section I, the principles of leakage current elimination can be summarized as follows: 1) disconnect the PV array from the utility grid in the freewheeling modes with a switch; and 2) let the common-mode voltage equal to half of the input voltage in the freewheeling modes with another switch. As a result, two basic NPC switching cells are found with two extra switches mentioned earlier combined with the original power switch to be used to build inverters instead of the original power switch.

These two basic NPC switching cells, as shown in Fig.3, are defined as P-NPCC which the clamp switch S_3 connected to the mid-point of the bridge with its collector, and N-NPCC which the clamp switch S_3 connected to the mid-point of the bridge with its emitter. There are three terminals in both of P-NPCC and N-NPCC: (P_+) or (N_+), (P_-) or (N_-), and (O_1) or (O_2).

To build a NPC inverter topology with cells mentioned, the following rules should be followed.

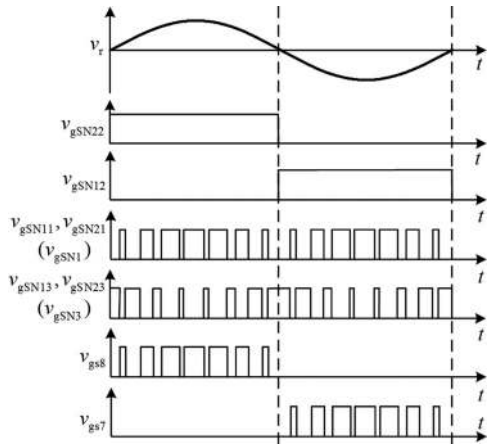

Fig. 7. Modulation strategies for DN-NPC.

Rule 1: Terminal (O_1) and (O_2) should be connected to the neutral point of the input split capacitors and the potential is

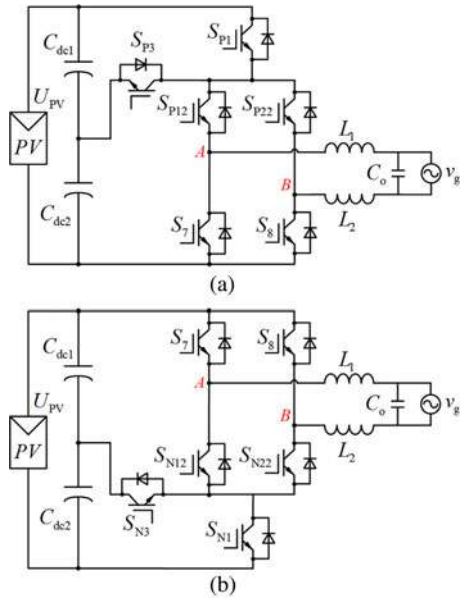

Fig. 8. oH5 topology proposed in [18]. (a) circuit A. (b) circuit B.

$v(O_1) = v(O_2) = 0.5U_{\rm PV}$. where $U_{\rm PV}$ is the voltage of PV array.

Rule 2: The P-NPCC has its (P_+) and (P_-) to be connected to the positive terminal of PV array and output filter inductor, respectively. On the other hand, the N-NPCC has its (N_-) and (N_+) to be connected to the negative terminal of PV array and output filter inductor, respectively.

Rule 3: One NPCC at least should appear in each bridge leg. Because we have to have three switches to separate grid from the PV array and still maintain the inductor current a loop during freewheeling mode.

III. NPC Transformerless Full-bridge Topologies Derived from NPCC

A. Family of Novel NPC Full-Bridge Inverters

The universal topology structure of a single-phase transformerless full-bridge inverter is shown in Fig. 4, where "AU," "AL," "BU," and "BL" are four leg switch modules of the full-bridge inverter, respectively.

Conventional single-phase full-bridge inverter topology employs single power switch in each switch module. If there is only one P-NPCC or one N-NPCC employed in the inverter, the purpose of disconnecting both the positive and negative terminals of PV array from the utility grid during the freewheeling period can not be achieved. Therefore, two NPCCs should be employed in phase A and phase B, respectively, the rest still employ the original power switches. As a result, a family of novel single-phase transformerless full-bridge NPC inverters is generated, as shown in Fig. 5.

Fig. 5(a) shows the topology in which modules "AU" and "BL" employ P-NPCC and N-NPCC, respectively. Thus, this topology is named as PN-NPC inverter topology. Fig. 5(b) shows the topology in which modules "AL" and "BU" employ N-NPCC and P-NPCC, respectively. So this topology is named as NP-NPC inverter topology. With the same principle, the dual P-NPCC (DP-NPC) and dual N-NPCC (DN-NPC) topologies are shown in Fig. 5(c) and (d), respectively.

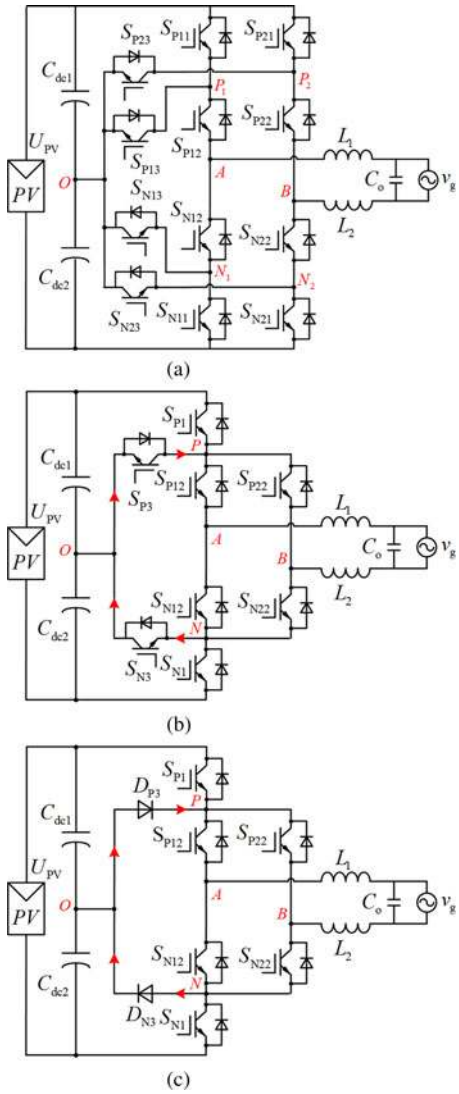

Fig. 9. Derivation of the FB-DCBP topology proposed in [7]. (a) DP&DN NPC. (b) simplified DP&DN NPC. (c) FB-DCBP.

B. oH5 Topology Generation

In Fig. 5(c) and (d), circuit structures of phase A and phase B are the same. Thus, some of the power switches could be merged. Take the topology shown in Fig. 5(c) as an example for analysis. During the positive half period of the utility grid, $S_{\rm P11}$ is turned ON in the active mode, while $S_{\rm P21}$ turned OFF, as shown in Fig. 6(a). Therefore, the potential of terminals (P_1), (P_2), and (O) can be obtained as

$$\begin{cases} v(P_1) = U_{\rm PV} \\ v(P_2) = v(O) = 0.5U_{\rm PV}. \end{cases} \tag{2}$$

If $S_{\rm P21}$ is turned ON in the active mode, the potential of terminals (P_1) and (P_2) are equal. Due to the blocking of antiparalleled diodes of $S_{\rm P22}$ and $S_{\rm P23}$, the topology can still operate

normally. Similarly, during the negative half period of the utility grid, $S_{\mathrm{P}11}$ and $S_{\mathrm{P}21}$ can be turned ON in the active mode. During the freewheeling, $S_{\mathrm{P}11}$ and $S_{\mathrm{P}21}$ are turned OFF, while $S_{\mathrm{P}13}$ and $S_{\mathrm{P}23}$ over the whole utility grid cycle. Therefore, $v(P_1) = v(P_2)$ is achieved.

According to the analysis above, with the improved modulation strategy shown in Fig. 6(b), the potential of terminals (P_1) and (P_2) are maintained at the same value whether in the active or freewheeling modes. That means terminals (P_1) and (P_2) can be connected directly. Then, $S_{\mathrm{P}11}$ is connected with $S_{\mathrm{P}21}$ in parallel, and $S_{\mathrm{P}13}$ connected with $S_{\mathrm{P}23}$ in parallel. The redundant switches are removed to simplify the circuit and as a result, the oH5 topology is generated, as shown in Fig. 8(a). To prevent input split capacitor $C_{\mathrm{dc}1}$ from shortcircuit, there must be a dead time between the drive signals of S_{P1} and S_{P2}. Moreover, if the improved modulation strategy shown in Fig. 7 is applied to DN-NPC topology, (N_1) and (N_2) can be connected directly. Then, another circuit structure of the oH5 topology is derived, as shown in Fig. 8(b), with the redundant power switches removed.

C. FB-DCBP Topology Generated

Fig. 9(a) shows the case where four NPCCs employed as all of the four switch modules. There are two P-NPCCs in "AU" and "BU", and two N-NPCCs in "AL" and "BL", respectively. According to the analysis in Section III-B, with an improved modulation strategy, the potentials of terminals (P_1) and (P_2), (N_1) and (N_2) are equal, respectively. Thus, (P_1) and (P_2), (N_1) and (N_2) can be connected directly. After the redundant switches are removed, a new topology is obtained, as shown in Fig. 9(b). Where S_{P1} and S_{N1} are turned ON in the active modes, while S_{P1} and S_{N1} are turned OFF in the freewheeling modes. Therefore, disconnection of PV array from utility grid during the freewheeling period is realized. Then, $\mathrm{S}_{\mathrm{N}22}$ is turned ON during the positive half-period of the utility grid, and $S_{\mathrm{N}12}$ is turned ON during the negative half-period of the utility grid. As a result, the potentials of terminals (*P*), (*N*), (*A*), and (*B*) are equal during the freewheeling period. If common-mode voltage v_{CM} is higher than that of the terminal (*O*) in the freewheeling modes, the clamping current flows through the antiparalleled diode of S_{N3} and the common-mode voltage v_{CM} is clamped to the half of input voltage. On the other hand, the clamping current flows through the antiparalleled diode of S_{P3} when the common-mode voltage v_{CM} lower than that of the terminal (*O*). The common-mode voltage v_{CM} is clamped to the half of input voltage as well. Then, the switches S_{P3} and S_{N3} can be replaced by two diodes. The FB-DCBP topology is derived, as shown in Fig. 9(c).

IV. Analysis on the PN-NPC Topology and Comparison With Other NPC Topologies

To analyze the operation principle, the proposed PN-NPC topology is redrawn in Fig. 10.

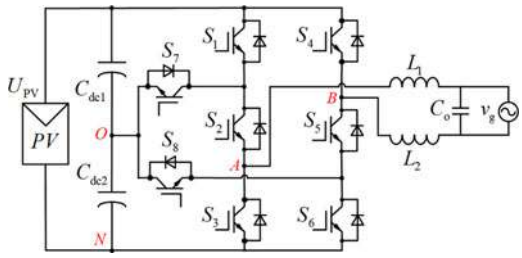

Fig. 10. Topology of the proposed PN-NPC.

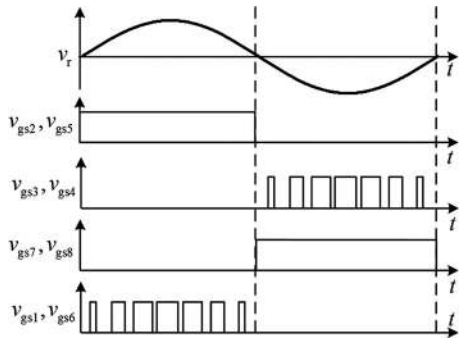

Fig. 11. Schematic of gate drive signals with unity power factor.

A. Operation Mode Analysis

Grid-tied PV systems usually operate with unity power factor. The waveforms of the gate drive signals for the proposed topology are shown in Fig. 11.

In Fig. 11, v_r is the output signal of inductor current regulator, also named as modulation signal. v_{gs1} to v_{gs8} represent the gate drive signals of power switches S_1–S_8, respectively.

There are four operation modes in each period of utility grid, as shown in Fig. 12.

In Fig. 12, v_{AN} is the voltage between terminal *A* and terminal *N*, and v_{BN} the voltage between terminal *B* and terminal *N*. v_{AB} is the differential-mode voltage of the topology, $v_{AB} = v_{AN} - v_{BN}$.

1) Mode I is the active mode in the positive half-period of the utility grid, as shown in Fig. 12(a). S_1, S_2, S_5 and S_6 are turned ON, and the other switches are turned OFF. $v_{AN} = U_{\mathrm{PV}}$ and $v_{BN} = 0$; thus, $v_{AB} = U_{\mathrm{PV}}$, and the common-mode voltage $v_{\mathrm{CM}} = (v_{AN} + v_{BN})/2 = 0.5U_{\mathrm{PV}}$.
2) Mode II is the freewheeling mode in the positive half period of the utility grid, as shown in Fig. 12(b). S_2 and S_5 are turned ON, the other switches are turned OFF. The inductor current flows through the antiparalleled diode of S_7 and S_8. $v_{AN} = 0.5U_{\mathrm{PV}}$ and $v_{BN} = 0.5U_{\mathrm{PV}}$; thus, $v_{AB} = 0$, and the common-mode voltage $v_{\mathrm{CM}} = (v_{AN} + v_{BN})/2 = 0.5U_{\mathrm{PV}}$.
3) Mode III is the active mode in the negative half-period of the utility grid, as shown in Fig. 12(c). S_3, S_4, S_7, and S_8 are turned ON, the other switches are turned OFF. Although S_7 and S_8 are turned ON, there is no inductor current flowing through these two switches. $v_{AN} = 0$ and $v_{BN} = U_{\mathrm{PV}}$; thus, $v_{AB} = -U_{\mathrm{PV}}$, and the common-mode voltage $v_{\mathrm{CM}} = (v_{AN} + v_{BN})/2 = 0.5U_{\mathrm{PV}}$.

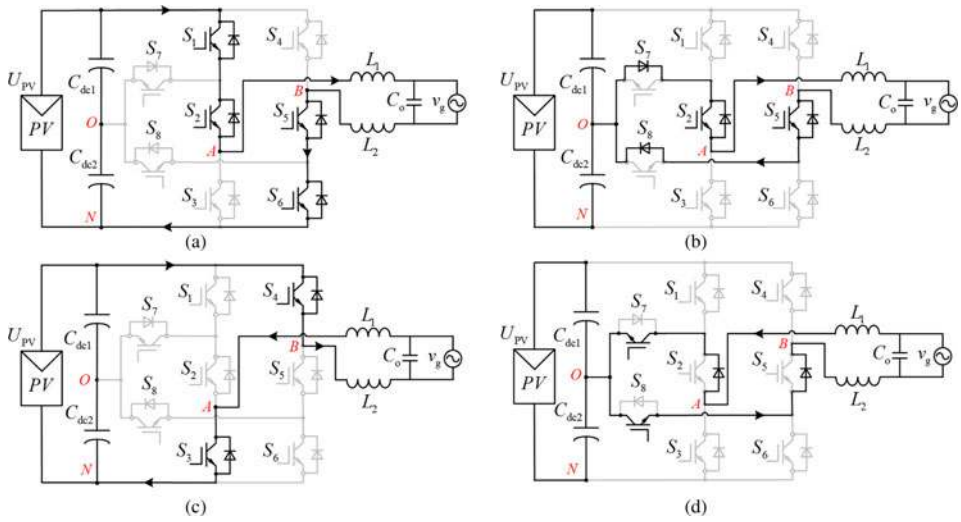

Fig. 12. Equivalent circuits of operation modes (a) Active mode in the positive half period. (b) Freewheeling mode in the positive half period. (c) Active mode in the negative half period. (d) Freewheeling mode in the negative half period.

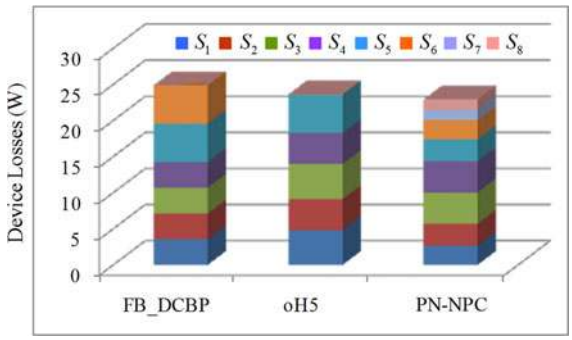

Fig. 13. Device losses distribution for NPC topologies with 1-kW power rating.

TABLE I
CALCULATED POWER LOSSES ON DEVICE

	S_1 (W)	S_2 (W)	S_3 (W)	S_4 (W)	S_5 (W)	S_6 (W)	S_7 (W)	S_8 (W)	Total losses(W)
FB-DCBP	3.562	3.562	3.562	3.562	5.315	5.315	0	0	24.878
oH5	4.833	4.316	4.833	4.316	5.315	0.039	0	0	23.652
PN-NPC	2.677	3.05	4.316	4.316	3.05	2.677	1.425	1.425	22.936

TABLE II
NUMBER OF POWER DEVICE COMPARISON

	FB-DCBP	oH5	PN-NPC
IGBT(1200V)	4	6	2
IGBT(600V)	2	0	6
Diode	2	0	0
Isolated driving power	5	5	6

4) Mode IV is the freewheeling mode in the negative half period of the utility grid, as shown in Fig. 12(d). S_7 and S_8 are turned ON, and the other switches are turned OFF. The inductor current flows through the antiparalleled diode of S_2 and S_5. $v_{AN} = 0.5U_{\rm PV}$, $v_{BN} = 0.5U_{\rm PV}$, thus, $v_{AB} = 0$, and the common-mode voltage $v_{\rm CM} = (v_{AN} + v_{BN})/2 = 0.5U_{\rm PV}$.

TABLE III
PARAMETERS OF THE EXPERIMENTAL PROTOTYPE

Parameter	Value
Rate power	1000 W
Input voltage	380~700 V
Switching frequency	20kHz
Filter inductor L_1, L_2	3mH
Filter Capacitor	0.47uF
Grid voltage/frequency	230V/50Hz
1200V IGBT	IRG4PH40U
600V IGBT	SGH40N60UFD
1000V Diode	MUR8100T
PV parasitic capacitor C_{PV1}, C_{PV2}	0.1uF

Based on the above analysis, the common-mode voltage $v_{\rm CM}$ of the proposed topology in each operation mode is unchanged, and equals to $0.5U_{\rm PV}$. Thus, the requirement for eliminating leakage current mentioned in Section II is fulfilled. Furthermore, the leakage current characteristic of this topology only depends on the turn-on speed of the antiparallel diodes of S_2, S_5, S_7, and S_8. Therefore, the leakage current characteristic of this topology is better than that of oH5 topology. The voltage stresses on S_3 and S_4 are equal to input voltage. The voltage stresses on S_1, S_2, S_5 to S_8 are the same, and equal to half input voltage.

B. Comparison of NPC Topologies

The calculated power losses on switches of the PN-NPC topology proposed, FB-DCBP topology [7] and oH5 topology [18], with the same parameters as that of the 1-kW prototypes given in Table III, are illustrated in Table I and Fig. 13. Both of the process and equations of the calculation mentioned

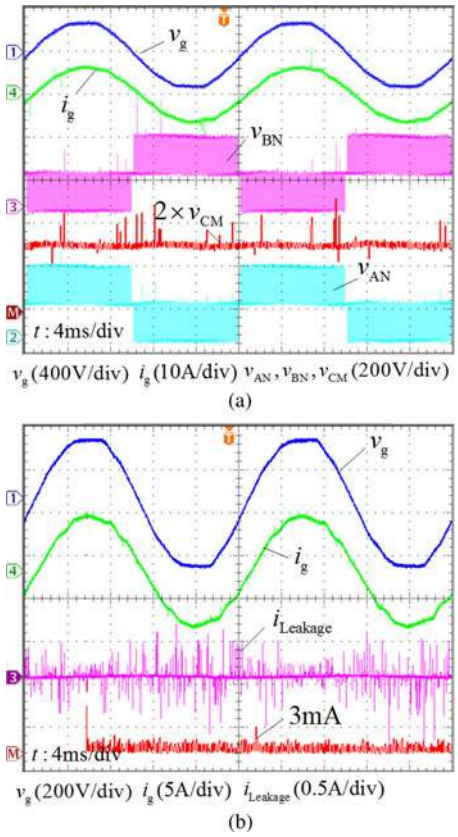

Fig. 14. Common-mode voltage and leakage current in FB-DCBP topology. (a) Common-mode voltage. (b) Leakage current.

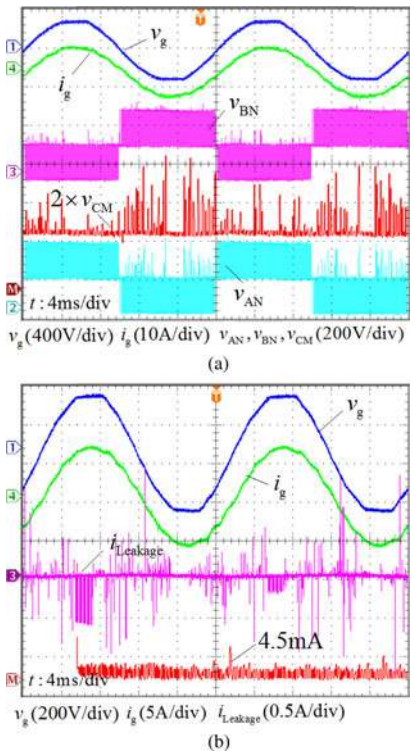

Fig. 15. Common-mode voltage and leakage current in oH5 topology. (a) Common-mode voltage. (b) Leakage current.

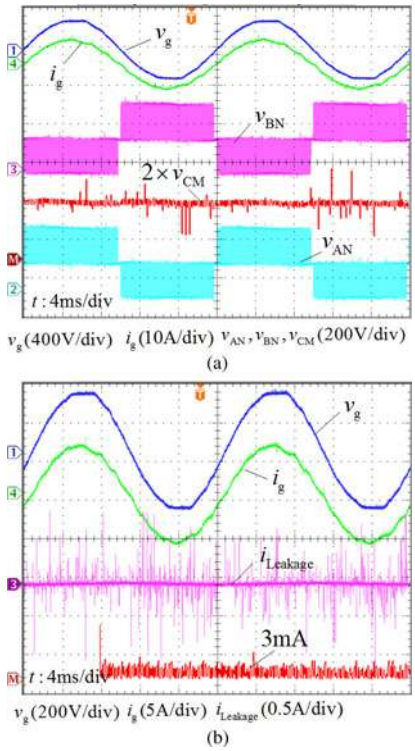

Fig. 16. Common-mode voltage and leakage current in PN-NPC topology. (a) Common-mode voltage. (b) Leakage current.

are according to [18], [29]–[32] and omitted in this paper. On the other hand, the inductor losses in the three topologies are the same due to the same v_{AB} modulation. The numbers of power devices and isolated driving power are summarized in Table II.

From Table II, Table III, and Fig. 13, it can be seen that the power losses in PN-NPC inverter is much lower than that in FB-DCBP because the voltage rating of some switches in PN-NPC topology are 600 V, half of that in FB-DCBP. The power loss in PN-NPC inverter is close to that in oH5 which with the least number of power device. However, PN-NPC inverter features lower leakage current than oH5 as analyzed above.

V. Experimental Results

A universal prototype of the three NPC topologies has been built up in order to verify the operation principle and compare their performances. The specifications of the NPC inverter topologies are listed in Table III. The control circuit is implemented based on a DSP chip TMS320F2808. The measure point of leakage current is shown in Fig. 4.

The common-mode voltage and the leakage current waveforms of these three topologies in unified experimental conditions are shown in Figs. 14–16, respectively. Where v_g and i_g are grid voltage and grid-tied current, respectively. v_{AN} and v_{BN} are voltages of mid-point A and B to terminal N, respectively. $v_{\rm CM}$ is the common-mode voltage, which equals to $0.5(v_{AN}+ v_{BN})$. $i_{\rm Leakage}$ is the leakage current. The tested leakage current of FB-DCBP, oH5, and PN-NPC inverter are 3 mA [see Fig. 14(b)], 4.5 mA [see Fig. 15(b)], and 3 mA [see Fig. 16(b)], respectively.

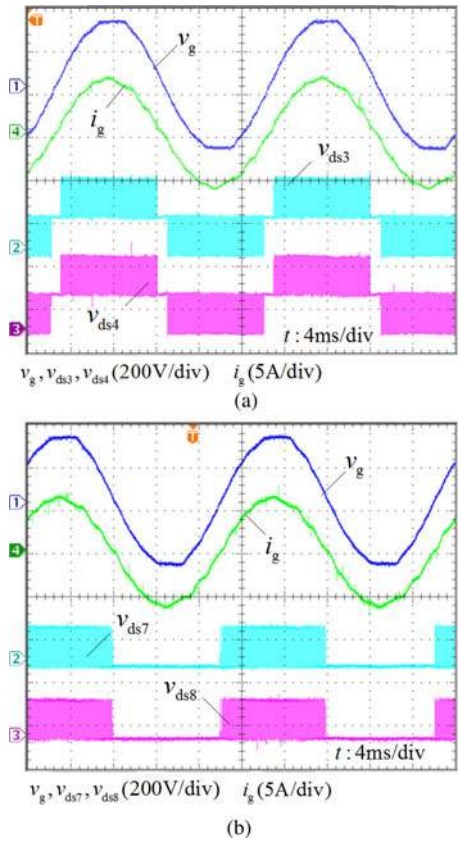

Fig. 17. Drain–source voltages in PN-NPC topology. (a) Voltage stress on S_3 and S_4. (b) Voltage stress on S_7 and S_8.

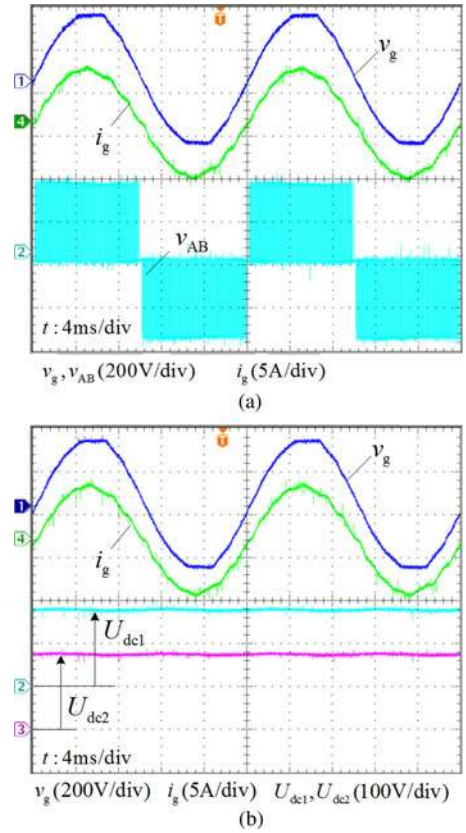

Fig. 18. Differential-mode characteristic of PN-NPC topology. (a) Differential-mode waveforms. (b) Capacitor divider voltage.

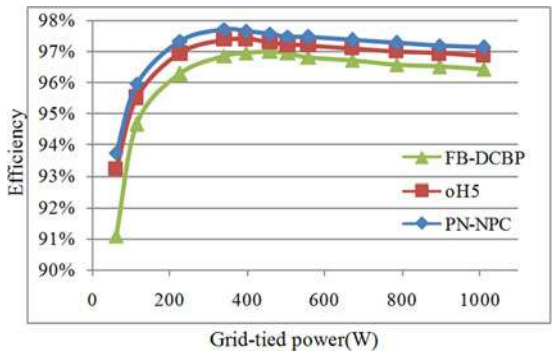

Fig. 19. Efficiency comparison of three NPC topologies.

Therefore, the leakage current of FB-DCBP and PN-NPC is the same, and less than that of oH5.

The drain–source voltage waveforms of switches in PN-NPC topology are shown in Fig. 17. where $v_{\rm ds3}$, $v_{\rm ds4}$, $v_{\rm ds7}$, and $v_{\rm ds8}$ are drain–source voltages of S_3, S_4, S_7, and S_8, respectively. It can be seen that the voltage stresses of all the switches shown in Fig. 17 are half of the input voltage. Furthermore, the maximum voltage stress on S_7 and S_8 are half of the input voltage. The experimental results are in accordance with the theoretical analysis well. Since PN-NPC topology uses more 600-V IGBT than the FB-DCBP topology, the conduction loss of the proposed PN-NPC topology is less.

Fig. 18 shows the differential-mode characteristic of the proposed PN-NPC topology, where v_{AB} is the differential-mode voltage. $U_{\rm dc1}$ and $U_{\rm dc2}$ are the voltages on the capacitors $C_{\rm dc1}$ and $C_{\rm dc2}$, respectively.

From Fig. 18(a), it can be seen that the output voltage v_{AB} has three levels as $U_{\rm PV}$, 0, and $-U_{\rm PV}$. It indicates that the PN-NPC topology proposed is modulated with unipolar SPWM, and features as excellent differential-mode characteristic as FB-DCBP and oH5 topologies under unipolar SPWM. Fig. 18(b) shows the mid-point voltage waveforms of $U_{\rm dc1}$ and $U_{\rm dc2}$. It can be seen that this voltage is well shared between these two divided capacitors.

Fig. 19 is the conversion efficiency comparison of these three NPC topologies. It is obvious that the efficiency of the proposed PN-NPC is the highest. The European efficiencies for FB-DCBP, oH5, and PN-NPC are 96.4%, 96.9%, and 97.2%, respectively. Experimental results show that the PN-NPC proposed topology has the same common-mode leakage current characteristic as that of FB-DCBP topology, and better than that of oH5 topology. Moreover, the power device loss of the PN-NPC topology is the lowest. Therefore, it could be a very good solution for single-phase transformerless grid-tied applications.

VI. Conclusion

In this paper, two basic switching cells, the P-NPCC, and the N-NPCC have been proposed for the grid-tied inverter topology generation to build NPC topologies. A systematic method of

the topology generation has been proposed. A family of single-phase transformerless full-bridge NPC inverter topologies with low leakage current based on the basic switching cell is derived. The PN-NPC topology proposed has the following advantages and evaluated by experimental results. 1) The common-mode voltage is clamped to a constant level, so the leakage current can be well suppressed effectively. 2) The excellent differential-mode characteristic is achieved like the isolated full-bridge inverter with uniploar SPWM. 3) The PN-NPC topology features the best conversion efficiency compared to that of oH5 and FB-DCBP.

The proposed NPC topologies also have the capability of injecting reactive power, which is a major advantage of future PV inverters. Therefore, the proposed NPC topology family is an attractive solution for transformerless grid-tied PV applications.

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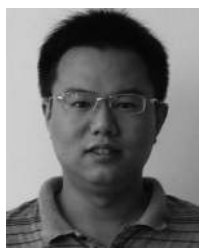

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