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A Family of Series-Resonant DC-DC Converter with Fault-Tolerance Capability

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***Abstract*—The Series-Resonant dc-dc converter (SRC) is widely applied in a large range of voltage and power. In most applications, fault tolerance is a highly desired feature and it is obtained through redundancy. This paper proposes a fault tolerance solution for the SRC, which could drastically reduce the need of redundancy. Using the proposed scheme, the full-bridge based SRC or multilevel based SRC can be reconfigured in a half-bridge topology, in order to keep the converter operational even with the failure (open circuit or short circuit) of one switch. Since the proposed scheme can be applied to the FB-SRC and multilevel SRC, then a family of fault-tolerant converter is proposed in this work. The advantage of the proposed approach are: minimum of additional hardware and no deterioration of the converter efficiency. The proposed fault tolerance solution was experimentally tested in a 10 kW SRC prototype with input voltage of 700 V to 600 V. A short-circuit fault in a semiconductor is tested and the results confirm the effectiveness of the proposed approach.**

***Index Terms*—Dc-dc converter, fault tolerance, multilevel topologies, reliability.**

I. Introduction

The series-resonant dc-dc converter (SRC) has been very used in a large range of voltage and power application. In some application, such as Smart Transformer [1], [2], telecommunication or even in renewable energy system, the continuity of operation is of paramount importance. For that reason, a highly reliable system (preferable with redundancies) is required. The fault tolerant feature contributes to increase the availability of system and several fault tolerance methods have been proposed in literature [3]–[6]. Most of these methods includes a significant amount of extra hardware (such as semiconductors/leg redundancy [3], [5] or series connection of fuses/switches to isolate the fault [3], [4], [6]), increasing the cost and compromising the efficiency of the system. In this context, this paper proposes a fault tolerance solution with minimum of additional hardware and no impact on efficiency for the SRC converter, using the advantage of inherent fault tolerant capability of this topology. The proposed fault tolerant solution has been briefly introduced in [7] for the unidirectional topology of the full-bridge converter and in this paper it is extended to the SRC based on multilevel topologies and also to the bidirectional version [8].

The generic scheme of the SRC is depicted in Fig. 1 and the primary side bridge can be implemented based on half-bridge, full-bridge or even multilevel topology, as those topologies presented in Fig. 2. The proposed fault tolerant scheme consists in re-configuring the full-bridge SRC (FB-SRC) or the multilevel SRC in a half-bridge SRC (HB-SRC) converter. Hence, the proposed approach can be applied to those topologies presented from Fig. 1 (c) to (f). Nevertheless, the output voltage generated by the HB-SRC is half of the output generated by the FB-SRC or the multilevel SRC, considering the same parameters (input voltage, transformer turn ratio and etc). Therefore, a re-configurable rectifier based on the voltage-doubler topology is used in order to keep the same output voltage. Finally, a family of series-resonant converters based on four different topologies is proposed in this paper. The operation principle of the HB-SRC, FB-SRC and multilevel SRC operating in discontinuous conduction mode (dcm) are presented in Section II. In Section III, the reconfiguration scheme is described in detail for each of the mentioned topologies. The re-configurable rectifier used on the proposed converters is introduced in section IV, and then the proposed fault tolerant converters based on the SRC are presented in this section. Finally, experimental results are provided in Section V, validating the theoretical analysis developed in this paper, and the conclusion is presented in Section VI.

II. Series-Resonant Converter: Topologies and Operation Principle

Fig. 1 shows the generic scheme of the SRC converter, while Fig. 2 shows possible topologies used to implement the SRC, that can be a half-bridge, full-bridge or even multilevel converter configurations. More specifically, the feasible topologies to be used as an active bridge in the primary side are: half-bridge with dc output (HBdc-SRC, Fig. 2 (a)), classic half-bridge (HB-SRC) with ac output (Fig. 2 (b)), full-bridge (FB-SRC, Fig. 2 (c)), flying-capacitor (FC-SRC, Fig. 2 (d)), 3-level converter (3L-SRC, Fig. 2 (e)) and finally the neural-point-clamped (NPC-SRC, Fig. 2 (f)). As a matter of nomenclature, the topologies based on two switches (Half-Bridges Fig. 2 (a) and (b)) are defined as basic topologies, while the topologies

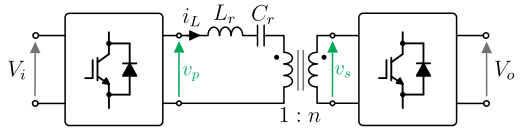

Figure 1. Topology of the series resonant dc-dc converter.

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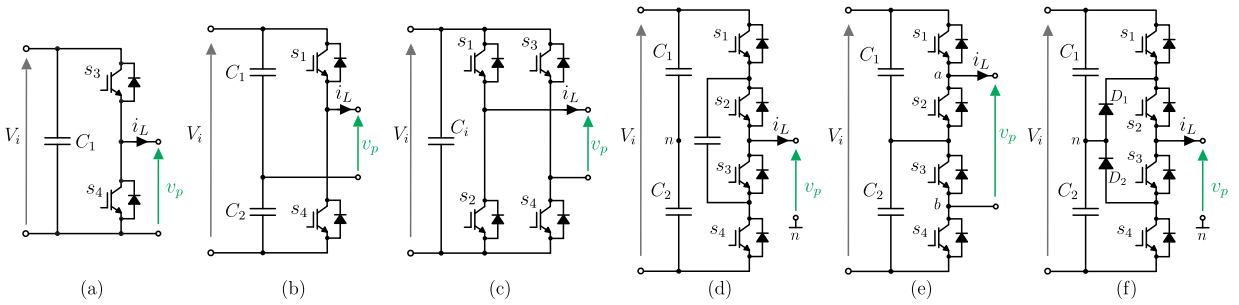

Figure 2. Possible topologies used to implement the active bridges of the series-resonant converter: (a) half-bridge with dc with dc output (HBdc-SRC), (b) classic half-bridge (HB-SRC) with ac output, (c) full-bridge (FB- SRC), (d) flying-capacitor (FC-SRC), (e) 3-level topology (3L-SRC) and (f) neural-point-clamped (NPC-SRC).

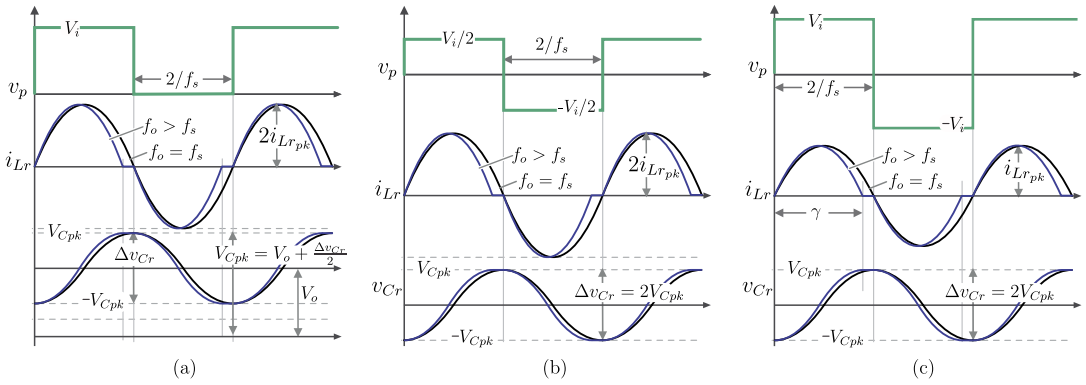

Figure 3. Main waveforms of the SRC for the different topologies implementation: (a) HBdc-SRC, (b) HB-SRC and multilevel topologies (FC-SRC, 3L-SRC, NPC-SRC), (c) FB-SRC.

based on four switches (FB Fig. 2 (a) and multilevel Fig. 2 (d) to (e)) are defined as reconfigurable topologies.

Although the multilevel converters or even the FB-SRC can work with 3 level modulation (creating a v_p voltage with 3 levels), the 2 level modulation is very beneficial, because it combines the advantages of the SRC converter, that are: high efficiency, well regulated output voltage, low EMI emission (reduced di/dt), with the advantage of the multilevel structure of reducing the voltage effort across the semiconductors. Therefore, the 2 level modulation is used in this work for the FB-SRC and multilevel SRC and the main waveforms for these converters are depicted in Fig. 3 (c).

A. FB-SRC and Multilevel SRC

The FB-SRC and Multilevel SRC operates with 2 level modulation, generating then a 2 level square waveforms v_p on the resonant tank circuit with magnitude varying from V_i to $-V_i$, as depicted in Fig. 3 (c), where V_i is the dc value of the input source. It is desired that the converter operates with switching frequency equal to the resonant frequency, given by (1), ($f_s = f_o$), or slightly above ($f_s > f_o$) [9], [10]. In that condition, the converter will operates with zero-voltage-switching (ZVS) on the primary side and zero-current-switching (ZCS) on the secondary side. For $f_s = f_o$, the resonant inductor current i_{Lr} and resonant capacitor voltage v_{Cr} fully resonate, resulting in pure sinusoidal waveforms. In case of $f_s > f_o$, the inductor current reaches zero before half of the switching period, and it remains zero until the primary bridge applies negative output voltage $v_p = -V_i$. Since the commutations take place when $i_{Lr} = 0$, all semiconductors switch at ZCS. The main waveforms for both operation point are shown in Fig. 3 (c). In these operation modes, the converter works with unity gain and, then the output voltage is given by (2).

$$f_s = f_0 = \frac{1}{2\pi\sqrt{L_r C_r}} \tag{1}$$

$$V_o = n \cdot V_i \tag{2}$$

B. HB-SRC and HBdc-SRC

Similarly to FB-SRC, the HB-SRC (Fig. 2 (b)) generates an ac square waveforms v_p on the resonant tank circuit, but in this case the magnitude varies from $V_i/2$ to $-V_i/2$, because of the half-bridge configuration. Consequently, the inductor current will be the double compared to the FB configuration, if the same amount of power is processed. The main waveform for this converter is shown in Fig. 3 (b), in which a similar operation to the FB-SRC is observed. The output voltage of the HB-SRC is given by (3). As it can be seen, the output voltage of the HB-SRC is half of the value, when compared to the FB-SRC output voltage (see (2)) for the same parameters (V_i and n).

$$V_o = n \cdot \frac{V_i}{2} \tag{3}$$

Differently from the FB-SRC and HB-SRC, the HBdc-SRC (Fig. 2 (b)) generates a dc waveforms voltage v_p on the tank circuit input, with zero and positive values (0, V_i). As

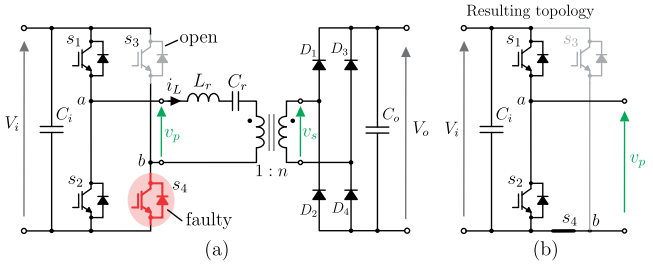

Figure 4. (a) FB-SRC under faulty condition: SC failure on the semiconductor s_4, (b) resulting topology after the reconfiguration of the FB-SRC.

a consequence of this dc voltage, the resonant tank voltage will have an dc value given by V_o. Similarly to the HB-SRC, the output voltage of the HBdc-SRC is defined by (3) and its inductor current is twice, when compared to the FB configuration for the case of same power processing.

III. Proposed Fault Tolerance Approach

Depending on the semiconductors failure mechanisms, the device will assume two possible states: open-circuit (OC) or short-circuit (SC) [11]. For voltage source converter, which is the case of the SRC, the OC fault is not catastrophic, since the power transfer will be naturally interrupted. Instead, the SC fault is the main issue, because it can cause destructive damage to the power converter. In addition, the SC failure type is mostly likely to happen in the real application than the OC failure. The proposed approach can be applied for both cases, but this work is focused on the SC fault, in which the theoretical analysis will be carried out.

A. Reconfiguration Scheme: Full-Bridge SRC

The proposed reconfiguration scheme for the SRC consists in configuring the FB-SRC in a HB-SRC after the fault, i.e. SC of a semiconductor. The detailed analysis is carried out in this section for the FB-SRC shown in Fig. 2 (c).

Initially, as an example, it is assumed that the switch s_4 is damaged in SC, as depicted in Fig. 4 (a), and hence the switch s_3 must remain open, avoiding short-circuit of the input voltage source. Since the switch s_4 is short-circuited, the point b highlighted in Fig. 4 (a) is directly connected to the primary side ground and the damaged device is used as a circuit path, resulting in the circuit shown in Fig. 4 (b). Meanwhile, the healthy leg (composed of s_1 and s_2) operates normally. As can be noticed, the resulting circuit after the fault (see Fig. 4 (b)) is the same HBdc shown in Fig. 2 (a). Hence, the FB-SRC operates as a HBdc-SRC after the semiconductor fault. Fig. 5 shows the operation states of the SRC after the fault, i.e. after the reconfiguration, where it can be seen that the damaged switch s_4 being used as a circuit path.

B. 3-Level SRC

As mentioned before, the proposed fault tolerant scheme can also be applied to those multilevel topologies depicted in Fig. 2 (d) to (f) and this section the proposed approach is described for the 3-Level topology (Fig. 2 (e)).

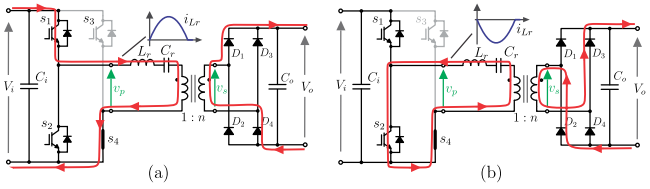

Figure 5. Operation of the FB-SRC as a HBdc-SRC after the reconfiguration. States operation of the SRC after the fault: (a) positive i_L current (first state), (b) negative i_L current(second state).

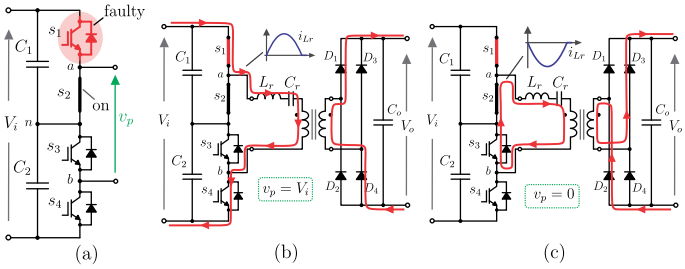

Figure 6. (a) 3L-SRC under faulty condition: SC failure on the semiconductor s_1. Operation of the 3L-SRC as a HB-SRC after the reconfiguration and the operation states: (b) positive i_L current (first state), (b) negative i_L current (second state).

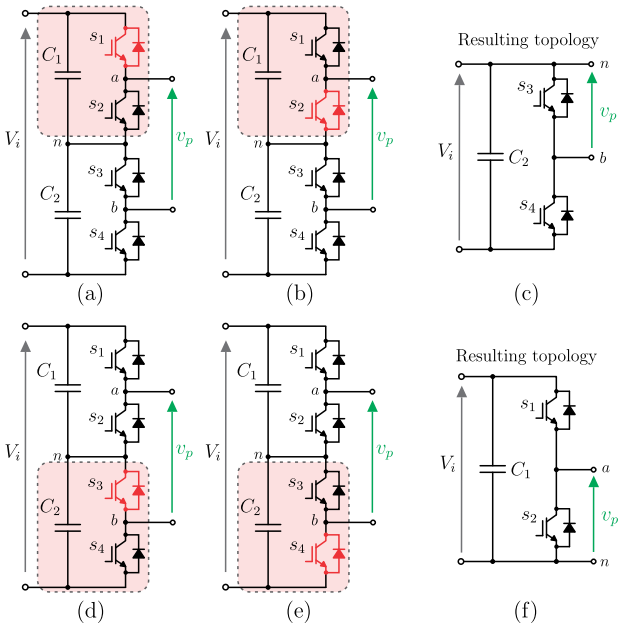

Figure 7. Proposed reconfiguration scheme for the 3L-SRC for a faulty case in every device and the resulting circuit after the reconfiguration: (a) fault in s_1, (b) fault in s_2, (c) resulting circuit (HBdc-SRC) after the reconfiguration in case of fault in s_1 or s_2, (d) fault in s_3, (b) fault in s_4, (c) resulting circuit (HBdc-SRC) after the reconfiguration in case of fault s_3 or s_4.

Table I
Switching States for the Reconfiguration Scheme for the 3-Level SRC

Faulty Device	s_1	s_2	s_3	s_4
s_1	SC	ON	switching	switching
s_2	ON	SC	switching	switching
s_3	switching	switching	SC	ON
s_4	switching	switching	ON	SC

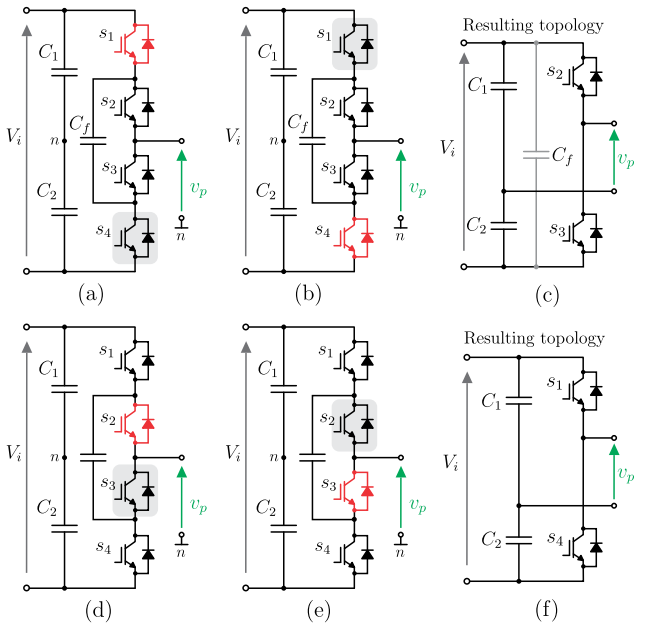

Figure 8. Proposed reconfiguration scheme for the FC-SRC for a faulty case in every device and the resulting circuit after the reconfiguration: (a) fault in s_1, (b) fault in s_2, (c) resulting circuit (HB-SRC) after the reconfiguration in case of fault in s_1 or s_2, (d) fault in s_3, (b) fault in s_4, (c) resulting circuit (HB-SRC) after the reconfiguration in case of fault s_3 or s_4.

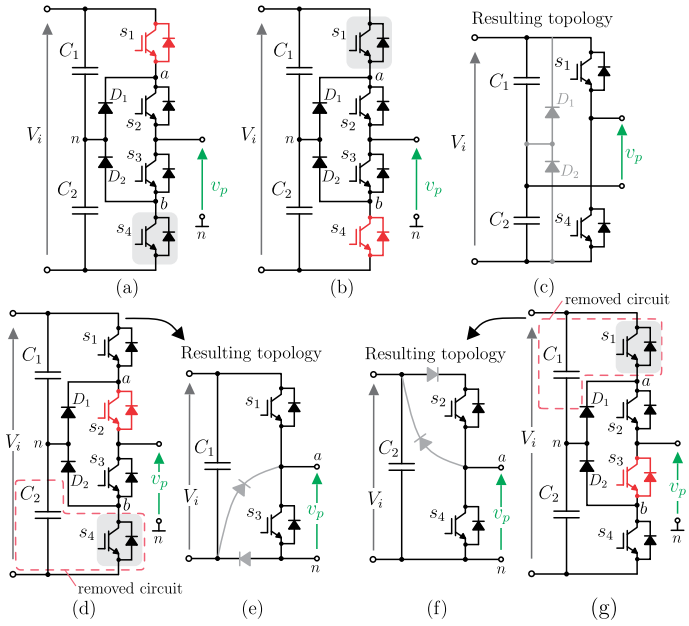

Figure 9. Proposed reconfiguration scheme for the NPC-SRC for a faulty case in every device and the resulting circuit after the reconfiguration: (a) fault in s_1, (b) fault in s_2, (c) resulting circuit (HB-SRC) after the reconfiguration in case of fault in s_1 or s_2, (d) fault in s_3, (b) fault in s_4, (c) resulting circuit (HBdc-SRC) after the reconfiguration in case of fault s_3 or s_4.

Table II
SWITCHING STATES FOR THE RECONFIGURATION SCHEME FOR THE FC-SRC

Faulty Device	s_1	s_2	s_3	s_4
s_1	SC	switching	switching	ON
s_2	switching	SC	ON	switching
s_3	switching	ON	SC	switching
s_4	ON	switching	switching	SC

Table III
SWITCHING STATES FOR THE RECONFIGURATION SCHEME FOR THE NPC SRC

Faulty Device	s_1	s_2	s_3	s_4
s_1	SC	switching	switching	OFF
s_2	switching	SC	switching	OFF
s_3	OFF	switching	SC	switching
s_4	OFF	switching	switching	SC

As an example, considering a failure on the switch s_1, the switch s_2 should be permanently on, as shown in Fig. 6 (a), discharging completely the capacitor C_1. Then, the part of the circuit composed by C_1, s_1 and s_2 and highlighted in Fig. 7 (a) is completely by-passed, resulting in the circuit in Fig. 7 (c). The healthy leg composed of s_3 and s_4 operates normally. As observed, the resulting circuit after the fault (see Fig. 7 (c)) is the same HBdc topology shown in Fig. 2 (a), but with transformer connected to the positive terminal of the input source V_i, instead the ground. Nevertheless, the modified connection has no influence on the converter operation. Fig. 6 (b) and (c) shows the operation states of the 3L-SRC after the reconfiguration.

The reconfiguration procedure for a failure on the other switches of the 3-Level topology is also presented in Fig. 7, while Table I describes the final state for every remaining healthy switch after the failure on each device.

C. Flying-Capacitor SRC

Similarly to the 3-Level converter, the Flying-Capacitor topology can also take advantage of the proposed fault tolerant method and the reconfiguration procedure is presented in Fig. 8, as well as the resulting circuit after the reconfiguration, for the faulty case in each switch. Considering a faulty on the switch s_1 as an example, the switch s_4 should remaining permanently on for the reconfiguration process. Then, the capacitor C_f will be charged with the full dc-link voltage V_i (operating in parallel with the array composed by C_1 and C_2). The switches s_2 and s_3 operate normally and the resulting circuit is shown in Fig. 8 (c). Differently from the FB-SRC and 3L-SRC, the resulting circuit after the reconfiguration of the FC-SRC is the HB-SRC, shown in Fig. 2 (b). It is important to note that the reconfigurable circuit for the 3L-SRC has a better performance compared to the FB-SRC or 3L-SRC, since the resonant capacitor of the will not operate with a dc voltage after the fault (see Fig. 3 (a) and (b)). Therefore, for the FC-SRC, the resonant capacitor does not suffer any impact after the reconfiguration, in this proposed approach. Table II describes the final state for every remaining healthy switch after the failure on each device.

D. Neutral Point Clamped SRC

Finally, the reconfiguration scheme for the NPC-SRC is described. For this converter, there are two faulty possibilities that will result in two different topologies after the reconfiguration: the first case is for a fault in the outer semiconductors, i.e. s_1 and s_4, whereas the second case is for inner semiconductors s_2 and s_3. The reconfiguration procedure of the NPC-SRC for

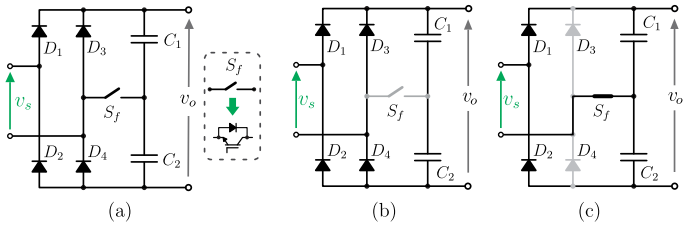

Figure 10. Topology of the re-configurable rectifier (a) and its operation possibilities: (b) operation as a FBR, (c) operation as a VDR.

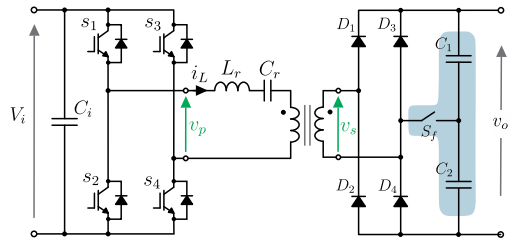

Figure 11. Topology of the proposed fault-tolerant FB-SRC.

both cases are presented in Fig. 9, as well as the resulting circuit after the reconfiguration, for the faulty case in each switch.

Analyzing the first case, a SC fault on the switch s_1 is assumed as a example, and hence the switch s_4 must remain permanently on for the reconfiguration. Consequently, the point a, highlighted in Fig. 9 (a), is connected to the positive terminal of the input dc-link V_i, whereas the point b (see Fig. 9) is connected to the ground, bypassing the clamp diodes D_1 and D_2 and resulting in the circuit shown in Fig. 9 (c). Meanwhile, the healthy switches s_2 and s_3 operates normally. Similarly to the FC-SRC, the resulting circuit for the first fault case of the NPC-SRC is a HB-SRC.

Evaluating the second case, a fault on the switch s_2 is assumed and, as part of the reconfiguration process, the switch s_4 must remain open. Furthermore, the part of the circuit composed by the capacitor C_2 and s_4 is removed from the entire circuit, resulting in the circuit shown in Fig. 9 (e). Thus, differently from the previous case, the resulting circuit after the reconfiguration is the HBdc-SRC. Table III describes the final state for every remaining healthy switch after the failure on each device.

IV. Proposed Family of Fault-Tolerant Series-Resonant Converter

As described in section II, the voltage v_p generated by the FB-SRC is V_i for first half of the switching period and $-V_i$ for second half, resulting in an effective voltage of V_i applied to the primary side of the converter. However, in faulty case, the FB-SRC is reconfigured, operating as a basic HB-SRC. Then, the voltage v_p will be V_i for first half of the switching period and 0 for second half, resulting in an effective voltage of $V_i/2$ applied to the primary side of the converter. Consequently, the output voltage of the re-configurable converters after the fault will be half of its original value (if the same rectifier is used on the secondary side), which is not desired. To overcome this problem and keep the output voltage constant after the failure, a re-configurable rectifier introduced in [7] is used. The full-bridge rectifier (FBR) topology is the most used in the secondary side of the SRC [12], [13]- [14], as depicted in Fig. 4 and Fig. 6. The voltage-doubler rectifier (VDR), which is also popular in the literature, can also be used in the SRC. While the FBR provides an output dc voltage of $v_o = v_{s_{pk}}$, where $v_{s_{pk}}$ is the effective voltage generated on the secondary side of the transformer, the VDR provides an output dc voltage of $v_o = 2 \cdot v_{s_{pk}}$.

In this context, the voltage doubler characteristic of the VDR can be used to keep the output voltage of the reconfigurable converters constant in case of fault. Thus, a re-configurable rectifier able to operate as a FBR or a VDR, previously introduced in [7], is employed to overcome the drawback of the proposed approach. The re-configurable rectifier circuit is presented in Fig. 10 (a). As can be seen in this figure, the re-configurable rectifier has two split capacitors and an additional switch (S_f) that allows to connect one side of the high frequency transformer secondary winding directly to the middle point of the capacitors, becoming a VDR.

The operation in normal and faulty conditions is depicted in Fig. 10 (b) and Fig. 10 (c), respectively. In normal operation, the switch S_f is open, and the rectifier operates as a standard FBR. In fault case, the switch S_f is activated, and then the leg composed of the diodes D_3 and D_4 is bypassed. The bottom side of the secondary winding is connected to the middle point of the capacitors C_1 and C_2, becoming an VDR. Therefore, the circuit operates as a VDR, and the output voltage value is twice the output voltage value in normal operation.

Using the reconfigurable rectifier on the FB-SRC, a fault tolerant FB-SRC (FT-FB-SRC) is generated, as presented in Fig. 11. Note that the multilevel SRC do not suffer for the aforementioned problem, because they generate a v_p voltage equal to $V_i/2$ for first half of the switching period and $-V_i/2$ for the second half, resulting in an effective voltage of $V_i/2$ on the resonant tank circuit, similarly to the voltage generated by the HB-SRC and the HBdc-SRC. Therefore, no modification on the secondary side rectifier is need, in the case of the multilevel SRC topologies. Finally, a family of fault tolerant series resonant converter based on the FB and multilevel topologies (previously depicted in Fig. 2 (c) to (f)) is generated, as shown in Fig. 11 and in Fig. 12. Fig. 11 shows the complete topology of proposed fault tolerant FB-SRC, while the Fig. 11 shows the topologies of the proposed fault tolerant multilevel SRC.

A. Fault-Tolerant Bidirectional SRC

The fault-tolerance capability of the SRC presented in the previous section for the unidirectional topology can also be easily extended to the bidirectional full-bridge topology [8]. In the topology depicted in Fig. 11, the diodes on the secondary side are replaced by active switches, in order to obtain an active bridge. Therefore, the operation is very similar to the unidirectional version, but active switches are used instead of diodes. Similarly to the unidirectional version, in faulty case, the secondary bridge must be reconfigured in a voltage-doubler

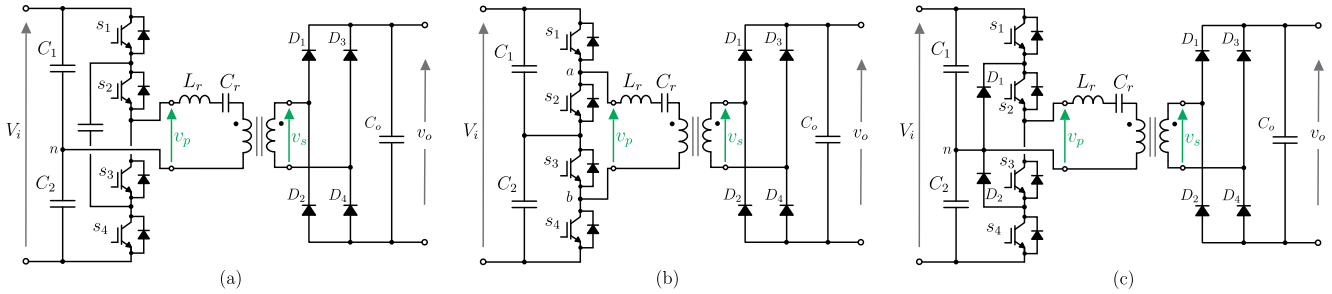

Figure 12. Proposed fault-tolerant series resonant dc-dc converter based on the multilevel topologies: (a) fault-tolerant FC-SRC (FT-FC-SRC), (b) fault-tolerant 3L-SRC (FT-3L-SRC), (c) fault-tolerant NPC-SRC (FT-NPC-SRC).

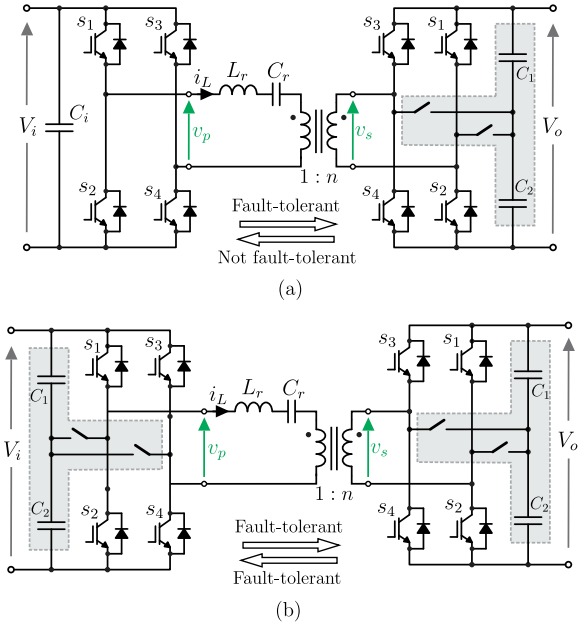

Figure 13. Proposed bidirectional fault-tolerant SRC topology.

Table IV
STRESSES ON THE MAIN COMPONENTS OF THE PROPOSED FAULT TOLERANT CONVERTERS BEFORE AND AFTER THE FAULT

Before the Failure					
Topology	FB	3L	FC	NPC	NPC
$V_{S(max)}$	V_i	$V_i/2$	$V_i/2$	$V_i/2$	$V_i/2$
$I_{S(rms)}$	$I_{L(pk)}/2$				
$I_{Lr(rms)}$	$I_{L(pk)}/\sqrt{2}$				
$V_{Cr(pk)}$	$\frac{I_o}{8nf_sC_r}$	$\frac{I_o}{8nf_sC_r}+V_i$	$\frac{I_o}{8nf_sC_r}$	$\frac{I_o}{8nf_sC_r}$	$\frac{I_o}{8nf_sC_r}$
After the Failure					
Topology	FB	3LC	FC	NPC	NPC
$V_{S(max)}$	V_i	V_i	V_i	V_i	V_i
$I_{S(rms)}$	$I_{L(pk)}$	$I_{L(pk)}/2$			
$I_{Lr(rms)}$	$I_{L(pk)}/2$	$I_{L(pk)}/\sqrt{2}$			
$V_{Cr(pk)}$	$\frac{I_o}{8nf_sC_r}+V_i$		$\frac{I_o}{8nf_sC_r}$		$\frac{I_o}{8nf_sC_r}+V_i$
Resulting	HBdc-SRC		HB-SRC		HBdc-SRC

bridge and therefore the reconfigurable bridge is obtained with additional switches as well. Fig. 13 (a) shows the proposed fault-tolerant bidirectional Series-Resonant dc-dc converter. Nonetheless, the fault-tolerance capability is obtained only when the power flows from the primary to the secondary side (i.e. from v_i to v_o), whereas only the secondary bridge is able to reconfigure in a voltage doubler bridge. To obtain a fully fault tolerant converter, either the primary and secondary bridge must be reconfigurable and therefore the completely fault-tolerant SRC topology is presented in Fig. 13 (b). Although more semiconductors are used, the efficiency is not deteriorated, since the additional switches are only activated in faulty case. Besides that, with the proposed topology, the availability of the topology is highly increased.

V. Evaluation of the Proposed Fault-Tolerance Approach

To verify the performance of the proposed approach, the voltage and current stresses on the main components before and after the fault are presented and discussed. Furthermore, a comparison of the proposed method with existing fault tolerant approach is presented, as well as numerical simulation results for each topology are provided.

After the fault occurrence, the semiconductors and the tank circuit components are submitted to different voltage and current stresses, according to the topology. Table IV presents the voltage and current stresses before and after the fault for each proposed fault tolerant converter, as well as the resulting topology after the reconfiguration. For the FT-FB-SRC, the voltage effort on the semiconductor remains the same after the fault, but the current doubles after the fault, if the output power is constant. It happens, because the voltage v_p drops to half of its original value after the fault, and to keep the same transfer power, the current must double. In addition, as the v_p presents a dc component, the voltage over the resonant capacitor (v_{cr}) will also present a dc components, increasing its peak value, while preserve the voltage ripple.

For the multilevel topologies, the current effort on the semiconductor remains the same after the fault, but the voltage over the devices will double. Consequently, the semiconductors must be properly design to support the voltage, in fault case. These are the main disadvantage of the proposed method.

In spite of these drawbacks, the proposed fault tolerant approach is still very advantageous when compared to the existing ones previous proposed in literature, because a reduced

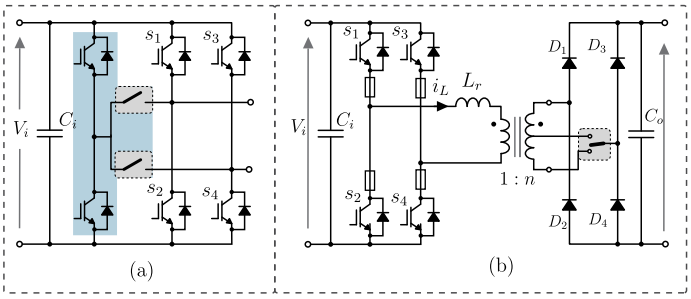

Figure 14. Existing fault tolerant approaches: (a) redundant leg [3], (b) method proposed in [6].

Table V
COMPARISON OF DIFFERENT FAULT TOLERANT APPROACH

Extra devices	Redundant leg [3]	Method 2 [6]	Proposed
Semiconductors	6	4	2
Fuses	6	4	0
Capacitors	0	0	1
Others	-	central tap trafo	-
Eff. impact	yes	yes	no

number of components are used and also there is no impact on efficiency after the reconfiguration. Note that for the FT-FB-SRC, only one additional switch and an additional capacitor is needed, while for the multilevel SRC, no additional component is needed. Thus, the impact on the cost is very reduced.

From the existing methods presented in literature, the redundant leg approach is the most popular one. It is shown in Fig. 14 (a) [3]. In this solution, an extra leg is used to replace the damaged leg in case of fault. To isolate the faulty leg, fuses must be used in series with the semiconductors, opening the circuit for the SC case. Consequently, this solution requires many additional components, increasing considerably the cost. Moreover, the fuses used in series with the main devices dissipate power, deteriorating the converter's efficiency. Another fault tolerance approach was proposed in [6] for the full-bridge phase-shift dc-dc converter, in which it is reconfigured in an asymmetrical half bridge converter in case of OC fault. This approach uses a redundant winding on the transformer, as shown in 14 (b), and it is valid only for OC failure. Furthermore, fuses are used in series with the main devices to isolate the faulty leg, deteriorating the converter's efficiency. The Table V shows the comparison of the described existing methods with the proposed one, in terms of components and efficiency impact. As can be noticed, the proposed approach provides an efficient and low cost solution, when compared to the existing ones.

A. Simulation Results

To verify the converters performance and the validity of the proposed fault tolerant approach proposed in this paper, every multilevel topology was simulated using the MATLAB/Simulink and the PLECS toolbox, considering the parameters presented in Table VI. For each case, a fault on the switch s_4 was imposed at moment of $t = 0.1s$ and the main waveforms are summarized in Fig. 15. The results consist in voltage and current on the tank circuit elements [i.e. primary side voltage (v_p), capacitor voltage (v_C) and inductor current (i_L)], faulty (s_4) and healthy devices (s_2), as well as the voltage over the capacitors C_1 (v_{C_1}) and C_2 (v_{C_2}) and the output voltage (v_o). As can be notices, the tank circuit components (v_p, v_C and i_L), as well as the output voltage (v_o)are not affected during the fault. On the other hand, the voltage over the semiconductors increases.

For the FT-3L-SRC, the capacitor C_2 is fully discharged, while the capacitor C_1 is charged with the total dc voltage after the fault, as described in Section III-B (see Fig. 7 (e)), and it can be seen in Fig. 15 (d). Similarly, for the FT-FC-SRC, the capacitor C_f is charged with the full dc-link voltage after the reconfiguration process, operating in parallel with the array composed by C_1 and C_2, as observed in Fig. 15 (h). For the FT-NPC-SRC, there is no variation on the capacitors voltage, but only the primary side semiconductors. These results demonstrate the effectiveness of the proposed methods and the proposed fault tolerant topologies.

VI. EXPERIMENTAL VALIDATION OF THE PROPOSED APPROACH

In order to verify the performance of the proposed fault tolerance approach, a prototype of 10 kW was built and experimental results were obtained. As a matter of simplicity, the FB-SRC presented in Fig. 11 was chosen to be implemented and evaluated experimentally. The specifications of the implemented power converter prototype, as well as the resonant tank circuit parameters are presented in Table VI. The IGBT IHW40N120 ($1200V/40A$, from *Infineon Technologies AG*) was selected as the main switch and it was used on the primary side and secondary sides. For the secondary side, the intrinsic diodes of the IGBT were used to rectifier. The converter operates in open loop and the gating signals are generated by the DSP. To evaluate dynamically the performance of the converter under fault case, a short-circuit on the switch s_2 was emulated by software in the DSP.

Fig. 16 shows the photo of the prototype and the main waveforms for the converter operating in steady-state at nominal condition. The results were obtained for the converter operating in steady-state (before and after the fault) and also dynamically during the fault and they are discussed herein. For safety reasons, the dynamic results were obtained for reduced input and output voltages.

Initially, the converter was tested considering only the reconfiguration scheme in the primary bridge, without the reconfigurable rectifier, with the aim to validate the fault tolerant approach and the reconfiguration methodology described in Section III. The test was performed with input and output voltage of 200 V and 300 V, respectively, and the result for this condition is presented in Fig. 17 (a). In this figure, it is observed the dynamic response of the FB-SRC during the fault of the switch s_2, in which the converter remains operational after the fault, proving its inherent ability to handle the fault. As expected, the output voltage drops to half of its value (from 300 V to 150 V) after the fault and the capacitor voltage has an offset of V_o. The inductor current is also reduced, because

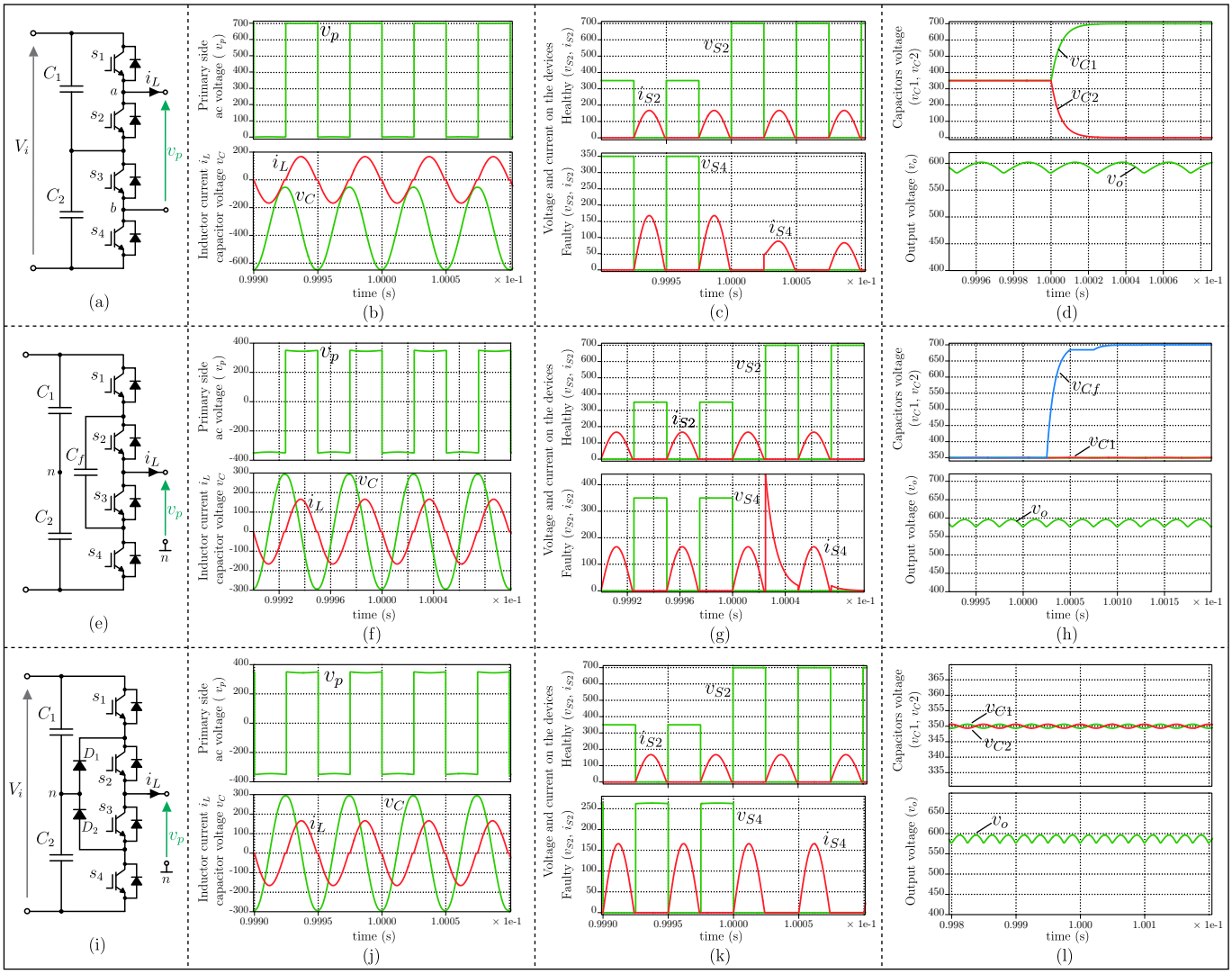

Figure 15. Simulation results for the proposed fault tolerant multilevel topologies, when a fault occurs in switch s_4 in each case. In each case, it is considered an fault at moment $t = 0.1s$. (a) to (b) operation of the FT-3L-SRC under fault: (b) primary ac side voltage (v_p), (b) resonant capacitor voltage (v_{cr}), (c) voltage and current on the faulty switch (s_4) and on the healthy device (s_2), voltage over the dc-link capacitors (C_1 and C_2). (e) to (h) similar results for the FT-FC-SRC under fault. (e) to (h) results for the FT-NPC-SRC under fault.

the test was performed with constant resistance as load and therefore reduction on the output voltage implies in reduction on power.

Subsequently, the prototype was tested including the reconfigurable rectifier, in order to validate the operation of the proposed fault-tolerant FB-SRC topology. For this test, it was considered an input voltage of 350 V and output voltage of 500 V, and the main results are presented from Fig. 17 (b) to (d). The dynamic behavior during the fault on switch s_2 is depicted in Fig. 17 (c), showing that the converter remains operational after the failure. Additional, the converter provides a constant output voltage (500 V) even after the fault, attesting the effectiveness of the proposed rectifier and the converter. As the output voltage remains constant, the amount of processed power is the same before and after the fault and therefore the amount of current on the resonant tank is twice after the fault, as previously described. The detailed waveforms before and after the fault can observed in the Figs. 17 (c) and (d), respectively. As can be observed in these figures, the converter behaves as a FB-SRC before the fault and as a HBdc-SRC after the fault, and the experimental waveforms (Figs. 17 (c) and (d)) are in accordance with the theoretical one shown in Fig. 3 (c) and (a).

To summarize, the results have shown that the proposed converter can handle a short-circuit fault in one device and still provide the required output voltage and power, keeping the continuity of operation.

One of the main advantages of the proposed approach is to preserve the converter's performance after the failure, and to demonstrate that, the converter's efficiency was measured before and after the fault. The efficiency test was carried for converter operating at input-output voltage levels of 600 V to 700 V and output power of 3 kW. The efficiency values were obtained experimentally using the high precision power analyzer WT1800 from Yokogawa. Before the fault the converter reached an efficiency of 98.25%, whereas it

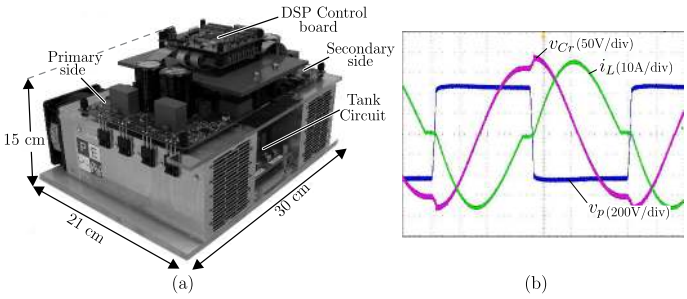

Figure 16. Implemented 10 kW fault tolerant SRC converter hardware prototype: (a) photo of the prototype (mechanical dimensions: 300 mm x 210 mm x 150 mm: power density: 1 kW/dm^3), (b) experimental result at nominal load ($V_i = 700$ V, $V_o = 600$ V, $P_o = 10$ kW), showing the operation of the prototype.

Table VI
SPECIFICATION OF THE SRC PROTOTYPE AND THE RESONANT CIRCUIT PARAMETERS

Power converter specification	
Input voltage	$V_i = 700$ V
Output voltage	$V_o = 600$ V
Nominal output power	$P_o = 10$ kW
Switching frequency	$f_s = 20$ kHz
Transformer turn ratio	$n = 1.45$
Resonant circuit parameter	
Resonant capacitance	$C_r = 0.68\mu F$
Resonant Inductor	$L_r = 79\mu H$
Tank resonant angular frequency	$\omega_0 = 1.364 \cdot 10^5$ rad/s
Resonant frequency	$f_o = 21.7$ kHz

presented 98.1% after the failure. As can be noticed, similar values of efficiency is obtained for the both cases. The small deviation between this values is observed, because the current effort after failure on the primary side semiconductor is higher, resulting in higher losses. On the other hand, there is less component on the current path of the secondary side, reducing the losses in this side. Consequently, these results show an acceptable deviation on the converter's performance and the small influence of the proposed fault tolerant approach on the converter's efficiency is verified.

VII. CONCLUSION

This paper proposed a family of series-resonant dc-dc converter with fault tolerance capability The proposed fault tolerance method consist in re-configuring the FB-SRC or multilevel SRC in a half-bridge SRC (HB-SRC or HBdc-SRC), in case of a semiconductor failure, keeping the converter operational. The proposed approach can be applied to the series resonant converter based on full-bridge, three-level, flying capacitor and neutral point clamped topologies, and the reconfiguration methodology for each of them was described. Furthermore, the bidirectional SRC based on Full-Bridge topology with fault tolerance capability was presented and described in this paper, as well. As a result of the reconfiguration, the output voltage is reduced. To overcome this problem a modified rectifier that can be reconfigured in a voltage doubler rectifier, keeping the output voltage constant, is used. Then, a family of SRC with fault capability is generated and presented.

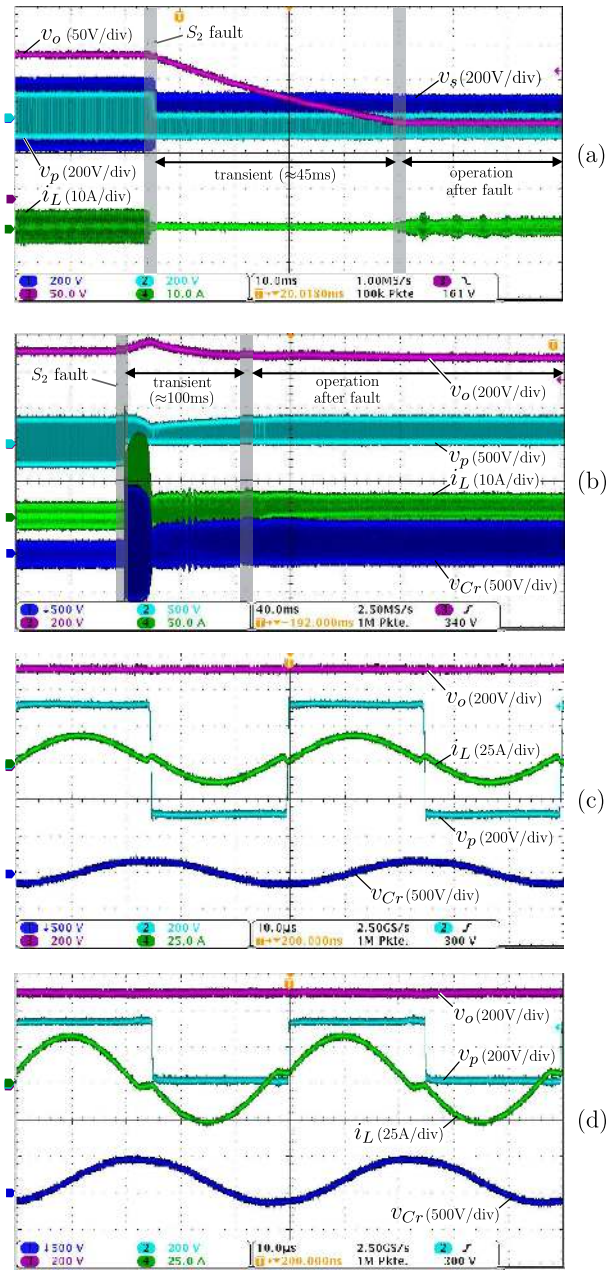

Figure 17. Experimental results of the FB-SRC under a fault on the switch s_2: (a) dynamic behavior of the converter during the fault, without the reconfigurable rectifier on the secondary side, (b) dynamic behavior of the converter during the fault, including the reconfigurable rectifier, (c) steady-state operation before and (c) after the fault, considering the re-configurable rectifier on the secondary side.

The main advantages of the proposed converter are: post-fault operation, simple implementation, reduced number of additional component and no efficiency deterioration. As a drawback, the resonant capacitor must be designed for higher voltage and the current effort on the healthy devices in failure mode operation is twice the than in normal mode operation.

Experimental results for a 10 kW prototype were obtained and the effectiveness and advantages of the proposed fault tolerant series resonant dc-dc converter has been demonstrated.

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