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A fast, ultra-low and frequency-scalable power consumption, 10-bit SAR ADC for particle physics detectors

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Abstract: The design and measurements results of a fast 10-bit SAR ADC with ultra-low and scalable with frequency power consumption, developed for readout systems for detectors at future particle physics colliders (ILC, CLIC, LHC Upgrade), are described. A prototype ASIC was designed and fabricated in 130 nm CMOS technology and a wide spectrum of static (INL$\lesssim$0.5 LSB, DNL$\lesssim$0.5 LSB) and dynamic (SINAD ~58 dB, ENOB~9.3) measurements was performed to study and quantify the ADC performance. The ADC works in wide 10 kS/s – 40 MS/s sampling frequency range, covering more than three orders of magnitude. In most of the range the power consumption scales linearly with sampling rate with a factor of about 22 μW/MS/s. A dynamic and asynchronous internal logic makes the ADC very well suited not only for commonly used synchronous sampling but also for applications with asynchronous sampling and/or the ones requiring power cycling, like the experiments at future linear collider (ILC/CLIC). The ADC layout is drawn with a small pitch of 146 μm to facilitate multi-channel integration. The obtained figure of Merit is in range 32-37 fJ/conversion for sampling frequencies 10-40 MS/s, placing the ADC among the best State of the Art designs with similar technology and specifications.

Keywords: VLSI circuits; Analogue electronic circuits; Front-end electronics for detector readout; Digital electronic circuits

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Contents

2015 JINST 10 P11012

1 Introduction

Future particle physics experiments, like the ones at future linear collider (ILC — International Linear Collider or CLIC — Compact Linear Collider) or at upgraded Large Hadron Collider (LHC), are setting more and more challenging requirements for their detectors and their readout systems. The readout electronics requirements are growing multi-dimensionally in: increasing number of channels per ASIC (Application Specific Integrated Circuit), finer channel segmentation matching the sensor pitch, faster signal processing, lower power consumption, lower noise, better radiation hardness, on-chip implementation of analogue-to-digital (ADC) conversion, on-chip digital signal processing (DSP, e.g. baseline subtraction, common-mode subtraction, zero suppression), faster serial data transmission, power cycling, and other specific features.

Integration of a fast sampling ADC in each readout channel, although natural and resulting in a simple and elegant architecture, has been a bottleneck in past readout systems because of excessively high ADC power consumption. During the last decade huge progress in ADC performance was achieved due to the use of a small size deep-sub-micron CMOS processes and fast development of ADC architectures. In particular the ADCs performing successive approximations (SAR — Successive Approximation Register) are among the most popular due to their simplicity and a very small number of mostly digital components. Improvements in the SAR ADC architecture have brought a continuous increase of their speed (presently beyond 100 MS/s) and a huge drop in the dissipated power. The latter is of crucial importance for present and future high density detector

readout systems, demanding for ultra-low power consumption per channel. A high performing readout system requires an ADC dissipating less power than the analogue front-end so that the overall power consumption is not dominated by the ADC.

The main goal of this work was to develop a medium-high resolution ADC fulfilling the requirements of the readout of luminosity detector (calorimeter) at ILC. At the same time the ADC was thought as a general purpose block fulfilling the most common requirements of readout systems performing amplitude measurement. Therefore, the following objectives have been delineated for the ADC:

- 10-bit resolution. Such resolution is needed for the luminosity detector and at the same time it is often required in other readout systems. For lower resolution applications, like readout for tracking detectors, we have already developed a fast 6-bit ADC [1];
- Wide sampling frequency range. For the luminosity detector the range between 3.5 MS/s (sampling rate in ILC) and 20 MS/s (sampling of pulse shape during beam-tests) is needed. To make the ADC general purpose this range was extended to some kS/s at lower frequencies and to 40 MS/s (nominal LHC frequency) at higher frequencies,
- Ultra-low power consumption scalable with frequency. A maximum power consumption below 1 mW at 40 MHz sampling was taken as a goal;
- Possibility of cycling the power. This feature is very important for applications in future linear colliders (ILC, CLIC) where the time between bunch trains is very long, and the best way to limit the power consumption is to switch off power between the trains;
- Asynchronous operation. This will extend the range of possible applications making the ADC more general purpose. In addition, with asynchronous operation, it is much easier to implement the power cycling.
- Small pitch adapted for multi-channel integration.

In this paper we present the design and measurements of a prototype ultra-low power 10-bit ADC fulfilling the discussed requirements. The second section describes the design, implementation of key circuit blocks, and optimisation of the chosen SAR ADC, with particular attention on low power issues. In the third section the measurements performed on a prototype ADC ASIC and a comparison with State of the Art ADCs are presented. Finally, the conclusions are given.

2 ADC architecture and design

A Successive Approximation Register type ADC consists of an input sampling circuitry, a Digital to Analogue Converter (DAC), a comparator, and a SAR control logic. The architecture of the actually implemented 10-bit ADC is shown in figure 1. A fully differential solution is used to improve the immunity to digital cross-talk and other disturbances. A capacitive DAC is used to eliminate the static power and to achieve the lowest power consumption. For the same reason all transistor-based circuitry is dynamic. As the result the ADC does not consume any power (except leakage) when not converting and, what was one of the main design goals, the power dissipation depends linearly on

2015 JINST 10 P11012

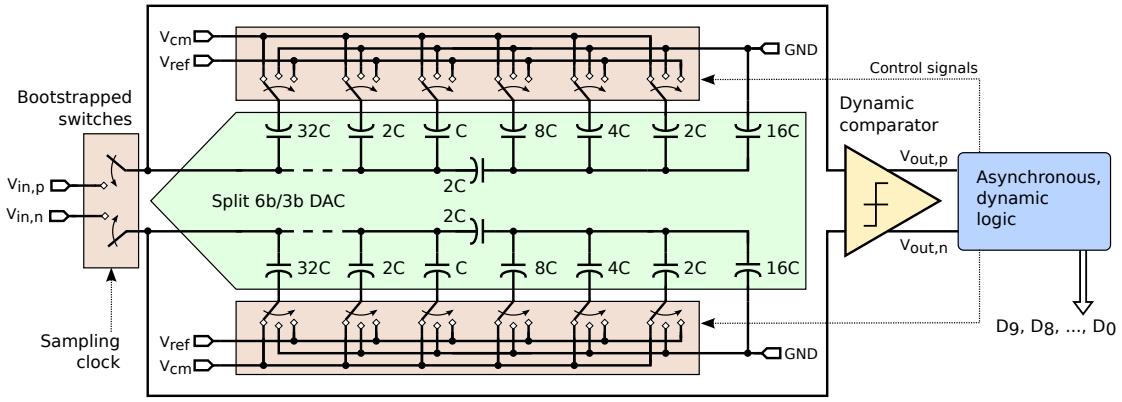

Figure 1. Architecture of 10-bit SAR ADC.

the sampling frequency. To eliminate the clock tree, to lower further the power consumption, and to increase the conversion speed, asynchronous control logic is implemented. In this way another very important goal is achieved — the ADC works asynchronously and needs only one sampling signal to start and perform the conversion, while the additional clock is not needed for bit cycling. The asynchronous operation together with the dynamic implementation allow to obtain the power cycling without any additional effort. The ADC starts to consume power when the sampling pulse (clock) arrives and stops when the conversion is completed. As mentioned, this feature is highly requested in linear collider applications.

The implementation of main ADC blocks is described in following subsections.

2.1 Input sampling and dynamic comparator

In order to decrease the sampling resistance and make it independent on signal amplitude bootstrapped MOS switches [2, 3] are implemented in the differential S/H input. Since the bootstrap switch has an internal capacitance which needs to be precharged before the sampling, therefore after a long (~ms) period of ADC downtime (like in power cycling operation), the first sample may not be fully correct (due to charge leak in internal capacitance).

To eliminate completely the static power and to reduce further the power consumption, a dynamic comparator was designed. Because of low intrinsic transistor gain in the used deep submicron CMOS technology, a solution with two gain stages and output-latch, providing high enough precision, shown in figure 2, was chosen [4].

2.2 Internal DAC architecture and switching scheme

As already mentioned a differential architecture is beneficial for robustness against various disturbances while capacitive DAC arrays are beneficial for power efficiency of the ADC. To further lower the dissipated power the Merge Capacitor Switching (MCS) scheme [5, 6] was applied in the DAC operation. The main features of the MCS are top-plate capacitance sampling and use of common mode voltage V_{cm} (roughly equal to half of V_{ref}) as initial potential on bottom plates of capacitive DAC arrays. Since in the chosen technology the best capacitance matching is offered by Metal-Insulator-Metal (MIM) capacitors, which are relatively large, a split capacitance DAC scheme was implemented, as shown in figure 1. In each of the DAC arrays there are $M = 6$ capacitances on the

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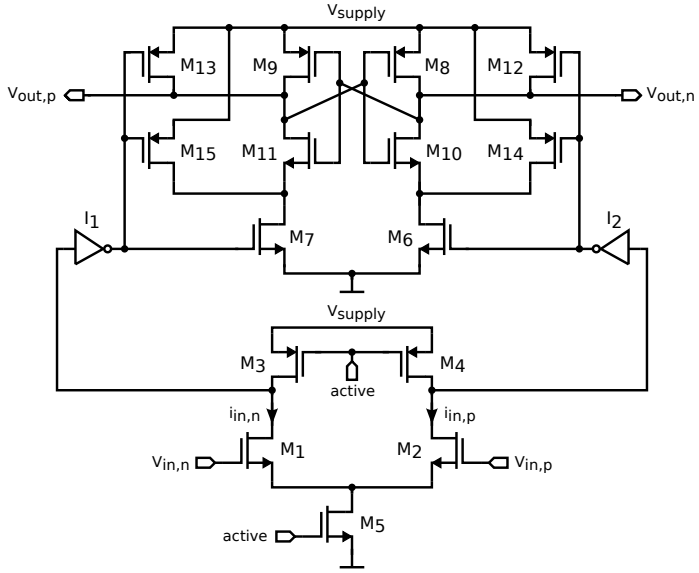

Figure 2. Schematic diagram of dynamic comparator.

Most Significant Bits (MSB) side (left), and $L = 3$ capacitances on the Least Significant Bits (LSB) side (right). On the LSB side there is additional capacitance ($16C$), not used for bit cycling, which is needed to obtain a binary voltage scaling. To obtain better matching, the splitting capacitance (between MSB and LSB arrays) is a multiple of the unit capacitance C, and in the implemented case it is double the capacitance C.

When the sampling is completed, the first iteration begins by comparing $V_{\mathrm{in,p}}$ and $V_{\mathrm{in,n}}$ and storing the result of comparison in the MSB bit D_9, which is equivalent to the sign of the result. One may also interpret this step as a comparison of $V_{\mathrm{in}} = V_{\mathrm{in,p}} - V_{\mathrm{in,n}}$ to the DAC differential voltage $V_{\mathrm{DAC}} = 0$. This step is performed without any switching in the DAC arrays. In next steps the subsequent capacitances in the DAC arrays, which are initially connected to V_{cm}, are switched either to V_{ref} or to GND (vice versa in top and down part of differential array in figure 1) according to the comparison result between the V_{in} and V^i_{DAC}, given by the formula:

$$V^i_{\mathrm{DAC}} = \begin{cases} 0 & \text{for } i = 0, \\ \dfrac{V_{\mathrm{ref}}}{2^{N-1}-1} \cdot \displaystyle\sum_{k=1}^{i} (2 \cdot D_{N-k} - 1) \cdot 2^{N-1-k} & \text{for } 0 < i < N-1, \end{cases} \tag{2.1}$$

where i is comparison step index (changing from 0 to N-1), N is number of bits (10 for 10-bit ADC), and D_{N-1-i} is i^{th} comparison result, i.e. the i^{th} ADC output bit. The algorithm is repeated sequentially in order to determine the value of each bit D_{N-1-i}. In the last comparison the LSB bit D_0 is obtained without further change of the DAC output voltage.

As seen in the equation (2.1), the V_{DAC} voltage is not a binary part of V_{ref} (in case of 10-bit ADC it is V_{ref} divided by 511). It is a consequence of the chosen splitting capacitance equal $2C$. However, each element of the sum in formula 2.1 is always two times smaller than the previous one.

2.2.1 Unit capacitance considerations

The value of the unit capacitance C is determined by matching and noise properties of the capacitor used.

The thermal noise $\overline{V^2_{\text{noise}}}$ for temperature T of capacitive DAC with total capacitance C_{DAC} is expressed by the well known formula:

$$\overline{V^2_{\text{noise}}} = \frac{k_B T}{C_{\text{DAC}}}, \tag{2.2}$$

where k_B is Boltzmann constant. It can be verified that for 10-bit ADC this noise contribution would be important for the C_{DAC} of the order of tens of fF or less. Since the total DAC capacitance is few orders of magnitude higher, quantitatively the thermal noise effect is negligible.

For a typical MIM capacitor it can be assumed that the standard deviation σ of capacitor mismatch is expressed as:

$$\frac{\sigma}{C} = \frac{K_\sigma}{\sqrt{A}}, \tag{2.3}$$

$$C = K_C \cdot A, \tag{2.4}$$

where K_C is capacitance density (K_C=2.05 fF/μm^2) , K_σ is technology dependent matching parameter (K_σ=4.12 %·μm) and A is area of capacitor C [μm^2].

Doing similar matching considerations as in [7] and performing Monte Carlo (MC) simulations of DAC resolution variation versus unit capacitance value, C = 40 fF was chosen. Since a minimum available MIM capacitance in the chosen technology is around 60 fF, to implement the smallest capacitance C (on the MSB side of DAC capacitive array) two 80 fF MIM capacitors were connected in series, while all other capacitances were built as parallel connections of 80 fF MIM capacitors.

2.3 Asynchronous SAR logic

The control logic for SAR ADC can be implemented as synchronous, driven by fast external clock, as well as asynchronous, event driven. The first implementation has two major drawbacks: speed is limited by the frequency of the external clock and additional power is consumed by the clock distribution network. Since for N-bit ADC the same circuit is used N times in the SAR architecture, the external clock driving synchronous logic has to be at least N times faster than the sampling clock. Aside some more sophisticated realisations, all the actions performed for each bit processing may require more than one clock cycle per bit, multiplying the clock frequency even more. On the other hand, it has been shown that for SAR architecture, the asynchronous implementation is much more efficient [8], allowing to obtain significantly higher sampling rate together with lower power consumption. Since asynchronous logic is driven, as will be shown later, by a sequence of events, it requires only the sampling signal determining the conversion beginning and no other signal (clock) is needed for bit cycling. Furthermore, the conversion process is completely independent from any external clock, so the sampling signal can be unevenly distributed in time, if only the time interval between consecutive samples is longer than the conversion time. This also means that the ADC can be stopped just by the absence of sampling signal and does not consume the power (equivalent to power cycling feature). To obtain a maximum possible sampling rate, any delay in data flow should

2015 JINST 10 P11012

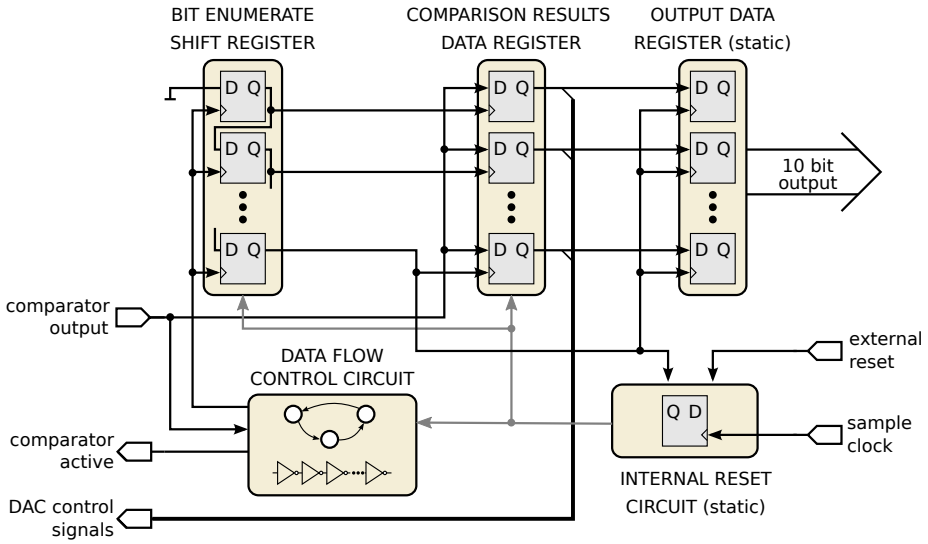

Figure 3. Diagram of the SAR ADC control logic.

be minimised as it is multiplied N times for N-bit ADC, increasing the total conversion time. For this reason, the dynamic logic was chosen for both internal registers and data flow control circuit. The complete control logic layout was drawn and optimised manually without using any standard logic cells and automated tools.

The diagram of SAR ADC control logic is shown in figure 3. It contains two registers based on dynamic flip-flops, one based on static flip-flops, a data flow circuit (also dynamic) and an internal reset circuit (static). The dynamic flip-flops are used in two internal registers to achieve sampling rate exceeding 40 MS/s. The first of these registers is shift register enumerating bits during the conversion while the second one stores the comparison result during the conversion. Since the ADC can be stopped at any time by no sending a sampling signal, dynamic registers have to be reset by an internal (static) circuit just after the conversion ends, to avoid a direct path current. To enable to subsequent logic to read the conversion result without stringent time constraints, the data stored in the dynamic register during the conversion are passed to a static output register, where it remains available until the end of the next conversion.

The data flow control circuit is realised as a FSM (Finite State Machine) with state diagram shown in figure 4. After power up the ADC remains in self reset state. The conversion begins at a time when the bootstrapped switches disconnect the input signal from the DAC. The first comparison is performed without any switching in the DAC arrays (as it was shown for the MCS switching scheme). Since the outputs of the comparator $V_{out,p}$, $V_{out,n}$ in reset phase are always in high state 11, and change to either 10 or 01 (according to the input voltages) when the comparison is done, the distinction between the finished and ongoing comparison can be done by simple logical conjunction of comparator outputs. In reality, since during the comparison a forbidden state 00 can appear on the comparator outputs, a logical XOR was used to ensure that this incorrect state is not recognised as a valid result. The result is then stored in the internal data register and the completed bit is counted by the enumerating register. Assuming that one or more bits are still to be processed, the two values from internal registers are then combined to create proper control signals for the analogue reference voltages switches in the DAC arrays. Simultaneously, the reset signal is sent to

2015 JINST 10 P11012

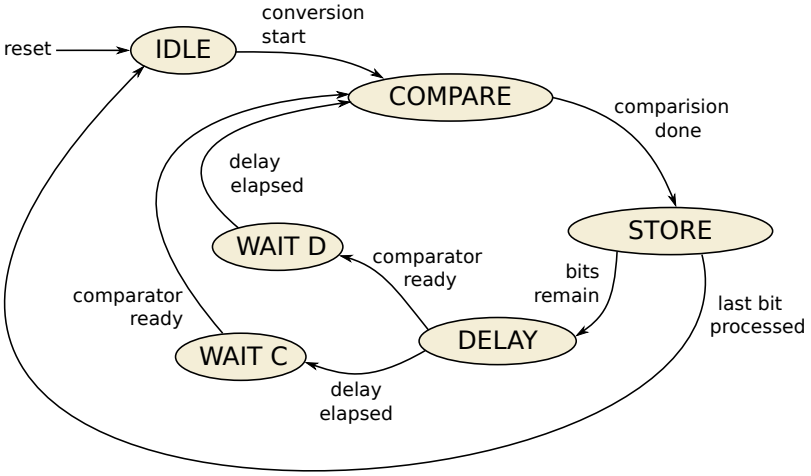

Figure 4. State diagram of the data flow FSM.

the comparator to prepare it for next iteration.

Since the DAC's capacitive arrays are recharged by non-zero resistance analogue switches, their output voltage changes, in first approximation, as in single pole R-C circuit. The next comparison should not be started until the DAC output voltage reaches the target value with sufficiently good accuracy, therefore a fixed delay needs to be introduced before performing the next comparison. Otherwise, the comparison result can be corrupted, what is called a settling error. This fixed delay is implemented as a chain of inverters with programmable length, which allows to control the delay via external control signal. In addition, since capacitance to be charged is decreasing for the subsequent bits, the DAC settling time is shortening. Thus, a long fixed delay, suitable for the largest capacitances, results in unnecessary time waste during the processing of the last bits. To avoid this waste, the length of inverters chain is, independently from external settings, controlled by the internal logic to decrease the delay for less significant bits. Since the comparator requires non-negligible amount of time to accomplish the reset phase, two conditions need to be fulfilled: the comparator has to be ready for the next comparison and the fixed delay has to elapse. Depending on the order of events, the FSM passes through the WAIT D state, if the comparator is ready before the delay has elapsed, or WAIT C in opposite case. When both conditions are met, the next comparison is performed, beginning the next bit processing.

The complete cycle is repeated nine times, while the last tenth cycle is interrupted just after the comparison, since the bit enumerating register reaches its final value. After the processing of the last bit, the result is sent to the output data register and the internal reset is sent to the control logic preparing the entire ADC for the next conversion.

2.4 Design optimisation

For a proper operation the ADC requires analogue and digital power supply, reference voltage (V_{ref}) and common-mode voltage (V_{cm}). The reference voltage is 1.2 V and is equal to supply voltages, while the V_{cm} should be around 0.6 V but its exact value and its stability is not critical for the ADC operation. Apart from the above DC voltages and configuration bits controlling internal delays, the only dynamic signal (apart from differential input) is the sampling signal (clock).

2015 JINST 10 P11012

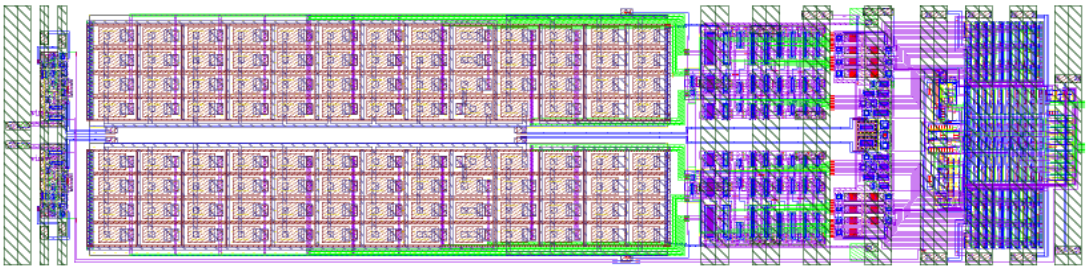

Figure 5. Layout of a single channel of 10-bit SAR ADC.

The layout of a single ADC channel is shown in figure 5. To facilitate multi-channel implementation a small ADC pitch, matching the analogue front-end pitch, is needed. In this design the pitch of 146 μm, corresponding to two input pads (differential input), was chosen. For such choice an ADC channel length of 600 μm was obtained. To minimise pitch and area the DAC layout was drawn without using dummy capacitors. The DAC occupies more than 50% of the total ADC area. A significant part of layout is used by the DAC reference voltages switches and the buffers driving these switches, composed of inverters (on the right side of DAC matrices). A good buffering is important for fast charging of DAC capacitances and so for high ADC sampling rate. On the other hand it contributes significantly to the ADC power consumption.

The performance of the designed ADC was simulated on different design stages, starting from the schematic, and continuing during the layout design. To verify the impact of statistical fluctuations the Monte-Carlo simulations were also done. The simulations were done iteratively, since various design details were modified until achieving satisfactory results in the post-layout simulations. Apart simple functional and static performance simulations (for constant input signals), also simulations of all important dynamic parameters, i.e. Signal to Non-harmonic Ratio (SNHR), Total Harmonic Distortions (THD), Spurious Free Dynamic Range (SFDR), and Signal to Noise and Distortions (SINAD), were done [9]. The completed design showed an Effective Number Of Bits (ENOB) in simulation of about 9.5-9.6 bits up to 40 MS/s sampling rate.

During the design phase, no specific techniques were used to improve radiation hardness. It was assumed that the chosen CMOS 130 nm process is itself sufficiently rad-hard. The actual radiation tolerance will be verified experimentally.

3 Measurements results

The prototype ASIC was fabricated in a 130 nm, eight-metal CMOS technology. The micrograph of the prototype ASIC containing 8 ADC channels is shown in figure 6. Not all channels are exactly the same, there are small differences in the comparator and the capacitive DAC layout. The eight channels are seen on the left, while the large area on the right side is occupied by the digital part.

To verify the ADC performance, a dedicated test setup, based on a Field Programmable Gate Array (FPGA), was developed. It is a modified version of the setup previously used [1, 13]. The DC signal, for static measurements, or sinusoidal signal, for dynamic measurements, is delivered to the ADC inputs and the 10-bit digital output is read out using the Scalable Low-Voltage Signaling (SLVS) standard. The ADC signal input range depends on V_{ref} value, and its amplitude is always slightly lower than V_{ref} because of the implemented split capacitor DAC scheme and parasitic capacitances.

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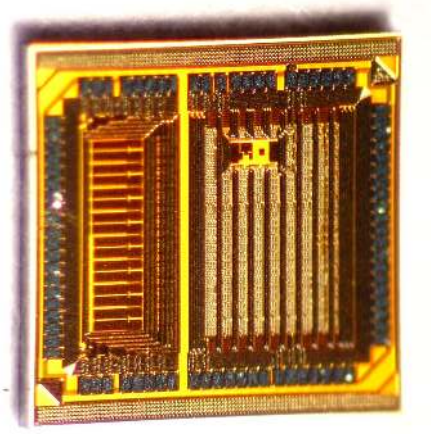

Figure 6. Micrograph of prototype ASIC.

Most of the measurements presented in this section were done for single ADC channel. To study the channels uniformity few example measurements were done for more channels. In particular, the channel to channel offset of a few LSB was observed. In addition, we have done few measurements on selected channels of four different ASICs, in total more than 10 ADC channels, and we have not found any visible difference in performance. From these studies we can conclude that the results presented in this paper show a typical ADC performance.

The ADC measurements were done using four external bias voltages: analogue and digital power supplies which were set to 1.2 V, reference voltage V_{ref} also set to 1.2 V, and common voltage V_{cm} set to 0.6 V. The results presented below were obtained for the separated bias voltages, but for a final check all 1.2 V supply voltages (analogue, digital, V_{ref}) were connected together and taken from a single source, while the V_{cm} was obtained from a resistive divider. Few example measurements were done for such simplified setting and no visible differences in the results were observed. This leads to the conclusion that for stable ADC power supply and good enough internal decoupling, the additional reference voltage may not be required. This issue will be studied further in the future for multi-channel operation.

The detailed study covering static and dynamic measurements, power consumption with its frequency scaling, and cross-talk are presented in the following sections.

3.1 Static INL and DNL measurements

The static measurements were performed at various sampling frequencies and with the input voltage ramped in the range from -1.2 V to 1.2 V. To eliminate the noise, the measurements were repeated several tens of thousand of times. The ADC performance was quantified with the integral non-linearity (INL) and differential non-linearity (DNL) measurements. Both parameters were obtained with the histogramming method [9].

The results obtained at 10 MHz and at 40 MHz sampling frequency are shown in figure 7. Very good linearity is observed and both INL and DNL stay almost completely within ± 0.5 LSB at both sampling frequencies.

As it was described in the ADC design a variable internal delay was implemented for bit processing. In figure 8(top) the INL and DNL non-linearities are presented as a function of the

2015 JINST 10 P11012

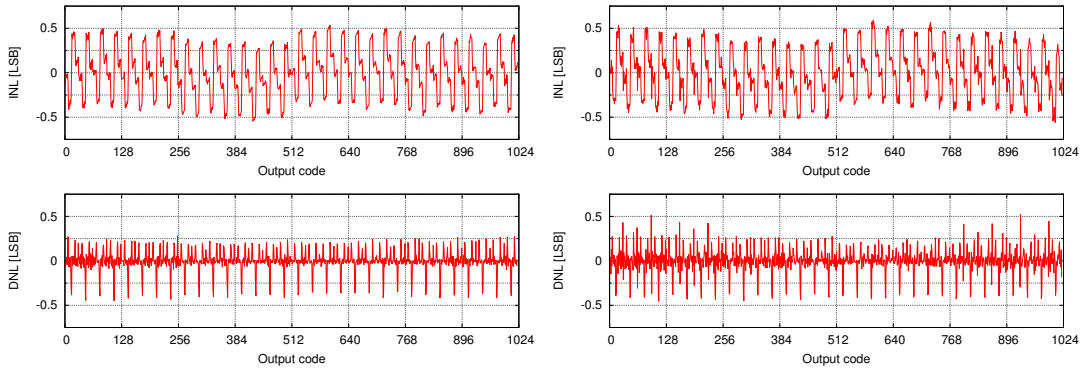

Figure 7. INL and DNL measured at 10 MHz (left) and at 40 MHz (right) sampling frequency and calculated using the histogramming method.

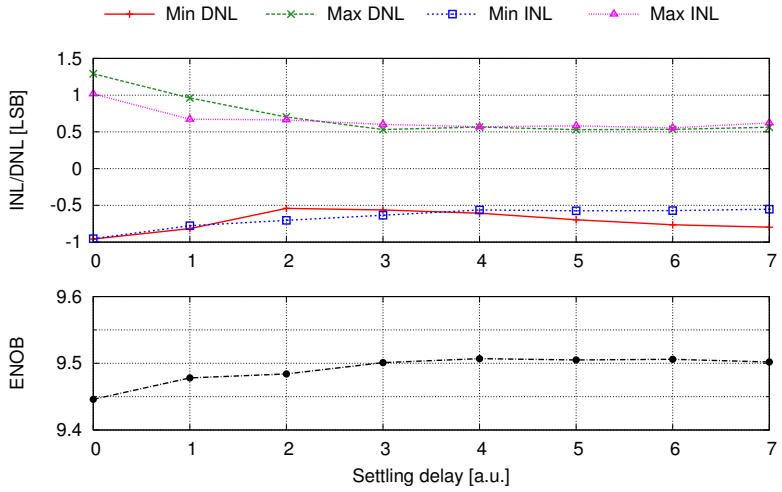

Figure 8. Top: INL and DNL measured at 10 MHz sampling frequency versus internal delay. Delay is plotted in arbitrary units — there are 3 bits and so 8 delay values are possible; bottom: static ENOB versus delay.

delay (in arbitrary units) at 10 MHz sampling frequency. The change of the delay by one corresponds roughly a 200 ps change in single bit processing time (about 1.8 ns in total conversion time). It can be seen that for the shortest delays the non-linearities are higher since the ADC has not enough time to charge the DAC capacitances. For the delay above 2 the INL and DNL almost saturate at the best values. On the basis of INL results one can calculate the static effective number of bits [10]:

$$\mathrm{ENOB}_{\mathrm{static}} = \log_2\left(\frac{N}{\sqrt{12\cdot\left[12^{-1}+(N-2)^{-1}\cdot\sum_{k=1}^{N-2}INL_k^2\right]}}\right), \tag{3.1}$$

where N is the number of ADC codes. As shown in figure 8(bottom), for high enough delay it saturates at about 9.5 bits. This very good static performance may be very useful for applications of the ADC for monitoring of (almost) DC signals. Although the ADC was designed for high rate

2015 JINST 10 P11012

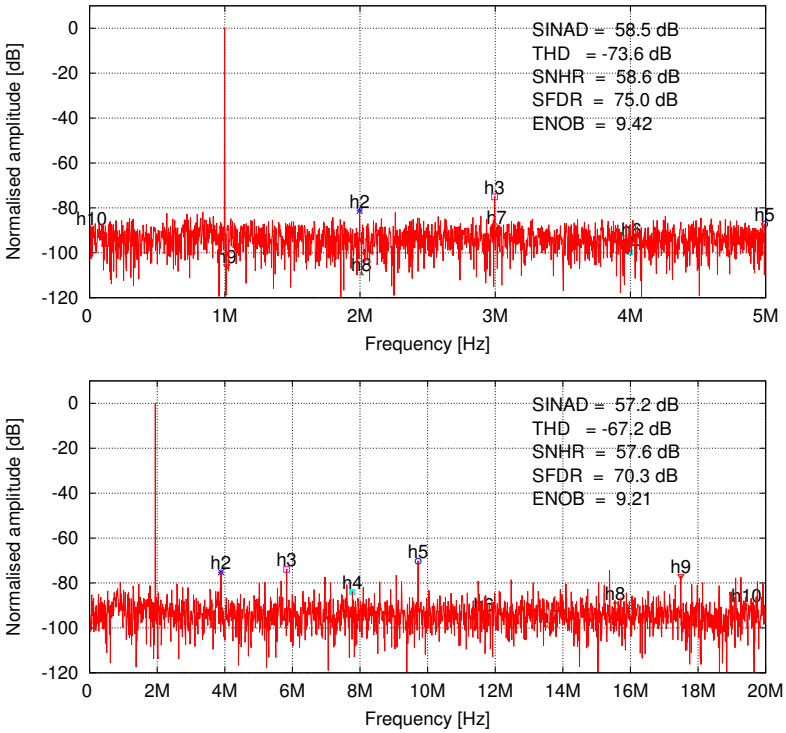

Figure 9. Example of DFT measured at 10 MS/s for 0.998 MHz input frequency (top) and at 40 MS/s for 1.943 MHz input (bottom). Harmonic frequencies are marked on the plots.

conversion, its ultra-low and frequency scalable power consumption allows also for its use in lower rate applications.

3.2 Dynamic parameters measurements

To evaluate the dynamic ADC performance, Discrete Fourier Transform (DFT) spectra were calculated from the measurements done with a sinusoidal input signal [9] (using Agilent 81150A arbitrary waveform generator). An optimum ADC internal delay was used for the selected signal frequency. A standard ADC metrics like SNHR, THD, SFDR, and SINAD are calculated to quantify the ADC dynamic performance. Two examples of the measured DFT spectrum for 10 MS/s rate at 0.2 Nyquist input frequency and for 40 MS/s at 0.1 Nyquist input frequency are shown in figure 9. For these measurements the setup was optimised (internal ADC delay, filtering of input signal) for highest performance at the chosen input frequencies. The obtained dynamic parameters values of SNHR, THD, SFDR and SINAD confirm very good ADC performance corresponding to the effective number of bits 9.42 at 10 MS/s and 9.21 at 40 MS/s.

The dependence of dynamic DFT metrics on ADC sampling frequency was studied in detail for moderate input signal frequencies. The measurements of dynamic metrics and ENOB as a function of sampling frequency for 0.1 of Nyquist input frequency are shown in figure 10(top). It is seen that all metrics are rather flat and the ENOB decreases very little from 9.3 bits at low sampling frequencies to 9.2 bits at 40 MHz sampling. The measurement was done with the internal ADC delay optimised for highest ENOB at 40 MS/s, so the results at lower sampling rates are slightly

2015 JINST 10 P11012

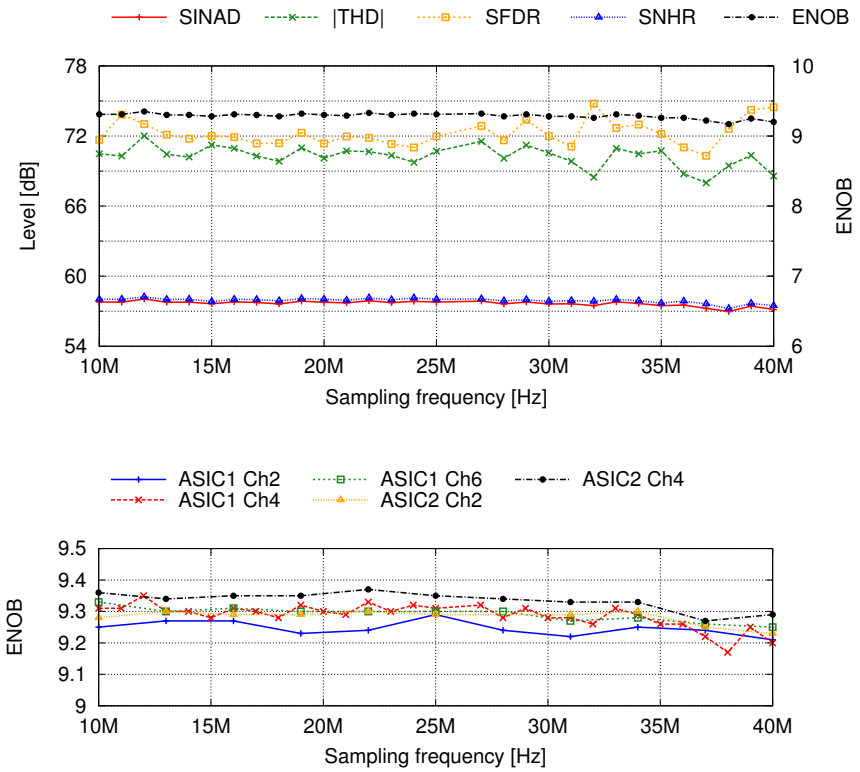

Figure 10. ADC dynamic performance as a function of sampling frequency obtained with 0.1 Nyquist input signal frequency. All dynamic metrics for single channel (top), and ENOB for five channels in two ASICs (bottom).

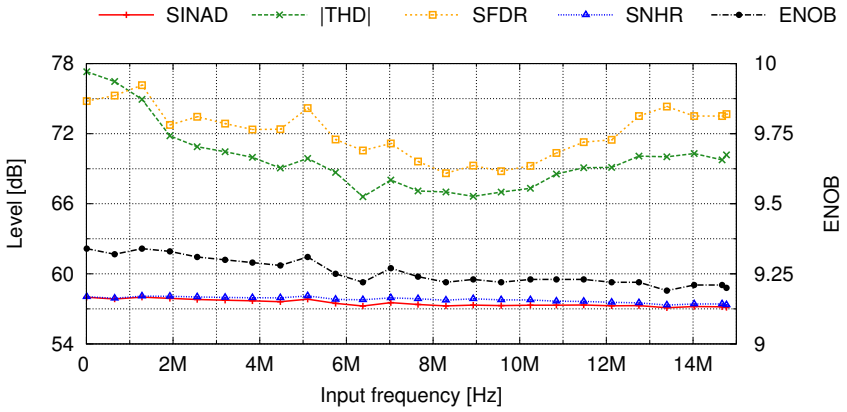

Figure 11. ADC performance as a function of input signal frequency at 30 MHz sampling frequency.

lower than best possible ones. It was verified that significant ENOB decrease starts above 43 MHz. In figure 10(bottom) the ENOB measured for few channels of two prototype ASICs is presented, confirming a good channel to channel uniformity.

The ADC performance was also studied as a function of input signal frequency. The measurements of dynamic metrics and ENOB versus input frequency are shown in figure 11 for 30 MHz sampling frequency. The SINAD is practically equal to SNHR what means that the resolution is limited by noise, while harmonic distortions may be neglected. The ENOB is almost flat and

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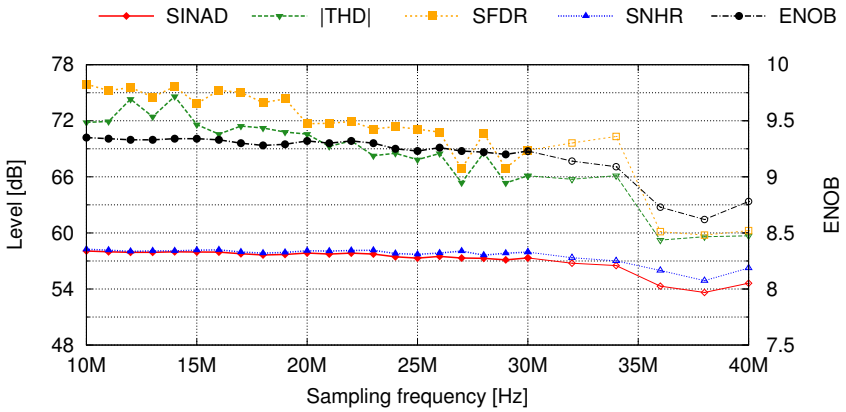

Figure 12. ADC dynamic performance as a function of sampling frequency obtained for Nyquist input signal frequency. Measurements above 30 MHz were done with modified, less precise setup.

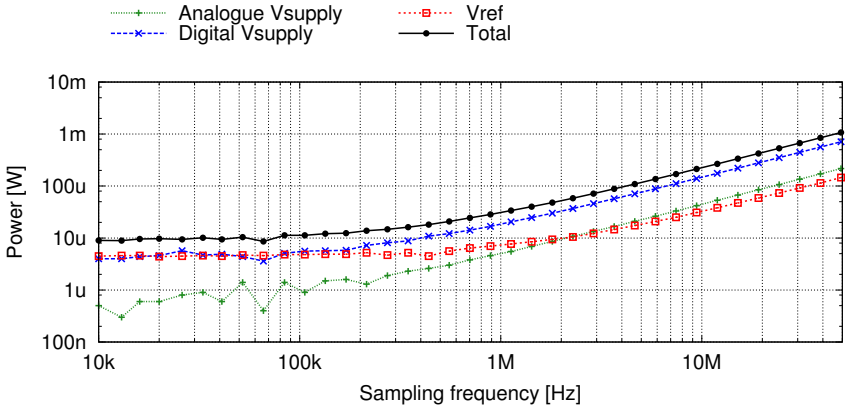

Figure 13. ADC power scaling with sampling frequency.

decreases slightly from 9.34 bits at the lowest input frequency to 9.2 bits at Nyquist input frequency. It confirms that for sampling rates up to about 30 MS/s the ADC maintains very high resolution (above 9 bits) even for highest (Nyquist) input signal frequencies. For higher sampling frequencies the ADC continues to work well (as was shown in figure 10) but for high frequency input signals the effective resolution starts to decrease. It is demonstrated in figure 12 where the dynamic metrics are shown versus sampling frequency at Nyquist input frequency. When approaching 40 MS/s sampling rate the ENOB decreases below 9 bits. It should be noted here that it was not possible with the standard setup to measure the dynamic metrics above 30 MS/s at Nyquist input frequency, because of the limited amplitude of sine generator. To perform this measurement the filter bandwidth was increased and few more points were taken in such less optimised setup. For this reason, and possible worse purity of input sine signal at higher frequency, the precision of these points may be worse than for the lower frequency part.

3.3 Power consumption and scaling with sampling rate

The ADC is designed to allow a linear scaling of power consumption with sampling frequency. The measured power consumption versus sampling frequency is shown in figure 13. The results shown in

2015 JINST 10 P11012

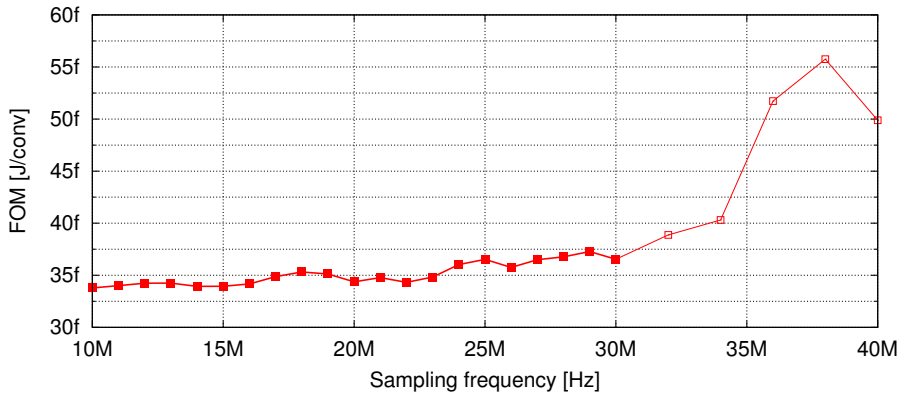

Figure 14. FOM versus sampling frequency. Results above 30 MHz were obtained with modified, less precise setup.

figure 13 are obtained for measurements at Nyquist input frequency. The measurements cover much wider low frequency range than the results presented in previous sections. We have not studied in detail the performance below 10 MS/s but we have done few lower frequency measurements which are consistent with other results. A few observations can be drawn looking at the results shown in figure 13:

- The ADC power consumption scales over two orders of magnitude from about 10 μW, for low rate operation, up to almost 1 mW, at 40 MS/s. Starting from few hundred kS/s the power consumption scales linearly with sampling frequency.
  - In the region of linear scaling the ADC consumes about 22 μW/MS/s.
  - For sampling rates below 100 kS/s the power consumption saturates at about 10 μW. Since the designed ADC does not consume static power it means that this 10 μW limit comes from leakage currents.
- The main contribution to the power consumption comes from the digital part. The analogue operation, and in particular the DAC switching scheme, is so power efficient that for further power decrease one needs to focus on the optimisation of digital part or/and use a smaller size technology.

To estimate the power efficiency of our design and compare it to other designs one can calculate the most commonly used figure of Merit (FOM) [11]:

$$\mathrm{FOM} = \frac{\mathrm{Power}}{2^{\frac{\mathrm{SINAD}-1.76}{6.02}} \cdot f_{\mathrm{sample}}}, \tag{3.2}$$

where SINAD is measured for Nyquist frequency of input signal. The obtained FOM is plotted in figure 14. For sampling frequencies between 10 MHz and 30 MHz the FOM varies between 34-37 fJ/conversion what places the discussed ADC within the best State of the Art designs, for similar specifications. For higher sampling frequencies FOM starts to increase but even at 40 MHz it is of the order of 50 fJ/conversion, which is an excellent result.

One can estimate the power drawn by the ADC in experimental conditions of linear collider. As an example lets take the ILC with 3.5 MHz bunch train frequency and 1% duty factor in power

2015 JINST 10 P11012

cycling. In such conditions the ADC instantaneous power is around 100 μW, so with power cycling one gets 1 μW. But since the ADC power consumption saturates at 10 μW, the realistic average power consumption would be around 11 μW. For a single barrel of luminosity detector with ~92000 channels, the average ADC contribution to the total power consumption would be around 1 W, which is a very small value.

3.4 Cross-talk between ADC channels

In this paper we report on single ADC channel performance, although, as it was mentioned at the beginning, the final goal is to build a multi-channel readout system with ADC in each channel. For this reason a small ADC pitch was chosen and 8 channels were placed in parallel in the prototype ASIC. An undesirable effect in multi-channel circuits, particularly in mix-mode designs, is channel to channel cross-talk. To verify whether the presented design is resistant to the cross-talk dedicated measurements were done. A full-scale sinusoidal input signal was sent to selected channel and the outputs of two closest neighbour channels, which had a DC signal on their inputs, were observed and their *rms* was measured. It was found that the output of each of two neighbours was fluctuating between two ADC codes (corresponding to the DC input) with *rms* below 0.5 LSB, independently whether the sine signal was or was not present in the channel between them. From this simple check we can conclude that the design is enough cross-talk resistant to continue with multi-channel integration.

3.5 Comparison to state of the art ADCs

To the authors knowledge, up to now no ultra-low power, fast 10-bit ADC for multi-channel readout electronics of particle physics detectors was designed and published. In the existing readout systems for particle detectors [12, 13] the power consumption is at least an order of magnitude higher than in the State of the Art designs. For this reason our work is compared with the State of the Art ADCs, with similar technology and specifications, taken from the best engineering papers. The comparison of the key parameters is presented in table 1. The fact that only for our design a wide range of sampling frequencies is given does not mean that other ADCs do not have variable sampling frequency. They are usually designed for a specific sampling rate and so such feature is not studied. In the last four rows the figures of Merit are presented in two different ways: first, the ENOB and FOM are calculated in a standard way for Nyquist input frequency; second, since various authors present and compare the metrics obtained for lower input frequencies (usually from DC up to around 0.1 of Nyquist), the $\mathrm{ENOB_{LowFreq}}$ and $\mathrm{FOM_{LowFreq}}$ are also shown, to allow a better comparison at lower input signal frequencies. Since the measurements done in this work were not optimised for lower frequency input signals (input signal filtering and internal ADC delay were optimized for Nyquist frequency) we present only the results based on two example measurements shown in figure 9, for which such optimisation was done.

Looking at the FOMs showing the power efficiency of the ADC it is seen that all compared designs have the FOM, $\mathrm{FOM_{LowFreq}}$ between 29–79 fJ/conversion. In all important metrics our design is within the highest performance ADCs, i.e. smallest FOMs, highest ENOBs, smallest area, and the best linearity. It may be concluded that the performance of the presented ADC places it among State of the Art ADCs.

2015 JINST 10 P11012

Table 1. Comparison with State of the Art ADCs.

	[14]	[15]	[16]	[5]	[17]	This work
Architecture	SAR	SAR	SAR	SAR	SAR	SAR
Technology (nm)	130	130	130	90	90	130
Resolution	10-bit	10-bit	10-bit	10-bit	10-bit	10-bit
Supply (V)	1.2	1.2	1.2	1.2	1	1.2
Area (mm^2)	0.095	0.052	0.32	0.18	0.1	0.088
f_{sample} (MS/s)	20	50	40	100	30	0.01–40
Power (μW)[(a)]	620	826	550	3000	980	220@10MS/s + 22/MS/s
Max INL (LSB)	0.47	1.36	1.55	0.86	1.32	~0.5
Max DNL (LSB)	0.34	0.91	0.78	0.79	0.88	~0.5
ENOB (bit)	9.32	$\lesssim$9[(b)]	8.11	8.6	8.68	9.35-9.2@10-30MS/s
FOM (fJ/conv.)	48	~32–35[(b)]	50	77	79	34–37@10–30MS/s
$ENOB_{LowFreq}$ (bits)	9.56	9.18	8.35	9.1	9.16	9.42–9.21@10–40MS/s[c]
$FOM_{LowFreq}$ (fJ/conv.)	41	29	42	55	57	32–37@10–40MS/s[(c)]

[(a)] In the quoted papers external reference voltage is used, usually it is power supply. No internal reference buffers are used.
[(b)] Exact ENOB and FOM are not given at Nyquist input frequency. A rough estimation from the plot is done.
[(c)] Example results shown in figure 9 are taken.

The reader should be aware of the fact that in table 1 we have limited the compared ADCs to those of similar specifications. A significantly lower FOM can be found for some ADCs designed in different technologies (smaller feature size), and/or different resolution (usually higher), and/or different sampling frequency (usually lower). An up-to-date information on State of the Art ADCs is maintained on the web by B. Murmann [18].

4 Conclusion

In this paper the design and measurements of an ultra-low and frequency-scalable power consumption 10-bit SAR ADC are presented. The prototype ADC has a pitch of 146 μm and occupies 0.088 mm^2, being ready for multi-channel integration. The ASIC is fully functional and the performed measurements confirm a good static (INL~0.5 LSB, DNL~0.5 LSB) and dynamic (SINAD ~58 dB) performance, which is reflected in ENOB between 9.2-9.35 bits. For DC signals the effective number of bits is even higher, in the range 9.42-9.5 bits. The ADC operates for sampling frequencies from 10 kHz to 40 MHz and the power consumption scales linearly with sampling rate (~22 μW/MS/s) over most of this range. This feature makes the ADC very flexible, allowing its use as a general purpose ADC. The ADC performance is confirmed by excellent FOMs 32-37 fJ/conversion for sampling frequencies 10-40 MHz, which place it within the best State of the Art designs. The scalable power, together with small pitch (and area), asynchronous operation, and power cycling extend the range of possible applications making the design very attractive for dedicated multi-channel readout systems digitising signals with the rate up to 40 MS/s. In particular, it is very favourable for future linear colliders (ILC/CLIC) readout systems where long idle times

2015 JINST 10 P11012

between bunch trains can be used for large power savings. In fact our next goal is such ultra-low power multi-channel 10-bit digitiser. For this purpose a fast power-efficient serialisation and data transmission circuitry needs to be developed and added.

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2015 JINST 10 P11012