A Fault Tolerant, Area-Efficient Architecture for Shor's Factoring Algorithm

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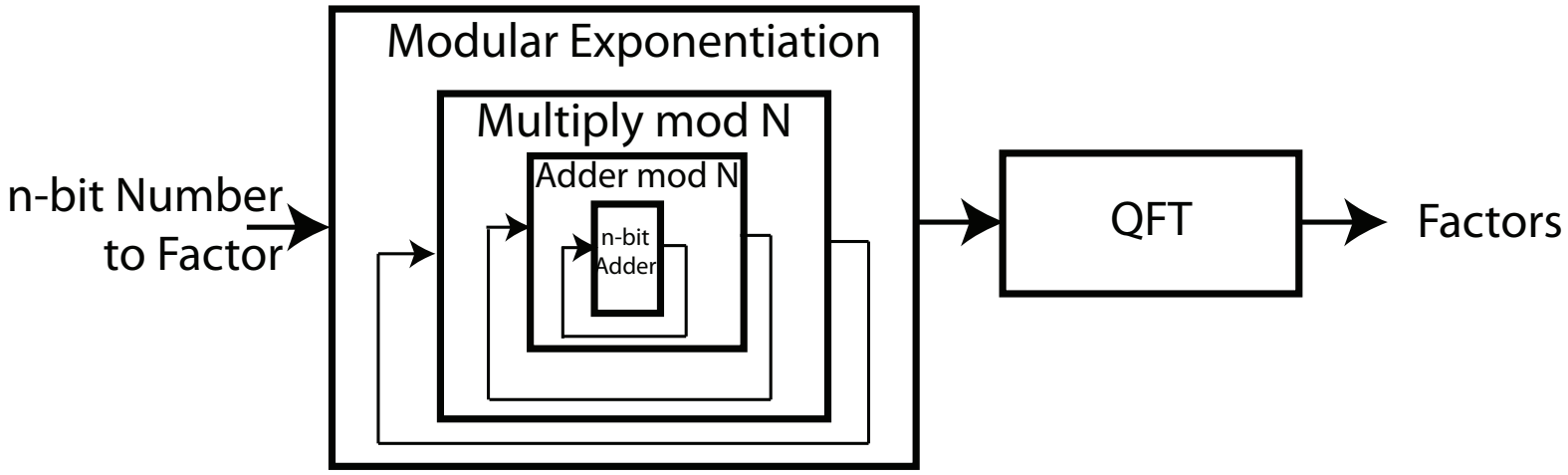
Univ. of California, Berkeley

June 23, 2009

Shor's Factoring Algorithm



- Killer app for quantum computing
  - Runtime polynomial in number of bits
- Key component to exponentiation: quantum adder
  - 1024-bit number: billions of operations, 100,000s of qubits
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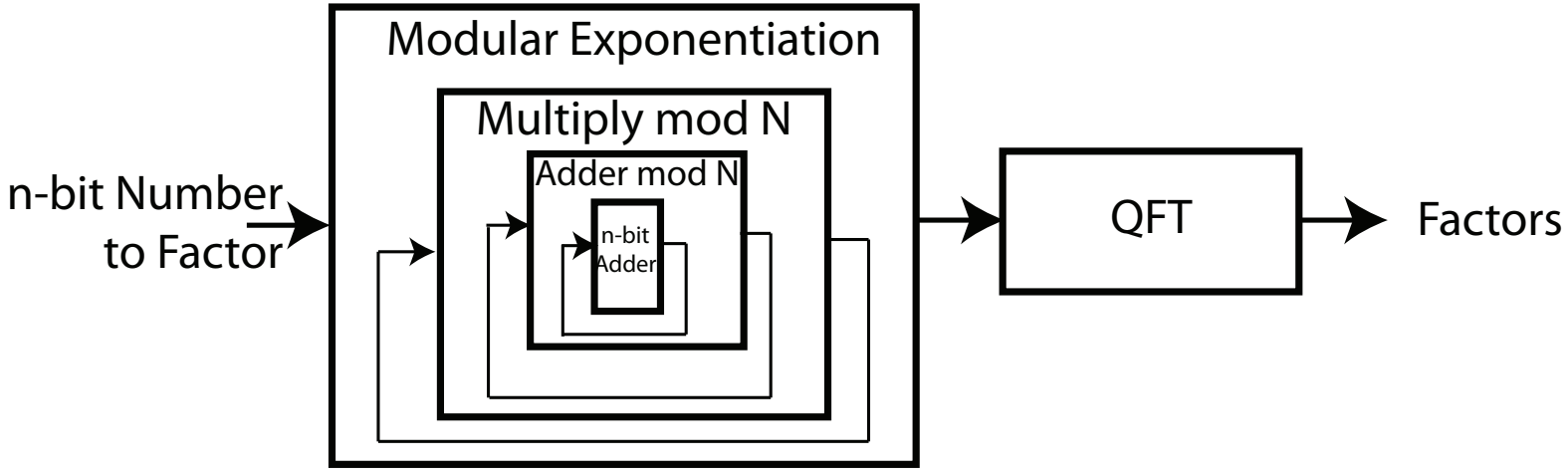

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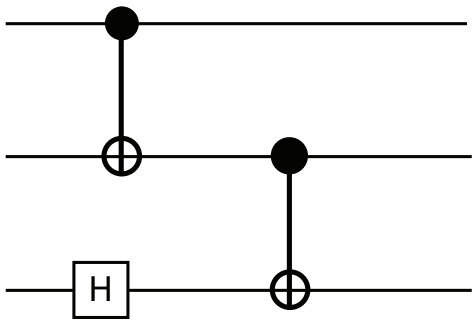
- High failure rates require strong fault tolerance
  - Previous area estimates for design were $0.9m^2$
  - 95% of operations are for fault tolerance

Quantum Fault Tolerance



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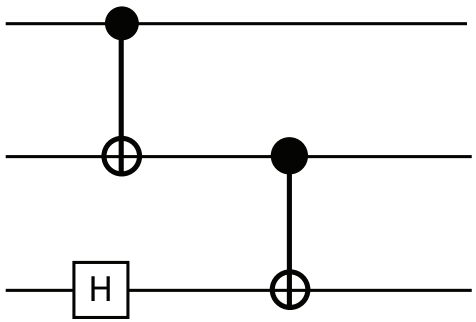

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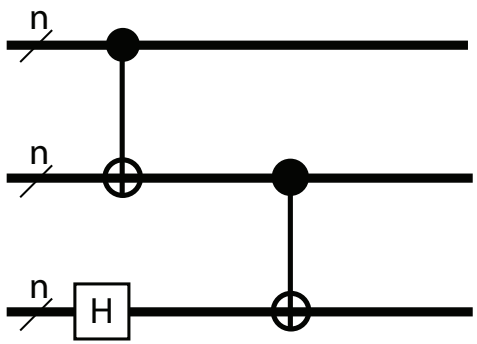

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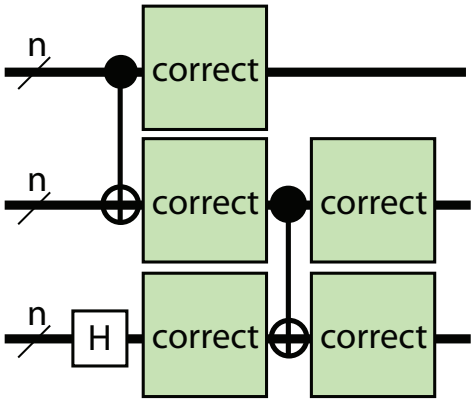

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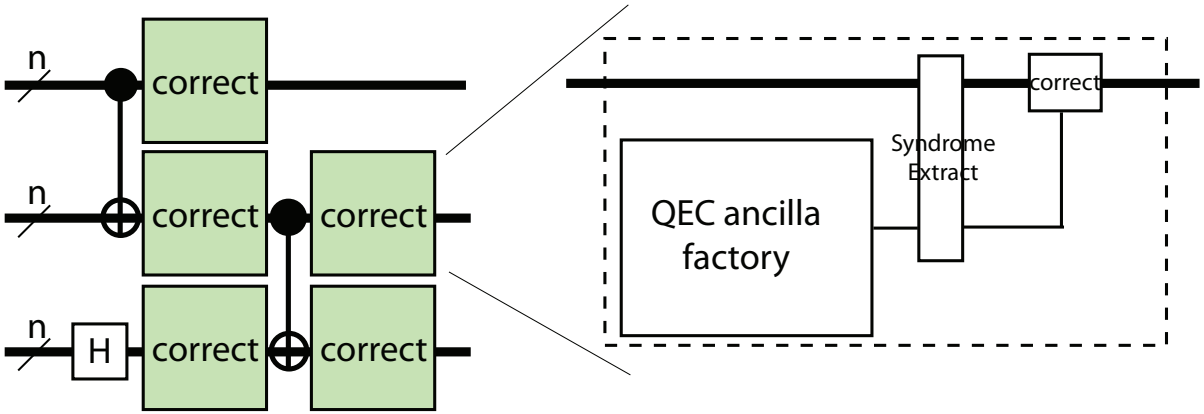

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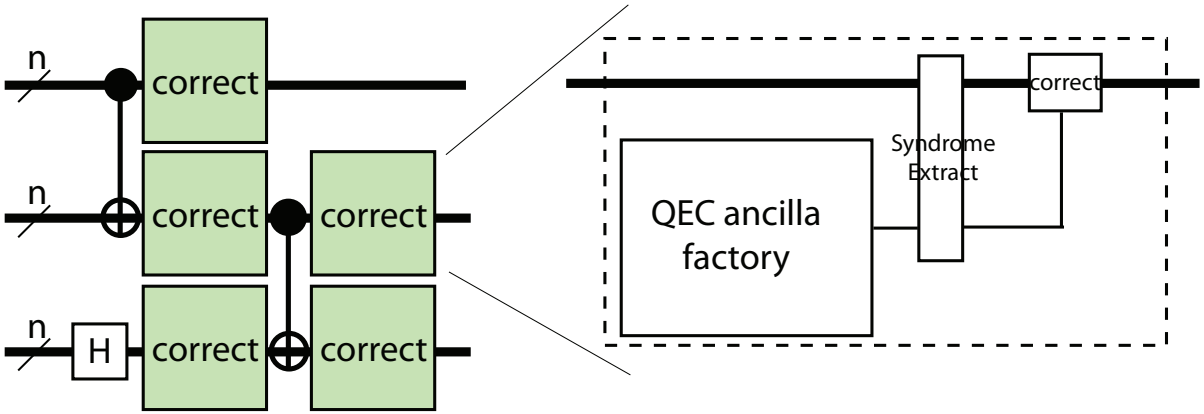

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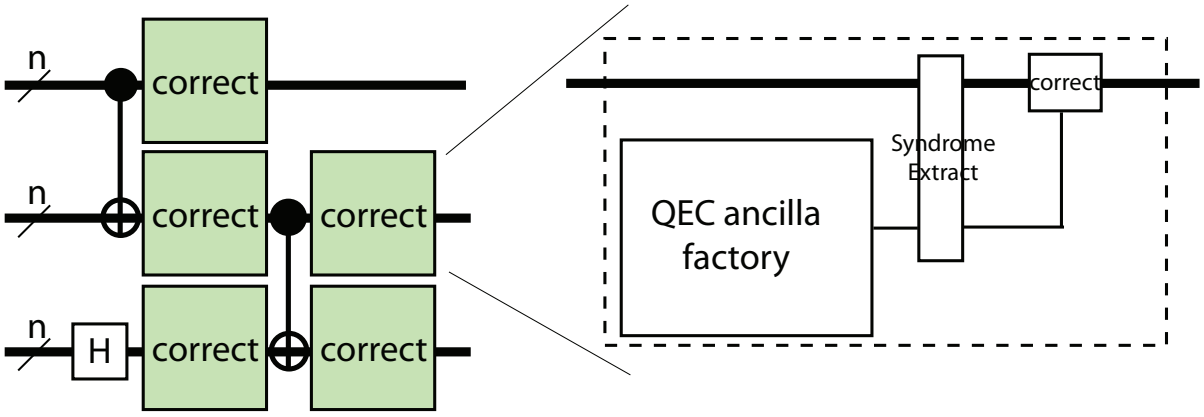

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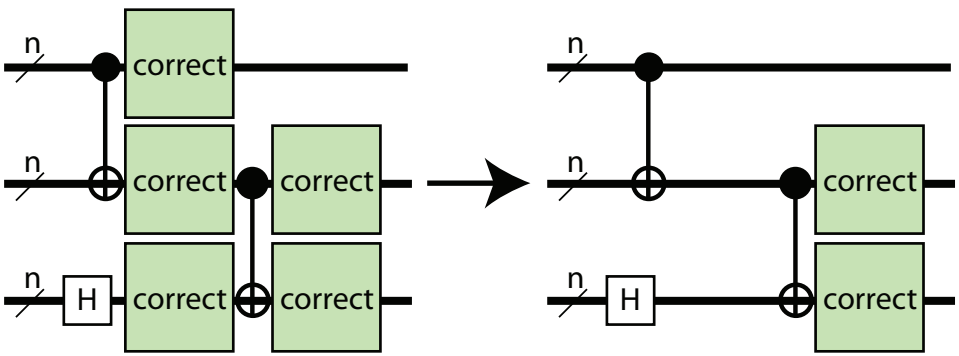
- $\geq$ 85% of all gates are ancilla production
- Efficient design requires managing ancilla production

Reducing FT Overhead

- 2 choices for reducing overhead:
  - Improve ancilla supply/make more efficient
  - Decrease demand for ancilla
- Our contributions:
  - Qalypso: flexible, efficient ancilla production
  - Error correction optimization to reduce correct steps



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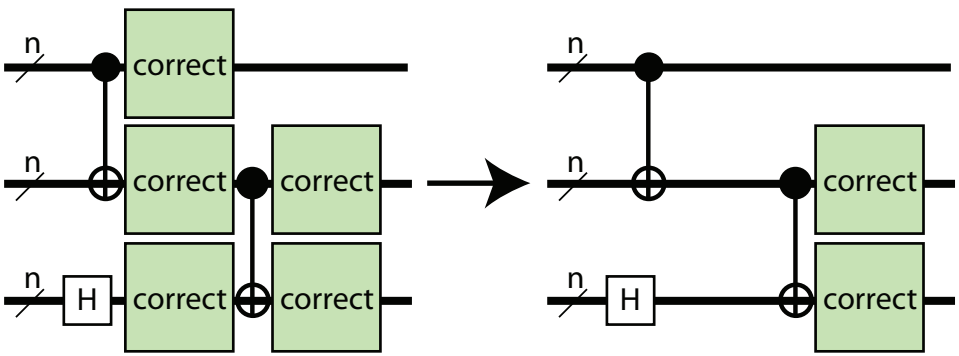
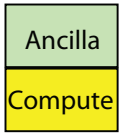


Tiled Quantum Architectures



- Compute and QEC ancilla regions in a single tile

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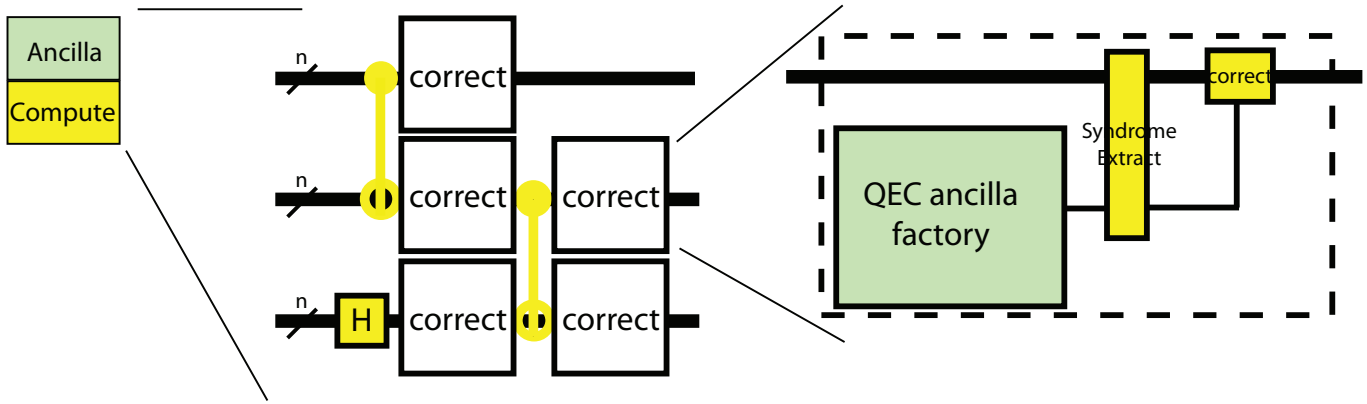

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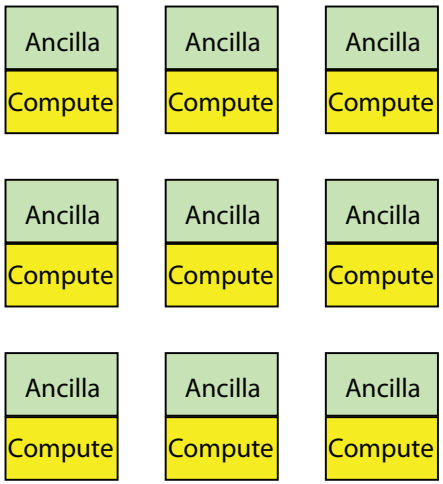

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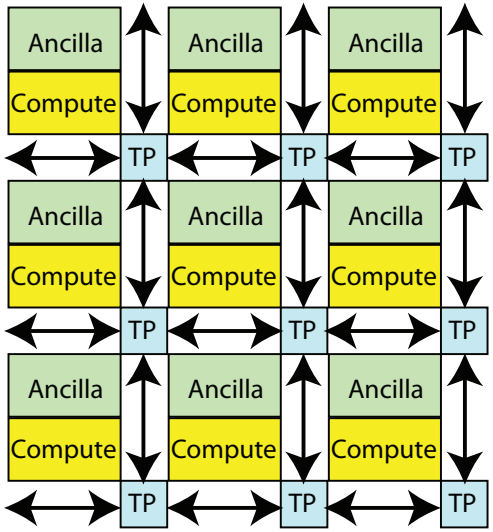

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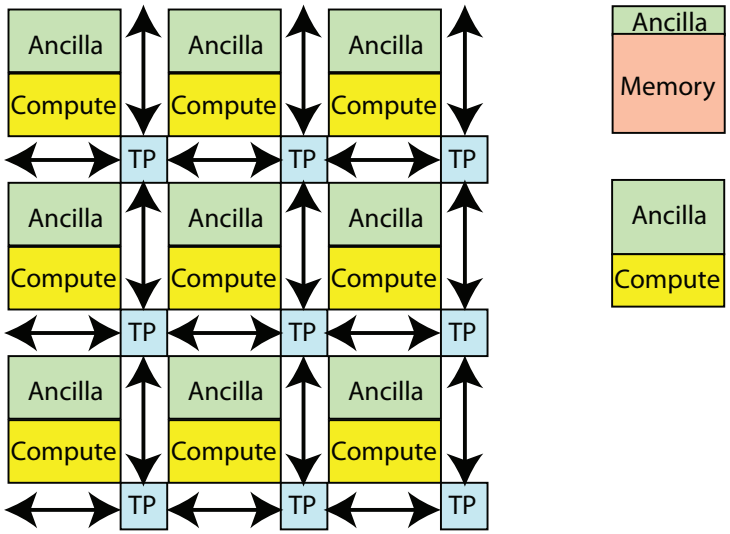

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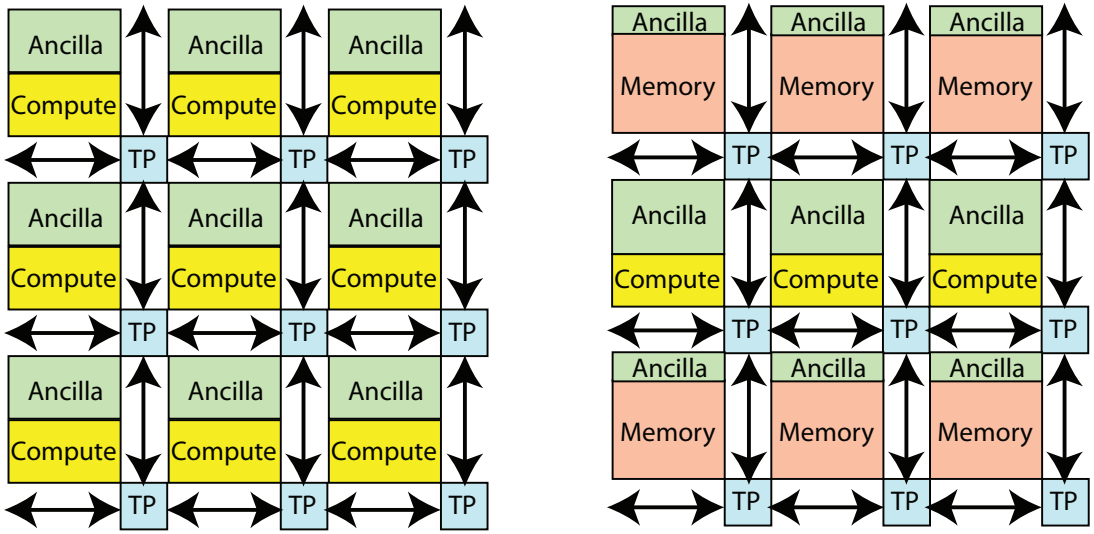

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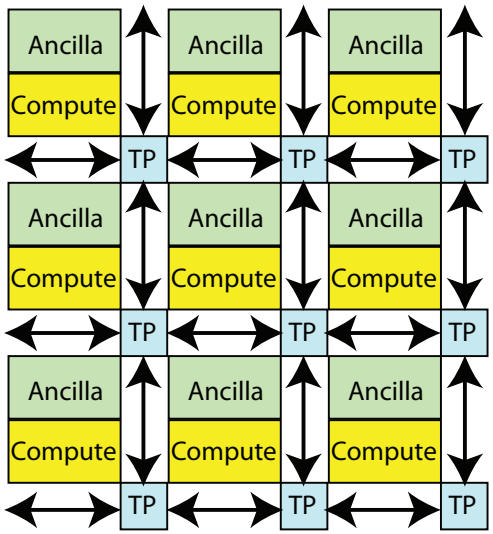

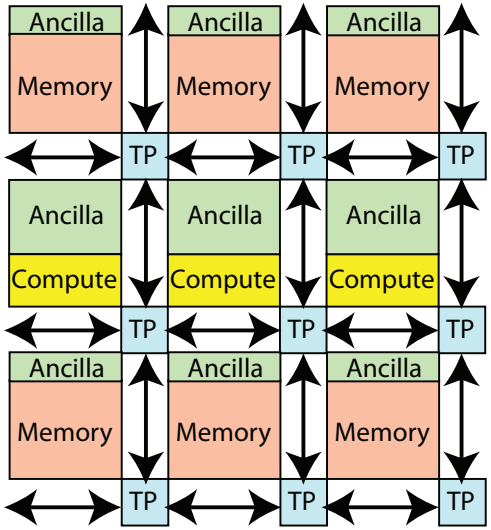

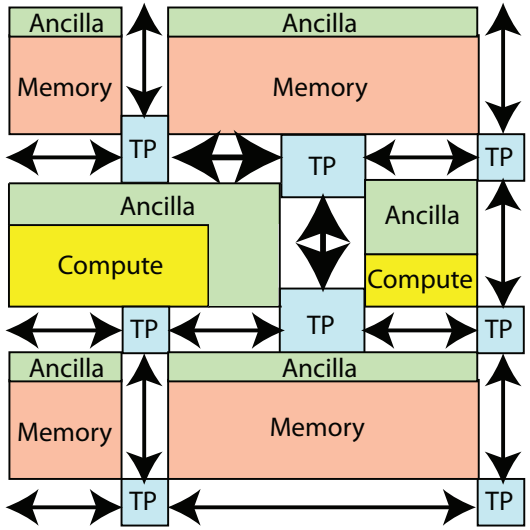

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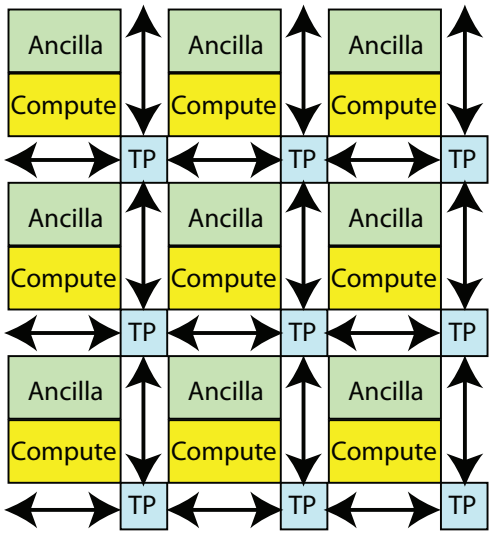

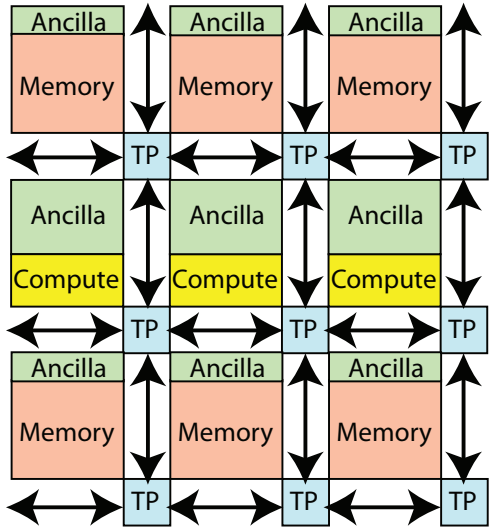

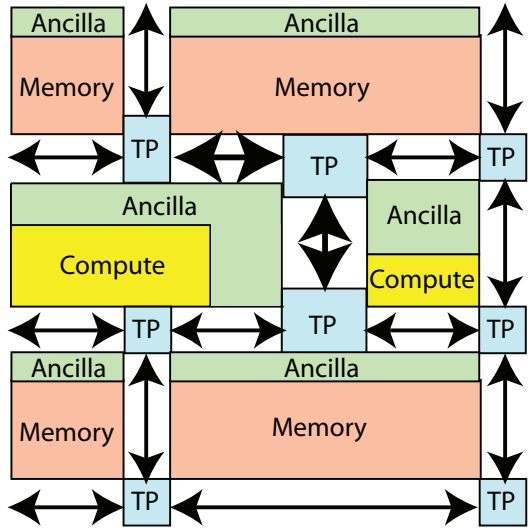

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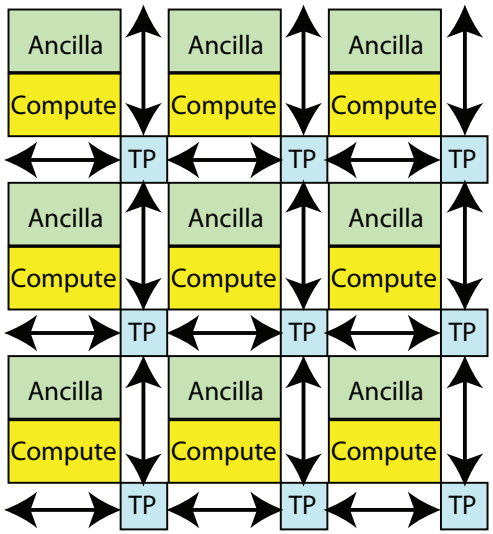

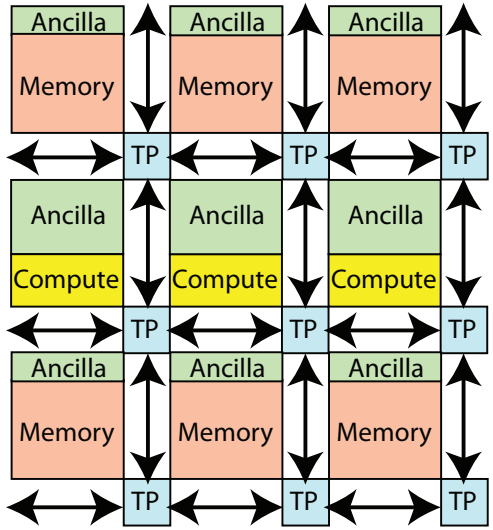

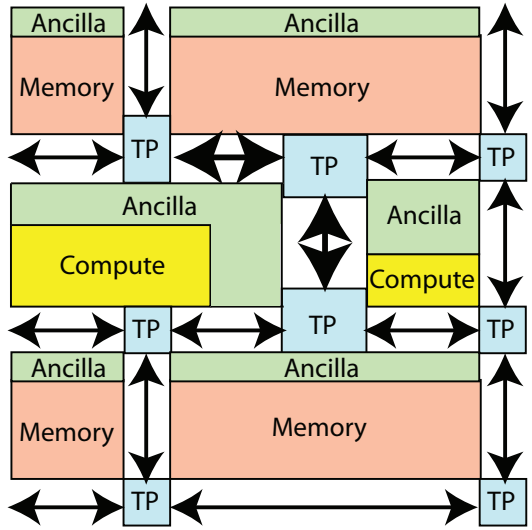

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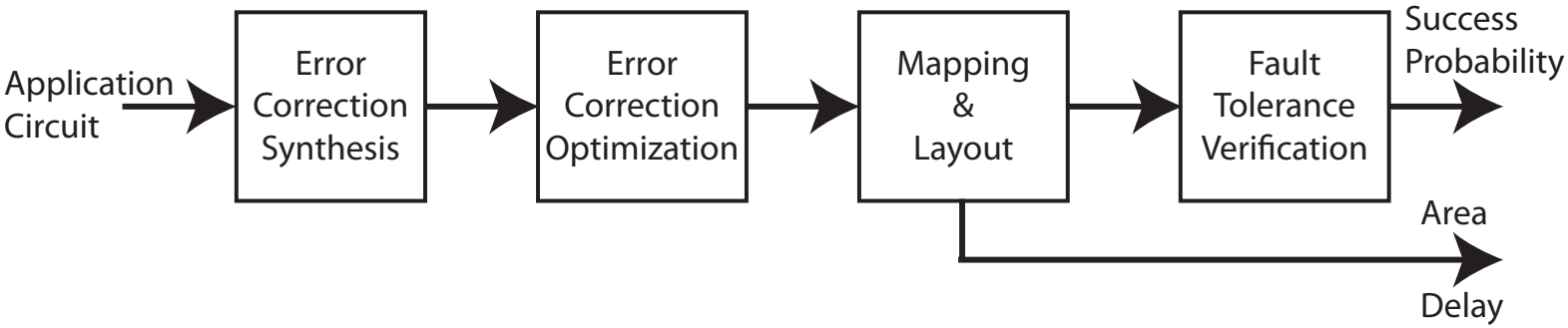
- Parameters: number of tiles, compute/memory distribution

Computer Aided Design Flow



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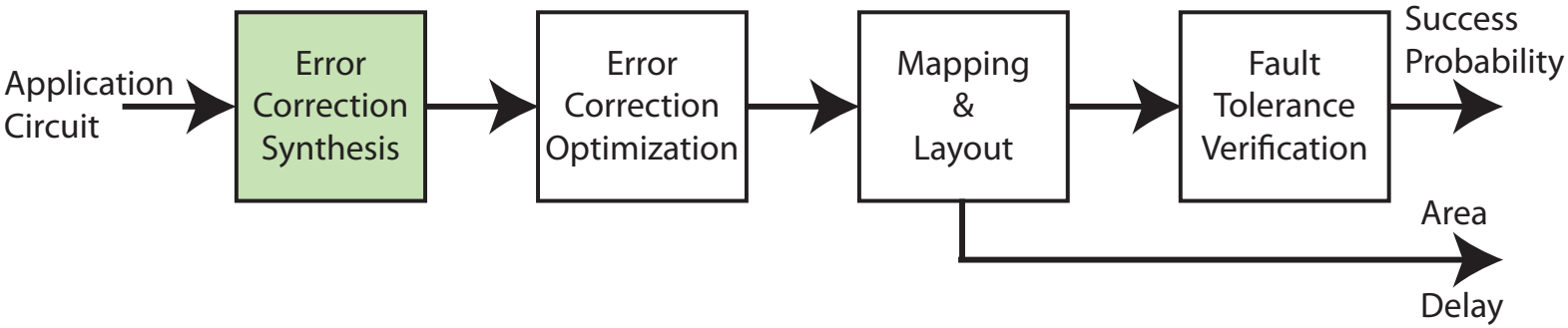

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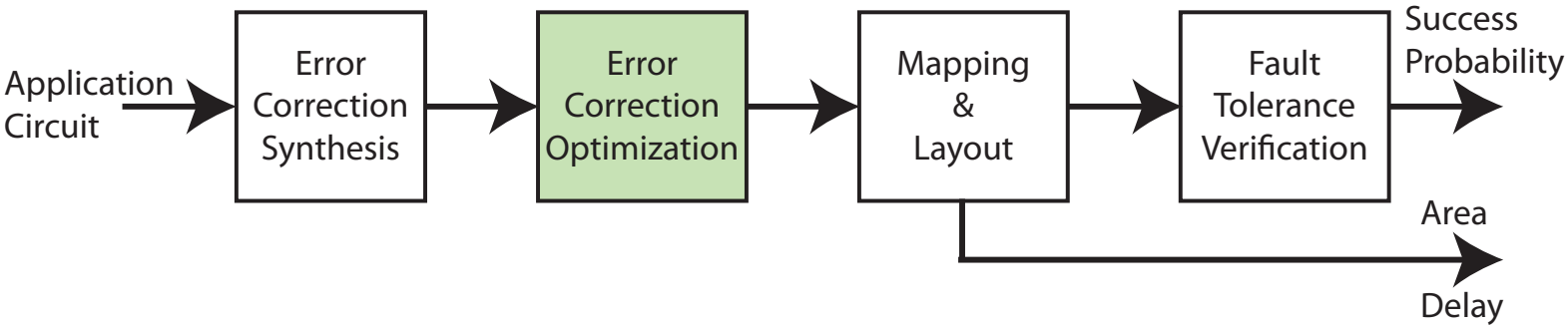

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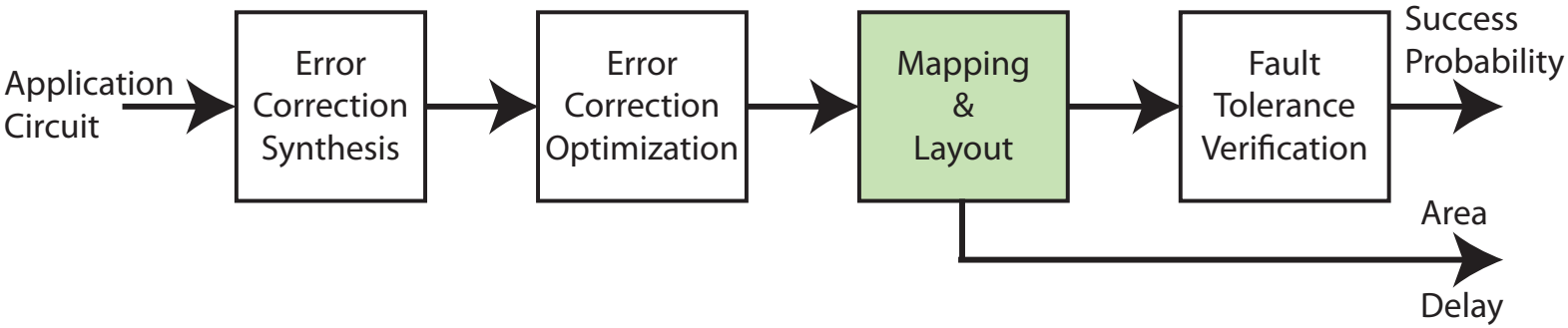

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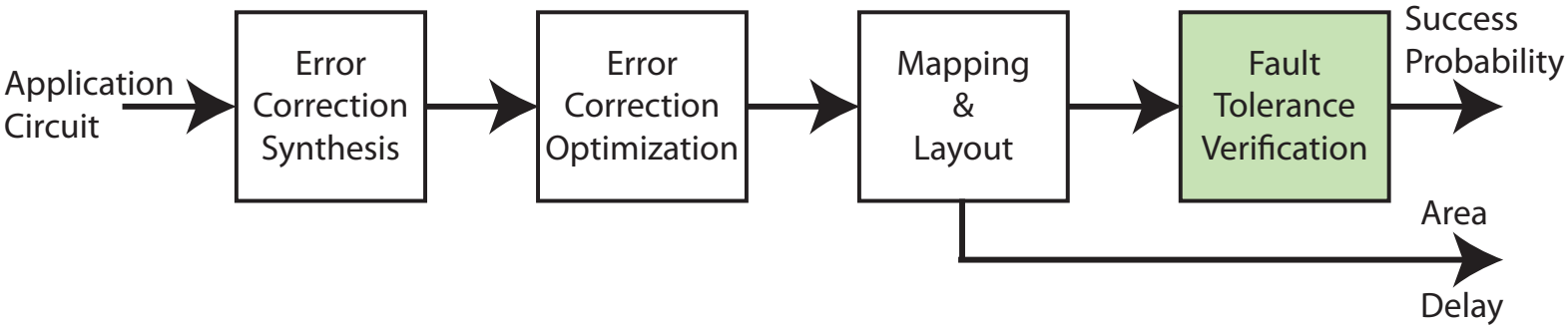

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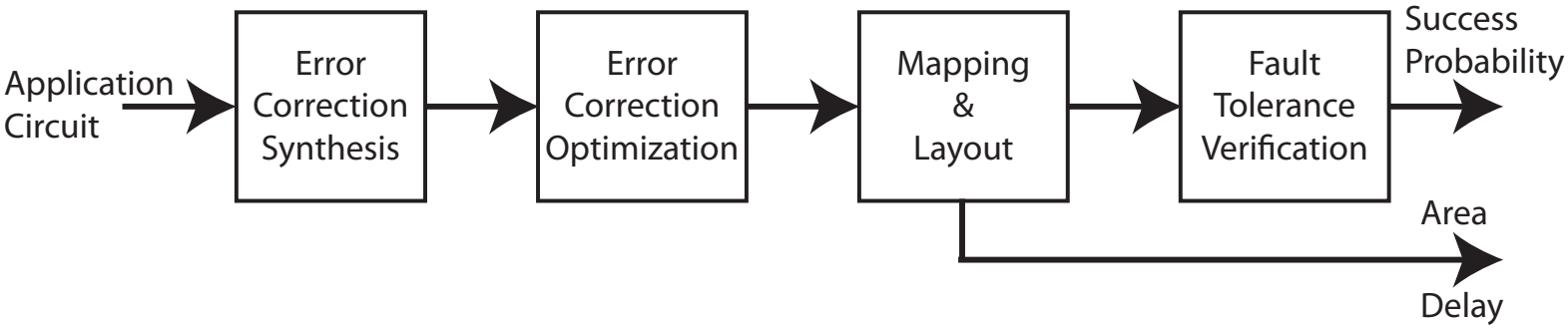

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- Advantages:
  - Detailed layout allows accurate comparison of designs
  - Can search large space of configurations

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- $ADCR_{optimal}$: best ADCR for over all possible configurations

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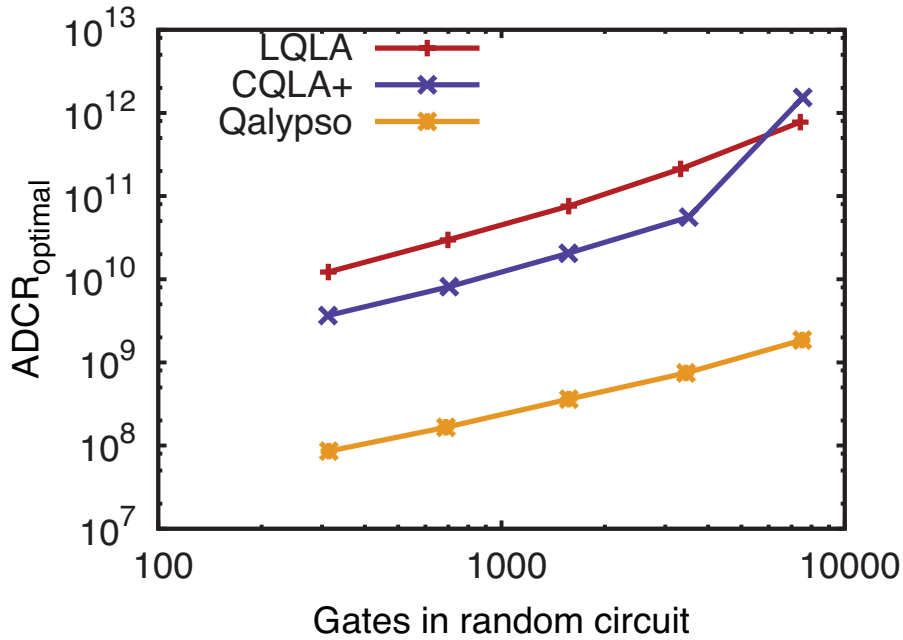

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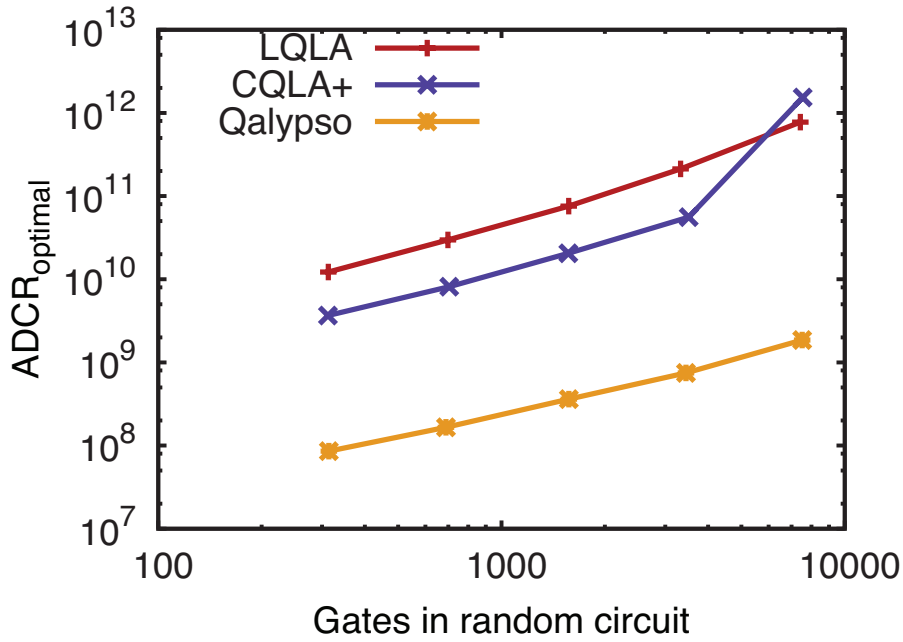

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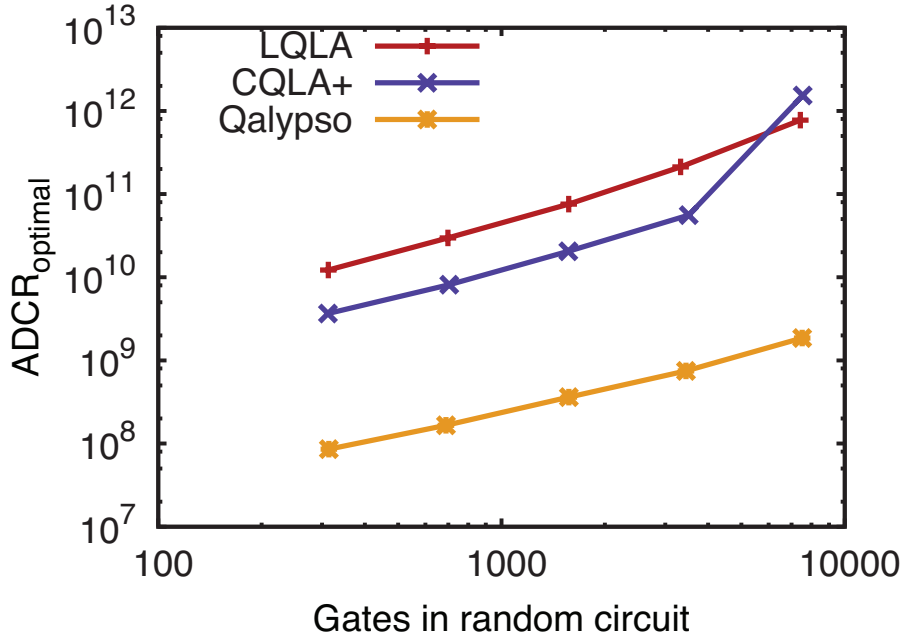

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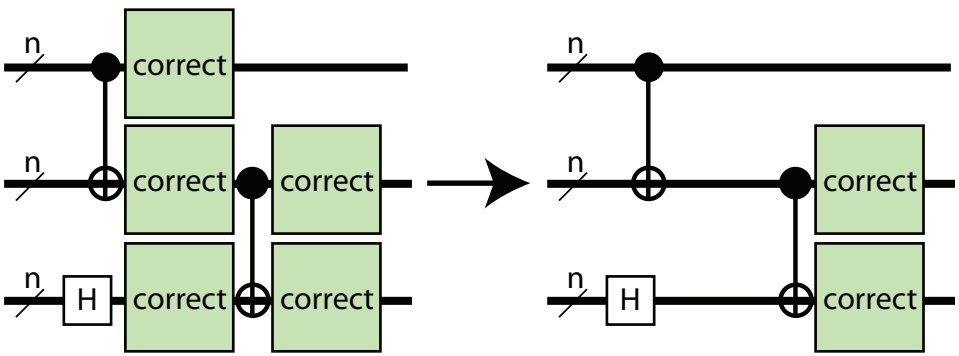

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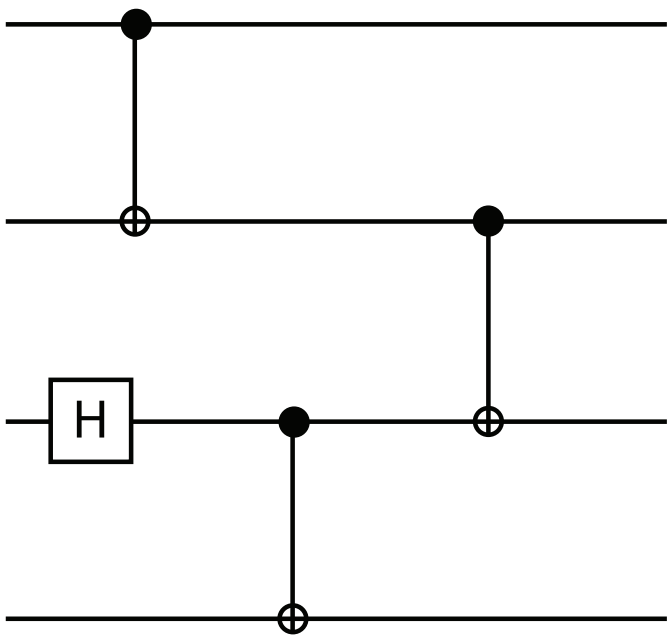

Reducing QEC Overhead

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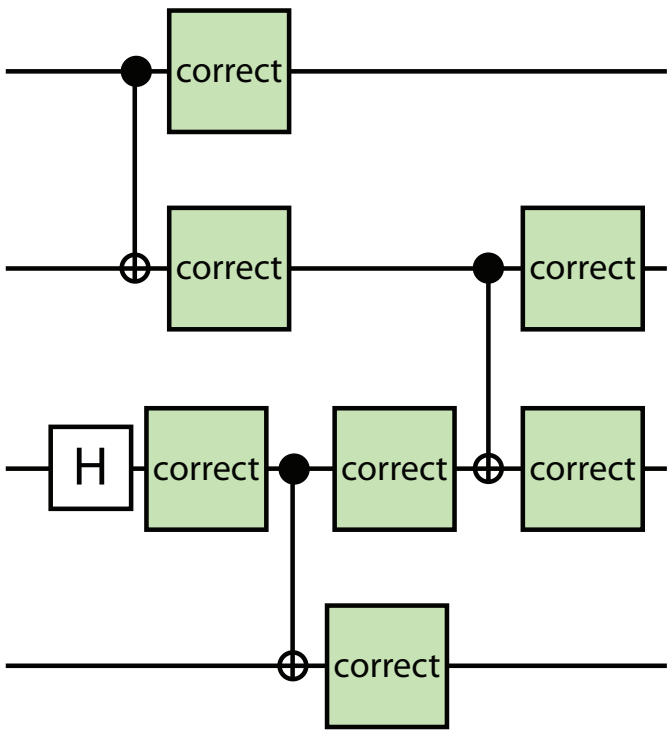

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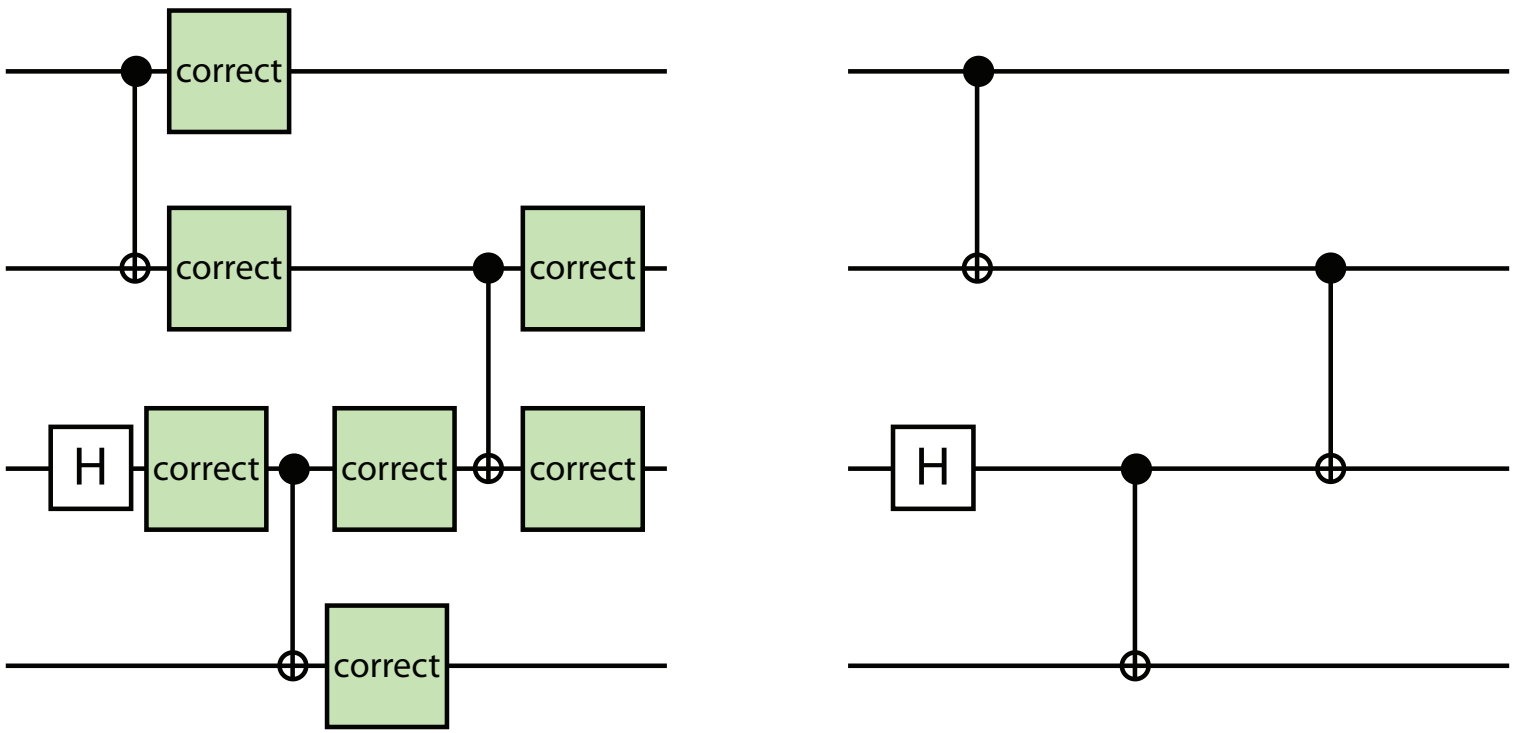

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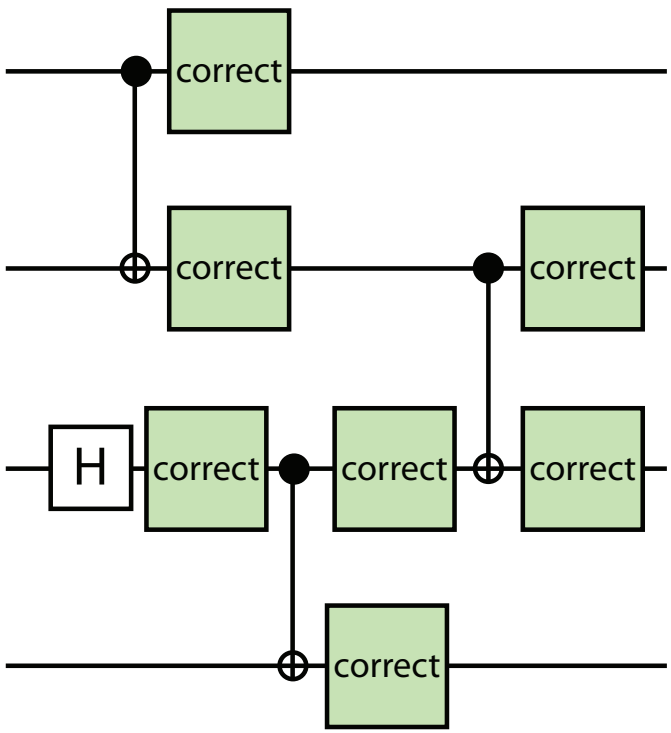

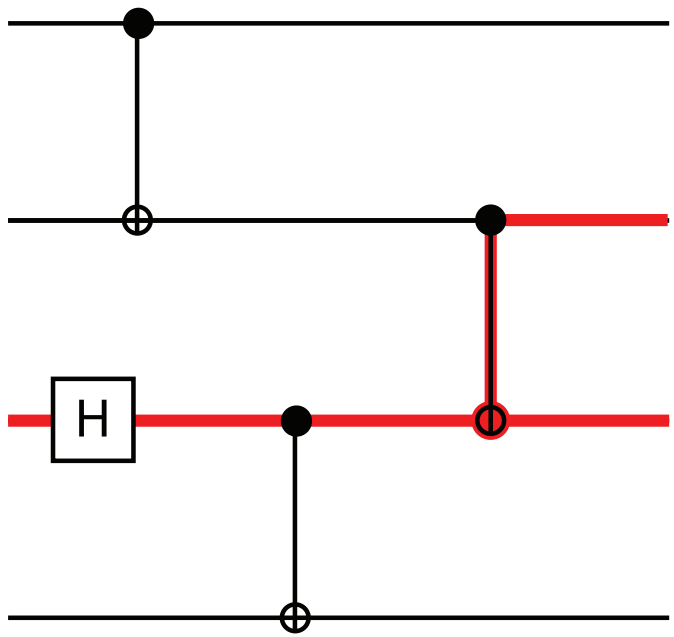

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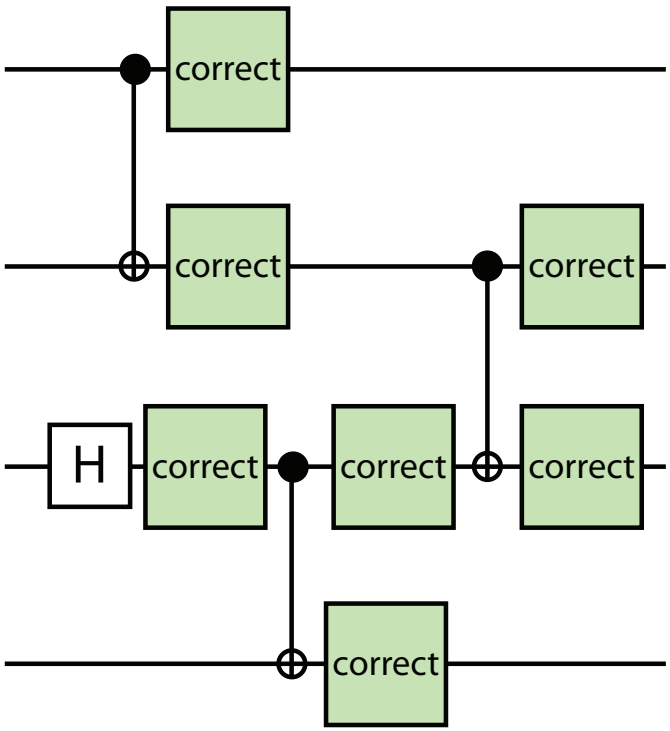

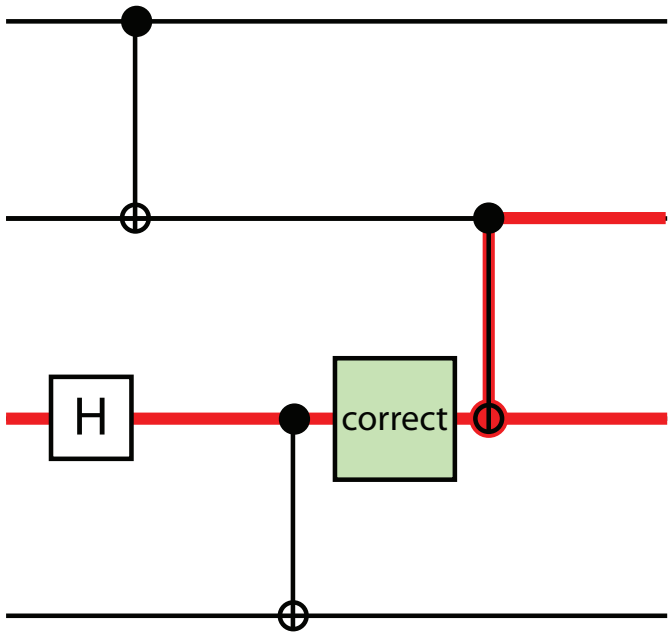

Simple Error Model for FT Circuits

- Identifying critical error paths

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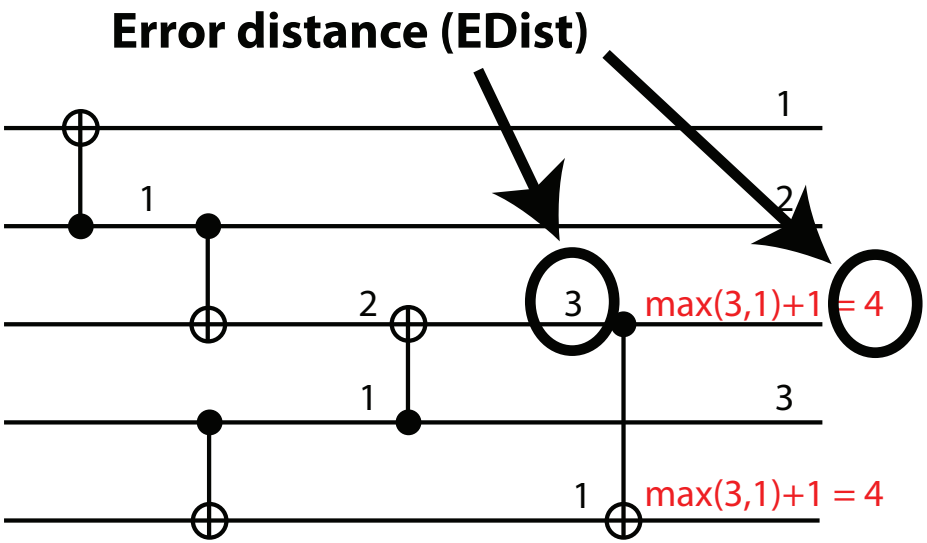
  - Gates propagate max input error distance to all outputs
  - Gates add 1 to error distance



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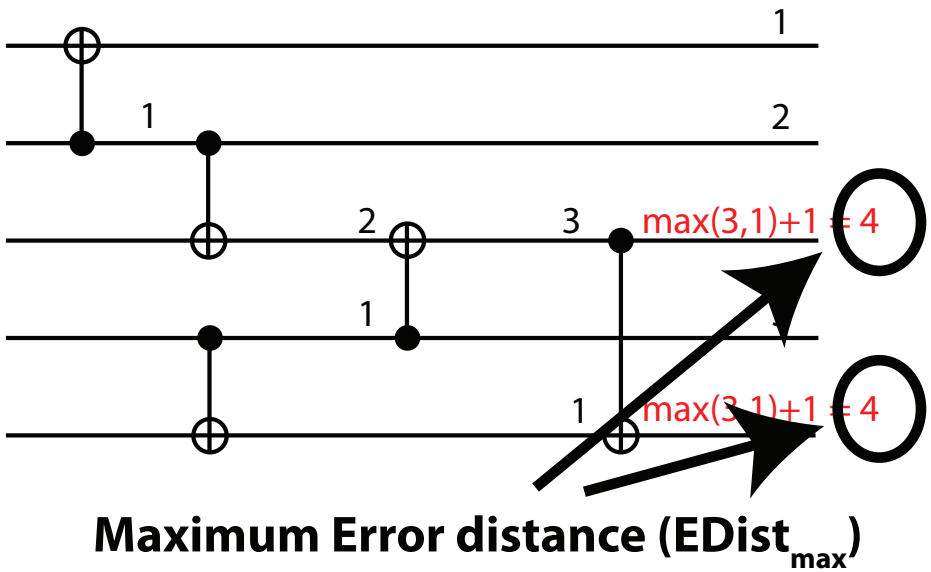

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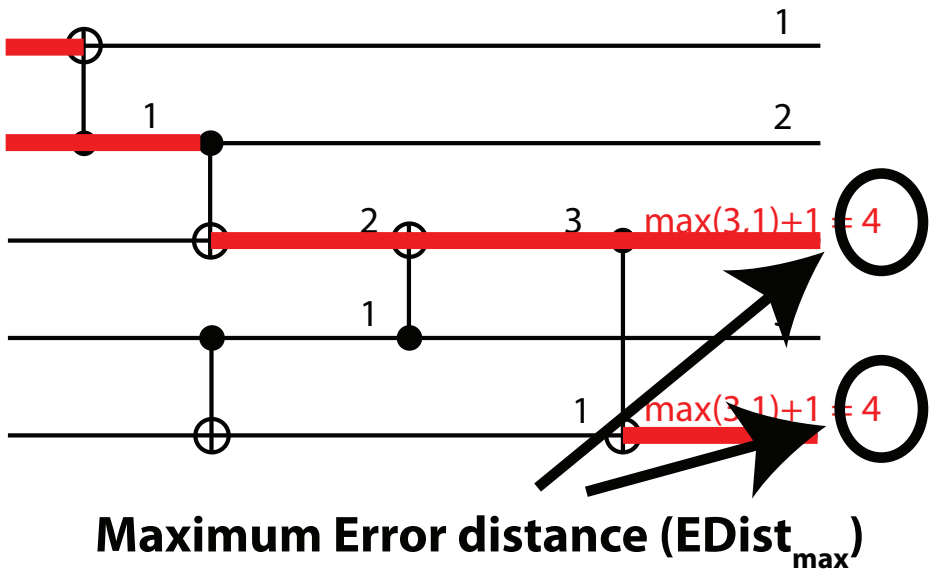

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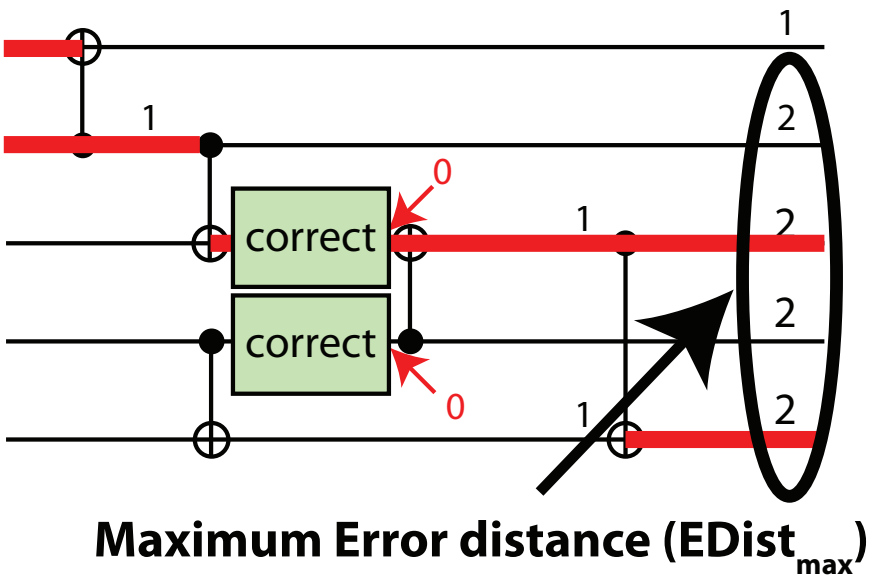

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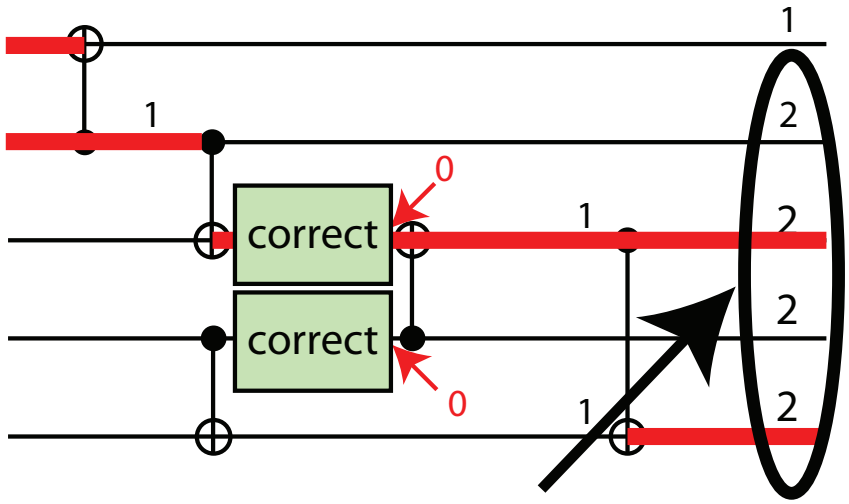
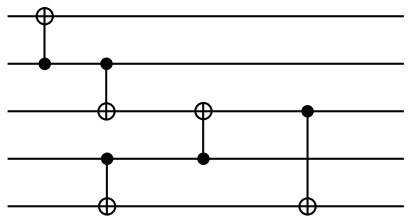


Maximum Error distance ($EDist_{max}$)

- Similar to delay in synchronous circuits
- Apply classical retiming approach: recorrection
  - Corrections balance EDist $\rightarrow$ Synch registers balance delay

QEC Optimization Through Circuit Recorrection



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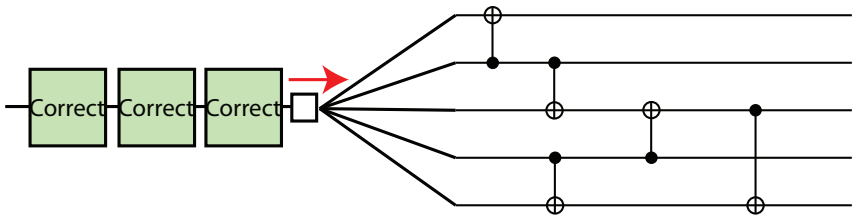

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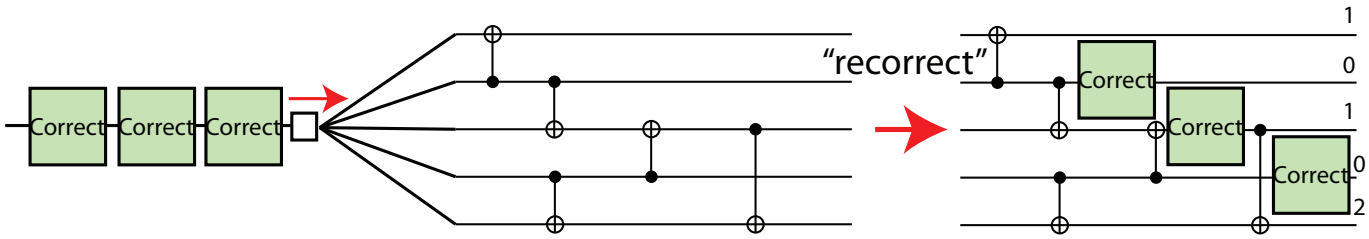

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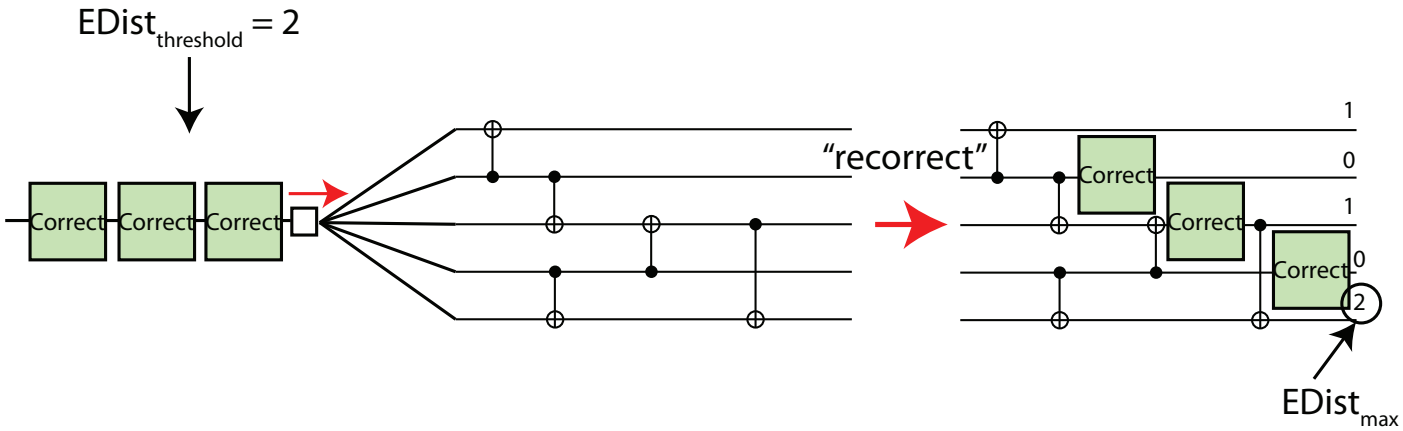

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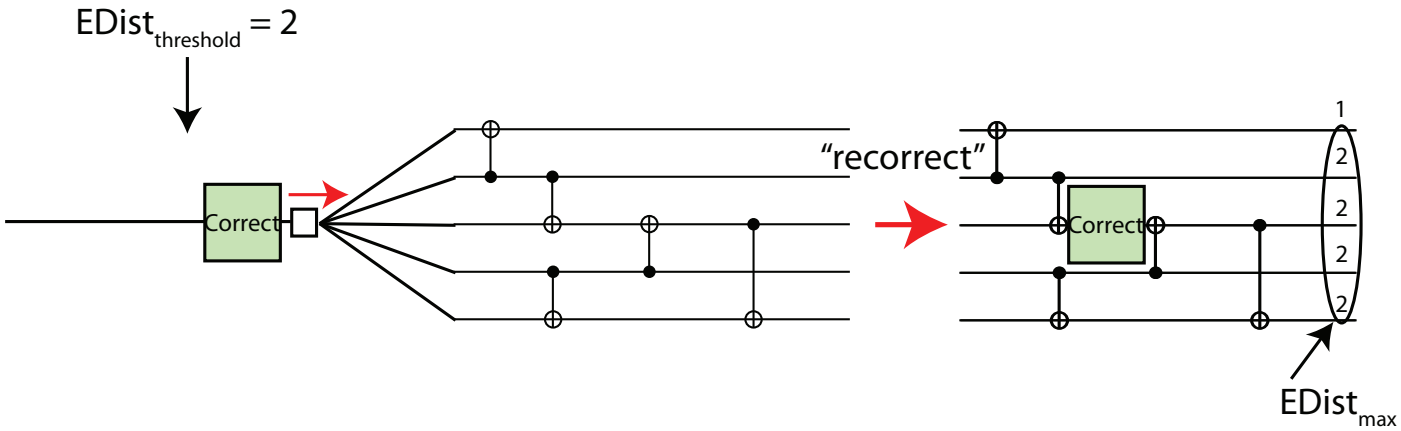

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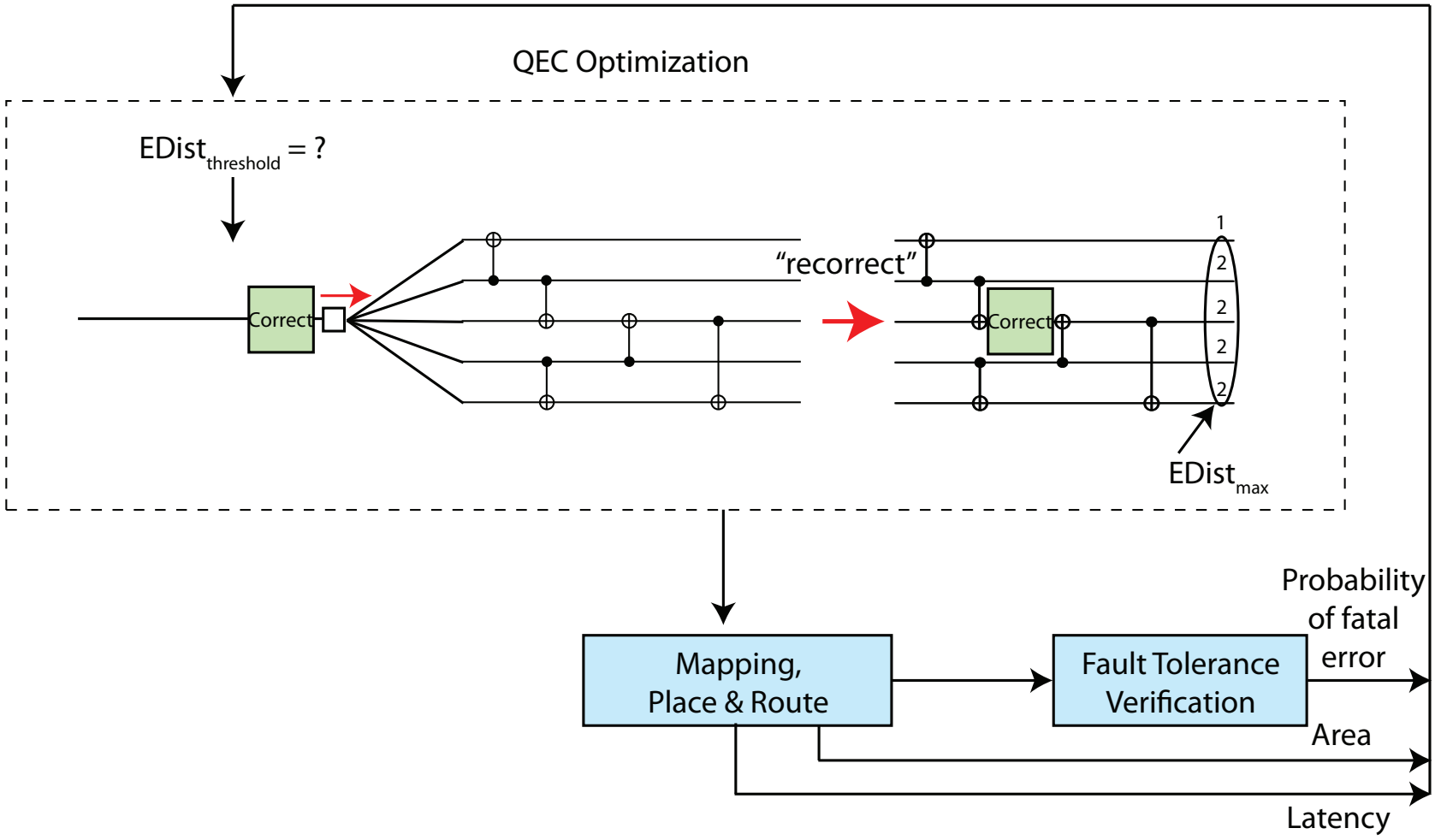

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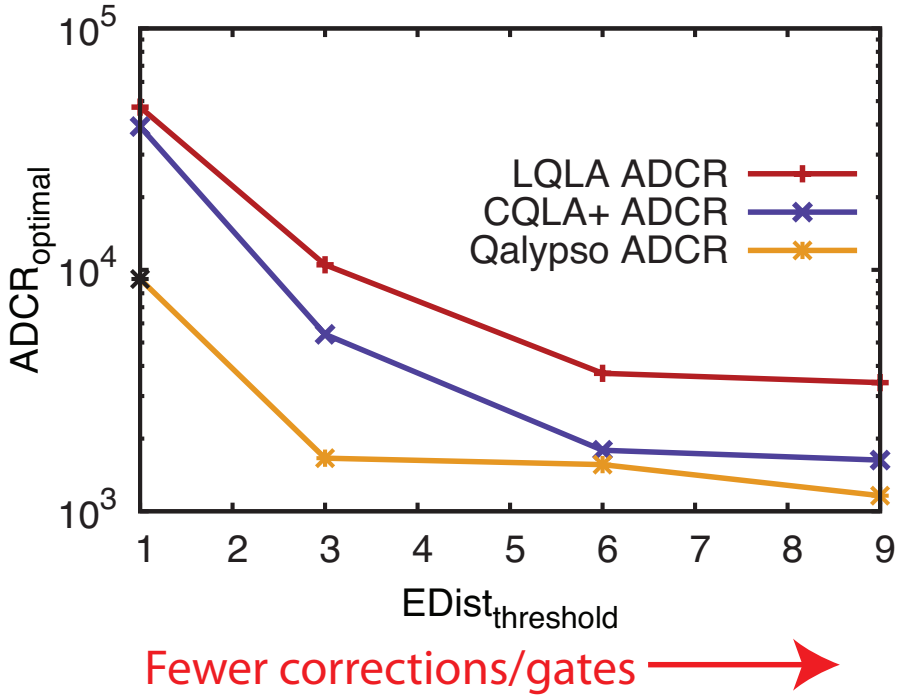
- Find minimal number of corrects so $EDist_{max} \leq EDist_{threshold}$
- Find $EDist_{threshold}$ for desired $p_{success}$/area/D_{single}/ADCR

Optimization and Adder Performance

- 1024-bit Quantum Carry Lookahead Adder



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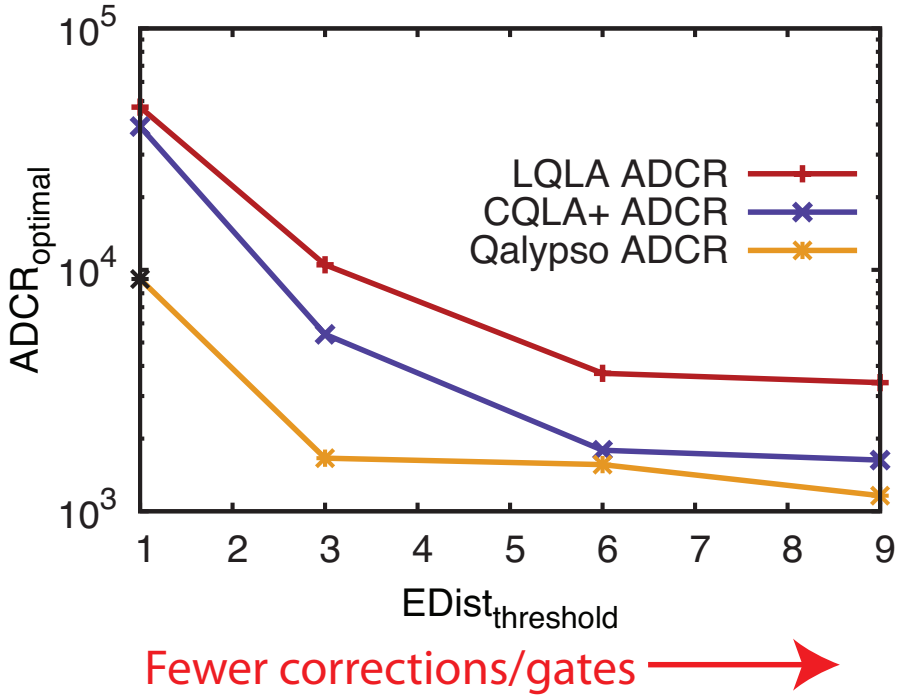

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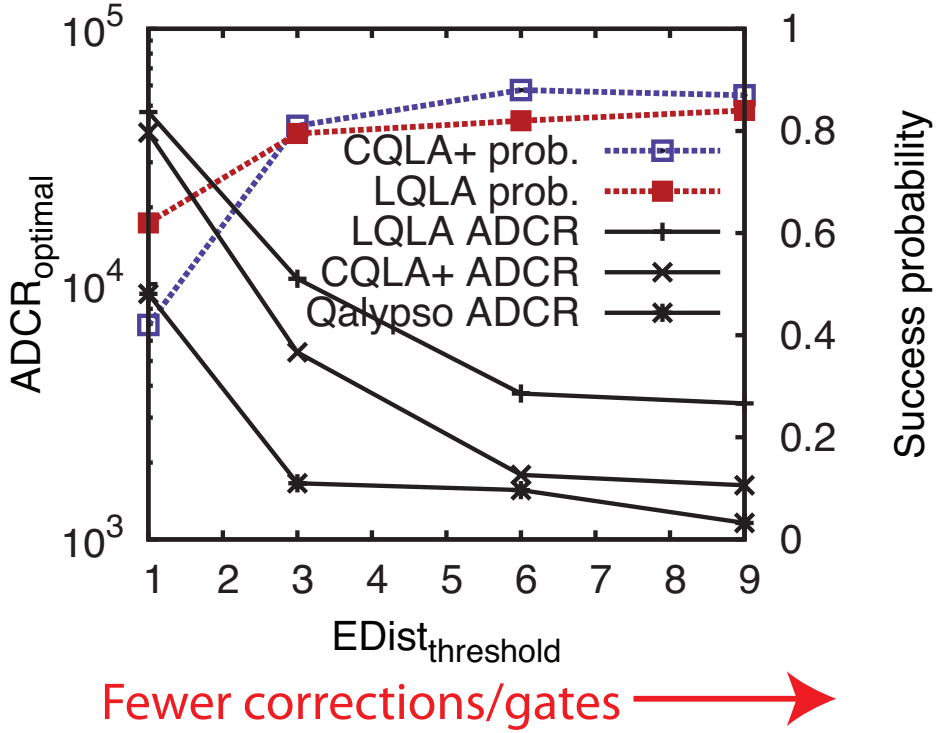

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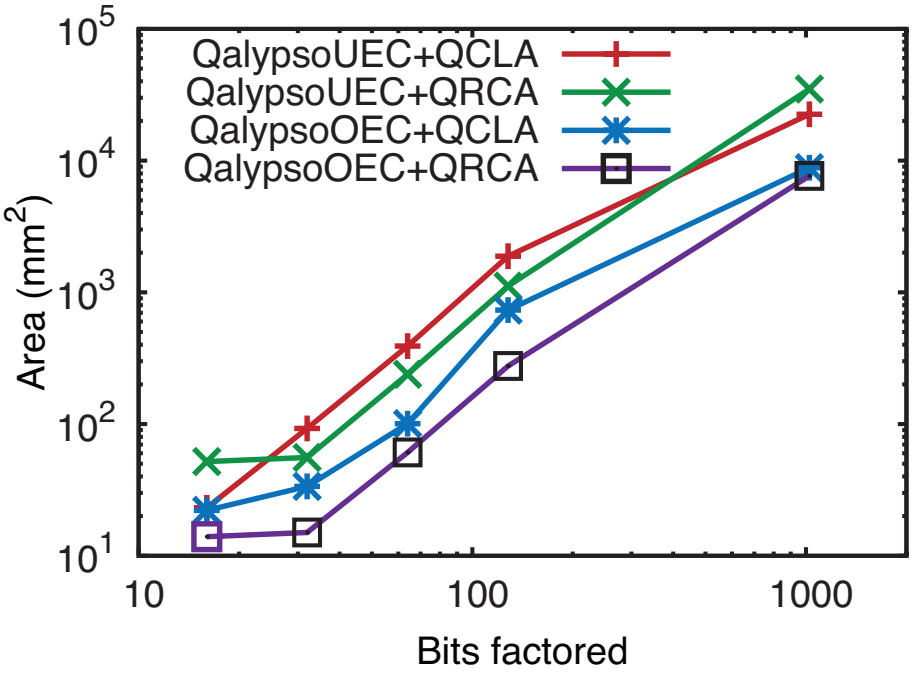

- 5x reduction in area for optimization (QRCA opt best)
- Best optimized Qalypso 1024-bit design is approx $0.01m^2$

Conclusion

- ADCR: New metric for evaluating FT quantum circuits
  - Area efficiency metric including reliability, area, delay
- Qalypso outperforms other QC architectures
  - Detailed layout and simulation allows accurate comparison
  - CAD flow enables automated search of configuration space
- Error correction optimization reduces area and latency
  - Minimal impact to reliability
- Together orders of magnitude area improvement for Shor's factoring