A Feedback Interference Cancellation Technique for Mitigation of Blockers in Wireless Receivers

Von der Fakultät für Elektrotechnik und Informationstechnik
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List of Abbreviations

ACI	Adjacent Channel Interferer
ADC	Analog-to-Digital Converter
AGC	Automatic Gain Control
BER	Bit Error Rate
CDMA	Code Division Multiple Access
CG	Common Gate
CS	Common Source
DAC	Digital-to-Analog Converter
DCOC	DC Offset Correction Circuit
DCR	Direct Conversion Receiver
DCS	Digital Cellular Service
DUT	Device-under-Test
EDGE	Enhanced Data Rates for GSM Evolution
ENOB	Effective Number of Bits
FDD	Frequency Domain Duplex
GMSK	Gaussian Minimum Shift Keying
GPIB	General Purpose Interface Bus
GPRS	General Packet Radio Service
GPS	Global Positioning System
GSM	Global System for Mobile Communications
HDSPA	High Speed Downlink Packet Access
HSUPA	High Speed Uplink Packet Access
IBB	Inband Blocker
IF	Intermediate Frequency
LMS	Least-mean-square
LNA	Low Noise Amplifier
LO	Local Oscillator
LTE	Long Term Evolution
MIM	Metal-Insulator-Metal
NF	Noise Figure
OBB	Out-of-band Blocker
OSR	Oversampling Ratio
PCB	Printed Circuit Board

PCS	Personal Communications Service
PSK	Phase Shift Keying
RF	Radio Frequency
Rx	Receiver
SAW	Surface Acoustic Wave
SNDR	Signal-to-Noise-and-Distortion Ratio
SNR	Signal to Noise Ratio
SoC	System-on-Chip
TCH	Transport Channel
TDD	Time Domain Duplex
TDMA	Time Domain Multiple Access
Tx	Transmitter
UMTS	Universal Mobile Telecommunications System
VGA	Variable Gain Amplifier
VPCM	Cadence Virtuoso Passive Component Modeler®
WCDMA	Wideband Code Division Multiple Access

1. Introduction

Over the last two decades, mobile information and communication has matured to ubiquity. This revolution has been spurred by the two big turning points of the late twentieth century – the advent of the Internet and the broad deployment of cellular networks. Convergence of these two megatrends has enabled an unprecedented mobile working, gaming, and living experience available to anyone, anywhere, and anytime. This is effecting the way we live our daily lives: be it the way we communicate and interact through social networks or how we find our directions in an unknown city.

Technically, this revolution has been facilitated by the evolution of voice-centric 2G standards like GSM to data-centric standards like 3G (HSDPA / HSUPA) and ultimately 4G (LTE). Still, these standards with their ever growing complexity need to be physically implemented. Fortunately, CMOS has literally "come of age" [1] from the 130 nm node onwards allowing the cost efficient implementation of RF front-ends and digital baseband circuits on a single chip thus taking full advantage of scaling [2] and Moore's law [3]. While 3G and 4G networks are mainly being deployed in densely populated areas, legacy GSM networks are widely installed in the field and offer the widest coverage of all networks. Moreover, handsets must allow global roaming and operation in different frequency bands. Hence, a handset must be capable of multiple standards and multiple frequency bands. Apparently, handset cost and form factor must be maintained or decreased to allow for integration of new features. This drives a trend towards higher integration, smaller size, and lower cost ultimately culminating in a single-chip, multi-standard, multi-band radio.

Recently, multi-mode, multi-band transceivers capable of GSM and UMTS [4] or of GSM, UMTS, and GPS [5] have been presented. These solutions integrate the RF front-ends including ADCs whereas the digital baseband signal processing is implemented in a separate chip. Other solutions integrate a single standard transceiver with the digital baseband signal processing in a system-on-chip (SoC) e.g. GSM [6, 7], WLAN [8], Bluetooth [9, 10], or mobile TV [11]. For connectivity standards, the highest level of integration has been presented by [12] comprising Bluetooth, FM radio, as well as WLAN with their respective digital baseband processing and power amplifiers.

This trend towards higher integration is facilitated by the evolution of radio

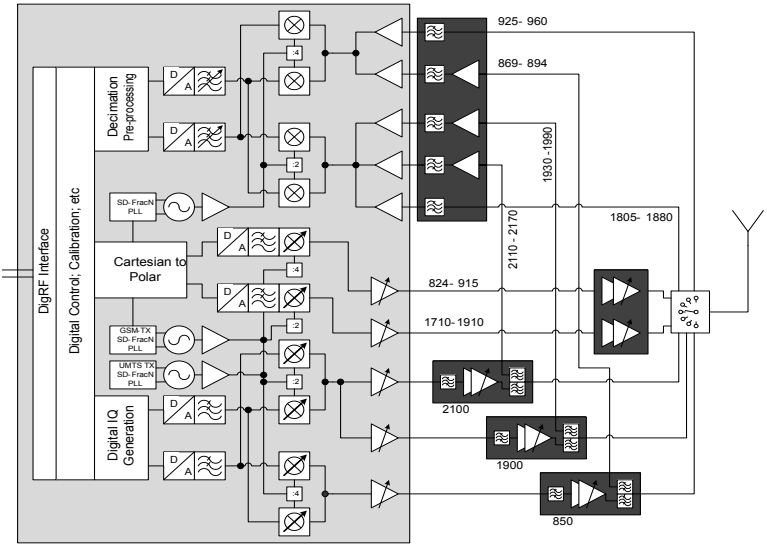


Figure 1.1.: Example of a simplified multiband, multistandard front-end comprising dual-band GSM and tri-band UMTS.

architectures. The prevalent architecture in the 1990s was the heterodyne receiver. Due to the required external image reject filters this architecture is unamenable to high integration. Therefore it has been superseded by the low-IF [13] and direct conversion [14, 15] architectures which eliminate the necessity for external image reject filters. This has facilitated integration of multiple bands on a single die. Still, a high number of external filters is required to protect the receivers from large signal interferers which would otherwise desensitize the receiver and block the desired signal from being properly received. The aforementioned trend towards a multiband, multimode radio has led to an explosion of these external filter components presenting a severe bottleneck for further integration.

To exemplify this point, a multiband, multistandard front-end for dual-band GSM and tri-band UMTS is presented in Fig. 1.1. Obviously, a state-of-the-art front-end integrating 2G, 3G, 4G, and possibly further connectivity standards like Bluetooth or WLAN will be even more complex. From the figure, it is perceived that the external components are dominated by SAW-filters of different types. For full-duplex operation of UMTS, duplex filters are required which separate the receive and transmit bands. As the duplexers lack isolation additional SAW-filters

are required to suppress transmitter leakage in the receiver. Additional low noise amplifiers precede the SAW-filters to compensate for the filter insertion loss. As GSM is operated in half-duplex mode only a SAW-filter is required to suppress out-of-band blockers emanating from adjacent user equipment. Transmit and receive paths are separated by a switch. Moreover, removing external filters helps streamlining logistics as the same phone can be delivered to different marketplaces operating in different bands. Considering the rising number of standards and bands integrated in a single radio, it is highly desirable to reduce the number of external filters – an issue, which will be addressed by this work.

In order to remove external filters, the filtering has to be accomplished on-chip. Obviously, it is desirable to avoid any specialty options deviating from the standard CMOS process for cost reasons. Different methods have been proposed to move the filtering on-chip including quality factor enhanced LC tank filters, N-path filtering, and translational loops. While quality factor enhancement relies on negative resistance circuits to cancel LC tank losses, N-path filtering and translational loops generate a narrow-band RF filter response by shifting a baseband impedance or transfer function to the RF domain by modulators. One promising filtering technique using a feedforward filtering path based on a translational loop has been proposed by [16]. Due to the feedforward, filtering is sensitive to mismatch effects in the quadrature paths of the translational loop. Another promising approach investigated in this work, is a feedback approach which achieves blocker rejection by a control loop.

1.1. Goal of this Work

Goal of this work is the implementation of a SAW-less GSM receiver front-end using a feedback translational loop for blocker mitigation. The GSM standard is chosen for two reasons. First, it must be implemented in any cellular multimode, multiband transceiver as a legacy standard because it is widely installed in the field and offers best coverage. Still, it is considered a commodity and is no differentiator to other products in the marketplace. Therefore, implementation at the minimum possible cost and board area is desirable. Hence, bulky and expensive SAW-filters are not justified. Moreover, GSM has the hardest linearity and blocking specification of all cellular standards. Consequently, it is a good candidate for benchmarking the capabilities of the investigated interference cancellation technique at hand.

First, a comprehensive understanding of the feedback interference cancellation mechanism and its system implications must be gained. Once the theoretical background of the proposed scheme has been clarified, a SAW-less receiver with

feedback interference cancellation can be devised from the GSM specification. In order to assess feasibility of the proposed scheme, testchips of the interference cancellation concept and the SAW-less front-end must be implemented.

1.2. Structure of this Work

This work is structured as followed:

- Chapter 2 introduces fundamentals of wireless receivers and summarizes the definition of common performance metrics. Moreover, the receiver requirements mandated by the GSM standard are given. The chapter is concluded by a literature review of state-of-the-art GSM receivers and out-of-band interference suppression techniques.
- Chapter 3 introduces the concept of feedback interference cancellation. The concept is investigated mathematically and from a system point of view. Finally, nonidealities that might occur in the implementation and might hinder proper operation are identified and analyzed.
- Chapter 4 presents a circuit implementation and measurement results of a first proof-of-concept hardware demonstrator.
- In chapter 5 the insights gained in chapter 3 and chapter 4 are used for the system design of a complete GSM direct conversion receiver with interference cancellation. First, the receiver line-up of a conventional GSM receiver for the DCS and PCS bands is presented and level plans are devised to map the GSM specification to individual circuit blocks. Subsequently, line-up of a SAW-less GSM receiver based on the devised receiver with SAW-filters is discussed.
- In chapter 6 an implementation of the SAW-less receiver devised in chapter 5 is presented. First, possible high dynamic range LNA topologies, which are capable of delivering the required linearity, are investigated and measurement results from a first testchip are presented. Then, implementation and measurement results of a second testchip comprising the SAW-less receiver are reported.
- In chapter 7 the findings of this work are summarized and the thesis is concluded.

2. Fundamentals of Wireless Receivers

In this chapter, fundamentals of wireless receivers are discussed. First, the direct conversion receiver and its characteristic performance trade-offs are introduced. Then, typical receiver performance metrics quantifying receiver behavior in terms of noise and linearity are summarized and the techniques required for receiver system design like cascaded block specifications are laid out. Subsequently, the GSM standard is briefly summarized and the required RF performance metrics are derived from the specification. Finally, a literature survey of state-of-the-art GSM receivers and out-of-band interference suppression techniques is conducted.

2.1. Receiver Architectures

The purpose of a wireless receiver is to pick up a wanted signal – typically in the GHz range – at the antenna and make it accessible for further signal processing. Usually, signal processing is implemented at low frequencies and thus frequency conversion of the received signal is required. Moreover, the receiver is subject to interferences from the environment it is operated in, hence requiring filtering and careful line-up of the individual signal processing steps to separate the wanted signal from disturbances. Different receiver architectures have been invented to address these issues in different ways, among which the heterodyne and direct conversion receiver architectures are the most well known. As focus of this work is on the direct conversion receiver, the introductory description is limited to this particular receiver architecture and only briefly contrasted to the well known heterodyne receiver.

2.1.1. Direct Conversion Receiver

The direct conversion receiver [14, 15] has become the receiver topology of choice for monolithically integrated receivers (e.g. [4, 7, 12]). In the wireless connectivity and cellular marketplace it has superseded the well established heterodyne architecture. In this section advantages of direct conversion receivers over the classic heterodyne approach and its challenges are addressed.

In a heterodyne receiver as shown in Fig. 2.1(a), the RF signal is translated to an intermediate frequency (IF) by mixing with a local oscillator signal. Before

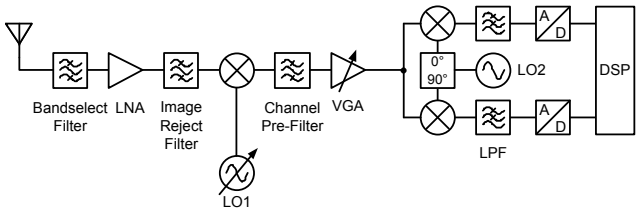
the signal is downconverted to the IF, an image filter is applied to suppress interferers at the image frequency. Subsequently, the signal is filtered at IF to lower adjacent channel interferers. A high IF results in good image rejection while adjacent channel interferers are not very well attenuated. Conversely, if a lower IF is chosen the image signal can be significant while adjacent interferers are well suppressed because better selectivity of the IF filter can be achieved at lower frequencies. Thus, a trade-off between image rejection and adjacent channel selectivity is sought. For both, image as well as IF filters, bulky external surface acoustic wave (SAW) filters are used. Obviously, this solution is not very amendable to integration. Moreover, the receiver must be designed to drive the off-chip components exacerbating the trade-off between power consumption, noise, and linearity. As the receiver can only be optimized for a single standard and a single band the architecture is not a good candidate for multistandard, multiband systems.

The drawbacks of the heterodyne architecture are in part alleviated by the homodyne or direct conversion receiver (DCR) architecture shown in Fig. 2.1(b). In the DCR the RF band is directly shifted to the baseband by a single complex mixing process using a quadrature mixer. Thus the problem of image interferers is alleviated as there is no image frequency. Furthermore, channel selection is achieved using on-chip lowpass filters with high selectivity and possibly reconfigurable bandwidth. Thus, no external filters are required except for the band select filter preceding the LNA. This results in lower cost, lower board area, lower power consumption, and increased flexibility.

Despite the aforementioned advantages of the DCR a number of technical challenges exist which complicate the implementation of DCRs.

DC offsets As the downconverted frequency band in a direct conversion receiver includes DC any DC disturbance directly affects the desired signal. In a DCR, the major part of the total gain in the receive chain is implemented in the baseband, often on the order of 70 dB [15]. Thus, even small DC offsets at the output of the mixer can saturate the receiver and render detection of the wanted signal impossible.

Different processes can lead to DC offsets or DC disturbances in a DCR. The local oscillator signal can leak into the mixer's RF port thus leading to a DC component. Similarly, any RF large signal interferer can leak into the mixer's LO port also resulting in DC disturbances. Static DC offsets can be removed by high pass filtering [15, 17], a lowpass feedback servo loop [18], or in TDMA systems by offset cancellation during the idle phase [15]. Moreover, sample-and-hold of the DC offset can be used for offset elimination. Depending on the modulation a



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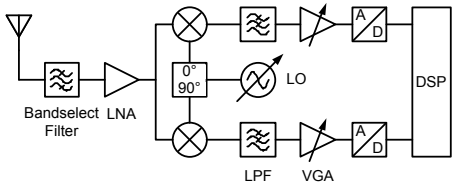


(b)

Figure 2.1.: Receiver block diagrams: heterodyne (a) and direct conversion (b).

considerable part of the signal energy can be concentrated around DC. Therefore, the equivalent highpass corner frequency has to be small not to significantly affect the SNR leading to large capacitors in passive implementations and long start-up transients. Variation of the antenna environment can make the offset component dynamic thus making it impossible to distinguish it from the desired signal.

Even-order distortion As will be discussed later, even-order nonlinear distortion leads to time varying interferer components in the baseband. Even-order distortion originating from the LNA can leak across the mixer due to finite RF to IF isolation thus causing a time varying offset in the baseband. This issue can be circumvented by AC coupling the LNA and the mixer. Even-order distortion of the mixer, on the other hand, cannot be filtered and will affect the baseband. Due to the preceding LNA gain mixer even-order nonlinearity dominates and usually leads to tough second order nonlinearity specifications for this block.

I/Q mismatch A further issue in a DCR are gain and phase mismatch between the quadrature paths. As pointed out before, the main part of the receiver gain is realized in the baseband. Therefore, the I- and Q-paths are prone to

gain mismatch. As pointed out in [15] mismatch leads to crosstalk between the I- and Q-paths thus leading to an SNR degradation. In comparison to discrete implementations I/Q mismatch is less troublesome in integrated systems because appropriate countermeasures like device matching and balanced layouts are facilitated by monolithic integration. In order to limit I/Q mismatch, care must be exercized in matching gain and phase of the quadrature paths. Low phase imbalance, for example, can be achieved by generating the quadrature LO through a quadrature frequency divider instead of a polyphase RC network. Gain imbalance can be minimized by providing discrete gain control steps in the baseband variable gain amplifiers (VGA) instead of continuously tuning their gain.

Flicker noise Finally, it must be noted that particularly in CMOS the baseband is significantly affected by flicker noise. Therefore, it is desirable to have significant gain of around 30 dB in in the RF domain preceding the baseband. Obviously, the gain in the RF is ultimately limited by the mixer linearity. Moreover, as frequencies are low in the baseband, other design techniques can be employed to lower flicker noise. Thus large devices can be used in order to decrease flicker noise.

2.2. Receiver Performance Metrics

In order to characterize wireless receivers and circuit blocks, suitable performance metrics have to be defined. In this section, fundamental parameters which characterize noise and nonlinearity are introduced [15]. Then, techniques for cascading noise and nonlinearity along the receive chain are laid out. Finally, the Volterra series and nonlinearities with memory are briefly discussed.

2.2.1. Noise

Random fluctuations of physical quantities like e.g. current or voltage are called noise. As these random signal variations are unrelated to the wanted signal they can deterioriate detection of the wanted signal if the wanted signal is weak or – more specifically – if its power is close to the noise power. Therefore, the minimum detectable signal power is set by the noise power present in a circuit.

Noise in CMOS circuits is mainly caused by three different processes: thermal noise, shot noise, and flicker noise [19]. Thermal noise is due to thermal movement of charge carriers and is found in resistors. Shot noise is caused by charge carriers randomly passing a potential barrier such as a pn-junction or the gate barrier if significant gate leakage is present in a MOS transistor. Both, thermal noise as

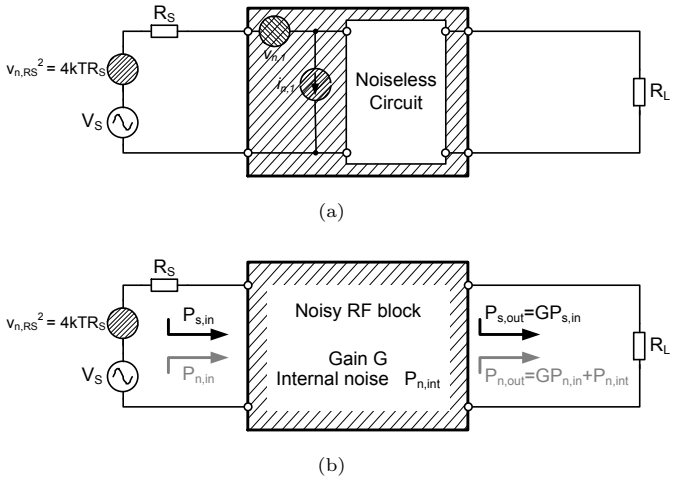


Figure 2.2.: Characterization of a noisy two-port by input referred noise sources (a) and noise factor (b) [20].

well as shot noise, have a constant spectral power density and can be modelled as white noise. Finally, flicker noise is caused by trap and release of charge carriers at imperfections at the interface between silicon and oxide. The time constants of these processes give rise to the typical $1/f$ frequency dependence. At higher frequencies the $1/f$ characteristic is superseded by thermal noise. The intersection of $1/f$ and thermal noise is usually referred to as the flicker noise corner.

In order to describe circuit noise performance independently of the actual physical processes leading to random signal fluctuations some common performance figures are defined which are discussed below.

Noise Factor

The noise of a circuit block can be represented in terms of input referred noise voltage and noise current sources as presented in Fig. 2.2(a). By input referring the noise sources the actual circuit itself can be considered noiseless. Often, measuring input referred noise sources is impractical - especially at high frequencies. Therefore a characterization of circuit noise in terms of power is sought which can be readily measured even at high frequencies.

The noise factor characterizes the signal-to-noise power ratio (SNR) degrada-

tion which is caused by a circuit block. As such the noise factor F can be defined as

$$F = \frac{SNR_{in}}{SNR_{out}}. \tag{2.1}$$

As the circuit always adds noise to the input signal the input SNR is degraded and the output SNR is worse than the input SNR. By calculating input and output SNR as indicated in Fig. 2.2(b) the noise factor can also be expressed by

$$F = 1 + \frac{1}{G}\frac{P_{n,int}}{P_{n,in}} = \frac{\text{total output noise power}}{\text{output noise power due to input source}}. \tag{2.2}$$

This expression can be particularly useful in calculating noise factors of transistor circuits or for evaluating simulation data. Eventually, the relation between noise factor and input referred noise sources is given by

$$F = 1 + \frac{\overline{v_n^2 + i_n^2 R_S^2}}{4kTR_S}. \tag{2.3}$$

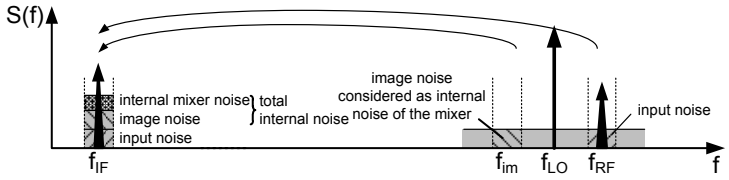
Mixer Noise

In a mixer, the definition of noise figure depends upon its system application. In a heterodyne system, the RF band is downconverted to the intermediate frequency whereas noise is downconverted from the RF and image bands to the intermediate frequency. As the wanted signal resides in a single sideband the noise contributed by the image band is considered internal to the mixer (Fig. 2.3(a)). Conversely, in a homodyne system the wanted signal and the noise reside in both sidebands. Therefore, the noise in both sidebands is considered as input noise (Fig. 2.3(b)) resulting in a 3 dB lower noise figure than for the single-sideband case.

Phase Noise and Reciprocal Mixing

The local oscillator is used for demodulation and mixing in receivers. Due to various noise mechanisms the local oscillator signal exhibits amplitude variations and phase modulation. While amplitude variations can usually be avoided by using a limiting stage behind the oscillator, phase modulation of the carrier results in sidebands around the carrier signal which is designated phase noise. As indicated in Fig. 2.4 phase noise $L(\Delta f)$ is referred to the carrier power and given per unit bandwidth in dBc/Hz, i.e. as "x dB per Hertz below the carrier".

If a large signal blocker resides close to the wanted RF signal an effect called reciprocal mixing occurs. The large signal blocker mixes with the local oscillator phase noise. As a result the phase noise is transferred to the intermediate frequency and overlaps with the downconverted wanted signal. Thus, the SNR



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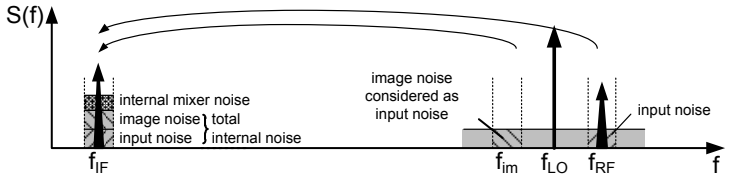


(b)

Figure 2.3.: Definition of single-sideband noise figure (a) and double-sideband noise figure (b) [20].

in the wanted band is degraded depending on the blocker level. The noise power density at a given offset frequency from the carrier can be calculated by

$$S_{n,Blocker} = P_{Blocker} - L(\Delta f). \tag{2.4}$$

Cascade Noise Figure

In a receiver, several noisy circuit blocks are cascaded to form the complete receive chain. If the individual circuit blocks have been characterized by simulation or measurements, the total receiver noise figure can be calculated by cascading the individual blocks. For the case of power matched inputs and outputs the well known Friis formula [21] can be used to calculate the cascade noise figure. If the input impedance is not well defined – as is usually the case for all blocks succeeding the LNA in an integrated receiver – a description in terms of input referred noise sources is preferred. Subsequently, the Friis formula as well as cascading on- and off-chip blocks is addressed.

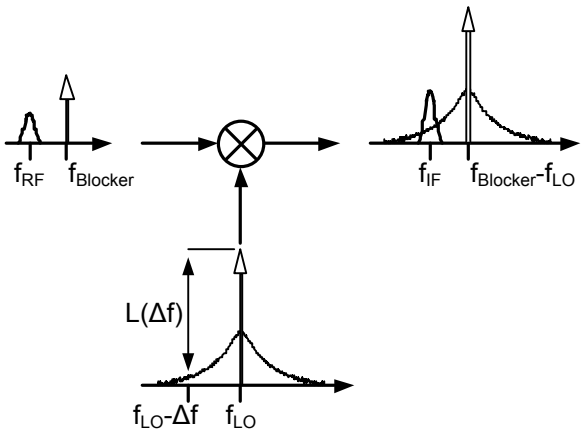


Figure 2.4.: Reciprocal mixing of local oscillator phase noise and blocker.

Cascade noise factor – Friis equation If all blocks are power matched at their input and outputs the cascade noise factor yields [21]

$$F_{tot} = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \dots \tag{2.5}$$

Note that the total noise factor is dominated by the first stages as the noise factor of the stages downstream is scaled down by the preceding gain. Therefore, it is vital for overall noise performance to have low noise and high gain in the first stage.

Input referred noise voltage While considerable efforts are made to match the input and output terminals of the chip to defined source and load impedances severe performance or power efficiency would be wasted if similar efforts were undertaken for cascading on-chip blocks. Hence, input and output impedances are usually not well-defined 50 Ohm on-chip but low- or high-impedance, respectively. Therefore, input referred noise voltages are used to characterize noise performance of on-chip blocks. This is shown in Fig. 2.5. As seen in the figure, the input referred noise current sources can be neglected if the output impedance of the circuit block is significantly lower than the input impedance of the following circuit block. This assumption often holds in CMOS as the input impedance seen into the gates of a differential input stage is high. Although this assumption might fail at high frequencies for nodes with high load capacitance it can usually

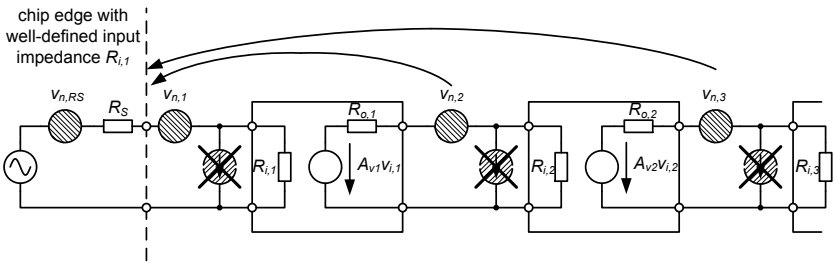


Figure 2.5.: Cascaded input referred noise voltages.

be considered a good approximation. As seen in Fig. 2.5 the input referred noise voltages of the individual stages can be input referred to the input of the chip by dividing through the voltage gain of the preceding stages resulting in a total input referred noise voltage of

$$v_{n,i}^2 = v_{n,1}^2 + \left(\frac{R_{i,1}+R_S}{R_S}\right)^2 \left(\frac{v_{n,2}^2}{A_{V1}^2} + \frac{v_{n,3}^2}{A_{V1}^2 A_{V2}^2} + \dots\right). \tag{2.6}$$

From (2.6) and (2.3) the noise figure can be calculated

$$F_{tot} = F_1 + \frac{(1+VSWR)^2}{4kTR_S}\left(\frac{v_{n,2}^2}{A_{V1}^2} + \frac{v_{n,3}^2}{A_{V1}^2 A_{V2}^2} + \dots\right) \tag{2.7}$$

where $VSWR = R_{i1}/R_S$ is the voltage standing wave ratio measured at the input of the chip.

2.2.2. Nonlinearity

So far, the low end of the dynamic range has been explored. At large input signals the circuit will deviate from its linear behavior and a variety of nonlinear effects comes into play which can interfere with the wanted signal ultimately limiting the dynamic range at the upper end. Before assessing the effect of nonlinearity in a circuit or system it must be modelled. Often it is sufficient to limit the analysis to memoryless nonlinearities and it is assumed that the system is only mildly nonlinear. In this case, a Taylor series expansion can be used to model the system. If the effect of storage elements like capacitors or inductors – and thus filtering – must be taken into account Taylor expansion is not sufficient. Instead, Volterra series have to be used to account for memory.

In this section the effect of nonlinearities is first explained for memoryless

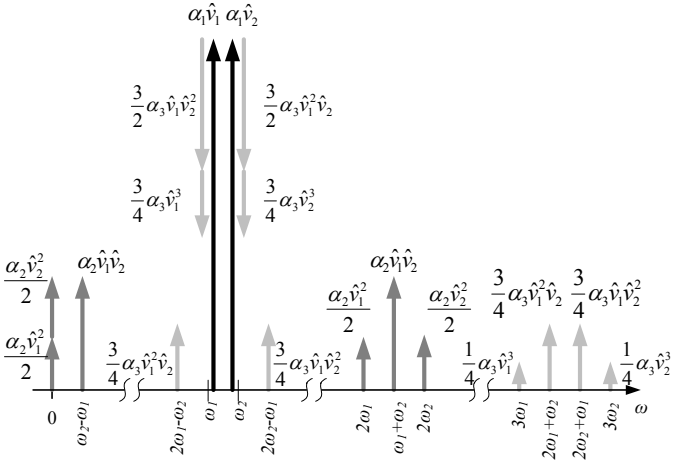


Figure 2.6.: Nonlinear response to a two-tone test comprising linear terms (black), second order distortion (dark gray), and third order distortion (light gray) [20].

nonlinearities and then the analysis is expanded for systems involving memory.

Taylor Series

If the circuit behaves mildly nonlinear, the analysis can be limited to nonlinearities up to third order. Then, the output of a nonlinear system can be approximated by

$$y(t) \approx \alpha_1 x(t) + \alpha_2 x(t)^2 + \alpha_3 x(t)^3. \tag{2.8}$$

The effect of nonlinearity is best seen by applying a two-tone test signal $x(t)$ to the nonlinearity with

$$x(t) = A_1 \cos\omega_1 t + A_2 \cos\omega_2 t. \tag{2.9}$$

The output spectrum can be calculated by inserting (2.9) in (2.8) and is depicted in Fig. 2.6. As seen in the figure, different nonlinearity coefficients give rise to tones at different frequencies which will be classified below.

Harmonics Nonlinearities cause integer multiples of the input signal frequencies. In the third order model, even order harmonics are caused by second order

distortion and odd order harmonics are caused by third order distortion.

Gain compression At the fundamental frequencies, third order distortion contributes a signal component which is commensurate to the third power of the input amplitude. Thus, a negative Taylor coefficient α_3 leads to gain compression of the input signal while a positive Taylor coefficient causes gain expansion. The input referred 1 dB compression point is derived as

$$V_{iCP,1dB} = \sqrt{\frac{4}{3}\left[1 - 10^{-1/20}\right]\left|\frac{\alpha_1}{\alpha_3}\right|}. \tag{2.10}$$

Desensitization When the circuit is subject to a small signal at the wanted frequency along with a large interferer at a second frequency the gain at the wanted frequency is compressed due to the large signal interferer thus increasing the noise contribution of the following stages. This effect is called desensitization and is caused by third-order nonlinearity. The interferer input amplitude where the gain at the wanted frequency is degraded by 1 dB is called input referred 1 dB desensitization point and is calculated by

$$V_{iDP.1dB} = \sqrt{\frac{2}{3}\left[1 - 10^{-1/20}\right]\left|\frac{\alpha_1}{\alpha_3}\right|}. \tag{2.11}$$

A comparison of (2.10) and (2.11) reveals that the 1 dB desensitization point iDP_{1dB} is 3 dB below the compression point iCP_{1dB}.

An additional desensitization effect emanating from second-order nonlinearity is pointed out in [22]. As seen in Fig. 2.6 second-order nonlinearity generates a signal component $\alpha_2 V_1 V_2$ at $\omega_2 - \omega_1$. Thus, a large signal blocker residing at ω_2 can mix with low frequency noise around ω_1 resulting in low frequency noise upconversion. As shown in Fig. 2.7 the wanted signal can be severely degraded if the large signal blocker is close, the circuit has excessive flicker noise, and high second-order nonlinearity.

Intermodulation When two signals with different frequencies are applied to the circuit both signals are subject to a mixing process resulting in intermodulation products at sum and difference frequencies.

Third order intermodulation products are located around ω_1, ω_2, and $3\omega_1$, $3\omega_2$ falling at the frequencies $2\omega_1 - \omega_2$, $2\omega_2 - \omega_1$, $2\omega_1 + \omega_2$, and $2\omega_2 + \omega_1$. While the components at $2\omega_1 + \omega_2$ and $2\omega_2 + \omega_1$ can be filtered, the components at the difference frequencies $2\omega_1 - \omega_2$ and $2\omega_2 - \omega_1$ can be particularly detrimental. If the interferers are located close to the wanted channel the intermodulation products

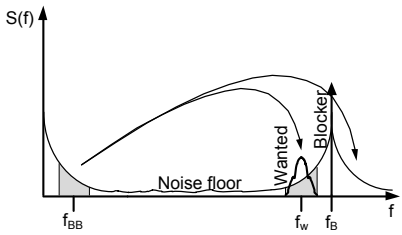


Figure 2.7.: Upconversion of low frequency noise due to second-order nonlinearity.

fall into the wanted channel and degrade the signal-to-noise ratio. The situation is not significantly improved by filtering of the interferers as they are close to the wanted channel and it is hard to obtain high selectivity at small offset frequencies – especially at RF. Third order intermodulation is usually characterized by the third order intercept point $IP3$ which is obtained by calculating the intersection of the linear output power and the power of the third order intermodulation product as depicted in Fig. 2.8(a). The input referred third order intercept point can be expressed in terms of Taylor coefficients

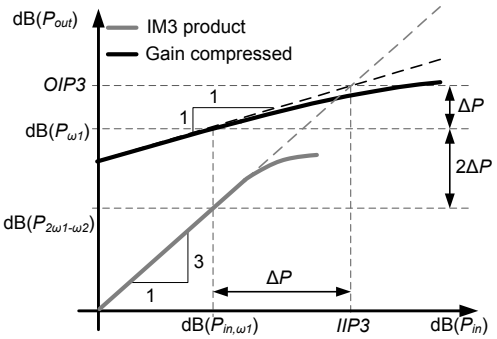
$$V_{IIP3} = \sqrt{\frac{4}{3}\left|\frac{\alpha_1}{\alpha_3}\right|}. \tag{2.12}$$

By comparison with (2.10) and (2.11) it is seen that the $IIP3$ is 9.6 dB higher than the input compression point and 12.6 dB higher than the desensitization point. Obviously, this relation only holds for a system which has no higher terms than the third order in the Taylor expansion. Usually, the Taylor coefficients are not directly accessible. Therefore, the $IIP3$ is calculated from the measured third order intermodulation product and the linear response depicted in Fig. 2.8(a) by

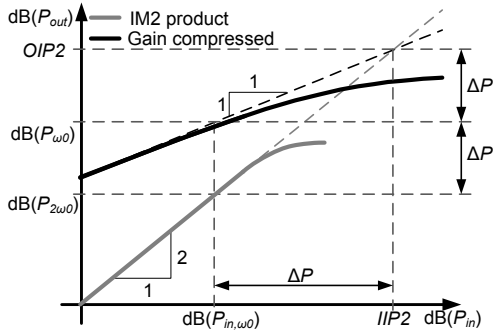
$$P_{IIP3} = dB(P_{in,\omega_1}) + \frac{dB(P_{\omega_1}) - dB(P_{2\omega_2-\omega_1})}{2}. \tag{2.13}$$

Second order intermodulation products occur at $\omega_1 + \omega_2$ and $\omega_1 - \omega_2$. If the frequencies are close the intermodulation product at $\omega_1 - \omega_2$ resides in the baseband and can deteriorate the wanted signal in a homodyne receiver. In other systems second order intermodulation can be less detrimental. The input referred second order intercept point can be calculated in terms of Taylor coefficients by

$$V_{IIP2} = \left|\frac{\alpha_1}{\alpha_2}\right|. \tag{2.14}$$



(a)



(b)

Figure 2.8.: Intermodulation plot for third order (a) and second order (b) intermodulation.

It can also be defined similarly to (2.13) by

$$P_{IIP2} = dB(P_{in,\omega_1}) + dB(P_{\omega_1}) - dB(P_{\omega_1-\omega_2}). \tag{2.15}$$

Cascade Nonlinearities

The cascade $IIP3$ can be calculated by examining Fig. 2.9, cascading the nonlinearities $\alpha_1, \alpha_2, \alpha_3$ and $\beta_1, \beta_2, \beta_3$. Applying the definition of $IIP3$ from (2.12)

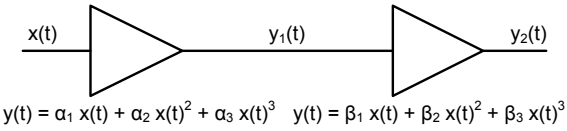


Figure 2.9.: Two cascaded nonlinear amplifiers.

and generalizing yields

$$\frac{1}{V_{IIP3,tot}^2} \approx \frac{1}{V_{IIP3,1}^2} + \frac{A_{V,1}^2}{V_{IIP3,2}^2} + \frac{A_{V,1}^2 A_{V,2}^2}{V_{IIP3,3}^2} + \dots \tag{2.16}$$

The same result can be expressed in terms of power

$$\frac{1}{P_{IIP3,tot}} \approx \frac{1}{P_{IIP3,1}} + \frac{G_1}{P_{IIP3,2}} + \frac{G_1 G_2}{P_{IIP3,3}} + \dots \tag{2.17}$$

Note that these results are approximate and do not account for third order intermodulation products which result from second order interaction between the first and the second stage [23]. Nonetheless, this result is extremely useful for calculating the $IIP3$ of a receive chain. An important conclusion which can be drawn from (2.16) and (2.17) is that the overall $IIP3$ is dominated by the $IIP3$ of the latter stages of the receive chain because it is scaled down by the total preceding gain.

Similarly, the cascade $IIP2$ can be calculated in terms of voltage

$$\frac{1}{V_{IIP2,tot}} = \frac{1}{V_{IIP2,1}} + \frac{A_{V,1}}{V_{IIP2,2}} \tag{2.18}$$

and power

$$\left(\frac{1}{P_{IIP2,tot}}\right)^{1/2} = \left(\frac{1}{P_{IIP2,1}}\right)^{1/2} + \left(\frac{G_1}{P_{IIP2,2}}\right)^{1/2} + \dots, \tag{2.19}$$

respectively.

Unequal test tones / Effect of filtering So far, it has been assumed for the definition of $IIP3$ that the interferers are of the same amplitude. In a receiver this assumption is not necessarily true. Especially in the baseband intermodulation interferers are reduced by channel filtering leading to improved intermodulation performance of the baseband blocks. Therefore, the effects of filtering and

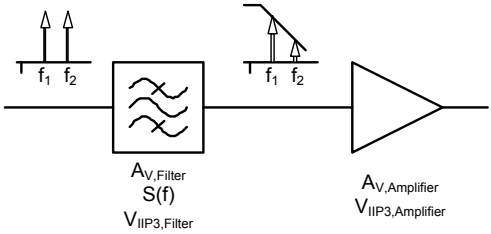


Figure 2.10.: Cascade of filter and amplifier.

unequally sized test tones have to be accounted for. As laid out in [24], this is done by specifying an effective amplitude according to

$$V_{eff}^3 = V_1 V_2^2. \tag{2.20}$$

Equating the linear and the third order intermodulation term at $2\omega_1 - \omega_2$ yields

$$\frac{3}{4}\alpha_3 V_1^2 V_2 = \alpha_1 V_{IIP3,eff} \tag{2.21}$$

with $V_1 = V_{IIP3,eff}/S(\omega_1)$ and $V_2 = V_{IIP3,eff}/S(\omega_2)$, where $S(\omega)$ represents the selectivity of the filter at the respective interferer frequency and $V_{IIP3,eff}$ the effective $IIP3$ voltage. By solving (2.21) it is easy to see that the $IIP3$ is improved by the selectivity of the filter

$$V_{IIP3,eff}^2 = S(\omega_1)^2 S(\omega_2) \cdot V_{IIP3}^2. \tag{2.22}$$

The filter itself might exhibit nonlinearity. Therefore, the cascade of the amplifier and the preceding filter results in a cascade $IIP3$ of

$$\frac{1}{V_{IIP3,casc}^2} = \frac{1}{V_{IIP3,Filter}^2} + \frac{1}{S(\omega_1)^2 \cdot S(\omega_2)} \frac{A_{V,Filter}^2}{V_{IIP3,Amplifier}^2}. \tag{2.23}$$

Volterra Series

When the effect of memory and thus filters must be taken into account merely analyzing a nonlinear system by Taylor series expansion is insufficient. Instead, Volterra series expansion is used. A detailed description of the method and its mathematical foundations is given in [25] and will only be briefly reviewed here for completeness.

Very similar to a Taylor series expansion the output $y(t)$ of a nonlinear system

can be described as a series of n-th order terms

$$y(t) = H_1[x(t)] + H_2[x(t)] + H_3[x(t)] + \dots \tag{2.24}$$

where $x(t)$ is the input signal and $H_1, H_2, H_3, \dots$ are the first, second, and third order Volterra operators, respectively. The first order Volterra operator is just the convolution integral of the input signal $x(t)$ and the linear impulse reponse $h_1(t)$

$$H_1[x(t)] = \int_{-\infty}^{+\infty} h_1(\tau_1)x(t-\tau_1)\,d\tau_1. \tag{2.25}$$

The second order operator is the two-dimensional convolution of the input signal $x(t)$ with the second order Volterra kernel $h_2(t_1, t_2)$

$$H_2[x(t)] = \int_{-\infty}^{+\infty}\int_{-\infty}^{+\infty} h_2(\tau_1,\tau_2)x(t-\tau_1)x(t-\tau_2)\,d\tau_1\,d\tau_2. \tag{2.26}$$

Similarly, the third order operator is obtained as the three dimensional convolution of the input signal and the third order Volterra kernel

$$H_3[x(t)] = \int_{-\infty}^{+\infty}\int_{-\infty}^{+\infty}\int_{-\infty}^{+\infty} h_3(\tau_1,\tau_2,\tau_3)x(t-\tau_1)x(t-\tau_2)x(t-\tau_3)\,d\tau_1\,d\tau_2\,d\tau_3. \tag{2.27}$$

Due to the convolution operation nonlinear systems with memory can be described by the Volterra series. If the Volterra kernels $h_n(\tau_1, \dots, \tau_n)$ are zero except for $\tau = 0$ the system has no memory and the Volterra series reduces to a power series expansion

$$y(t) = h_1(0)x(t) + h_2(0,0)x(t)^2 + h_3(0,0,0)x(t)^3 + \dots \tag{2.28}$$

where the coefficients $h_1(0)$, $h_2(0,0)$, $h_3(0,0,0)$ are the Taylor coefficients from the preceding section.

For circuit and system analysis a frequency domain description of the system is often more interesting. Note that the n-th order Volterra kernel can be considered as an n-th order impulse response. From linear system theory we expect that the frequency domain output of the n-th order Volterra operator results from a multiplication of the frequency domain input signal and the Fourier transform of the n-th order Volterra kernel. Thus, the n-th order nonlinear transfer function or

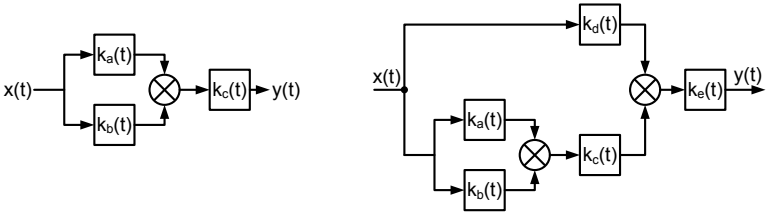


Figure 2.11.: Block diagram of second (a) and third (b) order Volterra kernels.

n-th order kernel transform is obtained from a multidimensional Fourier transform

$$H_n(s_1, \ldots, s_n) = \int_{-\infty}^{+\infty} \cdots \int_{-\infty}^{+\infty} h_n(\tau_1, \ldots, \tau_n) e^{-(j\omega_1\tau_1 + \ldots + j\omega_n\tau_n)} \, d\tau_1 \cdots d\tau_n. \tag{2.29}$$

Second and third order Volterra kernels In the proceeding analysis, a block diagram representation of second and third order nonlinearity will be required. Therefore, the general second and third order nonlinear transfer functions are introduced for general second and third order nonlinearities.

The second order system of Fig. 2.11(a) combines two signals by a single multiplication. The incoming signal is first processed by two linear systems with impulse responses $k_a(t)$ and $k_b(t)$. Then the results are multiplied and finally processed by $k_c(t)$. From the time domain Volterra kernel the frequency domain representation is obtained [25]

$$H_2(j\omega_1, j\omega_2) = K_a(j\omega_1) K_b(j\omega_2) K_c(j\omega_1 + j\omega_2). \tag{2.30}$$

If the system is memoryless, (2.30) reduces to

$$H_2(j\omega_1, j\omega_2) = K_c \tag{2.31}$$

which corresponds to the second order Taylor coefficient. If filtering is only applied after the multiplication the second order nonlinear transfer function is

$$H_2(j\omega_1, j\omega_2) = K_c(j\omega_1 + j\omega_2). \tag{2.32}$$

The third order system of Fig. 2.11(b) combines three input signals by two

multiplications. Thus the output of a second order system is combined with the linearly processed input signal by a second multiplication. Finally, the result is processed by a linear impulse response. The third order nonlinear Volterra kernel transform is obtained as

$$H_3(j\omega_1, j\omega_2, j\omega_3) = K_a(j\omega_1)K_b(j\omega_2)K_c(j\omega_1+j\omega_2)K_d(j\omega_3)K_e(j\omega_1+j\omega_2+j\omega_3). \tag{2.33}$$

If the system is memoryless (2.33) again reduces to the third order Taylor coefficient. If filtering is only applied after the nonlinearity, (2.33) yields

$$H_3(j\omega_1, j\omega_2, j\omega_3) = K_e(j\omega_1 + j\omega_2 + j\omega_3). \tag{2.34}$$

Nonlinear effects represented by Volterra kernel transforms All nonlinear effects that have been previously discussed can be expressed by n-th order Volterra kernel transforms. Thus, the analytical expressions obtained for the memoryless case are expanded to account for filtering. In Tab. 2.1 all responses to a two-tone excitation as shown in Fig. 2.6 are listed as obtained from Volterra series analysis. In comparison to Fig. 2.6 the Taylor coefficients are now substituted by their respective Volterra kernel transform evaluated at the frequency of the respective response.

2.3. Receiver Requirements mandated by the GSM Specification

In this section, the GSM physical layer aspects [26] are very briefly summarized and the receiver specification is derived from the GSM radio transmission and reception specification [27].

2.3.1. Overview of GSM Standard

The Global System for Mobile Communication (GSM) standard has originally been developed in Europe and is today the world's most widely used mobile communication standard. It was first developed for the 900 MHz band and has been extended to the bands listed in Tab. 2.2. The GSM standard combines frequency domain duplexing (FDD) and time domain multiple access (TDMA) techniques [26]. This means that the uplink from the handset to the basestation and the downlink from the basestation to the handset are separated in frequency. The channels are spaced at 200 kHz whereas data is transmitted in 4.615 ms time frames which are split in 8 slots. Each slot is associated with one user, which relates to the aforementioned TDMA. Moreover, frequency hopping can be

order	frequency of response	amplitude of response	type of response
1	ω_1 ω_2	$A_1\lvert H_1(j\omega_1)\rvert$ $A_2\lvert H_1(j\omega_2)\rvert$	linear
2	$\omega_1+\omega_2$ $\omega_1-\omega_2$	$A_1A_2\lvert H_2(j\omega_1,j\omega_2)\rvert$ $A_1A_2\lvert H_2(j\omega_1,-j\omega_2)\rvert$	2nd-order intermodulation products
2	$2\omega_1$ $2\omega_2$	$\frac{1}{2}A_1^2\lvert H_2(j\omega_1,j\omega_1)\rvert$ $\frac{1}{2}A_1^2\lvert H_2(j\omega_2,j\omega_2)\rvert$	2nd harmonics
2	0 0	$\frac{1}{2}A_1^2\lvert H_2(j\omega_1,-j\omega_1)\rvert$ $\frac{1}{2}A_1^2\lvert H_2(j\omega_2,-j\omega_2)\rvert$	DC shift
3	$2\omega_1+\omega_2$ $\lvert 2\omega_1-\omega_2\rvert$ $\omega_1+2\omega_2$ $\lvert\omega_1-2\omega_2\rvert$	$\frac{3}{4}A_1^2A_2\lvert H_3(j\omega_1,j\omega_1,j\omega_2)\rvert$ $\frac{3}{4}A_1^2A_2\lvert H_3(j\omega_1,j\omega_1,-j\omega_2)\rvert$ $\frac{3}{4}A_1A_2^2\lvert H_3(j\omega_1,j\omega_2,j\omega_2)\rvert$ $\frac{3}{4}A_1A_2^2\lvert H_3(j\omega_1,-j\omega_2,-j\omega_2)\rvert$	third-order intermodulation products
3	$\omega_1+\omega_2-\omega_2$ $\omega_2+\omega_1-\omega_1$	$\frac{3}{2}A_1A_2^2\lvert H_3(j\omega_1,j\omega_2,-j\omega_2)\rvert$ $\frac{3}{2}A_1^2A_2\lvert H_3(j\omega_1,-j\omega_2,j\omega_2)\rvert$	third-order desensitization
3	$2\omega_1-\omega_1$ $2\omega_2-\omega_2$	$\frac{3}{4}A_1^3\lvert H_3(j\omega_1,j\omega_1,-j\omega_1)\rvert$ $\frac{3}{4}A_2^3\lvert H_3(j\omega_2,j\omega_2,-j\omega_2)\rvert$	third-order compression or expansion
3	$3\omega_1$ $3\omega_2$	$\frac{1}{4}A_1^3\lvert H_3(j\omega_1,j\omega_1,j\omega_1)\rvert$ $\frac{1}{4}A_2^3\lvert H_3(j\omega_2,j\omega_2,j\omega_2)\rvert$	third harmonics

Table 2.1.: Responses to a two-tone excitation $A_1\cos\omega_1 t + A_2\cos\omega_2 t$ described by Volterra kernels (from [25]).

used to mitigate vulnerability to interference. GSM is a half-duplex system i.e. the handset is either receiving or transmitting. GSM and its evolution General Packet Radio Service (GPRS) use Gaussian minimum shift keying (GMSK) with a bandwidth-time-product of 0.3 and can transmit one bit per symbol, whereas Enhanced Data Rates for GSM Evolution (EDGE) uses 8-PSK with 3 bits per symbol. GSM achieves a channel data rate of 270.833 kbps.

Multiple access	FDMA / TDMA			
Duplex technique	FDD			
	GSM 850	E/GSM 900	DCS 1800	PCS 1900
Uplink [MHz]	869–894	925/935–960	1805–1880	1930–1990
Downlink [MHz]	824–849	880/890–915	1710–1785	1850–1910
Channel spacing	200 kHz			
Modulation	GMSK ($BT = 0.3$)			
Channel data rate	270.833 kbps			
Frame duration	4.615 ms			

Table 2.2.: Specification summary for the GSM cellular system [26].

2.3.2. Reference Sensitivity Level – Noise Figure

Reference sensitivity is defined as the minimum detectable signal with acceptable signal-to-noise ratio. Thus the reference sensitivity directly affects the maximum distance between handset and base station. Sensitivity can be calculated from the given minimum acceptable SNR, the signal bandwidth B, and the noise figure of the receiver by

$$dBm(P_{sensitivity}) = dBm(kT) + dB(B) + dB(SNR) + dB(NF). \tag{2.35}$$

At room temperature, the thermal noise floor resides at -174 dBm/Hz. The bandwidth is given by the standard. The minimum signal-to-noise ratio depends on the type of modulation, the bit error rate (BER) required by the standard, and the demodulator algorithm which is used. Thus, the maximum noise figure can be calculated for a given reference sensitivity.

The reference sensitivity required by the GSM standard is -102 dBm for all bands listed in Tab. 2.2. According to the standard [27] a bit error rate smaller than 0.1 % must be maintained. For a GMSK modulated signal with $BT = 0.3$ the

minimum acceptable SNR is obtained from Fig. 2.12. Note that in Fig. 2.12 BER is plotted versus the information bit-energy-to-noise-density ratio E_b/N_0 which is related to SNR by the symbol rate f_{sym} and the effective noise bandwidth of the receiver B through [28]

$$SNR = dB(\frac{f_{sym}}{B}\frac{E_b}{N_0}). \tag{2.36}$$

The effective noise bandwidth B of the receiver will be between 270 kHz and 300 kHz. According to Fig. 2.12 the E_b/N_0 which achieves a BER of 0.1 % depends on the demodulator algorithm. While symbol-by-symbol detection requires an E_b/N_0 of more than 8 dB, the same BER performance can be achieved by only 7 dB using the more sophisticated maximum likelihood sequence estimation [29]. Using the data given in Tab. 2.2 this results in a minimum required SNR between 6.5 dB and 7 dB. Therefore, a minimum SNR of 7 dB is assumed in all further considerations.

Thus, the maximum allowable noise figure is calculated from (2.35)

$$NF = -102\,\text{dBm} - (-174\,\text{dBm/Hz} + 53\,\text{dB} + 7\,\text{dB}) = 12\,\text{dB}. \tag{2.37}$$

2.3.3. Reference Interference Level

Reference interference performance specifies the receiver performance under co-channel and adjacent channel interference conditions. According to the GSM standard [27] the receiver must maintain a bit error rate below 0.1 % at a wanted signal 20 dB above the reference sensitivity while being exposed to the interferer levels listed in Fig. 2.13. As the adjacent channel interferers are very close to the wanted channel the reference interference specification is used to specify the corner frequencies of the channel filter and the required LNA linearity.

2.3.4. Blocking Characteristics

A GSM compliant receiver must be able to withstand blockers defined by a band specific blocking profile while receiving a desired GMSK modulated signal at a sensitivity of -99 dBm. It can be distinguished between inband and out-of-band blocking profiles. The out-of-band and inband blocking profiles for all relevant GSM bands are shown in Fig. 2.14 and Fig. 2.15, respectively. Blockers can have two major effects on the performance of an integrated receiver. First, a large signal blocker can desensitize the receive chain due to the nonlinear effects described in 2.2.2 and second, blockers can mix with local oscillator phase noise

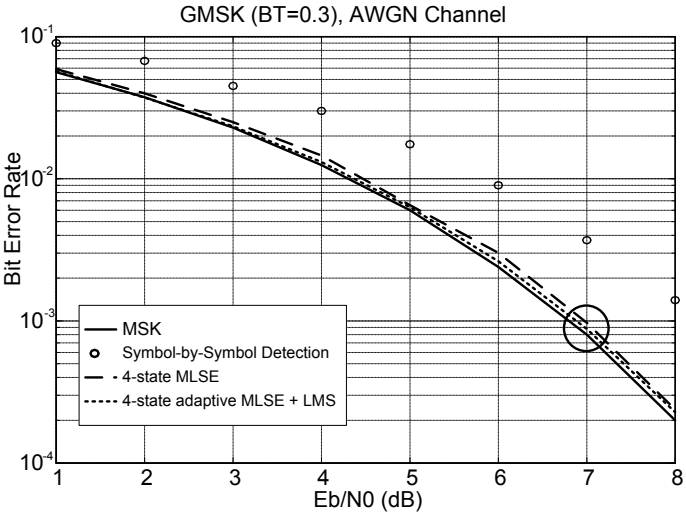


Figure 2.12.: Bit error rate vs. E_b/N_0 for different GMSK demodulator algorithms (from [29]).

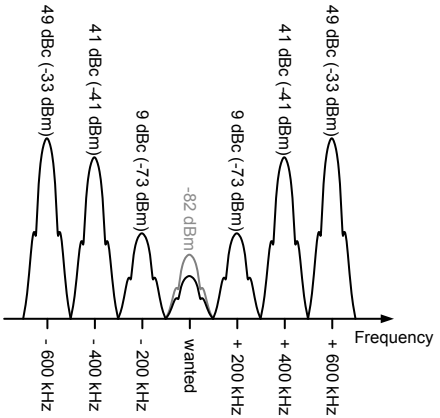


Figure 2.13.: GSM reference interference level specification.

Offset frequency MHz	Phase noise dBc/Hz			
	GSM 850	EGSM 900	DCS 1800	PCS 1900
0.6	-119	-119	-116	-116
1.6	-129	-129	-126	-126
3.0	-139	-139	-136	-136
10.0	-139	-157	-136	-136
20.0	-162	-162	-150	-150
80.0	-162	-162	-150	-162
100.0	-162	-162	-162	-162

Table 2.3.: Local oscillator phase noise requirements.

at the downconversion mixer stage(s) thus translating LO phase noise to the wanted channel as described in chapter 2.2.1. The large out-of-band blockers are usually attenuated to inband level by the RF bandselect filter preceding the receiver chip. Thus, the largest blockers the receiver itself must deal with are at inband blocker level. From Fig. 2.15 the most critical inband blocker is identified at 3 MHz offset from the wanted channel with a power of -23 dBm in the GSM low-bands and at -26 dBm in the GSM high-bands, because it is close to the wanted channel at relatively high power. The 3 MHz inband blocker specifies the 1 dB desensitization point of the receiver. The blocker mask itself is used to specify the local oscillator phase noise profile as discussed below.

Reciprocal mixing – Local oscillator phase noise requirements As the sensitivity is allowed to degrade by 3 dB under blocking conditions the maximum noise contribution due to reciprocal mixing is equal to the noise floor of -109 dBm. Thus, the maximum allowable phase noise for a given blocker level and offset frequency can be calculated by

$$dB(L(\Delta f)) = dBm(P_{noise}) - dBm(P_{blocker}) + dB(B). \tag{2.38}$$

For a bandwidth of 200 kHz and a noise floor of -109 dBm this yields

$$dB(L(\Delta f)) = -dBm(P_{blocker}) - 162\,\text{dB}. \tag{2.39}$$

The resulting local oscillator phase noise requirements for the GSM bands at hand are listed in Tab. 2.3. Note that the derived values do not account for a possible bandselect filter which would at least reduce the requirements for the out-of-band blockers by its selectivity.

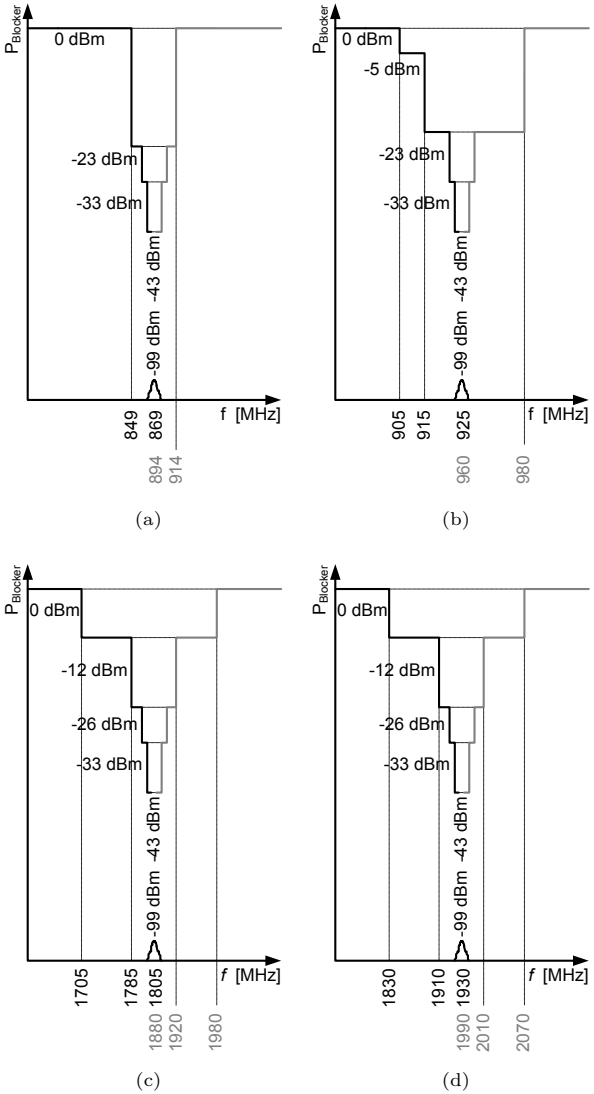


Figure 2.14.: GSM out-of-band blocking profiles for GSM 850 (a), EGSM 900 (b), DCS 1800 (c), and PCS 1900 (d).

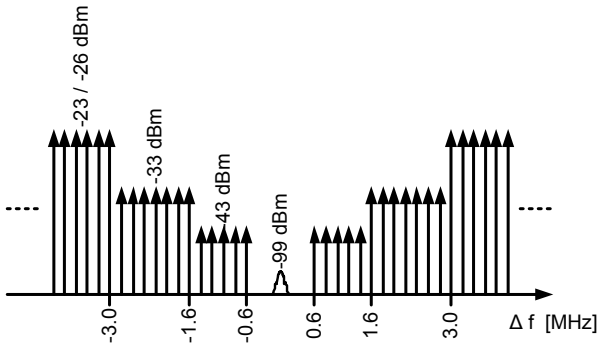


Figure 2.15.: GSM inband blocking profile. -26 dBm applies to DCS1800 / PCS1900, -23 dBm applies to GSM850 / EGSM900.

2.3.5. Intermodulation Characteristics – IIP3

According to the GSM standard [27] a static sine wave and a GMSK modulated interferer at -49 dBm are applied at 800 kHz and 1.6 MHz offset from the wanted channel. Thus the intermodulation product is generated in the wanted channel and interfers with the desired signal. Under these conditions, the sensitivity is allowed to degrade by 3 dB to -99 dBm. Due to the increased signal power the maximum allowable intermodulation product can be at the same level as the noise floor. Thus, the maximum allowable third order intermodulation product is

$$P_{IM3} = -102\,\text{dBm} - 7\,\text{dB} = -109\,\text{dBm}. \tag{2.40}$$

Using (2.13) the corresponding third order intercept point can be calculated

$$P_{IIP3} = -49\,\text{dBm} + \frac{-49\,\text{dBm} + 109\,\text{dBm}}{2} = -19\,\text{dBm}. \tag{2.41}$$

2.3.6. AM Suppression Characteristics – IIP2

The second order intercept point requirement can be derived from the AM suppression characteristic [27]. According to subclause 5.2 the receiver must withstand a -31 dBm GSM TDMA signal modulated in GMSK at offset frequencies larger than 6 MHz at a sensitivity of -99 dBm. Again, the maximum allowable second order intermodulation product is at -109 dBm. From (2.15) the second order intercept point is

$$P_{IIP3} = -31\,\text{dBm} - 31\,\text{dBm} + 109\,\text{dBm} = 47\,\text{dBm}. \tag{2.42}$$

2.4. System Considerations for a Direct Conversion Receiver – GSM Receivers State-of-the-Art

Over the last decade direct conversion and low-IF receivers have become the architecture of choice for GSM receivers. In this chapter design considerations and the state-of-the-art in GSM receiver design are discussed. A survey of performance data for GSM receivers published since 2002 are listed in Tab. 2.4 showing that the prevalent architecture is the direct conversion receiver.

As described in chapter 2.2.1 noise of the individual receiver building blocks is scaled down by its preceding gain. Therefore, the approach for achieving a given noise figure specification is to design for low noise and high gain in the first stages of the receiver. Obviously, this strategy is limited by mixer linearity – if the gain of the LNA is too high the mixer stage is easily overloaded and SNR degrades. Moreover, as discussed before, adjacent channel interferers and close-in blockers, which cannot be filtered in the RF, can be significantly higher than the wanted signal also limiting the permissible gain preceding the mixer. Typically, the RF gain implemented in GSM receivers is about 20 dB to 30 dB. After downconversion, at the intermediate frequency or baseband, the signal is filtered and amplified thus reducing blockers and adjacent interferers. Often, baseband filters are implemented as active RC filters [18, 30–34] due to their superiority to gm-C filters in terms of linearity. Recently, discrete time techniques have been presented which use switched capacitor filtering in the baseband [6]. The gain and the filter order implemented in the baseband depend on the dynamic range provided by the analog-to-digital converter (ADC). On the one hand, if the system is designed as a SoC with on-chip ADCs analog baseband performance can be traded for dynamic range of the ADCs [35]. On the other hand, if the receiver is utilizing low dynamic range ADCs, baseband performance must be good enough to fulfill the GSM specification in front of the ADC resulting in more stringent baseband filtering requirements.

In [18, 30, 31] low dynamic range ADCs are used resulting in a high gain range of roughly 100 dB to reduce the input referred noise of the ADCs. As mentioned above, about 20 dB to 30 dB are realized in the RF while the rest is implemented by variable gain amplifiers (VGA) in the baseband. A baseband gain up to 80 dB can easily lead to clipping of the ADCs as DC offsets are amplified by a factor of up to 10000. Thus, a typical offset of 1 mV would ideally be amplified to 10 V easily exceeding any realistic ADC full scale range. This requires DC offset correction circuitry (DCOC) adding design complexity, area, power consumption, and noise. Moreover, a significant amount of signal energy is concentrated around DC in the GMSK modulated GSM system resulting in severe SNR degradation

due to DC filtering. In addition, gain and phase of the inphase and quadrature baseband paths will have a certain mismatch which increases with the baseband gain thus increasing the I/Q mismatch problem. Moreover, tight gain control must be exercised in order to avoid overloading the ADCs at high wanted signal input power levels requiring fine gain steps in the baseband VGAs. While adding complexity for automatic gain control (AGC) the ADC inputs are operated close to fullscale and thus at maximum SNR over a large part of the input dynamic range. Due to limited ADC dynamic range adjacent channel interferers and blockers cannot be accomodated by the ADCs thus requiring the baseband filters to provide enough attenuation close to the wanted channel to reduce interferers to cochannel level. Hence, the filter order must be relatively high ranging between 5 and 9 [18, 30, 31].

In [32, 33, 36] baseband gain is reduced to a minimum thus alleviating its associated issues. In [36] active filtering in the baseband is completely eliminated and all gain is realized in the LNA and mixer. Instead, these designs [32, 36] rely on high dynamic range ADCs of around 14 bit resolution which are designed to accomodate all signals up to the +49 dBc adjacent interferer at 600 kHz offset (cf. Fig. 2.15). The preceding analog baseband filtering is merely used to reduce blockers at higher offset frequencies to the same level as the 600 kHz adjacent channel interferer while the actual channel filtering is realized in the digital domain. This approach is facilitated by high resolution continuous-time delta-sigma converters which use oversampling, noise shaping, high-order loop filters, and multibit quantization [37, 38]. As baseband gain is kept low DC offsets cannot saturate the ADC input thus avoiding complex DC offset correction circuitry. Moreover, gain control complexity can be greatly reduced to a single gain step in the LNA (20 dB in [36], 30 dB in [32]). Thus, the ADC is not always operated at maximum SNR. In case of tighter gain control, as described above, this does not pose a problem in a voice centric standard like GSM as the user cannot take advantage of SNR through a higher data rate.

2.5. Out-of-band Interference Suppression in Wireless Receivers

It has been mentioned that large blockers along with a weak wanted signal can desensitize the receiver and render reception of the wanted signal impossible. Depending on the system, the dominating blockers can either emanate from the transmitter of the handset itself or from other users' transmitters. The first case applies to frequency-division full duplexing (FDD) where receiver and transmitter are always active as seen in the UMTS / WCDMA standard. The second case corresponds to time-division duplex systems (TDD) where the handset is either

		[30]	[31]	[18]	[32]	[33]	[36]	[39]	[34]	[6]
Architecture		DCR	low-IF	DCR	DCR	DCR	DCR	low-IF	DCR	low-IF
NF	[dB]	3.1 – 4.1	2.7	2.7 / 3.3	2.6 / 3	3	2.1	2.5	2.7/3	2
Sensitivity	[dBm]	-109 – -107	-110			-108				-110
Gain	[dB]	10 – 100	100	5 – 102	57	50	31.5	2 – 94		
ADC DR	[dB]				14 bit	14 bit	14.5 bit	14 bit		> 80 dB
IIP2	[dBm]	50/50	40/40	51 / 41	50/50		50	> 45	50/45	46
IIP3	[dBm]		-15/-15	-13 / -12			-9.5	-11/-12	-12/-11	-25
P1dB	[dBm]			-25 / -23	-22/-22		-24			
3 MHz Blocker NF	[dB]	6.6 / 7.1		5.4 / 5.5			5	10.5/9		
DCOC		analog	analog	analog	DSP	DSP	DSP	DSP	DAC	
BB Filter Type		RC/gm-C	RC	RC	RC	RC	RC	gm-C	RC	SC
BB Filter Order		7	5	9	3	3	1		5	
Current / Power		80 mA	93 mA	56 mA	250 mW	75 mA	38 mA	140 mW	84 mA	60 mA
Technology		0.35 um BiCMOS	180 nm CMOS	250 nm CMOS	130 nm CMOS	250 nm BiCMOS	90 nm CMOS	130 nm CMOS	130 nm CMOS	90 nm CMOS
Voltage	[V]	2.7 – 3.6	2.7 – 3	2.8	1.5/2.5	2.7	1.5	1.5 / 2.7	2.8	1.4

Table 2.4.: Performance data of published GSM receivers.

receiving or transmitting. Here, other users' transmitters constitute the most severe blocking condition. In this section, methods of interference suppression are reviewed.

2.5.1. Conventional Front-End with SAW Filter

In FDD systems, the issue is usually solved by passive filters as shown in Fig. 2.16(a). The transmit and receive paths are separated by duplex filters which act as bandpass filters for the transmit and receive path, respectively. Due to the high power level at the output of the transmit power amplifier and finite Tx-Rx isolation of the duplexer the transmitter signal leaks into the Rx path. Hence, the wanted signal can be corrupted by third-order intermodulation products of Tx leakage and a received blocker. Therefore, an additional SAW bandpass filter is installed in the receive path further lowering the transmitter leakage. To overcome the SAW filter insertion loss and the associated sensitivity degradation the off-chip LNA1 with increased linearity requirements is inserted between duplexer and SAW bandpass filter.

In TDD systems, a switch connects either the receiver or the transmitter to the antenna. To lower large out-of-band blockers to a level which is acceptable for the receiver an external, passive SAW bandpass filter is used as shown in Fig. 2.16(b).

It is desirable to remove external SAW filters for several reasons. First of all, SAW filters add to the bill of materials and thus increase cost and board area, particularly in highly integrated multimode, multiband transceivers. Moreover, the SAW filters' insertion loss adds to the receiver noise figure and decreases sensitivity. Therefore, efforts are made to eliminate external filters.

2.5.2. On-chip Filtering Techniques

The techniques which have been presented to eliminate SAW filters are listed in Fig. 2.17. The purpose of all filtering approaches is to provide considerably better selectivity at RF than is possible with passive LC tanks. Their quality factor is usually limited by the Q of the inductors which is in the range of 5–20. All on-chip filtering techniques which have been presented for replacing SAW filters by on-chip filtering are based on one of the three techniques shown in Fig. 2.17.

Quality factor enhancement techniques [40–43] use negative resistance circuits to cancel LC tank loss and thus increase the effective LC tank Q. An example using a cross-coupled negative resistance pair is shown in Fig. 2.18(a).

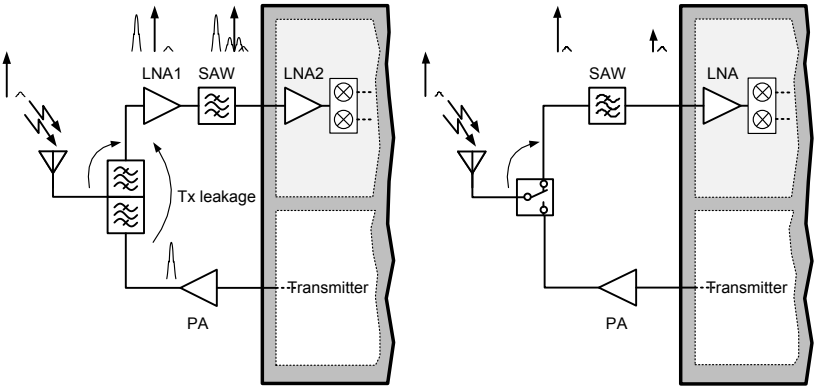


Figure 2.16.: Out-of-band blocking in a full duplex system (a), a half duplex system (b).

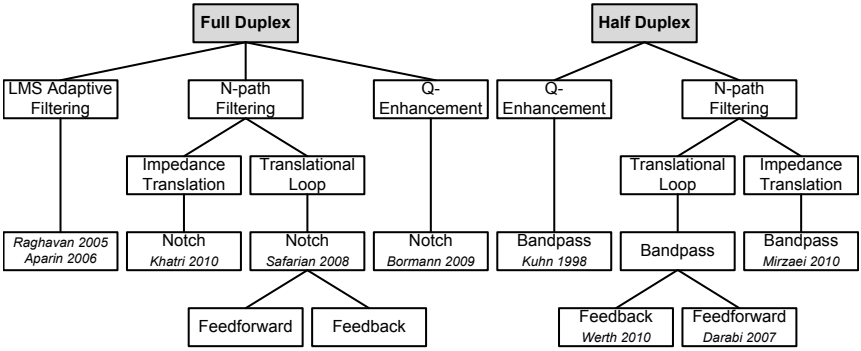


Figure 2.17.: Overview of interference suppression techniques in FDD full-duplex and TDD half-duplex systems.

N-path filtering The concept of a translational loop (Fig. 2.18(b)) as well as of a driving point impedance translation (Fig. 2.18(c)) are based on N-path filtering [44]. The idea of the concepts is to translate a narrow filter characteristic from the baseband to RF by modulators. Thus, the translational loop shown in Fig. 2.18(b) translates the baseband filter response $H(s)$ around the modulators' local oscillator frequency resulting in a transfer function of the baseband response shifted to RF. In Fig. 2.18(c), on the other hand, the driving point impedance seen into the modulator input node is the baseband impedance shifted to the local oscillator frequency.

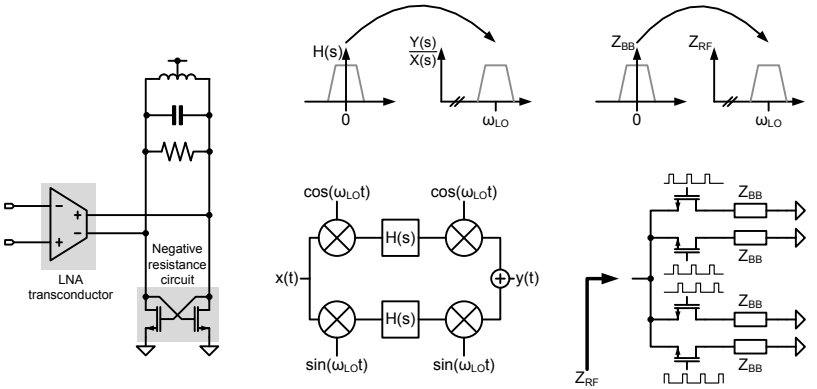


Figure 2.18.: Techniques for high-Q filtering at RF: Q-enhanced LC tank (a), translational loop (b), impedance translation (c).

Transmitter Leakage Suppression

Transmitter leakage suppression methods take advantage of the known interferer frequency and signal properties. Thus, several proposed techniques aim at realizing an on-chip notch filter at the transmitter frequency.

In [45] a WCDMA transceiver with tuned Q-enhanced LC notch filter to suppress Tx leakage is presented. [46] demonstrates another LNA with Q-enhanced LC notch filter for a WCDMA system which requires only a single inductor.

The concept of a low-pass translational loop is implemented in [47] and [48]. In both cases a low-pass baseband filter is frequency translated using the transmitter

local oscillator signal resulting in a bandpass translational loop. Using the bandpass, a Tx leakage replica is generated and subtracted from the Tx leakage signal incident on the LNA. Thus, a notch filter centered at the Tx frequency is generated. Both, [47] and [48], implement the low-pass translational loop in the feedback path. For comparison, the low-pass translational loop is also implemented as a feedforward path in [47]. It is pointed out [47] that the feedback configuration decreases linearity requirements for the loop, reduces sensitivity to I/Q mismatch, and does not affect input matching of the LNA.

Impedance translation for Tx leakage suppression in CDMA-2000 and WCDMA direct conversion receivers is proposed in [49] and [50], respectively. In [49] a notch at the Tx frequency is created by providing a low impedance load Z_{BB} to the receive mixer at the transmitter offset frequency $f_{Rx} - f_{Tx}$ while maintaining a high impedance load at DC. Upon translation of the baseband impedance to RF through the receive mixers a high impedance load is presented to the LNA in the receive band while the LNA load is low impedance at the transmitter frequency. Hence, wanted signals in the receive band are amplified and Tx leakage is suppressed.

Other techniques which have been proposed to mitigate Tx leakage or interference between different radios operating on the same chip involve adaptive filters. In [51] a cancellation signal is generated by amplitude and phase alignment of a replica signal of the original interferer. Here amplitude and phase alignment are controlled by an adaptive filter. The implementation in [51] is targeted at mitigating interference between collocated Bluetooth and IEEE 802.11b radios. A similar approach using continuous-time least-mean square (LMS) adaptive filtering for Tx leakage suppression in CDMA systems is taken in [52]. It is pointed out that duplexer group delay can severely limit Tx leakage suppression in the LMS adaptive filtering approach [52], while the translational loop notch filter approach does not suffer from this drawback as the signal is picked up after the duplexer [48].

RF Bandpass Filtering

In a half duplex system the strongest blocker is set by other users' transmitters. Thus, the location of the interferer is unknown and notch filtering cannot be applied. Instead, an RF bandpass filter is required which passes the wanted signal and attenuates interferers. As seen in Fig. 2.17 Q-enhancement as well as N-path filtering have been proposed to address the problem.

Q-enhanced tuned LC bandpass filters are presented in [40, 42] to address the problem.

The concept of a translational loop for bandpass filtering has been presented

by [53] and [16] to cancel interferers in narrow-band receivers. A high-pass filter is frequency translated by the receiver local oscillator thus generating a notch filter centered at the wanted channel frequency. The notch filter is used to suppress the wanted signal and pass a blocker replica which is subtracted from the incident blocker. Both, [53] and [16] apply the blocker subtraction in a feedforward configuration. In [16] the concept is proven for GSM in the 1900 MHz (PCS) band by a fully integrated solution in 65 nm CMOS. A stop-band rejection of 21 dB is achieved at a noise figure of 6.8 dB and a 1 dB desensitization point of 0 dBm for a blocker at 80 MHz offset. A corresponding feedback approach is focus of this work.

Recently, driving point impedance translation techniques for high-Q bandpass filtering have attracted interest [54–56]. In [54] GSM compliant operation in the 1900 MHz (PCS) band is demonstrated. The published front-end exhibits a noise figure of 3.1 dB without blocker. With 0 dBm blocker at 80 MHz offset the gain is compressed by 0.8 dB and the noise figure rises to 11.4 dB.

3. Feedback Interference Cancellation – System Considerations

In this section, system considerations for RF bandpass filtering using feedback interference cancellation are made. The observations from the system level are essential for proper circuit design. First, the concept of feedback interference cancellation is introduced, then the system transfer function is derived and used to assess stability and filtering performance. Then, the influence of nonlinearity in the loop is considered. Finally, an analysis of nonidealities like influence of I/Q mismatch and noise on the system performance is conducted.

The concept of active feedback interference cancellation is shown in Fig. 3.1. The incoming wanted and blocker signal are amplified by an LNA with LC tank load. The output signal is fed into the active cancellation filter core and downconverted to baseband by the receiver local oscillator signal. In order to boost the open loop gain, baseband amplifiers might be necessary. The wanted signal is eliminated by highpass filtering, a blocker replica is upconverted to RF and subsequently subtracted from the incoming blocker signal at the output of the LNA transconductor stage thus resulting in a partial cancellation of the blocker signal. In that sense, the interference cancellation loop acts as a control loop which suppresses the blocker by the open loop gain.

Subsequently, expressions will be derived describing the small signal behavior of the loop which facilitate stability and selectivity considerations.

3.1. Derivation of the System Transfer Function

The closed loop transfer function of the interference cancellation loop can be expressed by

$$G(s) = g_{m,\mathrm{LNA}} \cdot \frac{Z_{LC}(s)}{1 + Z_{LC}(s) \cdot H_{core}(s)}, \tag{3.1}$$

with $g_{m,\mathrm{LNA}}$ being the LNA transconductance, Z_{LC} the LC tank impedance,

$$Z_{LC}(s) = \frac{\frac{s}{\omega_{LC}}\omega_{LC}L}{\left(\frac{s}{\omega_{LC}}\right)^2 + \frac{1}{Q}\left(\frac{s}{\omega_{LC}}\right) + 1} \tag{3.2}$$

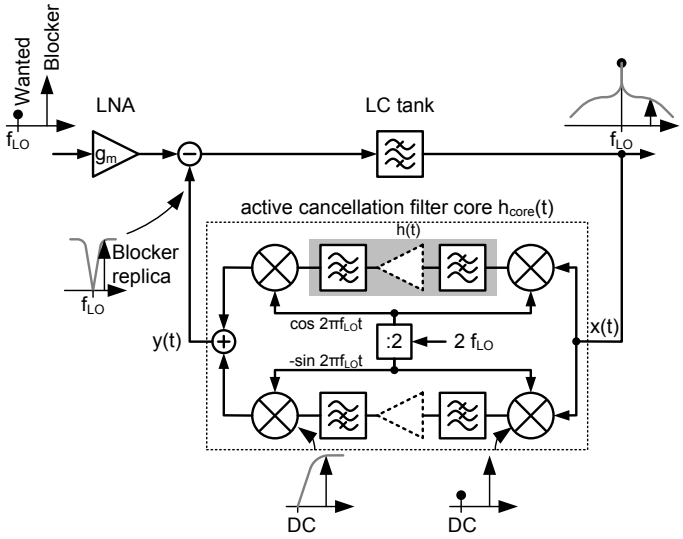


Figure 3.1.: Block diagram of feedback cancellation mechanism.

and $H_{core}(s)$ the filter core transfer function. The open loop gain is found to be

$$G_{ol}(s) = Z_{LC}(s) \cdot H_{core}(s). \tag{3.3}$$

It has been shown that the filter core transfer function $H_{core}(s)$ is merely a translation of the baseband filter response to the LO frequency [16]. By inspection of Fig. 3.1 the filter core impulse response $h_{core}(t)$ can be found by

$$\begin{aligned} y(t) &= \int x(\tau)h(t-\tau)\left[\cos(\omega_{LO}\tau)\cos(\omega_{LO}t) + \sin(\omega_{LO}\tau)\sin(\omega_{LO}t)\right] d\tau \\ &= \int x(\tau)h(t-\tau)\cos(\omega_{LO}(t-\tau))\, d\tau \\ &= x(t) * \underbrace{\left[h(t)\cos(\omega_{LO}t)\right]}_{=h_{core}(t)}. \end{aligned} \tag{3.4}$$

The filter core baseband transfer function consists of a high-pass and a low-pass filter with the low-pass corner frequency being two to three decades higher than

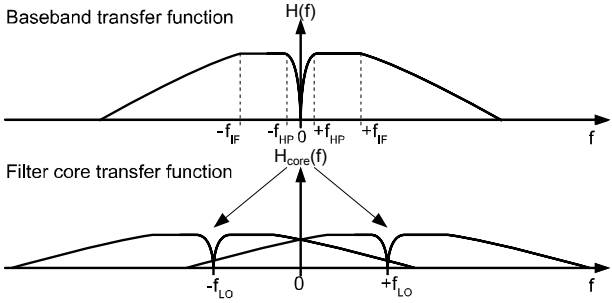


Figure 3.2.: Filter core transfer function as a result of translating the baseband transfer function to the LO frequency.

the high-pass corner frequency. The baseband transfer function is

$$H(s) = \frac{\frac{s}{j\omega_{HP}}}{1+\frac{s}{j\omega_{HP}}} \cdot \frac{1}{1+\frac{s}{j\omega_{IF}}}. \tag{3.5}$$

By using the frequency shifting property of the Laplace transform [16] the filter core transfer function can be expressed by

$$H_{core}(s) = \frac{g_{m,fb}}{2} \cdot \left[\frac{(s-j\omega_{LO})/\omega_{HP}}{\left(1+\frac{s-j\omega_{LO}}{\omega_{HP}}\right)\left(1+\frac{s-j\omega_{LO}}{\omega_{IF}}\right)} + \frac{(s+j\omega_{LO})/\omega_{HP}}{\left(1+\frac{s+j\omega_{LO}}{\omega_{HP}}\right)\left(1+\frac{s+j\omega_{LO}}{\omega_{IF}}\right)} \right], \tag{3.6}$$

where ω_{LO} represents the local oscillator frequency, ω_{HP} the highpass corner frequency, and ω_{IF} the downconversion mixer bandwidth. The effective filter core transconductance is represented by $g_{m,fb}$. A graphical representation of $H_{\mathrm{core}}(s)$ is provided in Fig. 3.2. As seen in (3.6), for the case of highpass baseband filters a notch at the Rx LO frequency is obtained yielding low loop gain at frequencies close to the receive LO and high loop gain at offset frequencies larger than the high pass corner frequency. Thus, the interference cancellation loop passes signals close to the Rx LO with an approximate gain of $g_{m,\mathrm{LNA}} \cdot Z_{LC}$

while signals at offset frequencies larger than the highpass corner frequency are rejected by approximately $\frac{1}{H_{core}(s)}$. Therefore, it is desirable to have large gain in the feedback path of Fig. 3.1.

3.2. System Stability Considerations

It is important to consider the filter core IF bandwidth for two reasons: depth of the filter core notch and feedback loop stability.

Note that the mixers act as up- and downconverters simultaneously. Thus, the downconversion mixer does not only generate a baseband component but also an RF signal at twice the LO frequency. The output spectral component of the downconversion mixer at $2f_{LO}$ falls into the passband of the highpass filter and appears at the input of the upconversion mixer. Subsequently, the component at $2f_{LO}$ is shifted to f_{LO} by the upconversion mixer. As a result, the passbands of the frequency shifted highpass filters tail off into the notches of the respective image band on the negative and positive frequency axis as shown in Fig. 3.2. This process leads to an imperfect, shallow notch response generated by the filter core and thus degrades in-band gain upon subtraction at the LNA transconductor stage output. Obviously, this effect is more severe the higher the IF bandwidth is.

On the other hand, it is desirable to have a high IF bandwidth for loop stability as the open loop phase around the LO frequency quickly approaches the $\pm 180^\circ$ limits for low IF bandwidth resulting in low phase margin. Moreover, a high IF bandwidth is advantageous as the interference cancellation loop will only attenuate blockers that fall within the loop bandwidth around the LO frequency.

Thus, a compromise between gain degradation, phase margin, and loop bandwidth must be sought. A qualitative view of open loop gain and phase is depicted in Fig. 3.3 demonstrating the influence of IF bandwidth on notch depth and phase margin.

3.3. Closed Loop Linearity Analysis

So far, only the linear loop behavior has been considered. This section expands on the linear system analysis by investigating the influence of nonlinearities in the loop. A system model comprising the most important nonlinearities is shown in Fig. 3.4.

Volterra series analysis [57] is used to analyze the nonlinear behavior of the circuit. It is presumed that the circuits are only mildly nonlinear and that the dominating nonlinearities are found in the LNA transconductance stage (G_m in

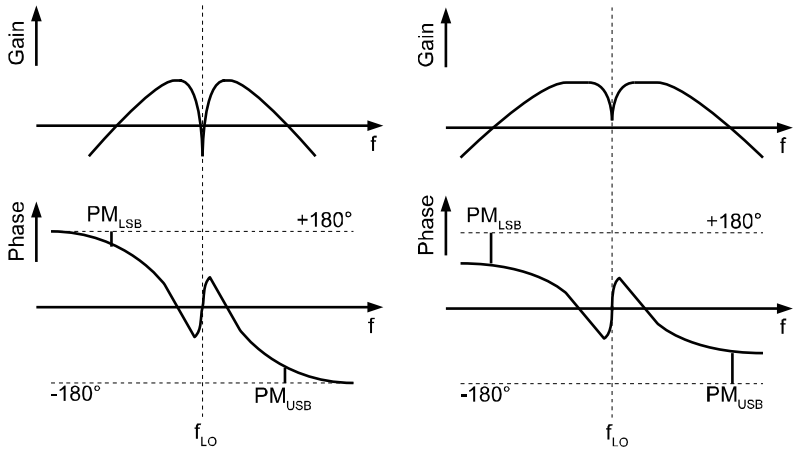


Figure 3.3.: Qualitative view of open loop frequency response low IF bandwidth: deep notch, low phase margin (a), high IF bandwidth: shallow notch, high phase margin (b).

Fig. 3.4) and in the input stage of the feedback loop mixer (F in Fig. 3.4). To simplify matters, only nonlinearities up to third order are evaluated. Furthermore, the forward path of the loop comprising a cascode stage and an LC tank load is assumed to be linear. This assumption can be justified by Volterra analysis as laid out in [57]. The LNA as well as the mixer input transconductance stages are presumed to be memoryless nonlinearities i.e. the input signal is not filtered before interacting with the nonlinearity. In the feedback path the nonlinear response of the mixer input stage is filtered by the active cancellation filter core thus introducing frequency dependency and memory in the system.

In this case the feedback path Volterra kernels up to third order can be expressed by

$$F_1(s) = F_1 H_{core}(s), \tag{3.7}$$

$$F_2(s_1, s_2) = F_2 H_{core}(s_1 + s_2), \tag{3.8}$$

$$F_3(s_1, s_2, s_3) = F_3 H_{core}(s_1 + s_2 + s_3), \tag{3.9}$$

where F_1, F_2, F_3 are the Taylor coefficients of the mixer input stage. Similarly, the LNA input stage nonlinearity can be expressed in terms of its Taylor coefficients

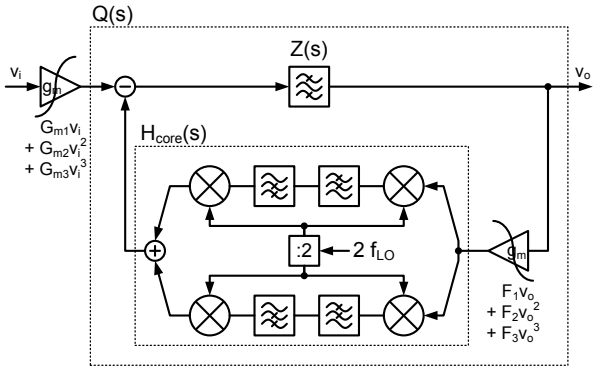


Figure 3.4.: Block diagram of the nonlinear feedback cancellation system model.

G_{m1}, G_{m2}, G_{m3}.

The closed loop Volterra kernels from the output of the LNA input stage to the LC tank load output are

$$Q_1(s) = Z(s)/\left[1 + F_1(s)Z(s)\right], \tag{3.10}$$

$$Q_2(s_1, s_2) = -Q_1(s_1)Q_1(s_2)Q_1(s_1 + s_2)F_2(s_1, s_2), \tag{3.11}$$

$$\begin{aligned} Q_3(s_1, s_2, s_3) &= Q_1(s_1)Q_1(s_2)Q_1(s_3)Q_1(s_1 + s_2 + s_3) \\ &\quad \times \left[-F_3(s_1, s_2, s_3) + 2F_2(s_1, s_2)Q_1(s_1 + s_2)F_2(s_3, s_1 + s_2)\right]. \end{aligned} \tag{3.12}$$

This result has been obtained from the general expression of nonlinear feedback by assuming a linear forward path.

The complete nonlinear system can be characterized by cascading the feedback loop kernels $Q_1(s), Q_2(s_1, s_2), Q_3(s_1, s_2, s_3)$ and the LNA nonlinearity Taylor coefficients

$$G_1(s) = Q_1(s)G_{m1}, \tag{3.13}$$

$$G_2(s) = Q_1(s_1 + s_2)G_{m2} + Q_2(s_1, s_2)G_{m1}^2, \tag{3.14}$$

$$\begin{aligned} G_3(s) &= Q_3(s_1, s_2, s_3)G_{m1}^3 + Q_1(s_1 + s_2 + s_3)G_{m3} \\ &\quad + \frac{2}{3}\left[Q_2(s_1, s_2 + s_3) + Q_2(s_2, s_1 + s_3) + Q_2(s_3, s_1 + s_2)\right]G_{m1}G_{m2}. \end{aligned} \tag{3.15}$$

From the cascade connection in (3.13), (3.14), and (3.15) all nonlinear responses including gain compression, second and third order intermodulation, as well as desensitization of the feedback interference cancellation loop can be calculated.

Thus the input referred third order intercept point of the feedback loop according to Tab. 2.1 is given by

$$IIP3_Q = \sqrt{\frac{4}{3}\left|\frac{Q_1(j\omega_1)}{Q_3(j\omega_1, j\omega_1, -j\omega_2)}\right|}. \tag{3.16}$$

Similarly, the input referred 1 dB desensitization point is

$$iDP_{1dB,Q}(\Delta\omega) = \sqrt{\frac{2}{3}\left(1-10^{-1/20}\right)\left|\frac{Q_1(j\omega_{LO})}{Q_3(\omega_{LO}, \omega_{LO}+\Delta\omega, -(\omega_{LO}+\Delta\omega))}\right|}. \tag{3.17}$$

As seen in (3.16) and (3.17) $IIP3$ and desensitization depend on the third order nonlinearity $Q_3(s_1, s_2, s_3)$. Hence, it is instructive to examine (3.12) more closely to understand operation of the feedback loop. As seen in the equation the interacting tones at s_1, s_2, and s_3 are first filtered by the linear closed loop transfer function $Q_1(s)$. Next, the filtered tones interact with the third order nonlinearity forming a response at $s_1 + s_2 + s_3$ which is fed back to the input and filtered by the linear closed loop transfer function. If the feedback path exhibits significant second order nonlinearity yet another mechanism contributes third order distortion represented by the second term in (3.12). Two filtered tones at s_1 and s_2 interact with the second order nonlinearity producing a response at $s_1 + s_2$. This response is fed back to the input of the loop, filtered by $Q_1(s)$, and interacts with the third tone s_3 at the second order nonlinearity thus ultimately causing a third order response at $s_1 + s_2 + s_3$. Finally, the tone at $s_1 + s_2 + s_3$ is processed again by the linear closed loop transfer function $Q_1(s_1 + s_2 + s_3)$.

From (3.7) – (3.16) the cascade $IIP3$ and 1 dB desensitization points can be derived. For simplicity it is assumed that second order nonlinearity can be neglected and that $H_{core}(j\omega_{LO}) \approx f_{IF}/4f_{LO}$ holds which is a valid assumption as long as $f_{LO} \gg f_{IF}$.

The inband $IIP3$ can be approximated by

$$\frac{1}{IIP^2_{3,G}} \approx \frac{A_V^3}{IIP^2_{3,F}} \cdot \frac{F_1}{G_{m1}} \cdot \frac{f_{IF}}{4f_{LO}} + \frac{1}{IIP^2_{3,G_m}}, \tag{3.18}$$

where A_V represents the inband voltage gain.

Similarly, the input referred 1 dB desensitization point for a blocker at offset frequency Δf from the carrier can be derived

$$\frac{1}{iDP^2_{1dB,F}(\Delta f)} \approx \frac{A_V^3}{S(\Delta f)^2} \cdot \frac{F_1}{G_{m1}} \cdot \frac{f_{IF}}{4f_{LO}} \cdot \frac{1}{iDP^2_{1dB,F}} + \frac{1}{iDP^2_{1dB,G_m}}, \tag{3.19}$$

with A_V being the inband voltage gain, $S(\Delta f)$ the loop selectivity at offset frequency Δf from the carrier at f_{LO}, and $iDP_{1dB,F}$ and iDP_{1dB,G_m} being the inband input referred 1 dB desensitization points of feedback path and LNA input transconductance, respectively.

From (3.19) it is noted that the input referred 1 dB desensitization point of the feedback loop is improved from its inband value by the loop selectivity $S(\Delta f)$. Conversely, the desensitization point of the LNA input transconductance stage remains unaffected. This is due to blockers at offset frequency Δf being filtered by the loop.

f_{HP}	4 MHz
f_{IF}	250 MHz
f_{LC}	1900 MHz
f_{LO}	1900 MHz
Q	10
L	3 nH
G_{m1}	20 mS
$IIP_{2,Gm}$	∞
$IIP_{3,Gm}$	+8 dBm
F_1	40 mS
$IIP_{2,F}$	∞
$IIP_{3,F}$	0 dBVrms

Table 3.1.: Parameters for the simulation example of Fig. 3.5.

A numerical example for the parameters given in Tab. 3.1 is presented in Fig. 3.5. In the figure the linear response (black) as well as the nonlinear behavior (gray) have been calculated. As pointed out before the inband gain is degraded by the finite filter core notch at the wanted frequency. From comparison of the closed loop transfer function $G_1(f)$ and the transfer function of the LNA with LC tank load ($G_m Z(f)$) this amounts to roughly 2 dB in the example at hand. Moreover, the center frequency of the open ($G_{ol}(f)$) and closed loop response ($G_1(f)$) is shifted by approximately 260 kHz above the carrier frequency. It has been noted before that the closed loop selectivity is set by the open loop gain. As seen in the figure, a maximum open loop gain and selectivity of 19 dB are reached at offset frequencies of 10 MHz to 200 MHz from the carrier. At higher offset frequencies selectivity is reduced due to the limited open loop bandwidth of approximately 300 MHz. From Fig. 3.5 the inband compression point ($iCP_{1dB,G}$) is -12.5 dBm and the inband 1 dB desensitization point ($iDP_{1dB,G}$) is -15.5 dBm. If the LNA input transconductance stage is considered to be linear the desensitization point

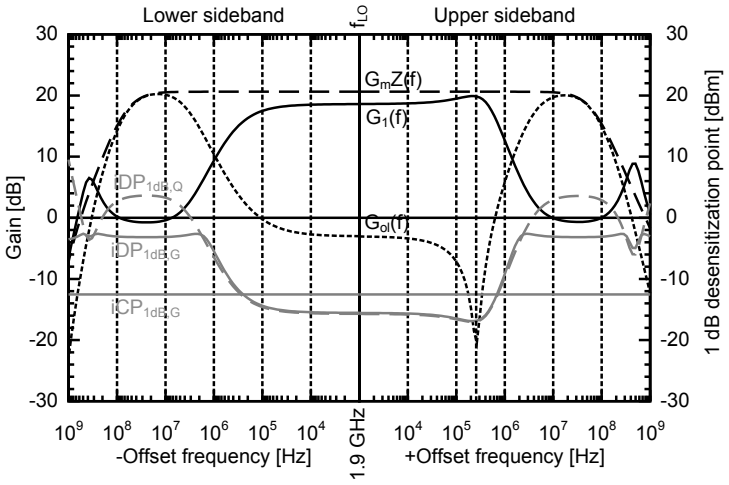


Figure 3.5.: Lower and upper sideband characteristic of linear transfer function without filtering (G_mZ), linear transfer function with filtering ($G_1(f)$), closed loop input referred 1 dB desensitization point ($iDP_{1dB,Q}$), closed loop input referred 1 dB desensitization point with LNA transconductance ($iDP_{1dB,G}$).

$iDP_{1dB,Q}$ is commensurate to the closed loop selectivity as given by the linear loop transfer function. Thus, the desensitization point is increased by 19 dB to +4 dBm at offset frequencies of 10 MHz to 200 MHz. When the LNA input transconductance nonlinearity is included the overall cascade desensitization point $iDP_{1dB,G}$ is limited by the LNA and results in roughly -3 dBm. Thus it can be concluded that although the closed loop filter characteristic improves the input desensitization point, linearity is ultimately limited by the LNA input stage where no filtering is applied.

3.4. Nonidealities

The ideal filtering previously described can be impaired by nonidealities like an asymmetric closed loop transfer function, I/Q gain and phase mismatch effects, as well as filter core excess noise. These effects will be addressed subsequently.

3.4.1. Asymmetric Closed Loop Transfer Function

As shown in Fig. 3.6(a) the closed loop transfer function according to (3.1) can be asymmetric around the local oscillator and LC tank center frequency thus leading to degraded filtering in the upper sideband of the LO. This is due to the open loop gain which tails off much quicker below the LO frequency than above as shown in Fig. 3.6(b). Consequently, the upper sideband phase margin is lower than the lower sideband phase margin. The reduced phase margin as well as the flatter impedance characteristic of the LC tank in the upper sideband result in a gain peak and a reduced upper sideband selectivity as seen in Fig. 3.6(a).

To some degree, the asymmetry can be mitigated by reducing the LC tank center frequency as indicated in Fig. 3.6(a). Thus, the local oscillator frequency and the LC tank center frequency do not coincide and the upper sideband phase margin is improved at the expense of the lower sideband phase margin. Obviously, the lower sideband phase margin can be severely degraded if the LC tank center frequency is chosen too low.

3.4.2. Center Frequency Shift

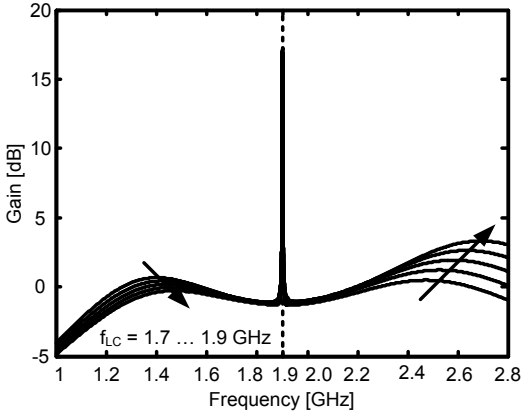
As seen in Fig. 3.5 a center frequency shift occurs. The shift results in the minimum open loop gain not being centered at the carrier frequency f_{LO} but at the offset frequency $f_{LO} + \Delta f$. Correspondingly, the maximum inband gain does not appear in the middle of the wanted band but at the offset frequency Δf above the carrier frequency f_{LO}. In [58] the center frequency shift is evaluated by calculating the minima of the filter core transfer function (3.6). According to [58] the center frequency shift is approximately given by

$$\Delta f \approx \sqrt{f_{LO}^2 + f_{IF} f_{HP}} - f_{LO} \approx \frac{f_{IF} f_{HP}}{2 f_{LO}}. \tag{3.20}$$

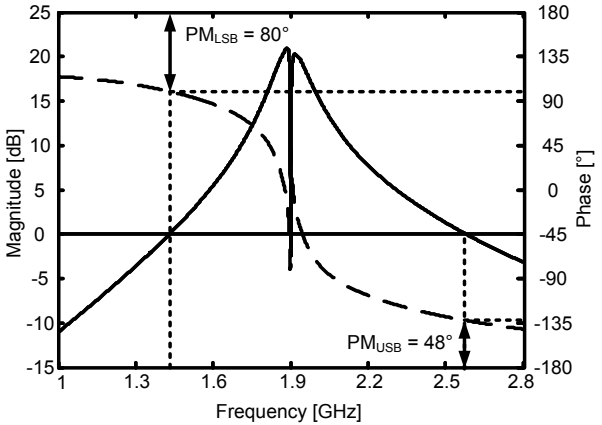
For the numerical example of Tab. 3.1 and Fig. 3.5 (3.20) yields a frequency shift of Δf of 263 kHz which is in good agreement with the value obtained from the plot.

3.4.3. Influence of I/Q Mismatch

A mismatch of the inphase and quadrature components in the filter core shown in Fig. 3.1 can significantly deteriorate the performance of interference cancellation schemes [16, 47, 59]. Therefore the influence of I/Q gain and phase mismatch is assessed subsequently. The ideal case without I/Q mismatch [16] results in a shifted baseband filter response as shown in Fig. 3.8(a) and pointed out before.



(a)



(b)

Figure 3.6.: Exemplary transfer functions with $f_{LO} = 1.9\,\mathrm{GHz}$, $Q = 15$, and maximum open loop gain of 20 dB: closed loop with LC tank center frequencies $f_{LC} = 1.7 \ldots 1.9\,\mathrm{GHz}$ (a), open loop with $f_{LC} = 1.9\,\mathrm{GHz}$ (b).

Subsequently, the effects of I/Q mismatch are analyzed. A detailled derivation of the equations is found in appendix B.

Analysis with Gain Mismatch

The system block diagram describing I/Q gain mismatch is presented in Fig. 3.7(a). Gain mismatch is modeled by different gain factors I and Q for the inphase and quadrature path. The filter core output signal can be described by the convolution integral

$$y(t) = \int x(\tau) \left[I \cos(\omega_{LO}\tau) \cos(\omega_{LO}t) + Q \sin(\omega_{LO}\tau) \sin(\omega_{LO}t) \right] h(t-\tau)\, d\tau. \tag{3.21}$$

After rearranging (3.21) the equivalent block diagram consisting of an ideal path and a mismatch path is obtained in Fig. 3.7(c). Using the frequency shifting property of the Laplace transform the mismatch path output spectrum is determined as

$$M_G = \frac{I-Q}{2} \cdot \frac{1}{2} \left[X(s - j2\omega_{LO}) H(s - j\omega_{LO}) + X(s + j2\omega_{LO}) H(s + j\omega_{LO}) \right]. \tag{3.22}$$

Analysis with Phase Mismatch

Similar to the case of gain mismatch phase mismatch $\Delta\phi$ is incorporated by offset phase angles $\phi_I = +\Delta\phi/2$ and $\phi_Q = -\Delta\phi/2$ for the inphase and quadrature local oscillator signals as shown in Fig. 3.7(b). The output signal can be represented by

$$\begin{aligned} y(t) = \int x(\tau) \big[&\cos(\omega_{LO}\tau + \phi_I) \cos(\omega_{LO}t + \phi_I) \\ &+ \sin(\omega_{LO}\tau + \phi_Q) \sin(\omega_{LO}t + \phi_Q) \big] h(t-\tau)\, d\tau. \end{aligned} \tag{3.23}$$

Rearranging (3.23) yields the equivalent representation of Fig. 3.7(d) consisting of the ideal filter core path and a mismatch path. Similarly, the mismatch path output spectrum is obtained

$$\begin{aligned} M_{Ph} = \sin(\Delta\phi) \cdot \frac{j}{2} \big[&X(s - j2\omega_{LO}) H(s - j\omega_{LO}) \\ &- X(s + j2\omega_{LO}) H(s + j\omega_{LO}) \big]. \end{aligned} \tag{3.24}$$

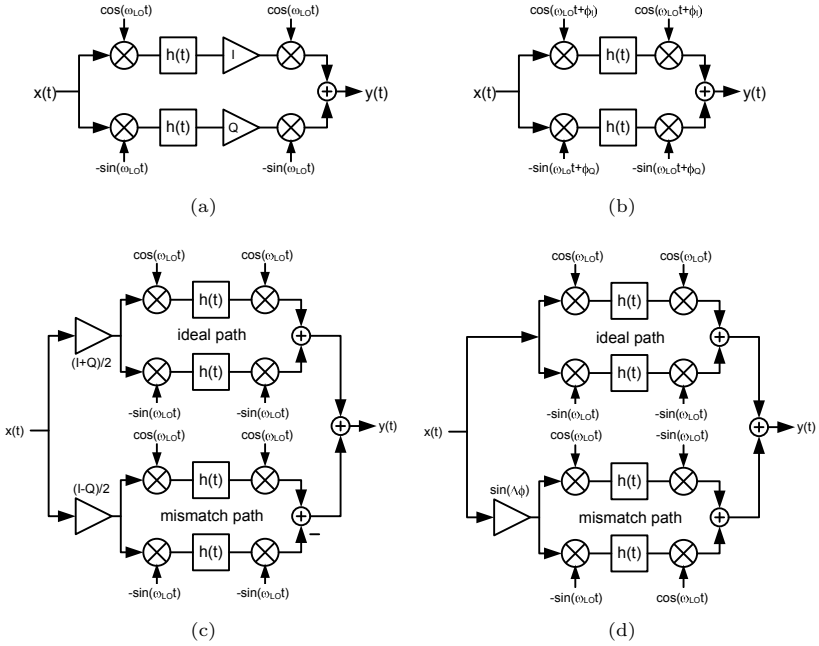


Figure 3.7.: System block diagram describing I/Q mismatch in active cancellation filter core gain mismatch in I- and Q-path (a), phase mismatch in I- and Q-path (b), gain mismatch split into ideal and mismatch path (c), phase mismatch split into ideal and mismatch path (d).

Image Spectrum due to I/Q Gain and Phase Mismatch

As seen in Fig. 3.7(c) and in Fig. 3.7(d) the filter core output signal consists of the ideal output signal contributed by the ideal path and a signal corrupting the ideal output due to I/Q mismatch. The effect of I/Q mismatch can be assessed by inspection of (3.22) and (3.24). A graphical representation is shown in Fig. 3.8. In the ideal case without I/Q mismatch the baseband filter response $H(j\omega)$ is shifted around the local oscillator frequency yielding the filter core transfer function $H_{\text{core}}(j\omega)$. In the case of I/Q gain or phase mismatch the input spectrum $X(j\omega)$ is shifted around twice the LO frequency yielding an image component in the band of interest at f_{LO} and at three times the LO frequency. The image spectrum is weighted by the amount of I/Q mismatch present. Thus, instead of generating a single-sideband blocker replica, a blocker image appears at the image frequency.

Influence of I/Q Mismatch in Feedback Cancellation

In feedback cancellation the blocker image appears at the output of the filter core and is fed into the subtraction node at the input as seen in Fig. 3.1. Thus the image signal appears like an additional blocker signal at the input of the cancellation loop and is suppressed in the same way as the original blocker signal. As seen in the simulated frequency response [59] in Fig. 3.9(a) an I/Q gain mismatch as high as 10 dB has marginal influence on the frequency response. Moreover, as seen in Fig. 3.9(b), blocker image rejection is better than 20 dB for typical values of gain (1 dB) and phase (1 degree) mismatch. A comparison to I/Q mismatch mechanisms in feedforward cancellation [59] reveals that the active feedback cancellation scheme is less susceptible to I/Q mismatch because the image blocker is reduced by the loop. In feedforward schemes the blocker image directly affects the output. Due to the immunity to I/Q mismatch it seems improbable that a blocker image can become large enough to desensitize the receive chain while the original blocker is suppressed by the loop.

3.4.4. Noise

As indicated in Fig. 3.10, two sources of noise from the active feedback cancellation loop can be identified: the downconversion mixers including baseband amplifiers and the upconversion mixer. If the IF bandwidth of the downconversion mixers is chosen appropriately inband noise from the feedback loop downconversion mixers is attenuated well by the succeeding highpass filters. Conversely, if the IF bandwidth is chosen too high the active filter core frequency response exhibits

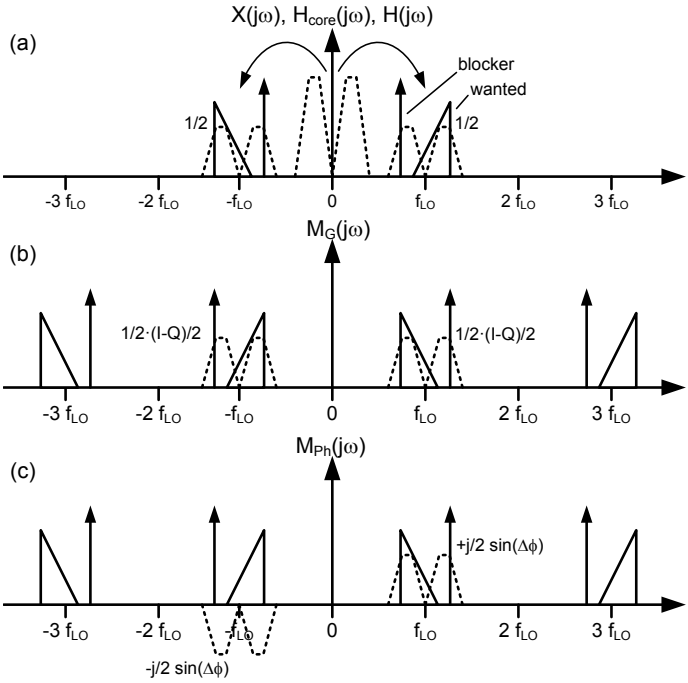
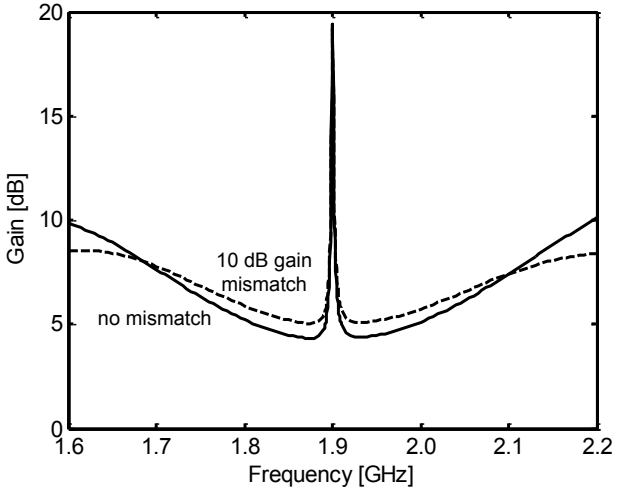


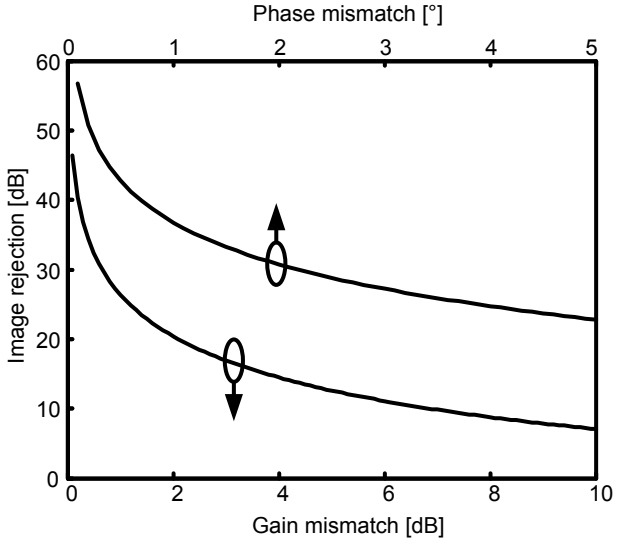
Figure 3.8.: Filter core output spectrum ideal (a), image due to I/Q gain mismatch (b), image due to I/Q phase mismatch (c).

only weak inband attenuation thus allowing inband noise from the downconversion mixer to propagate towards the LNA subtraction node.

As the upconversion mixer experiences no filtering it must be considered the main source of inband noise at the subtraction node. The dominating noise mechanisms at the upconversion mixer are thermal noise and local oscillator phase noise due to reciprocal mixing. The reciprocal mixing noise mechanism is illustrated in Fig. 3.10. The blocker replica extracted by highpass filtering in the baseband mixes with the LO phase noise tail thus resulting in a transfer of LO phase noise to the wanted frequency band. The input referred noise power



(a)



(b)

Figure 3.9.: Frequency response without mismatch and with 10 dB I/Q gain mismatch (a), image rejection vs. I/Q gain and phase mismatch (b).

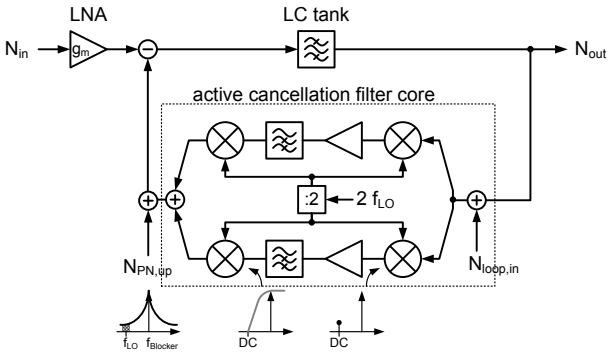


Figure 3.10.: Noise mechanisms in the filter core.

density due to the loop is expressed by

$$S_{n,loop} = S_{n,loop,th} + P_{B,in} \cdot \underbrace{\left(1 - 10^{-S(\Delta f)/10}\right) \cdot 10^{-\mathscr{L}(\Delta f)/10}}_{N_{PN,up}}, \quad (3.25)$$

where $S_{n,loop,th}$ denotes the input referred thermal noise power density contribution of the filter core, $P_{B,in}$ the input blocker power level, $S(\Delta f)$ the active feedback interference cancellation loop selectivity in dB at offset frequency Δf from the wanted signal, and $\mathscr{L}(\Delta f)$ the LO phase noise in dBc/Hz at offset frequency Δf. Especially at high input blocker levels and thus high blocker replica levels at the active filter core output local oscillator phase noise can dominate the inband noise in the wanted channel. The situation is further aggravated for blockers close to the wanted channel as the oscillator phase noise is large close to the carrier. The phase noise is shaped by the same transfer function as the input signal i.e. by the closed loop transfer function (3.1). Thus, upconverted close-in phase noise is transferred to the output while far-off upconverted phase noise is blocked by the loop.

Noise emanating from the loop input stage in front of the highpass filters as indicated in Fig. 3.10 is subject to a different noise transfer function

$$NTF_{Loop,in} = \frac{N_{out}}{N_{loop,in}} = \frac{G_{ol}(s)}{1 + G_{ol}(s)}, \quad (3.26)$$

as is easily found by inspection of the figure. At offset frequencies with high open loop gain the input referred noise of the loop appears unfiltered at the LNA output whereas noise at offset frequencies with low open loop gain is reduced.

Usually, the highpass corner frequency is designed to ensure a notch at the wanted frequency. Still, as pointed out before, notch depth depends on the filter IF bandwidth and in-channel noise can still propagate across the filter core. In particular, flicker noise can reach high levels close to the carrier so that it can significantly contribute to the in-channel noise despite the highpass filtering.

4. Feedback Interference Cancellation – Hardware Demonstrator

In this chapter, circuit design and measurement results of the first hardware demonstrator [60, 61] in 65 nm CMOS are described. First, circuit design is briefly summarized and subsequently exemplary measurement results are presented. In the first hardware demonstrator, focus is on a proof of concept and basic evaluation of the principles found by theoretical system analysis. The implemented front-end does not comprise a complete receiver but merely the RF part with LNA and interference cancellation blocks for simplicity. In addition, the interference cancellation loop has been combined with a quality factor enhanced LC tank [42, 62].

4.1. Circuit Design

The interference cancellation loop has been implemented as shown in Fig. 4.1. The LNA consists of an inductively degenerated common-source stage with LC tank load [42]. Cascode devices are used to form a low impedance node at the transconductor output to facilitate feedback signal summation in the current domain. An additional Q-enhancement circuit, which is focus of other work [62], is used to increase the LC tank quality factor. In contrast to a classic cross-coupled pair which is often used to cancel parasitic resistance, the implemented Q-enhancement reuses LNA current by a special arrangement of differential stages.

The LNA output signal is sensed at the LC tank and downconverted by a folded I/Q downconversion mixer [63]. A transconductance input stage first converts the LNA output voltage to a current which is equally divided to the inphase and quadrature paths by cascode devices. Subsequently, the signal is downconverted by commutating the RF signal current through double balanced switching quads. The input stage is a pseudodifferential stage for better linearity. The IF-bandwidth of the loop is set by the mixer output capacitors C_{IF}.

Baseband buffers are used to boost the feedback path gain and are designed for a linear gain of 30. They have been implemented as class-A cascoded current buffers with low input impedance [64]. The high-swing current mirror connection

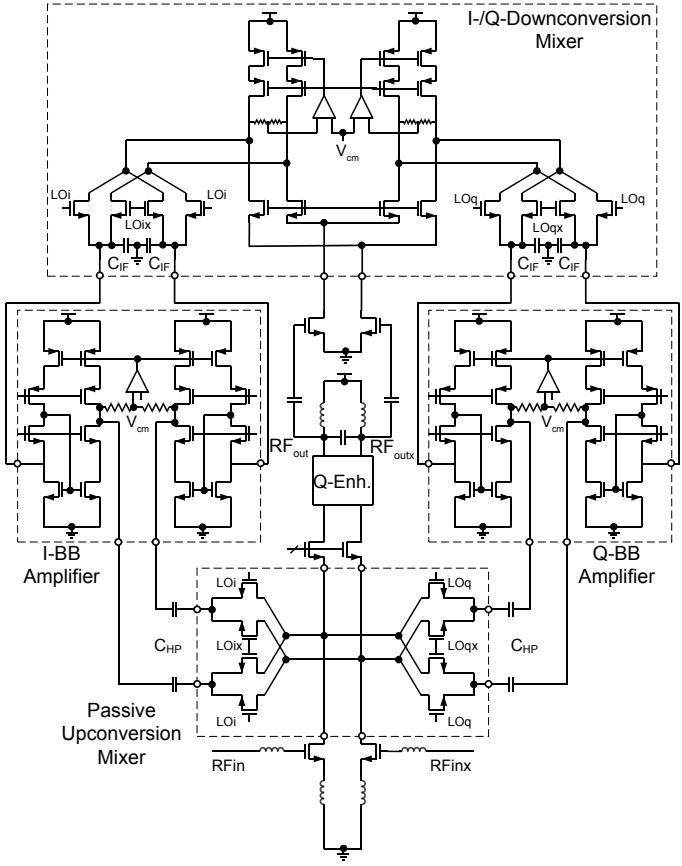


Figure 4.1.: Circuit implementation of active feedback cancellation.

around the input cascode device facilitates lowering the input impedance by shunt-shunt feedback. The input impedance seen into a simple cascode source node is approximately $1/g_{m,casc}$. Due to the feedback connection around the common-source and cascode devices, the impedance is further lowered by the loop gain of the local feedback loop. Thus an input impedance between 50 Ω and 100 Ω is achieved. The low input impedance avoids high voltage swings which is expected to improve linearity. The current consumption of each current buffer is 30 mA due to the class-A design and the required gain and linearity.

The common-mode levels at the downconversion mixer switching quad and at the baseband buffer outputs are controlled by local common-mode feedback loops to match with the DC reference levels at the switch gates. The common-mode level is set midrail at 1.25 V and can be tuned by a digital control word.

The highpass filters are formed by fixed AC coupling capacitors C_{HP} which are followed by an I/Q passive upconversion mixer. MOS capacitors are used to reduce area consumption. The highpass filters are designed for a corner frequency of 600 kHz.

The upconverted signal currents are DC coupled to the low impedance cascode summation node at the LNA transconductor output.

The quadrature LO signals are generated by a divide-by-two frequency divider circuit from a single clock signal at twice the LO frequency.

4.2. Measurement Results

A prototype has been fabricated in a 65-nm standard CMOS process (Fig. 4.2) covering an active area of $1.5 \times 0.8\,\mathrm{mm}^2$. The circuit including LNA, filter core, and frequency divider draws a current of 150 mA from a 2.5 V supply. The current consumption is mainly due to a class-A design of the baseband current buffers which has been chosen for simplicity and draws a nominal current of 60 mA. This could be significantly reduced by a class-AB design.

4.2.1. Transfer Functions

Fig. 4.3 shows the measured frequency response of the interference cancellation loop with and without a -15 dBm single tone blocker at 1880 MHz. When no blocker (Fig. 4.3(a)) is present the LNA has a gain of 24.7 dB. The gain at 1900 MHz drops by 2.2 dB when feedback interference cancellation is turned on by activating the LO. The frequency response results in a narrow, asymmetric peak around the LO frequency as shown in Fig. 4.3(a). Simulations reveal, that the asymmetry is due to different phase margins of the feedback loop below and above the LO frequency as pointed out in chapter 3.4.1. A low phase margin

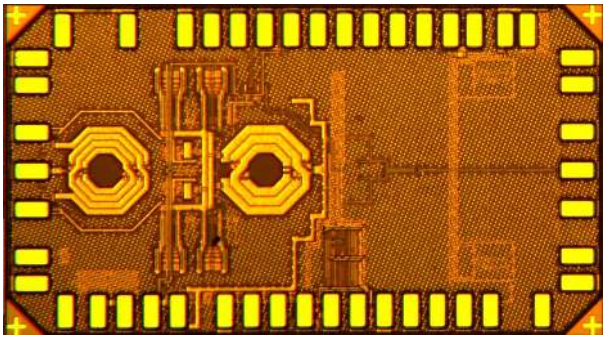


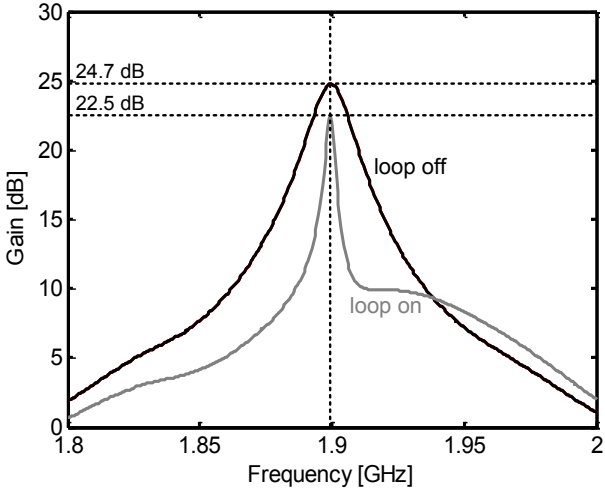
Figure 4.2.: Die micrograph comprising LNA input stage (left) and active cancellation filter core (right).

above the LO frequency results in gain peaking which is mitigated by the LC tank attenuation. A maximum additional selectivity of 10.5 dB at 5 MHz offset from the LO is attained with active interference cancellation compared to the case where the loop is deactivated. It is also interesting to note that the frequency responses for both cases converge at larger offset frequencies. This is a result of the limited loop bandwidth of approximately 200 MHz around the LO when regulation can no longer be maintained by the interference cancellation loop.

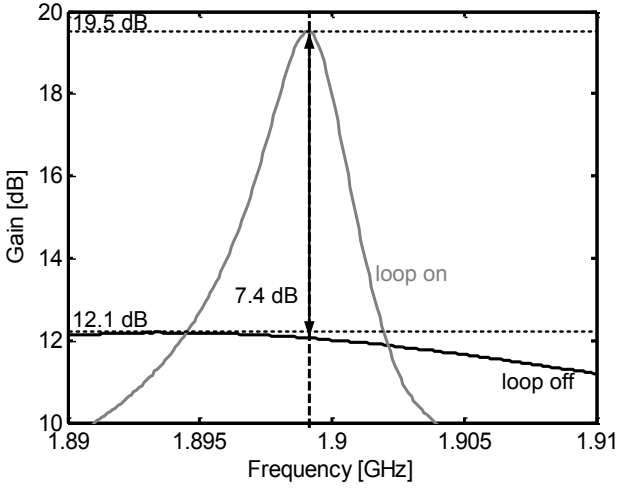
4.2.2. Blocking and Desensitization

When a -15 dBm single tone blocker signal at 1.88 GHz is activated, the gain without feedback cancellation degrades by 12.6 dB to 12.1 dB. When the LO is turned on, thus activating feedback cancellation, the gain drops by only 3 dB to 19.5 dB (Fig. 4.3(b)). A similar measurement has been carried out with a -15 dBm GSM modulated blocker at 1880 MHz. As seen in Fig. 4.5 gain is maintained in the same way as for an unmodulated blocker.

The overall noise figure is determined to be 7 dB and rises with blocker level, as shown in Fig. 4.4. For low blocker levels the interference cancellation loop degrades the overall noise figure by about 0.2 dB. In comparison to [60] the noise figure is improved by 1.8 dB by an optimized input matching network. In particular, an inductive series-shunt (Ls-Lp) matching network has been used in [60] while the optimized case comprises an inductive shunt-series (Lp-Ls) matching network. In comparison, the gain is improved by about 1 dB due to a higher passive input resonance gain of the shunt-series matching network. Thus, the inductive shunt-series matching network exhibits lower noise figure and benefits



(a)



(b)

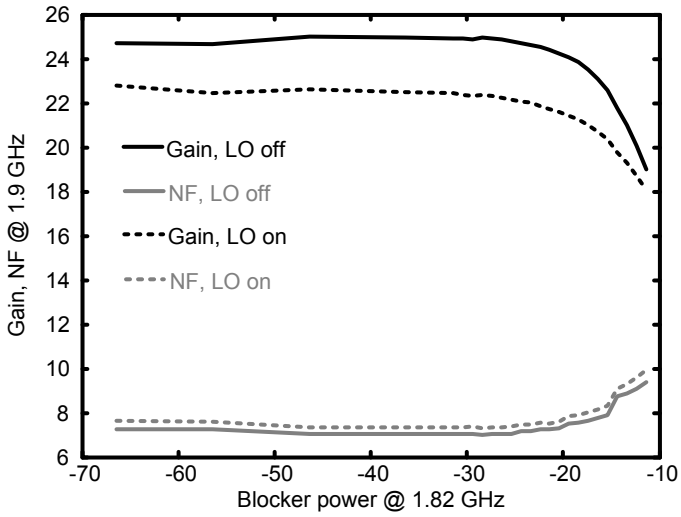
Figure 4.3.: Measured frequency response with and without cancellation without blocker (a), with -15 dBm cw blocker at 1.88 GHz (b).

from its higher shunt inductance [65].

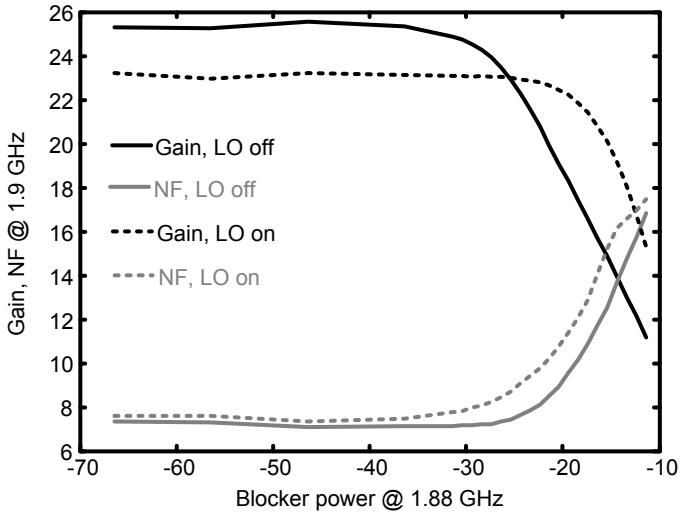
At high blocker levels the noise figure degrades faster with feedback interference cancellation activated although the gain is maintained. Further measurements reveal that both noise figure curves get closer when the DC level at the gates of the upconversion mixer switches is increased. This indicates that the excess noise at high blocker levels with interference cancellation activated is added by the upconversion mixer switches which do not switch fast enough due to a low DC reference level at the gates. Moreover, the increase in noise figure at high blocker levels indicates that the upconverter phase noise mechanism, as pointed out in chapter 3.4.4, plays an important role. In Fig. 4.4 the noise figure degradation due to a single tone blocker at offset frequencies of 20 MHz and 80 MHz is shown. Obviously, noise figure degradation is much more severe for the close-in blocker at 20 MHz offset than for the blocker at 80 MHz offset. Assuming that the noise at high blocker levels is dominated by reciprocal mixing of LO phase noise the phase noise level at the upconversion mixers can be estimated from (3.25) as -147 dBc/Hz at 20 MHz offset. As seen in Fig. 4.4(a) the noise figure with a blocker applied at 80 MHz offset does not rise faster when interference cancellation is turned on which results in a low estimated LO phase noise level. Therefore, the influence of LO phase noise can be neglected at large offset frequencies. On the other hand, the estimated phase noise at the upconversion mixer is increased by 10 dB at 20 MHz offset frequency in comparison to the phase noise of the Rohde & Schwarz SMJ100A Vector Signal Generator which has been used as the local oscillator in the measurement setup. Apparently, this is a worst case estimate as other nonlinear effects that might influence noise figure degradation at high blocker levels are not accounted for in the loop excess noise equation (3.25). Nonetheless, this indicates that an overall improvement of the desensitization performance especially at low offset frequencies can be obtained by optimizing the LO path for lower phase noise.

4.2.3. I/Q Mismatch

Fig. 4.5 shows the output spectrum when a -15 dBm GSM modulated blocker at 1.88 GHz is applied in combination with a small single tone input signal. Clearly, the blocker image is more than 16 dB below the original blocker. According to Fig. 3.9(b), this indicates an I/Q gain mismatch of about 2.5 dB and an I/Q phase mismatch smaller than 2 degree which is in the range of realistic values. Although a reduction of the blocker output power level in Fig. 4.5 by approximately 8 dB is expected with cancellation loop turned on it remains at approximately -15 dBm with loop on and off. This is due to compression of the output buffer used to drive the 50 Ohm measurement equipment. Nonetheless, the blocker level at the



(a)



(b)

Figure 4.4.: Gain and noise figure at 1.9 GHz vs. input blocker power for blocker frequencies of 1.82 GHz (a) and 1.88 GHz (b).

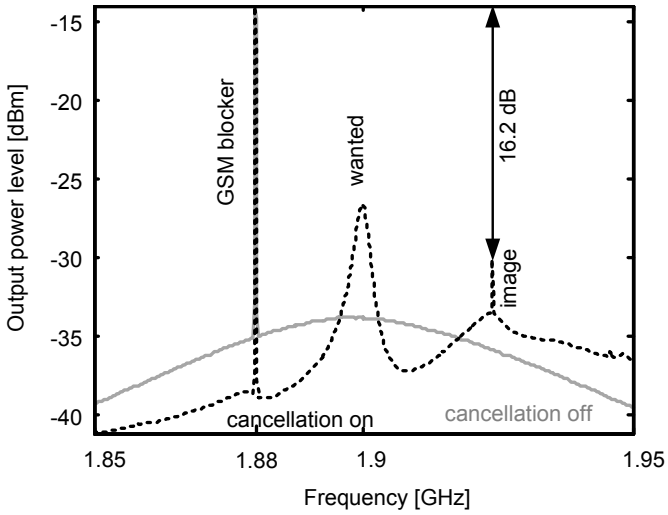


Figure 4.5.: Measured power level vs. frequency with -15 dBm GSM modulated blocker applied at −20 MHz offset frequency and -40 dBm wanted cw signal.

internal LNA output node at the LC tank load is effectively reduced by the loop which is indicated by the gain at the wanted frequency being maintained with loop turned on.

4.2.4. Conclusion

Basic functionality of the interference cancellation concept has been demonstrated. The measured transfer function shows a narrow, asymmetric peak as is expected from theory and simulations. Moreover, gain is maintained under blocking conditions when the interference cancellation loop is enabled.

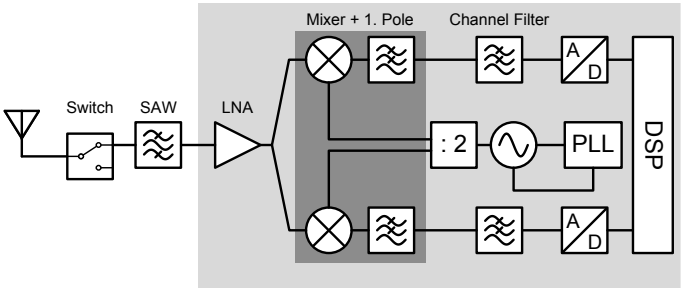
5. Receiver with Feedback Interference Cancellation – System Design

In this chapter, application of the presented interference cancellation approach in a receiver frontend is evaluated at system level. First, a receiver concept for the upper GSM bands (DCS and PCS) for a conventional receiver comprising a SAW filter in the frontend is established. Then trade-offs for a SAW-less frontend with interference cancellation are discussed [66].

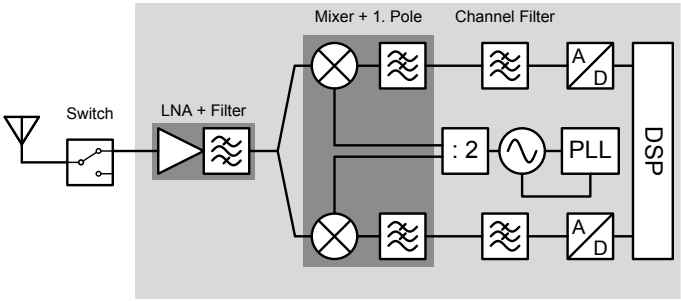
5.1. Receiver Concept

The receiver line-up for a conventional direct conversion receiver, which is preceded by a SAW-filter for band selection, is presented in Fig. 5.1(a). It comprehends an external antenna switch, which allows for selection of transmit or receive mode, a passive external SAW-filter, and the integrated receiver portion which is scope of this work. The integrated receiver consists of a low noise amplifier, a quadrature downconversion mixer comprising a first filter pole, and a channel select filter. The interface between the analog and digital signal processing domain consists of two analog-to-digital converters for the inphase and quadrature channels, respectively. The quadrature local oscillator signals are generated by an integrated phase-locked loop, as indicated in the figure. Although only the RF frontend is scope of this work, a holistic system view is required to derive specifications for the receiver blocks, as is pointed out subsequently. Fig. 5.1(b) shows the receiver line-up for a SAW-less implementation with on-chip blocker filtering after the LNA. In this work, the on-chip filtering is realized by an interference cancellation loop.

The basic considerations for GSM receiver design have already been laid out in chapter 2.4. For completeness, the main considerations are briefly summarized. As pointed out before, two approaches exist in the literature which depend on the baseband ADC resolution. If a low resolution ADC is used the receiver frontend must offer high gain to minimize the effect of ADC noise on the receiver noise figure. The associated issues, as pointed out in chapter 2.4, are sensitivity to DC offsets as well as I/Q mismatch, requirement for tight gain control, DC offset correction, and high order filters. If a higher resolution ADC is used, frontend gain can be reduced thus obviating the requirement for DC offset correction circuitry



(a)



(b)

Figure 5.1.: Receiver line-up for a DCR with SAW filter (a), a SAW-less DCR (b).

and reducing the gain control requirements. Moreover, analog baseband filter order preceding the ADC can be reduced. Why does an increased ADC dynamic range offer these system design benefits? First, as the ADC dynamic range is increased, its input referred noise voltage is reduced. Hence, gain of the receive chain can be reduced without affecting the receiver noise figure. As the gain is reduced the input referred offset voltage of the receive chain as well as adjacent channel interferers are amplified to a lesser extent. Moreover, ADC resolution can be traded for fullscale range i.e. the full scale range can be increased if the ADC resolution is increased without affecting the input referred noise. Therefore, DC offset as well as adjacent channel interferers can be accommodated by the

Offset frequency MHz	Blocker level dBm	Attenuation dB
3	-26 / -23	
20	-12	14
100	0	26

Table 5.1.: RF selectivity required to suppress out-of-band interferers to the inband blocker level in the GSM system.

ADC full scale range. Consequently, DC offset removal and adjacent channel filtering is implemented in the digital domain through digital signal processing.

Due to these advantages, high resolution ADCs are assumed in this work. Detailed system level implications for the receiver lineup are first explored for a direct conversion receiver comprising SAW filters as shown in Fig. 5.1(a) and then the results are extended to a SAW-less receiver with interference cancellation loop as depicted in Fig. 5.1(b).

5.1.1. Selectivity Requirements

Filtering is implemented in the RF and the baseband domains. The purpose of RF filtering is mainly to avoid overloading the mixer stage which usually presents the linearity bottleneck of the receiver. The RF filtering requirements are set by the out-of-band blocking profile as discussed in chapter 2.3.4. As a rule of thumb, the purpose of RF filtering is to reduce out-of-band blockers to roughly inband blocker level as the receiver must be linear enough to handle these power levels. In the case of GSM out-of-band blockers as high as 0 dBm must be reduced to -23 dBm or -26 dBm at 20 MHz to 80 MHz offset frequency depending on the band. In a conventional design this goal is achieved by external passive SAW filters while in a SAW-less design on-chip filtering techniques as introduced in chapter 2.5 can be used to fullfil this objective. If RF selectivity is limited such that this specification cannot be achieved, a trade-off between RF selectivity and inband compression / desensitization point of the receiver must be sought. In the GSM system the blocker at 3 MHz offset from the wanted channel is most critical as it cannot be reduced by RF filtering and can have relatively high power levels of up to -23 dBm. Therefore, the inband desensitization point is set by the 3 MHz blocker.

Channel selection, on the other hand, is achieved by the baseband filters. Therefore, baseband filtering requirements are set by close-in interferers such as inband blockers and adjacent channel interferers. If low resolution ADCs

are employed, baseband filters must ensure that the ADCs are not overloaded by close-in interferers. Consequently, these must be reduced significantly below the wanted signal, usually to co-channel interference level. This requires high order baseband filters, as mentioned in the GSM receiver survey in chapter 2.4. In this work, however, the approach is to provide high dynamic range in the ADCs and filter adjacent channel interferers in the digital domain. Therefore, it is sufficient to reduce adjacent channel interferers below the ADC fullscale range. Consequently, baseband filtering is designed to pass the three adjacent channel interferers at 200, 400, and 600 kHz offset specified in the GSM reference interference testcase as discussed in chapter 2.3.3.

5.1.2. ADC Requirements

The ADC requirements are closely related to the preceding filter stages. As the 600 kHz adjacent channel interferer must be resolved by the ADC, the ADC signal bandwidth f_{BW} is set to 600 kHz. The fullscale range is set by the level of the largest interferer and the expected output referred offset voltage of the receive chain. The resolution depends on the maximum allowable input referred noise voltage of the ADC which still achieves the overall receiver noise figure specification for a given fullscale range. Moreover, fullscale range can be traded for an increased ADC resolution.

Usually, higher order delta-sigma ADCs which use oversampling and noise shaping techniques to increase resolution are used [37, 38, 67, 68]. In order to estimate the required resolution for a given input referred noise voltage, as will be obtained from the level plan, SNR calculation for delta-sigma ADCs is briefly summarized [67, 68]. The SNR of an Lth order delta-sigma modulator with an N-bit quantizer can be expressed in terms of the oversampling ratio

$$OSR = \frac{f_s}{2f_{BW}}, \tag{5.1}$$

where f_s represents the sampling frequency and f_{BW} the signal bandwidth, the modulator order L, and the quantizer resolution N by

$$SNR = 10\log_{10}\frac{3}{2}\frac{2L+1}{\pi^{2L}}OSR^{2L+1}2^{2N}. \tag{5.2}$$

Usually, the ideal delta-sigma ADC resolution is impaired by non-ideal effects like nonlinearities, spurs, or sampling clock uncertainty. Therefore, an effective number of bits ($ENOB$) is specified, by representing the effective resolution of

the data converter by the signal-to-noise-and-distortion-ratio ($SNDR$)

$$ENOB = \frac{SNDR - 1.76}{6.02}. \tag{5.3}$$

In the level plan, the ADC noise must be input referred to the antenna. Therefore, an input referred noise voltage density representation is desired. This can be obtained from the ADC RMS fullscale range $V_{FS,rms}$, the $SNDR$, and the signal bandwidth by

$$v_{n,in} = \frac{V_{FS,rms}}{10^{SNDR/20} f_{BW}}. \tag{5.4}$$

Usually, the fullscale range V_{FS} is given as a peak-to-peak value, such that the RMS value can be calculated by

$$V_{FS,rms} = \frac{V_{FS}}{2\sqrt{2}}. \tag{5.5}$$

For the receiver at hand, the sampling clock is assumed to be directly derived from the system crystal oscillator which operates at $f_s = 26\,\text{MHz}$. The bandwidth f_{BW} is set by the 600 kHz adjacent channel interferer resulting in an ADC oversampling ratio $OSR \approx 22$. The ADC fullscale range must accomodate the largest adjacent channel interferer, which is determined in the level planning phase. Moreover, as no DC offset correction circuitry is implemented, it must be designed with enough margin for the output referred offset voltage of the receive chain. At an estimated gain between 40 dB and 50 dB along the receive chain and an estimated input referred offset voltage of 1 mV this amounts to an implementation margin of 100 – 300 mV.

5.1.3. GSM Requirements

The fundamental GSM specification has already been derived in chapter 2.3. Obviously, the specifications given in 2.3 are minimum specifications which must be fulfilled in order to confirm to the standard [27]. Usually, an implementation exceeds the specified performances and is subject to the designated boundary conditions or specific benefits in the marketplace. As an example, the noise figure often exceeds the minimum specification conforming to the standard by almost 10 dB thus achieving reference sensitivities of -110 dBm or better [6, 31]. This offers wider coverage of the handset and thus a direct benefit for the customer. Hence, an implementation can assess the importance of performance parameters differently, as long as the minimum specification is fulfilled.

In the work at hand, a highly linear SAW-less GSM receiver implementation is sought. Therefore, noise figure is traded for linearity and current consumption.

	Unit	Min	Typ	Max	Comment
f_{RX1}	MHz	1805		1880	DCS1800
f_{RX2}	MHz	1930		1990	PCS1900
NF	dB		6	12	Reference sensitivity, filter on
NF	dB		5	12	Reference sensitivity, filter off
$IIP3$	dBm	-19			Intermodulation
$IIP2$	dBm	47			AM suppression
$NF_{blocking}$	dB		12	15	Blocker mask

Table 5.2.: GSM receiver specification.

The typical noise figure is specified as 6 dB when on-chip filtering is enabled and 5 dB when the receiver is operated with external SAW filters. Note, that a typical state of the art implementation achieves noise figures around 3 dB and rises by the insertion loss of the SAW-filter, typically more than 2 dB, so that the overall system noise figure is in the same range as in the specified case. Under blocking conditions, as mentioned in chapter 2.3.4, the sensitivity is allowed to degrade to -99 dBm. Hence, the maximum noise figure under blocking conditions can be calculated according to (2.35)

$$NF_{blocking} = -99\,\text{dBm} - (-174\,\text{dBm/Hz} + \underbrace{53\,\text{dB}}_{200\,\text{kHz}} + 7\,\text{dB}) = 15\,\text{dB}. \tag{5.6}$$

In the conventional receiver line-up, the out-of-band blockers are suppressed by the SAW-filter and the specification must mainly hold for the inband blockers, among which the 3 MHz is the most critical. In a SAW-less receiver, the out-of-band blockers are filtered on-chip, so that this specification must hold for the whole blocker mask. The intermodulation testcases for second and third order intermodulation are not affected by blockers, as they are specified for inband interferers. Therefore, the conditions derived in chapter 2.3.5 and 2.3.6 hold for both receiver line-ups and must be met or exceeded in the implementation. Tab. 5.2 summarizes the core receiver specifications.

5.2. Level Plan

After the receiver specification has been established block level specifications must be derived and mapped to the system architecture from Fig. 5.1. This is achieved by a level plan which can be implemented using a spreadsheet software. In the level plan, block specifications such as gain, noise, $IIP2$, $IIP3$, selectivity, ADC resolution, ADC fullscale range, and local oscillator phase noise are listed.

The cascaded gain, noise, and intercept points are calculated using the techniques outlined in chapter 2.2 and block level specifications are adjusted to fulfill the receiver specification according to Tab. 5.2. Moreover, all critical signal levels such as adjacent channel interferers and blockers specified by the GSM standard are calculated from the given data and can be traced along the receive chain. Thus the effect of filters can be easily examined and the required filter order and pole locations can be determined.

The level planning phase is an iterative process as feasibility of a given block specification or parameter is not necessarily known. In these cases, possible circuit topologies for the block must be explored by circuit simulation and backannotated to the level plan.

5.2.1. Level Plan for Receiver with SAW-Filter

The basic level plan for a direct conversion receiver with SAW-filter is shown in Fig. 5.3. Feasibility of the block specifications for the receiver frontend has been verified using extensive circuit simulations. The specification for the ADC and the local oscillator phase noise have been obtained from a literature survey [66] while SAW-filter performance data is taken from datasheets [69, 70].

Receiver line-up In the level plan of Fig. 5.3 a set of block specifications is listed for the case of a receiver with SAW-filter. The overall noise figure is set by the LNA which is specified with a noise figure of 3.3 dB and a gain of more than 20 dB. The LNA specification has been obtained from measurements of a high dynamic range LNA which trades noise figure for linearity as discussed in chapter 6.1. The receive mixer is specified with a relatively high gain of 26 dB and a low input referred noise voltage of $3\,\mathrm{nV}/\sqrt{\mathrm{Hz}}$. This is required to scale down the relatively high input referred noise of the baseband biquad filter of $47.5\,\mathrm{nV}/\sqrt{\mathrm{Hz}}$. As will be pointed out in chapter 6.2.1, this relatively high input referred noise level results from a trade-off of input referred noise versus current consumption and capacitor area. The required ADC resolution is specified as 14 bit with a full scale range of 0.7 V which corresponds to a dynamic range of 84 dB. According to chapter 5.1.2 given a signal bandwidth of 600 kHz and a sampling clock of 26 MHz, this can be achieved by a third-order delta-sigma ADC with a 2-bit quantizer. For performance margin, a higher modulator order or quantizer resolution might be required. In [37], a fourth-order 3-bit delta-sigma ADC achieves 90 dB dynamic range while [38] obtains 74 dB dynamic range using a third-order modulator and a 5-level quantizer.

The resulting cascaded gain, noise figure, $IIP3$, and $IIP2$ values along the receive chain are listed in Fig. 5.3.

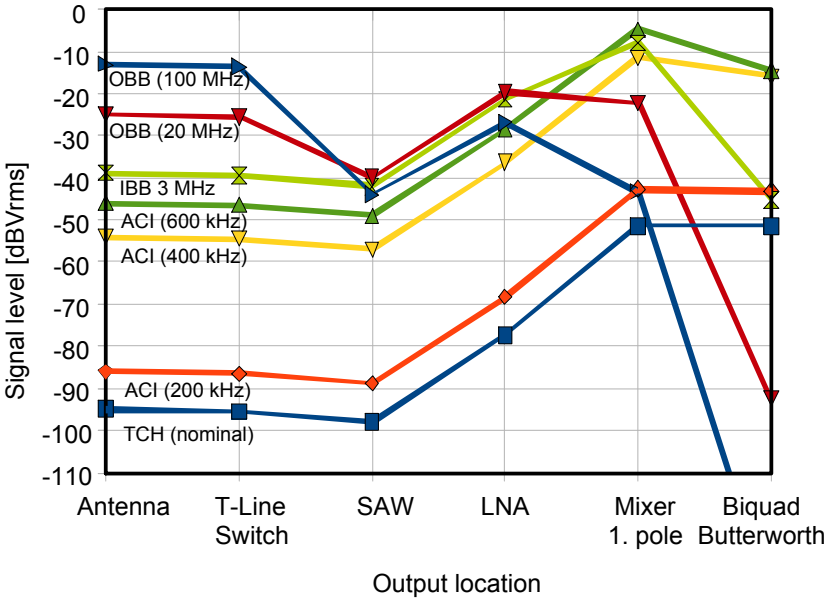


Figure 5.2.: Level diagram for all critical signals along the receive chain.

Filtering The out-of-band blockers are filtered by an external SAW-filter with a typical insertion loss of 2.4 dB. This directly adds to the noise figure resulting in an overall noise figure of 7.5 dB. Moreover, the LNA LC tank load provides some far-off selectivity. Channel filtering is designed to reduce the 600 kHz adjacent channel interferer below the specified ADC full scale range. A first pole at the mixer output provides some coarse selectivity and suppresses far-off blockers as well as LO-to-IF leakage whereas a biquad filter with Butterworth characteristic reduces close-in interferers to the desired levels. The first filter pole is set at 750 kHz while the biquad corner frequency is at 350 kHz. The filtering and the ADC full scale range are again subject to a trade-off: If the pole locations of the filter stages are too high, the ADC full scale range must be increased. This requires a higher ADC resolution in order to maintain the specifed input referred noise level. On the other hand, if the pole locations are low the filter might affect the wanted signal under process variations. Moreover, low corner frequencies require larger *RC* products in the filter implementation. Unfortunately, impedance levels cannot be chosen arbitrarily high due to noise

issues. Therefore, low corner frequencies require large capacitors and result in increased area and current consumption.

A level diagram with the most critical signals defined by the GSM standard is shown in Fig. 5.2. As seen in the figure, the 400 kHz and 600 kHz adjacent channel interferers constitute the largest signals at the ADC input with a maximum signal level of -14.4 dBVrms which corresponds to a 540 mV peak-to-peak voltage. Hence, the ADC can accomodate a maximum offset voltage of 160 mV in its 0.7 V full scale range.

Gain control The maximum input power level specified by the GSM standard is -15 dBm. If the wanted input signal level at the antenna is too high the receiver is easily overloaded. In this case, receiver gain must be backed off. In the design at hand this can be achieved by a 30 dB gain step in the LNA. Care must be taken, that the gain step does not effect the receiver sensitivity i. e. it must be carried out at a sufficiently high input power level. Moreover, as pointed out in [17], hysteresis must be used to avoid switching the gain back and forth as the input power level is around the threshold. In contrast to more sophisticated gain control mechanisms, this approach does not optimize SNR at the ADC input over the input dynamic, but merely avoids overloading the ADC. This approach is justified for the voice centric GSM standard, as no benefit is gained from any excess SNR. In a data centric standard, on the other hand, data rate and thus SNR must be maximized and more elaborate control mechanisms are required.

5.2.2. Level plan for SAW-less receiver

The level plan for the SAW-less receiver with interference cancellation shown in Fig. 5.6 is based on the line-up previously discussed. The performance of the receive chain, i.e. receive mixer, baseband filters, and ADCs is assumed not to be affected by the interference cancellation loop. LNA performance, however, is affected by the loop due to the effects lined out in chapter 3. First, high frequency leakage across the interference cancellation filter core due to finite roll-off of the IF bandwidth results in gain reduction, as pointed out before. In addition, gain at the wanted frequency band is reduced by the center frequency shift as described in chapter 3.4.2 and local oscillator leakage across the filter core upconversion mixer.

Therefore, a decreased LNA gain must be assumed in the level plan. Circuit simulations indicate a gain decrease of 4 to 6 dB at the center frequency depending on the settings of the loop filter core. Moreover, it is estimated from circuit simulations that the noise figure will rise by 1.5 dB due to noise contribution of the loop and the gain reduction.

RX /w SAW	DCS1800		Antenna	T-Line Switch	SAW	LNA				Mixer 1. pole		Biquad Butterworth		ADC
T		290												
BW		2,00E+05												
kT		4,00389E-21												
Rs		50												
Stage Parameters	**High gain mode**													
Gp (power gain)	dB			**-0,5**	**-2,4**								**VFS [V]**	**0,7**
		1		0,89	0,58								**SNDR**	**86**
Gv (voltage gain)	dB					**21,5**				**28**		**0**		**0**
		1				11,89				25,12		1		1
block input referred noise voltage	nV/sqrt(Hz)					0,42				**3,04**		**47,5**		27,74
F		1		1,12	1,74	1,86				12,55		2818,58	**ENOB**	13,99
NF	dB			0,5	2,4	**2,7**				10,98		34,50		
IIP2	dBm			**1000**	**1000**	1013								
	dBVrms					**1000**				**58**		**70**		**70**
	Vrms					1E+50				794,33		3162,28		3162,28
IIP3	dBm			**100**	**100**	**8**								
	dBVrms					-5,01				**-9**		**53**		**10**
	Vrms					0,56				0,35		446,68		3,16
Selectivity														
			Offs.et Frequency	*Type*	B9402 (DCS)	Total	*Loop*	*LC*	*Pole*	**7,50E+05**	*Pole*	**3,50E+05**		*Total*
Adjacent Channel Interference (200 kHz)	dB		2,00E+05		0	0				-0,3		-0,4		-0,7
Adjacent Channel Interference (400 kHz)	dB		4,00E+05		0	0				-1,1		-4,3		-5,4
Adjacent Channel Interference (600 kHz)	dB		6,00E+05		0	0				-2,1		-9,8		-12,0
IBB 600 kHz	dB		6,00E+05		0	0				-2,1		-9,8		-12,0
IBB 800 kHz	dB		8,00E+05		0	0				-3,3		-14,5		-17,8
IBB 1.6 MHz	dB		1,60E+06		0	0				-7,4		-26,4		-33,9
IBB 3 MHz	dB		3,00E+06		0	0				-12,3		-37,3		-49,6
GMSK blocker (6 MHz, AM suppr. TC)	dB		6,00E+06		0	0				-18,1		-49,4		-67,5
OOB 10 MHz	dB		1,00E+07		0	-0,1		-0,05		-22,5		-58,2		-80,9
OOB 20 MHz	dB		2,00E+07		-12	-0,2		-0,2		-28,5		-70,3		-111,2
OOB 80 MHz	dB		8,00E+07		-12	-2,6		-2,6		-40,6		-94,4		-152,1
OOB 100 MHz	dB		1,00E+08		-28	-3,4		-3,4		-42,5		-98,2		-175,5
OBB 1 GHz	dB		1,00E+09			-16,0		-16,0		-62,5		-138,2		-232,7
Phase Noise														
800 kHz	dBc/Hz					-133				-133				
1.6 MHz	dBc/Hz					-136				-136				
3 MHz	dBc/Hz					-139				-139				
10 MHz	dBc/Hz					-146				-146				
20 MHz	dBc/Hz					-149				-149				
80 MHz	dBc/Hz					-150				-150				
100 MHz	dBc/Hz					-155				-155				
Signals			dBm	dBVrms									CIR / dB	
Cascade Gain	dB			-0,5	-2,9	18,6				46,6		46,6		**46,6**
Cascade NF	dB			**6,63**	6,13	**3,73**				12,68		35,77		
Cascade IIP3	dBm			**-14,61**	-15,11	**-17,51**								
Cascade IIP2	dBm			**51,61**	51,11	**48,71**								
NF due to desensitization and reciprocal mixing		block gain and NF desensitization, reciprocal mixing at RX mixer, reciprocal mixing at loop upconversion mixer												

Key Performance Metrics	**DCS1800**	**Sensitivity / dBm**	**Spec**	**Margin/ dB**	**NF / dB**
SNRmin @ REFSENS	dB	8			
SNRmin @ interference	dB	7			
min. margin	dB	1			
1. Reference Sensitivity	dBm	**-106,34**	-102	4,34	6,63
2. Intermodulation	dBm	-106,04	-99	7,04	
3. AM Suppression	dBm	-105,59	-99	6,59	
4. Blocking / Desensitization					
4.1 Sensitivity (IBB 3 MHz)	dBm	-102,88	-99	3,88	11,09
4.2 Sensitivity (CW 10 MHz)	dBm	-105,84	-99	6,84	8,13
4.3 Sensitivity (CW 20 MHz)	dBm	-104,46	-99	5,46	9,50
4.4 Sensitivity (CW 80 MHz)	dBm	-107,10	-99	8,10	6,86
4.5 Sensitivity (CW 100 MHz)	dBm	-103,91	-99	4,91	10,06

Figure 5.3.: Levelplan for direct conversion receiver with SAW-filter in high-gain mode.

Selectivity requirements It is assumed that the baseband filter line-up of the main receiver path can remain unaffected of the implications made for RF front-end filtering. Hence, only RF filtering is considered subsequently. The maximum attainable selectivity using the feedback interference cancellation concept can be estimated using the system considerations from chapter 3. According to the closed-loop system transfer function (3.1) the maximum selectivity depends on the maximum open-loop gain of the control loop. Usually, the loop input stage, which sets the maximum open loop gain, is realized as a transconductance stage characterized by the effective transconductance $g_{m,fb}$ from (3.6). Hence, the maximum realizable transconductance for a given current consumption limits the open loop gain and thus selectivity. The maximum loop gain can be calculated by

$$G_{ol,max} = \frac{g_{m,fb,max}}{2a_{DWN}a_{BBF}a_{UP}} Z_{LC}, \tag{5.7}$$

where $g_{m,fb,max}$ represents the maximum realizable downconversion mixer input transconductance, Z_{LC} the LC tank impedance, and a_{DWN}, a_{UP}, a_{BBF} the attenuation due to the downconversion mixer quad, upconversion mixer quad, and the baseband filters, respectively. The insertion loss of a switching quad driven by a 50 % duty-cycle is $2/\pi$ and $\sqrt{2}/\pi$ if driven by a 25 % duty-cycle. The attenuation of the baseband filtering section at the maximum loop gain point depends on the exact locations of the lowpass and highpass filter corner frequencies. As the highpass corner frequency is usually one to two decades lower than the lowpass corner frequency to ensure a steep selectivity profile, filter attenuation at the maximum loop gain frequency is neglected. Furthermore, a center frequency of 1.9 GHz, an LC tank with an inductance of 5 nH, and a quality factor of 10 are assumed. Assuming a 25 % duty-cycle the required transconductance for a given maximum open loop gain can be calculated. Obviously, this rather crude model does not account for the loading effects and different impedance levels seen in a real circuit. Nonetheless, it facilitates a rough estimation of maximum achievable selectivity. In Fig. 5.4 the required transconductance for a given loop gain and selectivity is shown. It reveals that a very high transconductance of almost 200 mS would be required to reduce a 0 dBm out-of-band blocker by 23 dB to inband blocker level. Clearly, such high transconductance levels are hard to achieve in a single stage and require high quiescent currents. Therefore, front-end selectivity must be reduced to achieve reasonable transconductance and current consumption. From Fig. 5.4, assuming a maximum realizable transconductance of 75 mS, the maximum loop gain and hence selectivity is limited to 15 dB. This raises linearity requirements for the receive mixer.

Moreover, yet another effect must be considered. In chapter 3.4.4, noise due to reciprocal mixing of the blocker replica with LO phase noise at the loop

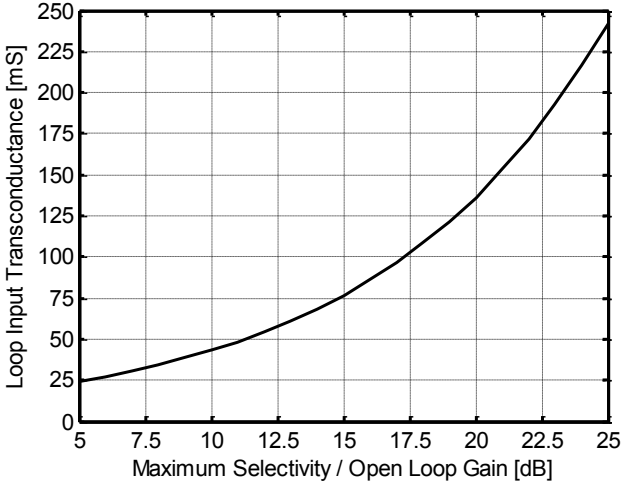


Figure 5.4.: Estimated loop input transconductance for given selectivity.

upconversion mixer is discussed. As the input blocker power is increased, the replica level at the upconversion mixer also rises to achieve the desired selectivity of the loop thus increasing the phase noise contribution in the wanted channel as described by (3.25). On the other hand, the receive mixer of the main receiver path sees a reduced blocker level due to the selectivity provided by the loop. Consequently, the phase noise contribution in the wanted channel due to reciprocal mixing is reduced by the preceding selectivity. Therefore, the total input referred phase noise at offset frequency Δf due to reciprocal mixing can be expressed by

$$P_{n,pn}(\Delta f) = P_{Blocker} 10^{-\mathscr{L}(\Delta f)/10} \left[\left(1 - \frac{1}{S}\right)^2 + \frac{1}{S^2} \right], \tag{5.8}$$

where the first term characterizes reciprocal mixing at the loop upconversion mixer from (3.25) whereas the second term describes reciprocal mixing at the receive mixer, and $\mathscr{L}(\Delta f)$ is the LO phase noise in dBc/Hz at offset frequency Δf. The phase noise scaling factor in brackets from (5.8) is plotted in Fig. 5.5. At low selectivity up to 5 dB total phase noise is scaled down by the selectivity preceding the receive mixer stage. As selectivity is increased, upconversion mixer phase noise starts to dominate until no improvement of phase noise due to the selectivity is seen. Nonetheless, a small improvement of roughly 2 – 3 dB can be

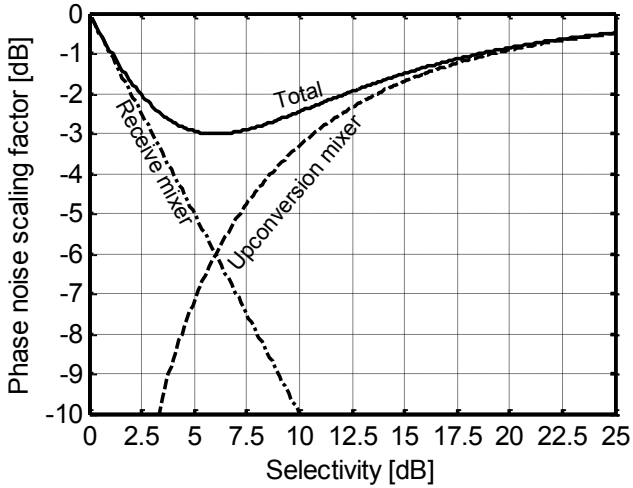


Figure 5.5.: Phase noise scaling factor vs. selectivity for SAW-less front-end.

noted at low to medium selectivities from 2.5 – 12.5 dB.

5.2.3. Comparison

Some differences between the conventional receiver with SAW-filter and the SAW-less receiver with interference cancellation must be considered in order to appreciate the specific advantages and disadvantages of a SAW-less implementation. As indicated in Fig. 5.1(a), the conventional receiver is preceded by a SAW filter which has a typical insertion loss of 1.3 dB to 2.3 dB [69, 70] and can have a worst case insertion loss of up to 3.2 dB. Obviously, this degrades sensitivity and raises the noise figure requirement of the receiver. Still, the SAW filter relaxes the linearity requirements of the front-end for out-of-band blockers. Moreover, the LO phase noise requirements for far-off phase noise are greatly relieved as large signal out-of-band blockers are lowered by the SAW-filter and consequently reciprocal mixing with LO phase noise in the receive mixer is reduced.

In the SAW-less implementation a gain reduction due to the interference cancellation must be accepted thus increasing the noise figure of the receiver. Moreover, the interference cancellation blocks contribute noise themselves as pointed out in chapter 3.4.4 thus raising the overall noise figure. Moreover, as discussed in the previous section, reciprocal mixing of LO phase noise is

more pronounced in the SAW-less implementation with interference cancellation thus increasing the requirements for the synthesizer. In particular, a maximum improvement of noise due to reciprocal mixing of 3 dB can be expected at moderate selectivity according to Fig. 5.5. Hence, the full burden for fulfilling the sensitivity specification under out-of-band blocking conditions is on the receiver synthesizer phase noise as specified in Tab. 2.3. In a receiver implementation with SAW-filter it can be relaxed by the selectivity of the filter. Still, in state-of-the-art GSM transceiver implementations receiver and transmitter can share the same synthesizer due to half-duplex operation. As the GSM transmitter specification mandates a phase noise level of -162 dBc/Hz or better at an offset of 20 MHz in order to avoid spurious emissions in the receive channels [20], synthesizers are usually capable of achieving the phase noise specification of Tab. 2.3. This mitigates the issue of phase noise in the interference cancellation scheme to some degree. Moreover, it has been pointed out that selectivity is limited by realizable transconductance hence possibly raising the linearity requirement of the main receive path.

The SAW-less implementation can have a possible sensitivity advantage over the conventional receiver with SAW-filter if the noise contribution due to the loop is lower than the insertion loss by the SAW-filter.

RX SAW-less	DCS1800		Antenna	T-Line Switch	(SAW)	LNA + Loop				Mixer 1. pole		Biquad Butterworth		ADC
T	290													
BW	2,00E+05													
kT	4,00389E-21													
Rs	50													
Stage Parameters	High gain mode													
Gp (power gain)	dB			**-0,5**	**0**								**VFS [V]**	**0,7**
	1			0,89	1								**SNDR**	**86**
Gv (voltage gain)	dB					**17,5**				**28**		**0**		**0**
	1					7,50				25,12		1		1
block input referred noise voltage	nV/sqrt(Hz)					0,58				**3,04**		**47,5**		27,74
F	1			1,12	1	2,69				12,55		2818,58	**ENOB**	13,99
NF	dB			0,5	0	**4,3**				10,98		34,50		
IIP2	dBm			**1000**	**1000**	1013								
	dBVrms					**1000**				**58**		**70**		**70**
	Vrms					1E+50				794,33		3162,28		3162,28
IIP3	dBm			**100**	**100**	**8**								
	dBVrms					-5,01				**-9**		**53**		**10**
	Vrms					0,56				0,35		446,68		3,16
Selectitvity														
		Offs.et Frequency		*Type*	w/o filter	Total	*Loop*	*LC*	*Pole*	**7,50E+05**	*Pole*	**3,50E+05**		*Total*
Adjacent Channel Interference (200 kHz)	dB	2,00E+05			0	0				-0,3		-0,4		-0,7
Adjacent Channel Interference (400 kHz)	dB	4,00E+05			0	0				-1,1		-4,3		-5,4
Adjacent Channel Interference (600 kHz)	dB	6,00E+05			0	0				-2,1		-9,8		-12,0
IBB 600 kHz	dB	6,00E+05			0	0				-2,1		-9,8		-12,0
IBB 800 kHz	dB	8,00E+05			0	0	0			-3,3		-14,5		-17,8
IBB 1.6 MHz	dB	1,60E+06			0	0	0			-7,4		-26,4		-33,9
IBB 3 MHz	dB	3,00E+06			0	-2	-2			-12,3		-37,3		-53,6
GMSK blocker (6 MHz, AM suppr. TC)	dB	6,00E+06			0	-3	-3			-18,1		-49,4		-73,5
OOB 10 MHz	dB	1,00E+07			0	-14,6	-14,55	-0,05		-22,5		-58,2		-110,0
OOB 20 MHz	dB	2,00E+07			0	-15,26	-15,06	-0,2		-28,5		-70,3		-129,3
OOB 80 MHz	dB	8,00E+07			0	-12,7	-10,1	-2,6		-40,6		-94,4		-160,3
OOB 100 MHz	dB	1,00E+08			0	-12,4	-9,0	-3,4		-42,5		-98,2		-165,6
OBB 1 GHz	dB	1,00E+09				-25,0	-9	-16		-62,5		-138,2		-250,7
Phase Noise														
800 kHz	dBc/Hz					-133				-133				
1.6 MHz	dBc/Hz					-136				-136				
3 MHz	dBc/Hz					-139				-139				
10 MHz	dBc/Hz					-146				-146				
20 MHz	dBc/Hz					-149				-149				
80 MHz	dBc/Hz					-150				-150				
100 MHz	dBc/Hz					-155				-155				
Signals		dBm dBVrms											CIR / dB	
Cascade Gain	dB			-0,5	-0,5	17				45		45		45
Cascade NF	dB			6,45	5,95	5,95				12,68		35,77		
Cascade IIP3	dBm			-13,03	-13,53	-13,53								
Cascade IIP2	dBm			59,21	58,71	58,71								
NF due to desensitization and reciprocal mixing		block gain and NF desensitization, reciprocal mixing at RX mixer, reciprocal mixing at loop upconversion mixer												
Key Performance Metrics	DCS1800	**Sensitivity / dBm**	**Spec**	**Margin/ dB**	**NF / dB**									
SNRmin @ REFSENS	dB	8												
SNRmin @ interference	dB	7												
min. margin	dB	1												
1. Reference Sensitivity	dBm	**-106,51**	-102	4,51	6,45									
2. Intermodulation	dBm	-106,36	-99	7,36										
3. AM Suppression	dBm	-106,37	-99	7,37										
4. Blocking / Desensitization														
4.1 Sensitivity (IBB 3 MHz)	dBm	-103,96	-99	4,96	10,01									
4.2 Sensitivity (CW 10 MHz)	dBm	-106,76	-99	7,76	7,20									
4.3 Sensitivity (CW 20 MHz)	dBm	-103,29	-99	4,29	10,68									
4.4 Sensitivity (CW 80 MHz)	dBm	-105,50	-99	6,50	8,46									
4.5 Sensitivity (CW 100 MHz)	dBm	-100,37	-99	1,37	13,59									

Figure 5.6.: Levelplan for SAW-less direct conversion receiver in high-gain mode.

6. Receiver with Feedback Interference Cancellation – Hardware Demonstrator

In this chapter, a GSM receiver with interference cancellation loop is implemented according to the specifications which have been derived in chapter 5. First, LNA topologies with high dynamic range, i.e. with high desensitization points and acceptable noise performance, are investigated. Different LNA desensitization effects are evaluated and explained. Then, two implementations of a suitable topology are presented and measurement results are discussed. Ultimately, an implementation of a complete GSM front-end is presented.

6.1. High Dynamic Range LNA

While filtering by the feedback interference cancellation loop relieves the burden on the receive mixer and all succeeding stages of the receiver the LNA is still subject to large interferers of up to 0 dBm as specified in the blocking profiles in Fig. 2.14. This means that blockers of up to 0 dBm must not desensitize the LNA beyond a certain point.

6.1.1. Topology Selection

In order to determine a suitable circuit topology which can fulfill the imposed requirements a comparison of the most auspicious topologies is conducted. Inductorless LNA topologies [71, 72] are not further considered at this point because their linearity performance is too low for the intended application. Most promising candidates are topologies using inductors to maximize signal swing. Therefore, a comparison of inductively degenerated common source LNA [73], common gate LNA [74], and capacitor cross-coupled common gate LNA [75] is given.

Inductively degenerated common-source LNA The inductively degenerated common-source LNA [73] shown in Fig. 6.1 can attain very low noise figures of 1 dB and better. Input matching is realized by a reactive matching network consisting of a source degeneration inductor L_S , the gate-source capacitance C_{gs} of the transistor, and a gate inductor L_g. Due to series feedback of the

source inductor the equivalent input impedance shown in Fig. 6.1 is accomplished. The real part is used to match the LNA input to the antenna impedance R_S while L_g and L_s are designed to resonate the gate-source capacitance at the center frequency. As the input impedance constitutes an LC series resonator the gate-source voltage peaks at the resonance frequency resulting in a gate-source voltage Q times larger than the input voltage. Thus a "passive gain" is attained before the LNA resulting in a low overall noise figure. In [73] it is pointed out that a high quality factor Q results in amplification of induced gate noise and thus an optimum Q exists which minimizes noise figure. The optimum Q can be calculated from technology parameters and ranges from 3 to 5 [73]. The excellent noise performance is compromised by poor linearity if a high quality factor is chosen.

As an example, a common scenario is a differential LNA with 100 Ω differential input impedance matched to the 50 Ω antenna impedance by a balun with a winding ratio of $1 : \sqrt{2}$. For a 0 dBm blocker the 50 Ω port of the balun exhibits a peak-to-peak voltage swing of 0.63 V. Hence, the differential output peak-to-peak voltage swing of the balun is 0.89 V and each input of the differential LNA exhibits a swing of 0.45 V. Now, the swing between the gate and source terminals is enhanced by the quality factor of the matching network. For the values given above this results in a gate-source voltage swing between 1.3 V and 2.2 V.

Obviously, linearity is severely degraded at such high input signal swings across the transistor. Hence, signal swing must be limited. Two strategies exist to accomplish this goal. First, voltage gain prior to the LNA should be avoided, and second, input matching quality factor must be decreased. Clearly, both approaches raise the noise figure. A good compromise is to limit the quality factor to values around 2 and to match the input impedance to 50 Ω differential.

Common-gate LNA The input impedance of the common-gate LNA [74] as shown in Fig. 6.2 is set by the transconductance of the common-gate transistor while parasitic capacitances at the input are tuned out by a parallel shunt inductor. Hence, the equivalent input impedance constitutes an LC parallel resonator and the gate-source voltage exhibits no peaking at resonance as indicated in Fig. 6.2. This is favorable for input linearity. The voltage swing for a 0 dBm input signal at a 50 Ω match is only 0.63 V and a factor 2 to 4 smaller than in the previous example. Moreover, due to the $\frac{1}{g_m}$ termination a broadband match is possible. The lowered gate-source voltage peaking is compromised by a higher noise figure

$$F = 1 + \frac{\gamma}{\alpha} \cdot \frac{1}{g_m R_S}, \tag{6.1}$$

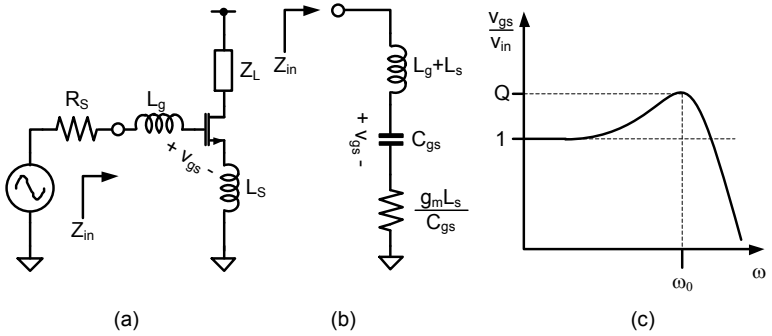


Figure 6.1.: Common source LNA with inductive degeneration (a), equivalent input impedance (b), gate-source voltage resonance (c).

where $\gamma/\alpha = 2/3$ for long-channel devices [19]. Hence, the minimum achievable noise figure of the common-gate LNA is 2.2 dB for long-channel devices while the noise figure is usually raised to 3 dB or more [74] by short-channel effects.

g_m-boosted common-gate LNA The performance of common-gate LNAs can be improved by g_m-boosting [75–77]. The basic idea is to increase the gate-source voltage swing of the common-gate device and thus increase its effective transconductance. As the channel noise is solely determined by the intrinsic device transconductance its overall noise contribution is lowered by the g_m-boosting [75]. An example of a g_m-boosted common-gate LNA is shown in Fig. 6.3. Due to the inverting gain $-A$ between source and gate terminal of the device the gate-source voltage is raised by $A+1$ resulting in an effective transconductance of $g_m(A+1)$ in comparison to g_m for a simple common-gate LNA. In this case the input resistance is

$$R_{in} = \frac{1}{g_m(A+1)}, \tag{6.2}$$

and the noise factor becomes

$$F = 1 + \frac{\gamma}{\alpha} \cdot \frac{1}{A+1} \cdot \frac{1}{g_m(A+1)R_S}. \tag{6.3}$$

If the LNA is power-matched to the source impedance the noise factor is

$$F = 1 + \frac{\gamma}{\alpha}\frac{1}{A+1}. \tag{6.4}$$

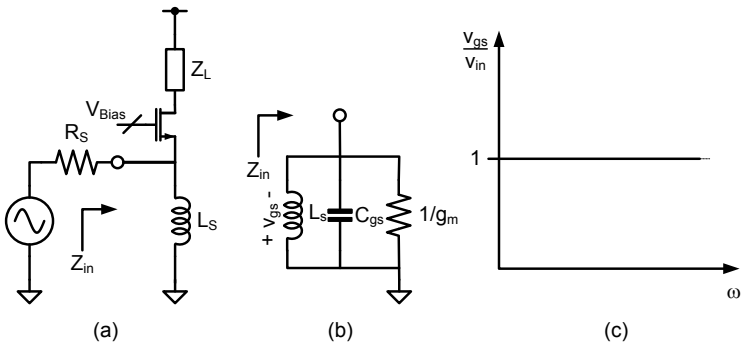


Figure 6.2.: Common gate LNA (a), equivalent input impedance (b), gate-source voltage (c).

Thus the second term of the noise factor is reduced by the gate-source voltage boost factor. For low noise operation, a reactive implementation of the inverting gain is desirable which does not contribute to noise itself. In [75] capacitive cross-coupling of two common-gate amplifiers is used to realize the inverting gain, while transformer-coupling is proposed in [77]. An implementation of the capacitor cross-coupled common-gate LNA is shown in Fig. 6.9. As seen in the figure, the gate-source voltage of the input transistors is obtained from the capacitive voltage divider formed by C_{gs} and the cross-coupling capacitor $C_{c,in}$. If $C_{c,in}$ is significantly larger than C_{gs} the whole differential input voltage drops across the gate and source terminals while the simple differential common-gate LNA exhibits only half the input voltage drop. Consequently, the g_m-boost factor $A+1$ is approximately two and the noise factor of the capacitor cross-coupled common-gate LNA from Fig. 6.9 yields

$$F = 1 + \frac{\gamma}{2\alpha}. \tag{6.5}$$

g_m-boosted cascode stage The g_m-boosting technique presented for the common gate LNA can also be applied to cascode stages as depicted in Fig. 6.4. Thus, the effective transconductance of the cascode transistor is increased and the cascode input impedance is lowered. In detail, a small signal analysis of

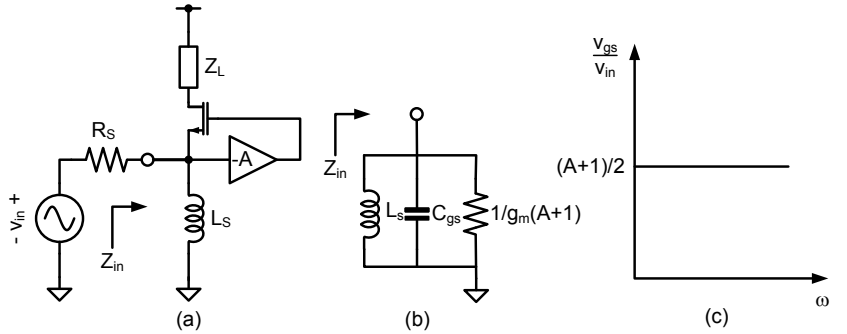


Figure 6.3.: g_m-boosted common-gate LNA (a), equivalent input impedance (b), gate-source voltage (c).

Fig. 6.4b yields the cascode input impedance

$$Z_{in,casc,boost} = \frac{r_{ds} + Z_L}{1 + g_m r_{ds}(A+1)}. \tag{6.6}$$

In comparison to a regular cascode common-gate stage which has the input impedance

$$Z_{in,casc} = \frac{r_{ds} + Z_L}{1 + g_m r_{ds}}, \tag{6.7}$$

the transconductance is boosted by the negative gain $-A$ thus resulting in lowered input impedance for the same biasing conditions. The lowered cascode input impedance results in a lower voltage swing at the cascode source node. This is advantageous for the linearity of input transistor M1 as its drain voltage swing is reduced. Conversely, the gate-source voltage swing of the cascode transistor is increased by $A+1$ due to g_m-boosting as pointed out before. Obviously, this can lead to inferior linearity performance of the cascode transistor M2 and concessions between input and cascode device linearity have to be made.

Desensitization Mechanisms

So far, it has been implied that LNA desensitization is mainly affected by nonlinearity of the input devices. In order to mitigate the linearity problem, it has been proposed to limit voltage peaking at the input devices and to avoid "passive" voltage gain in the unbalance to balance conversion network preceding the differential LNA. During the circuit design process it turned out that additional

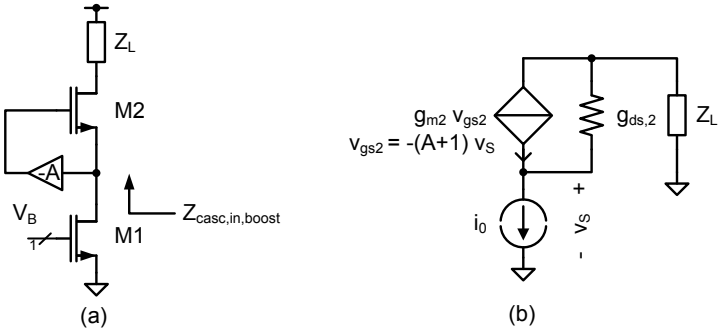


Figure 6.4.: g_m-boosted cascode stage (a), small signal equivalent circuit (b).

phenomena must be considered when the LNA is exposed to high blocker power levels. First, all LNAs presented in the preceding section are usually realized with a cascode stage for improved reverse isolation. The cascode stage affects overall LNA linearity and must be accounted for. Second, upconversion of low-frequency noise due to blockers raises the noise figure and is briefly summarized.

Influence of cascode stage on linearity At high input blocker levels linearity of the input devices is influenced by the cascode. For a deeper understanding it is helpful to consider the drain-source and gate-source voltages at the input transistor as depicted in Fig. 6.5. As the blocker level rises the gate-source voltage v_{gs} rises as well leading to an increased drain current. The drain current drives the source terminal of the cascode thus establishing the drain voltage of the input device. The drain-source voltage v_{ds} determines the operating region of the input device: if v_{ds} is lower than the saturation voltage $v_{ds,sat}$, the transistor operates in the triode region, otherwise it operates in the saturation region. In the triode region, transconductance drops while transistor output conductance rises thus leading to gain compression of the device.

Now, two things must be noted. First, $v_{ds,sat}$ rises with the gate voltage until the device is velocity-saturated. Second, the drain-source voltage is in antiphase with the gate-source voltage. This implies that, as the gate-source voltage rises, the minimum drain-source voltage required to keep the input device in saturation also rises. At the the same time, the drain voltage decreases as it is in antiphase with v_{gs}. As a result, v_{ds} is minimum as v_{gs} is maximum. Consequently, the input device can easily enter the triode region at this point. Furthermore, as the current through the cascode increases its gate-source voltage rises thus lowering

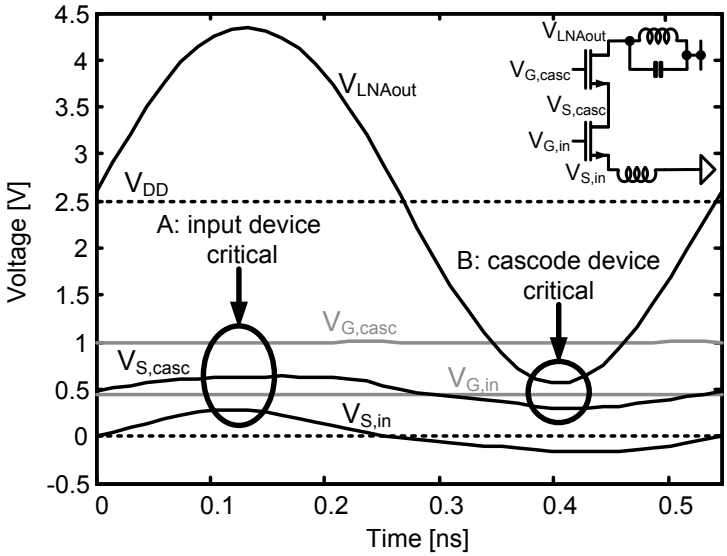


Figure 6.5.: Transient voltages in common-gate LNA for a 0 dBm input signal at 1.83 GHz.

the voltage at the input device drain node.

For the design, these observations have several implications. First, the cascode quiescent point must be chosen such that the voltage at its source node and thus v_{ds} of the input device is high enough to stay in the saturation region. This involves a trade-off between the cascode's and the input device's drain-source voltages. If the cascode gate is biased close to the supply the input device stays in the saturation region even for relatively high blocker levels as its drain voltage is maximized. Unfortunately, the cascode device can easily enter the triode region in this case as it exhibits relatively low voltage swing at its low impedance source node and high voltage swing at its high impedance drain node.

Thus its drain-source voltage can easily drop below the saturation voltage as the output swings low. Second, the impedance at the cascode source node should be kept low such that voltage swing around the quiescent point is minimized. Both approaches prevent the input transistor from entering the triode region.

The cascode input impedance can be lowered by increasing the cascode tran-

sistor transconductance as discussed before and indicated by (6.7). Transconductance is maximized by maximizing the gate-source voltage and by increasing its width. Obviously, the first strategy is limited by the bias trade-off discussed above, while the latter is limited by the maximum permissible parasitic capacitance. To further decrease the cascode input impedance g_m-boosting can be applied as previously discussed. In the same context is has been pointed out, that the cascode gate-source voltage is raised by g_m-boosting thus leading to reduced linearity of the cascode stage. The ramifications of cascode nonlinearity are discussed in the following.

Center frequency shift in cascoded LNAs A shift of the LNA LC load center frequency towards lower frequencies is observed at high blocker power levels as simulated for a common gate LNA in Fig. 6.6. This phenomenon can be understood by examining the influence of the parasitic source capacitance C_{par} on the cascode output impedance shown in Fig. 6.7. A small signal analysis of the circuit shown in Fig. 6.7a yields the equivalent output impedance

$$Z_{casc,out} = \frac{g_{m,2}}{g_{ds,2}} \cdot \frac{1}{g_{ds,1} + j\omega C_{par}} + \frac{1}{g_{ds,1} + j\omega C_{par}} + \frac{1}{g_{ds,2}} \tag{6.8}$$

which is depicted in Fig. 6.7b. The typical parasitic capacitance at the cascode source node is 100 fF to several hundred fF. At frequencies of roughly 2 GHz the corresponding admittance is on the order of several mS. Under regular operating conditions this is considerably higher than the drain-source output conductance $g_{ds,1}$. Consequently, the cascode output impedance $Z_{casc,out}$ is dominated by the parasitic capacitance at these frequencies and (6.8) reduces to

$$Z_{casc,out} \approx \frac{1}{j\omega C_{casc,out}} = \left(\frac{g_{m,2}}{g_{ds,2}} + 1\right) \cdot \frac{1}{j\omega C_{par}}. \tag{6.9}$$

Hence, the parasitic capacitance seen at the cascode output node is

$$C_{casc,out} = \frac{C_{par}}{1 + \frac{g_{m,2}}{g_{ds,2}}}. \tag{6.10}$$

Equations (6.8), (6.9), and (6.10) also hold for a g_m-boosted cascode if the intrinsic device transconductance $g_{m,2}$ is substituted by the effective transconductance $g_{m,2}(A+1)$. As indicated by (6.10) the parasitic capacitance seen at the cascode node is reduced by the intrinsic voltage gain of the cascode device, which is typically on the order of ten to fifty, as long as it is operated in the saturation region. As the input blocker power increases, the current generated by transistor M1 rises and voltage swing around the cascode transistor M2 rises. Consequently,

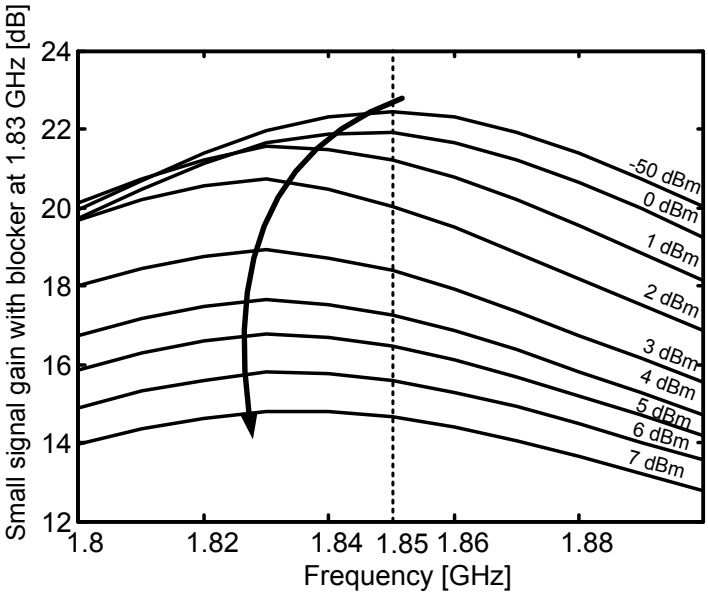


Figure 6.6.: Simulated small signal gain of common-gate LNA with blocker applied at 1.83 GHz.

the cascode device does not remain in the saturation region for the complete signal period and its effective transcondutance g_m is decreased while its output conductance g_{ds} is increased. This results in reduced intrinsic voltage gain of M2 and larger parasitic capacitance seen at the cascode output node according to (6.10). With increasing blocker power the cascode transistor becomes increasingly more transparent to its parasitic source capacitance and the load capacitance at the LNA LC tank load rises resulting in the observed frequency shift.

Low-frequency noise upconversion In the previous paragraphs desensitization is discussed as a consequence of gain compression due to blockers. In chapter 2.2.2 low-frequency noise upconversion is indentified as another critical desensitization mechanism in presence of substantial blocker power. In particular, the blocker modulates the input device's operating point resulting in upconversion of low-frequency noise emanating from the transistor itself and its associated biasing circuitry to the blocker frequency. The upconverted noise spreads into the wanted

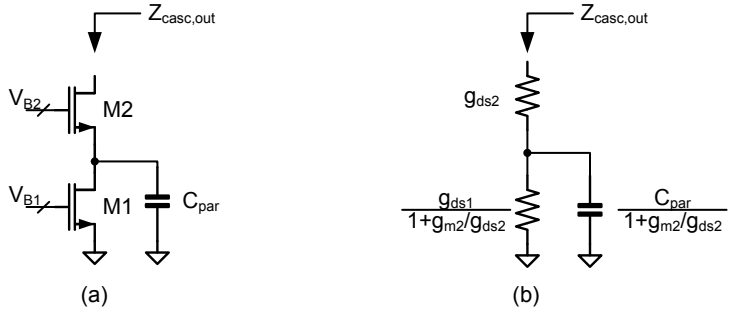


Figure 6.7.: Cascode with parasitic capacitor at the source node (a), small signal equivalent output impedance (b).

frequency band and increases the noise figure. Here, flicker noise of the LNA input devices can be particularly detrimental as it reaches high levels close to the blocker. The flicker noise current is proportional to the transistor bias current I_D as given by [67]

$$i^2_{nd,flicker} = \frac{K_F I_D}{f c_{ox} L^2} \Delta f. \tag{6.11}$$

Hence, increasing the bias current can result in excessive upconversion of flicker noise when a substantial blocker is present. In addition, flicker noise cannot be filtered as it is intrinsic to the device. Conversely, noise contributed by the input device's bias circuitry can be low-pass filtered as shown in Fig. 6.8. If the low-pass corner frequency is sufficiently low flicker noise contribution of the biasing circuitry is reduced.

Performance Comparison

The described LNA topologies have been simulated to compare noise and linearity performance. In order to allow for a fair comparison, all LNAs have been designed for roughly equal current consumption and gain. Moreover, all LNAs are fully differential and comprise a regular cascode stage without g_m-boosting. The common-source and capacitor cross-coupled common-gate LNAs have been adjusted for a differential input impedance of 50 Ω. Due to the capacitive cross-coupling and an input quality factor of two in the common-source amplifier, respectively, the gate-source voltage peaks at twice the single-ended input voltage of each LNA branch.

In Tab. 6.1 small signal gain, noise, $IIP3$, and large signal desensitization

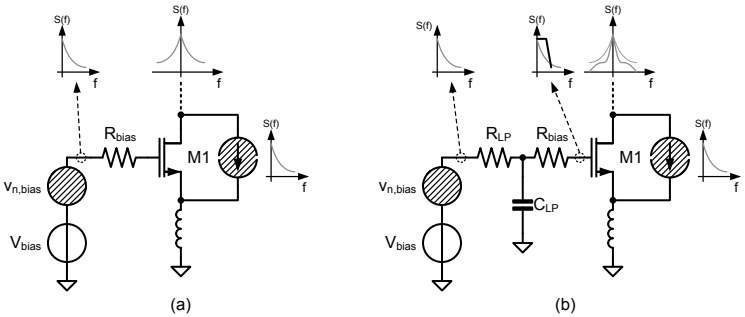


Figure 6.8.: Bias noise upconversion without filtering (a), with filtering (b).

			CS	CG	CCC
NF		dB	2.2	2.9	2.3
Gain		dB	22.3	22.8	22.3
IIP3		dBm	9.5	9.5	13.1
Effective input quality factor [1]			2	2	2
Differential input impedance		Ω	50	100	50
Current consumption		mA	3.4	3.5	3.5
1-dB gain desensitization	20 MHz	dBm	1.4	-0.8	0.8
	80 MHz		3.2	3.4	3.9
	100 MHz		4.1	4.5	5.0
NF with 0 dBm blocker at	20 MHz	dB	6.1	6.3	6.6
	80 MHz		3.3	4.1	3.4
	100 MHz		3.1	3.9	3.2

Table 6.1.: Simulation results for differential LNA topologies (CG – common gate, CS – common source, CCC – capacitor cross-coupled common gate).
[1] Ratio of v_{gs} drop to single ended device input voltage.

simulation results are listed. For the described boundary conditions, the common-source LNA and the capacitor cross-coupled common gate LNA exhibit approximately equal performance. The capacitor cross-coupled common-gate LNA has a slightly better $IIP3$. The pure common-gate LNA noise figure is 0.6 dB higher making it the inferior topology.

6.1.2. Capacitor Cross-Coupled Common Gate LNA

In the previous section, the common-source LNA and capacitor cross-coupled common-gate LNA have been identified as suitable choices for a high dynamic range LNA due to their moderate noise figure and high input desensitization points. In this section, circuit design and measurement results of the capacitor cross-coupled common gate LNA are presented. The topology is chosen, because it allows operation with differential inputs and external balun as well as integration of an on-chip input transformer for single-ended operation with minimum pin count. This is highly desirable in a highly integrated front-end for a multimode, multiband transceiver.

Circuit Design

As discussed in the previous section, capacitive cross-coupling of the input devices is used to achieve a target noise figure of 3 dB. Cascode devices are used to facilitate a low impedance node for current summation of the blocker replica in the intended interference cancellation scheme as indicated in Fig. 6.23. Capacitive cross-coupling is also used to boost the transconductance of the cascode devices and thus lower impedance at the summation node. In order to achieve high linearity load resistors or current sources cannot be used thus requiring source and load inductors. Moreover, the LNA is designed for a differential input impedance of 50 Ω. The impedance transformation from 50 Ω single-ended to 50 Ω differential is achieved by a lumped element off-chip balun consisting of only two inductors and two capacitors. A switched capacitor bank can be used to tune the input matching center frequency. The LNA center frequency can be tuned by a bank of switched capacitors in parallel to the LNA load inductor. To facilitate measurements, a 50 Ω source-follower output driver (not shown in Fig. 6.9) has been used.

Measurement Results

A test chip (Fig. 6.10) has been fabricated in a 90 nm CMOS technology with an area of 0.4 x 1.35 mm^2 including the output buffer. For all subsequent measurements, the off-chip lumped element input balun has been centered at 1.85 GHz with $L_B = 4.3$ nH and $C_B = 1.2$ pF. The LNA load and source inductors are 5 nH and 10.3 nH, respectively. The LNA operates from a 2.5 V supply at a DC current consumption of 4 mA including bias circuits. The measurement output buffer operates from 3.3 V at a DC current consumption of up to 40 mA to ensure that linearity is not limited by the output buffer.

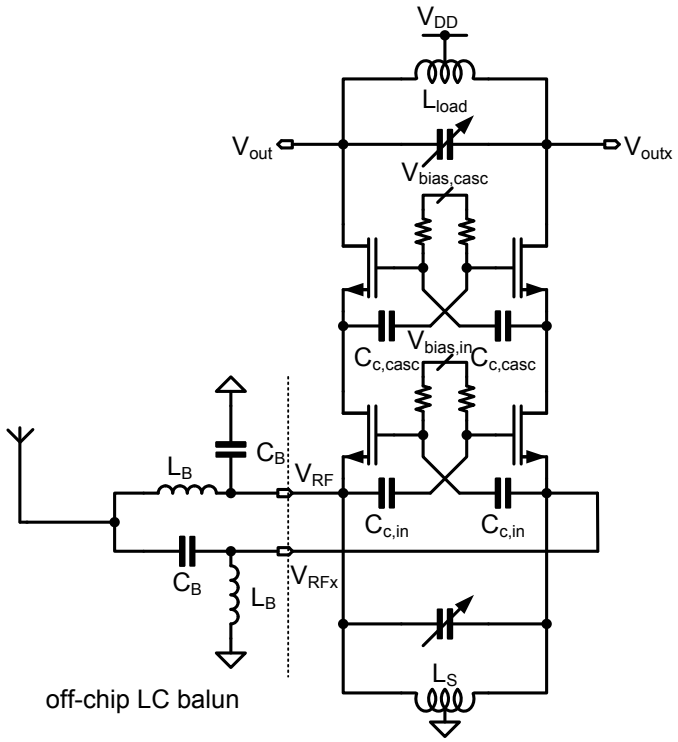


Figure 6.9.: Cross-coupled common-gate LNA with external LC balun.

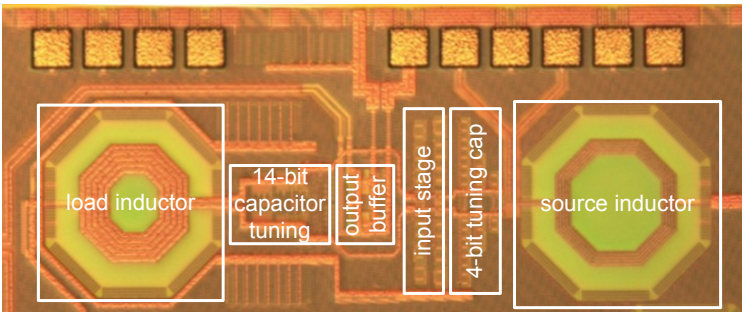


Figure 6.10.: Chip micrograph of the LNA implemented in 90 nm CMOS.

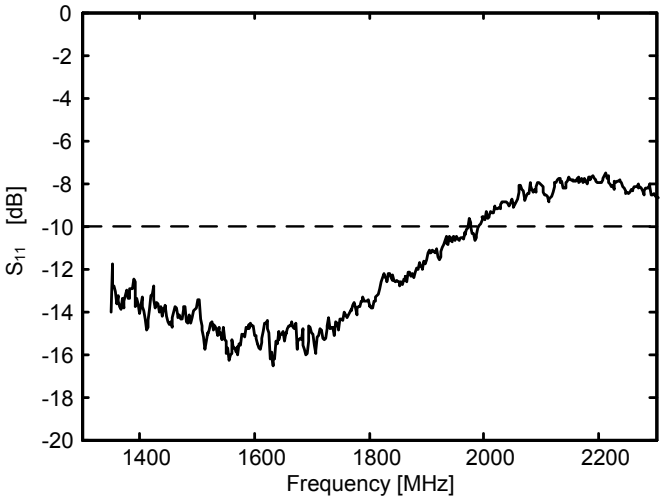


Figure 6.11.: Measured input matching S_{11} for lumped element balun center at 1.85 GHz.

In Fig. 6.11 the measured input matching (S_{11}) is presented. S_{11} remains well below -10 dB across the DCS 1800 band and most of the PCS 1900 band. Depending on the actual requirements at hand, the center frequency of the lumped element balun can be adjusted to improve matching at higher frequencies as the LNA input impedance itself is inherently broadband.

Center frequency tuning In Fig. 6.12 S_{21} for different LC tuning words is shown. The DCS 1800 and PCS 1900 target bands are not completely covered by the LC tuning. As seen in the figure, the maximum achievable LC tuning frequency is 1960 MHz whereas a maximum frequency of 1990 MHz must be achieved for the PCS 1900 band. This is due to the LC tuning range being shifted by approximately 100 MHz towards lower frequencies. Post-layout simulations reveal that the frequency shift can mainly be attributed to excess inductance of the relatively long lines connecting LNA cascode transistors and the LC tank.

Gain and noise figure Noise and gain measurement results are presented in Fig. 6.13. A noise figure of 4.1 dB is measured across both bands with the maximum gain centered at the frequency where the noise figure is measured. The measured noise figure includes board losses, the noise of the lumped element

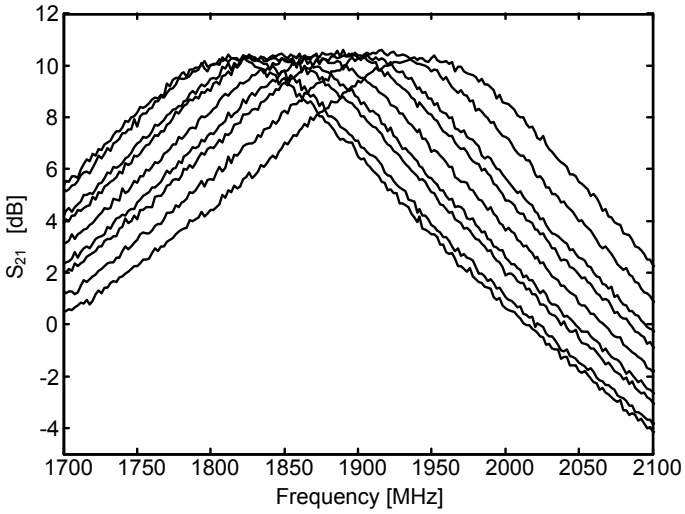
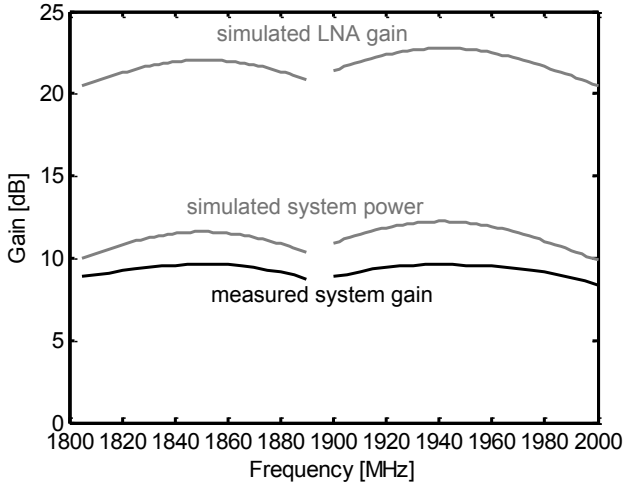
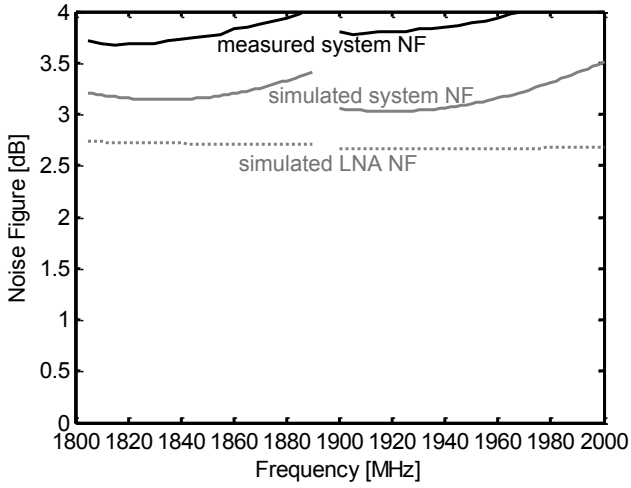


Figure 6.12.: Center frequency tuning.

balun, as well as noise and insertion loss of the on-chip output buffer used to drive the measurement equipment. The board losses in front of the lumped element balun have been measured to be 0.45 dB. Thus, the effective system noise figure of lumped element balun, LNA, and output buffer is 3.65 dB. Similarly, a maximum system power gain of 9.6 dB from balun input to buffer output is measured when correcting for board losses. In the intended system application [66] the LNA is not used as a standalone component but as part of a receiver chain. Thus, it is crucial to estimate the internal LNA gain and noise figure i.e. the gain and noise figure from balun input to the LNA output nodes at the LC tank. In order to enable these estimations measurement results are compared to post-layout simulation results. As seen in Fig. 6.13(a) a maximum gain of 9.6 dB is measured in the DCS and PCS band whereas the maximum simulated gain is 11.6 dB and 12.2 dB in the DCS and PCS band, respectively. The maximum simulated internal LNA gain in the DCS and PCS bands are 22 dB and 22.8 dB, respectively. In the worst case, all losses can be attributed to the LNA thus leading to a worst case estimate of maximum internal LNA gain of 20 dB in the DCS band and 20.2 dB in the PCS band. Similarly, a worst case internal LNA noise figure can be estimated from the simulated noise figure yielding an internal worst case noise figure of 3.3 dB and 3.46 dB in the DCS and PCS bands, respectively.



(a)



(b)

Figure 6.13.: Simulated (gray) and measured (black) gain (a) and noise (b) for two center frequency settings in DCS and PCS band.

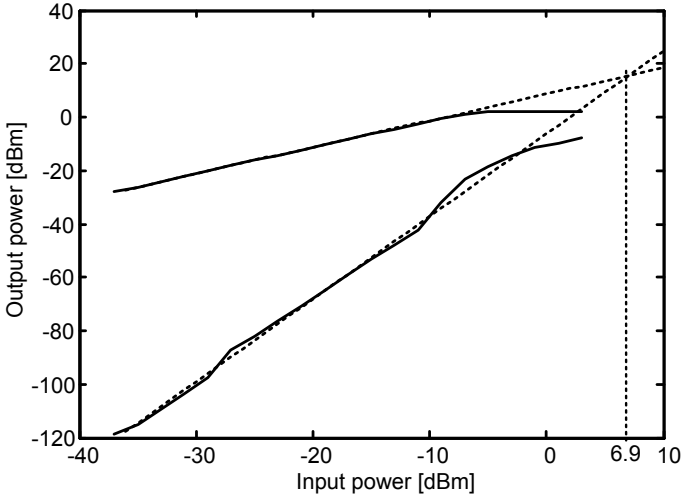
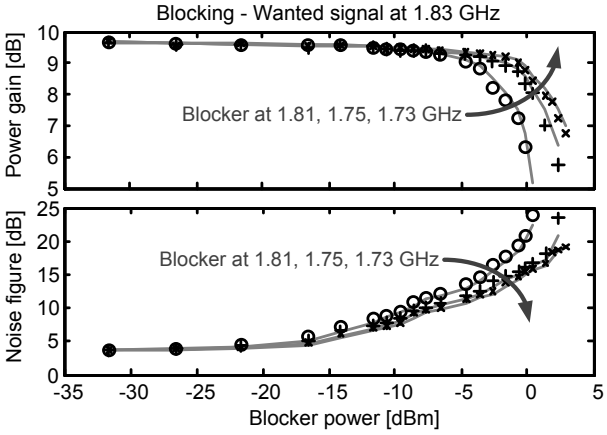


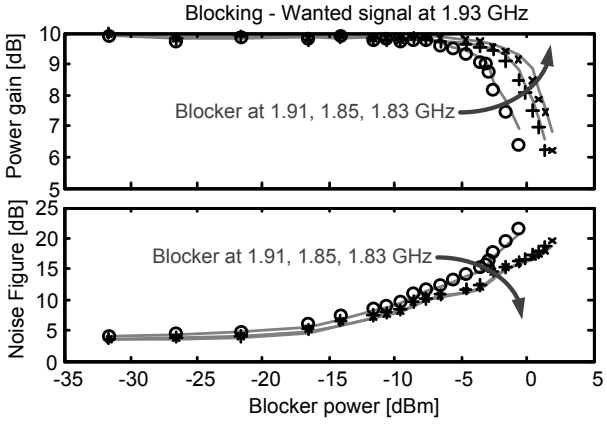
Figure 6.14.: $IIP3$ measurement at 1.85 GHz with interferers at 800 kHz and 1600 kHz offset.

Third order intermodulation distortion Third order intermodulation measurement results are shown in Fig. 6.14. The intermodulation product is measured at 1.85 GHz with the two-tone interferers applied at 800 kHz and 1.6 MHz offset above the wanted signal. From the measurement, the input referred IP3 is +6.9 dBm. A similar measurement yields an input referred 1 dB compression point of -1 dBm at 1.85 GHz center frequency.

Desensitization In order to characterize the desensitization performance of the LNA, gain and noise figure have been measured while sweeping the blocker power below the wanted signal at 20 MHz, 80 MHz, and 100 MHz offset, respectively. Results for the DCS and PCS bands are shown in Fig. 6.15. At low blocker powers, gain and noise figure are the same as measured before. As blocker power increases, the noise figure rises before the gain starts to drop. As seen in Fig. 6.15, the noise figure rises and gain drops faster the closer the blocker signal is applied to the wanted frequency. The 1 dB gain desensitization points, i.e. the blocker power where the gain at the wanted frequency has dropped by 1 dB, are -3 dBm, -0.4 dBm, and 0 dBm at 20 MHz, 80 MHz, and 100 MHz offset in the DCS band as seen in Fig. 6.15a. The respective 1 dB gain desensitization points in the PCS band are -2.9 dBm, -0.85 dBm, and 0 dBm (Fig. 6.15b).



(a)



(b)

Figure 6.15.: Blocking measurement results in DCS band (a), in PCS band (b).

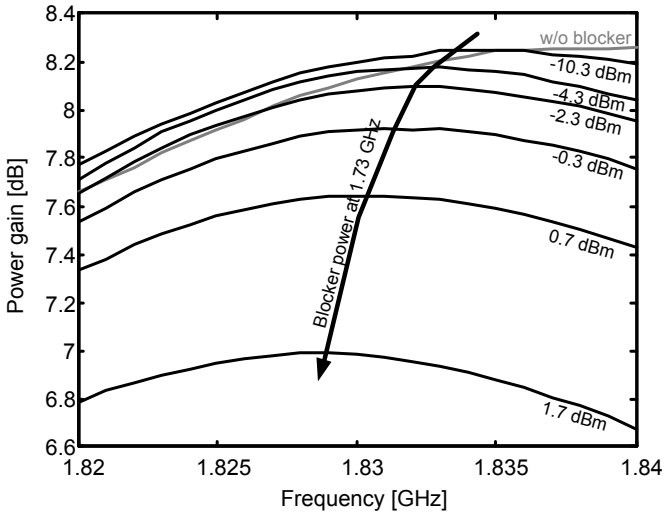


Figure 6.16.: Measured power gain vs. frequency for increasing blocker levels.

Moreover, the center frequency shift due to the LNA cascode devices which leave the saturation region at high blocker levels is observed in the measurements. As shown in Fig. 6.16, the maximum gain appears at a center frequency of 1.84 GHz without blocker. As the blocker power at 1.73 GHz is increased to levels of -10 dBm to 2 dBm gain decreases and the maximum shifts by 10 MHz to 15 MHz towards lower frequencies. Thus, gain at the wanted frequency of 1.84 GHz is not only reduced by compression of the input devices but also by a shift of the maximum gain point to lower frequencies.

In order to illustrate the effect of low-frequency upconversion a low frequency upconversion measurement has been conducted. A -11 dBm sinusoidal signal is swept from 100 kHz to 80 MHz using an Agilent A33250a signal source and combined with a blocker signal at 1.83 GHz from a Rohde & Schwarz SMU200A through a power combiner. The resulting upconverted signal power in the upper sideband of 1.83 GHz is depicted in Fig. 6.17. The comparatively high power level of the low frequency input signal is chosen to raise the input signal above the flicker noise floor. Moreover, the LNA input impedance is very low at low input signal frequencies resulting in a small voltage drop across the source inductors requiring high input signal levels to illustrate the effect at hand. As seen in

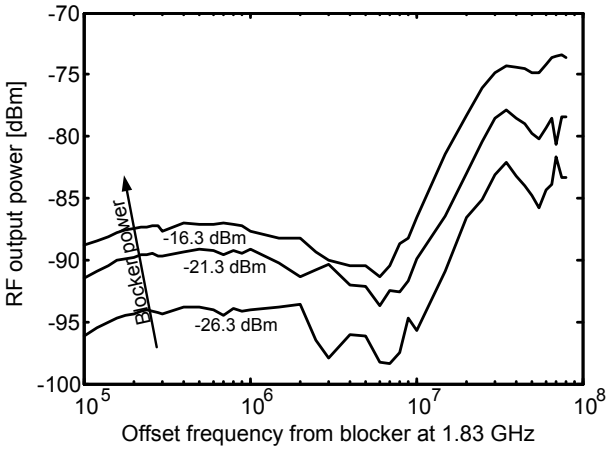


Figure 6.17.: Measurement of low frequency signal upconversion from LNA input to output.

the figure, the RF output power rises as the blocker power is increased thus clearly demonstrating the effect. In addition, a frequency dependence is seen as follows: At low frequencies the voltage drop across the LNA input impedance and consequently gain is small. As frequency and consequently input impedance rise output power also rises. As the offset frequency is further increased the output power does not increase anymore or decreases due to the selectivity of the LC tank load. This also exemplifies low frequency noise upconversion due to blockers. Similar considerations can be made for each noise source in the circuit revealing the filtering and frequency upconversion process whereas most circuit nodes are not accessible for measurements.

Discussion

Gain is lower and noise figure is higher than expected from the post-layout simulation. As mentioned above, the internal LNA noise figure and gain are worst case estimates as the gain drop and all excess noise are attributed to the LNA although the output buffer might also suffer from excess noise. The measured $IIP3$ of 6.9 dBm is 7.9 dB above the measured 1 dB compression point which compares to theory where a distance of roughly 10 dB is expected. The desensitization measurements agree well with the measured 1 dB compression point. From theory [23], a 2 dB gain drop due to blocking is expected at the 1 dB

compression point which is readily seen in the measurements with a blocker applied at 20 MHz offset. The LC tank load provides more selectivity for blockers at larger offset frequencies (80 MHz and 100 MHz) resulting in higher 1 dB desensitization points. While the gain is maintained at relatively high blocker power levels the noise figure already increases at medium power levels from around -15 dBm thus ultimately limiting sensitivity. Low frequency noise upconversion due to second order nonlinearity is identified as the main reason for this issue and exemplified by low frequency signal upconversion in presence of a blocker.

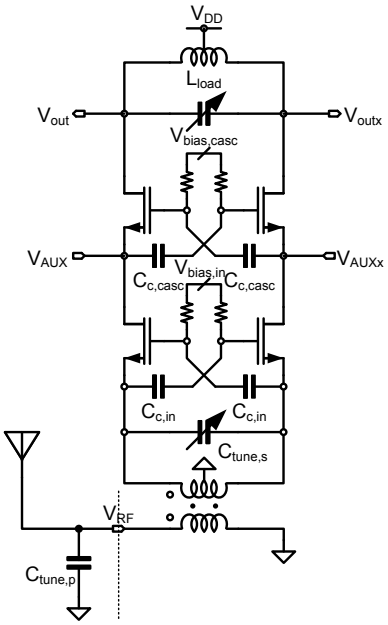
6.1.3. Single-Ended Input LNA

The goal of this work is to reduce front-end complexity. The capacitor cross-coupled common gate LNA exhibits high linearity and a good noise figure. Nontheless, a matching network or external balun is required. In order to further reduce front-end complexity, only a single pin in the whole solution is desirable. This requires an LNA with single-ended input. On the other hand, a differential LNA output is required for signal summation of the interference cancellation loop requiring an input unbalanced-to-balanced conversion on chip. One possible solution would be an active balun circuit like e.g. [78]. While this might be a viable solution for some applications it is not feasible if high linearity is required. Therefore, a passive transformer based approach is investigated.

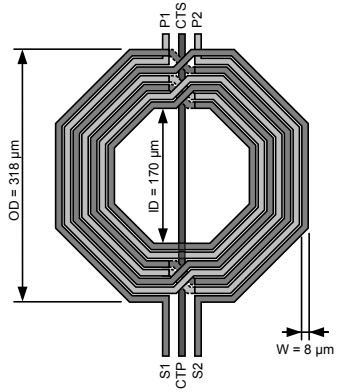
Circuit Design

The LNA core, i.e. the cross-coupled input stage, cascode stages, LC tank load, as well as bias and center frequency tuning, is left unchanged from the differential input implementation. Conversely, the source degeneration inductor is exchanged for a 4:3 on-chip transformer. The corresponding circuit diagram is depicted in Fig. 6.18(a).

Transformer design An octagonal symmetric (Rabjohn) balun [79] as shown in Fig. 6.18(b) is chosen as input balun. Its advantage over all other asymmetric types of baluns is that its winding arrangement locates all terminals at the outside edge making it readily accessible to the connecting circuit. Moreover, the center taps are located on the symmetry axis of the transformer as seen in the figure [79]. The implemented transformer has a turns ratio of 3:4, an outer diameter $OD = 318\,\mu m$, an inner diameter $ID = 170\,\mu m$, and a winding width $W = 8\,\mu m$. The minimum winding spacing $S = 3\,\mu m$ permitted by the design rules has been chosen to maximize edge coupling of the magnetic field between the windings. The associated increased interwinding capacitance and also the



(a)



(b)

Figure 6.18.: Capacitor cross-coupled common gate LNA with on-chip balun (a), 4:3 input transformer balun layout (b).

parasitic substrate capacitance resonate with the self-inductance of the primary and secondary windings. Above this self-resonant frequency the transformer input impedance is capacitive [79]. Therefore, care must be excercised that the self-resonant frequency is well above the intended frequency of operation. In addition, the insertion loss from the primary to the secondary winding must be as small as possible because any loss preceding the LNA adds to the noise figure. As pointed out in [79], insertion loss can be tuned by placing shunt capacitors at the primary and secondary windings as indicated in Fig. 6.18(a). The primary shunt capacitor is external to the chip and remains the only external component required for input matching. The secondary shunt capacitor is realized through a 4-bit tunable bank of MIM capacitors spanning a capacitance range from 0 pF to 2.1 pF.

The balun depicted in Fig. 6.18(b) has been designed using the Cadence Virtuoso Passive Component Modeler®(VPCM) [80]. VPCM automatically generates a layout, a compact model, and an electromagnetic full wave model. Moreover, to verify the exported models the design has been simulated using the Agilent Momentum®[81] field solver. The resulting transmission coefficients from the unbalanced to the balanced ports are depicted in Fig. 6.19. For an ideal 4:3 transformer the transmission coefficients from the unbalanced to balanced ports is 2/3 or -3.5 dB. The simulated transmission coefficients in the frequency range of interest are -3.8 dB and -4.8 dB for the lumped and the full wave electromagnetic model, respectively. The discrepancy between the lumped and the full wave electromagnetic model might be due to differences in the layer stack models used by the different tools as well as in effects not captured by the lumped model. The slight differences of the transmission coefficients between the the inverting and non-inverting balanced ports is due to interwinding capacitance as pointed out in [79].

Measurement Results

The single-ended input LNA has been implemented on the same die as the differential input cross-coupled common gate LNA. A chip micrograph is shown in Fig. 6.20(a) while the PCB area savings of the on-chip balun LNA in comparison to the LNA with external LC-balun are illustrated in Fig. 6.20(b).

Similar measurements as in the previous case have been conducted for two exemplary center frequency settings in the DCS and PCS bands. Gain and noise figure measurements are presented in Fig. 6.21. Again, system power gain as well as system noise figure have been measured. As in the previous case, insertion loss of the input lines (0.28 dB) has been accounted for in the results presented in the figure. Noise figure and gain have been optimized by tuning the

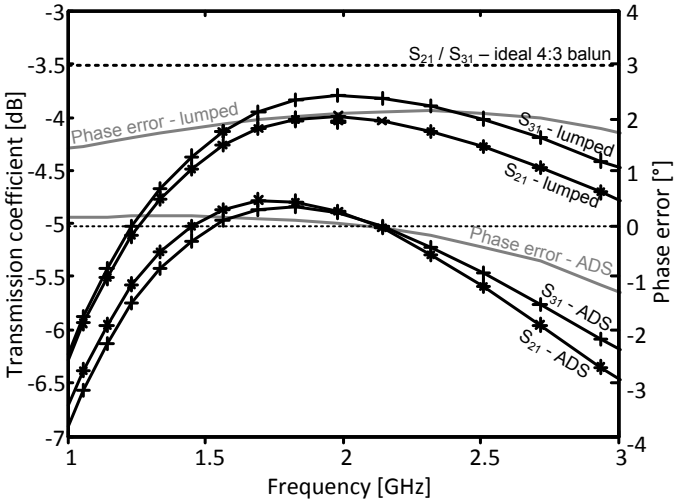


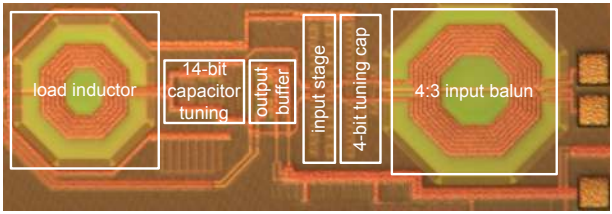
Figure 6.19.: Balun transmission coefficients from unbalanced port 1 to balanced ports 2 and 3.

primary and secondary winding capacitors to minimize balun insertion loss. The maximum gain in the DCS and PCS bands is 9 dB and 8.7 dB, respectively. The minimum measured system noise figure is 4.5 dB in the DCS as well as in the PCS bands. Again, internal LNA gain and noise figure are estimated by comparing the system power gain and noise figure to simulation results. As seen in Fig. 6.21(a) simulated system power gain is about 2.2 dB higher than the measured system power gain. Moreover, the measured system noise figure is 0.9 dB and 1 dB higher than simulated. Thus, by applying the worst case estimation approach laid out before, the internal LNA gain is 18.2 dB vs. the simulated 20.3 dB in the DCS band and measured 18 dB vs. simulated 20.8 dB in the PCS band. Similarly, the LNA noise figure is 4.15 dB and 4.25 dB in the DCS and PCS bands, respectively.

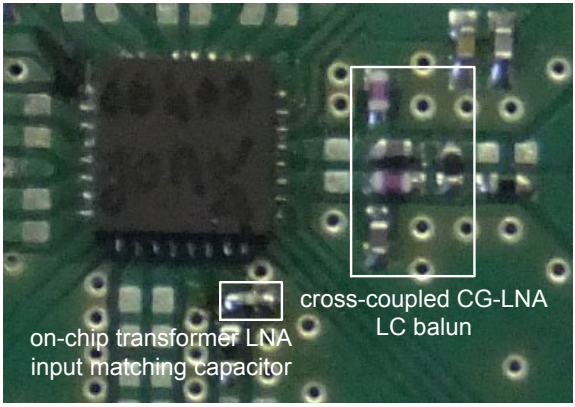
Moreover, third order intermodulation has been measured in the DCS band at 1.85 GHz with intermodulation interferers located at 800 kHz and 1600 kHz offset frequency (Fig. 6.22). The input referred $IIP3$ results in +7 dBm.

Discussion

Gain is about 2.1 dB and 2.8 dB lower than simulated in the DCS and PCS bands, respectively. Consequently, the noise figure is increased by roughly 1 dB. This

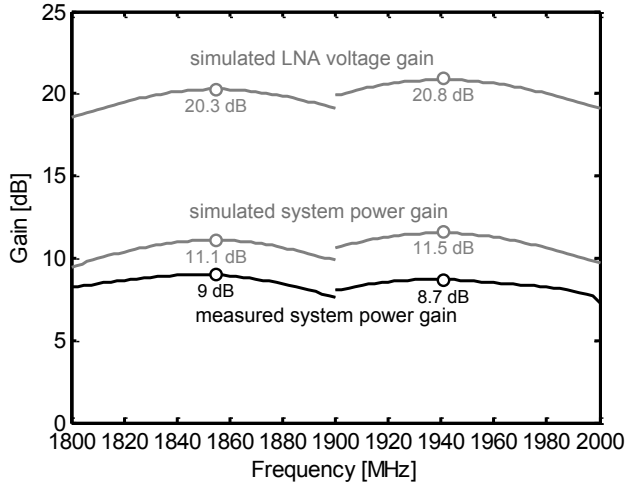


(a)

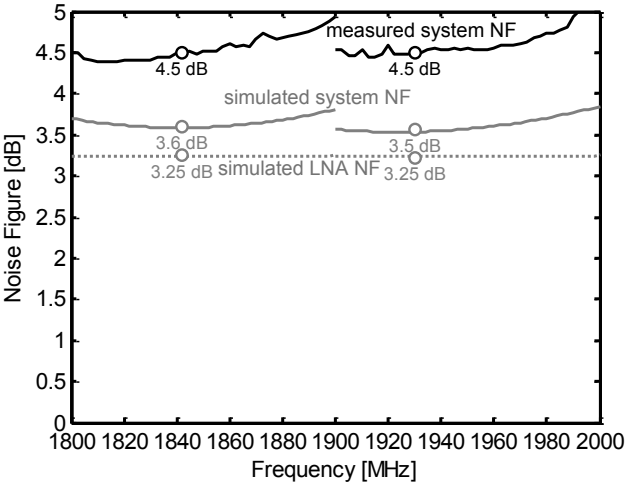


(b)

Figure 6.20.: Chip micrograph of LNA with input balun (a), PCB photograph showing cross-coupled CG-LNA and single-ended LNA matching networks (b).



(a)



(b)

Figure 6.21.: Simulated (gray) and measured (black) gain (a) and noise figure (b) of the single-ended LNA.

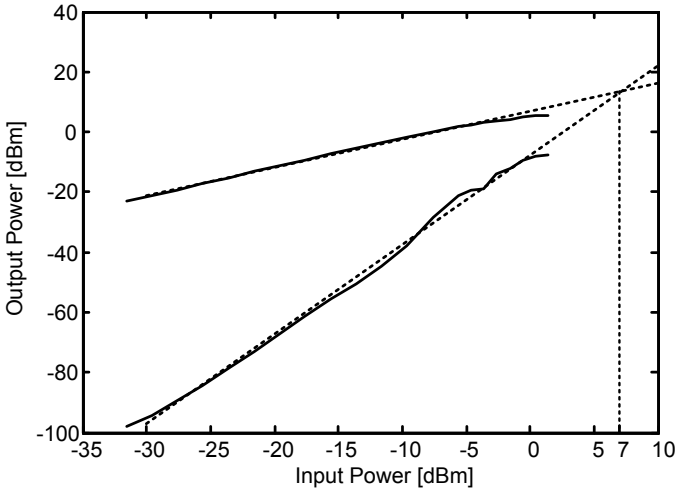


Figure 6.22.: $IIP3$ measurement at 1.85 GHz with interferers at 800 kHz and 1600 kHz offset.

is caused by increased insertion loss of the transformer balun compared to the model obtained from the electromagnetic field simulation. The $IIP3$ of +7 dBm is comparable to the differential input implementation. If the reduced pin count due to single ended operation outweighs the disadvantage of an increased noise figure, this must be accounted for in the level plan.

6.2. Direct Conversion Receiver

The requirements for a SAW-less direct conversion receiver capable of GSM-operation have been discussed in chapter 5 while fundamental system design aspects of the interference cancellation loop have been pointed out in chapter 3. In this section, circuit design and measurement results of an implemented receiver front-end with interference cancellation are described. The circuit block specifications identified in the level plan are used for the design of the individual receiver blocks.

An overview of the implemented front-end is given in Fig. 6.23. It uses a capacitively cross-coupled LNA as described in the previous section to obtain the required linearity before the filtering by the interference cancellation loop. The LNA output signal is fed back into the interference cancellation core which

processes the output signal and subtracts the blocker replica by current summation into the LNA cascode node. The LNA output signal can be monitored using an RF output buffer which is capable of driving the 50 Ω load impedance of the measurement equipment. The filtered LNA signal is downconverted in the main receiver path by an I/Q mixer. In the baseband, two filtering stages suppress close-in interferers. For debugging purposes, the output voltages of each filter stage can be multiplexed to the output using two multiplexers. All mixer stages are supplied with the local oscillator clock from the local oscillator path consisting of a predriver stage, a 25 % duty cycle quadrature frequency divider, and buffer stages to drive the clock lines and the mixer switches.

A 3-wire bus interface provides configuration data for tuning and circuit reconfiguration of individual circuit blocks. An on-chip bandgap reference and central programmable bias current mirrors are used to deliver stable reference currents.

The main receiver blocks are operated from a nominal supply voltage of 2.5 V, while the LO path can work from a supply of 1.1 V to 1.3 V. The RF output buffer has a nominal supply voltage of 3.3 V.

6.2.1. Circuit Design

In this section, design of the constituent circuit blocks of Fig. 6.23 is discussed.

Receive Mixer

The receive mixer circuit is shown in Fig. 6.24. It adopts the mixer architecture presented in [63] and has also been used in the downconversion mixer of the first interference cancellation hardware demonstrator from Fig. 4.1. The mixer circuit consists of two quadrature paths which share a common transconductance input stage for voltage-to-current conversion. In each path, the transconductance stage is followed by a double-balanced switching quad which accomplishes frequency conversion by commutating the RF currents. The downconverted currents flow into a transimpedance amplifier which acts as a lowpass filter and converts the current back to the voltage domain. The operational amplifier inputs form a low-impedance node such that the first nodes which exhibit significant voltage swing are the operational amplifier outputs. Advantageously, interferers have already been filtered to some extent at this point by the RC lowpass thus relieving linearity burdens.

As seen in Fig. 6.24, the transconductor consists of a pseudo-differential input stage to minimize the number of stacked transistors and thus maximize available voltage headroom. Its bias voltage is generated using a replica bias circuit which

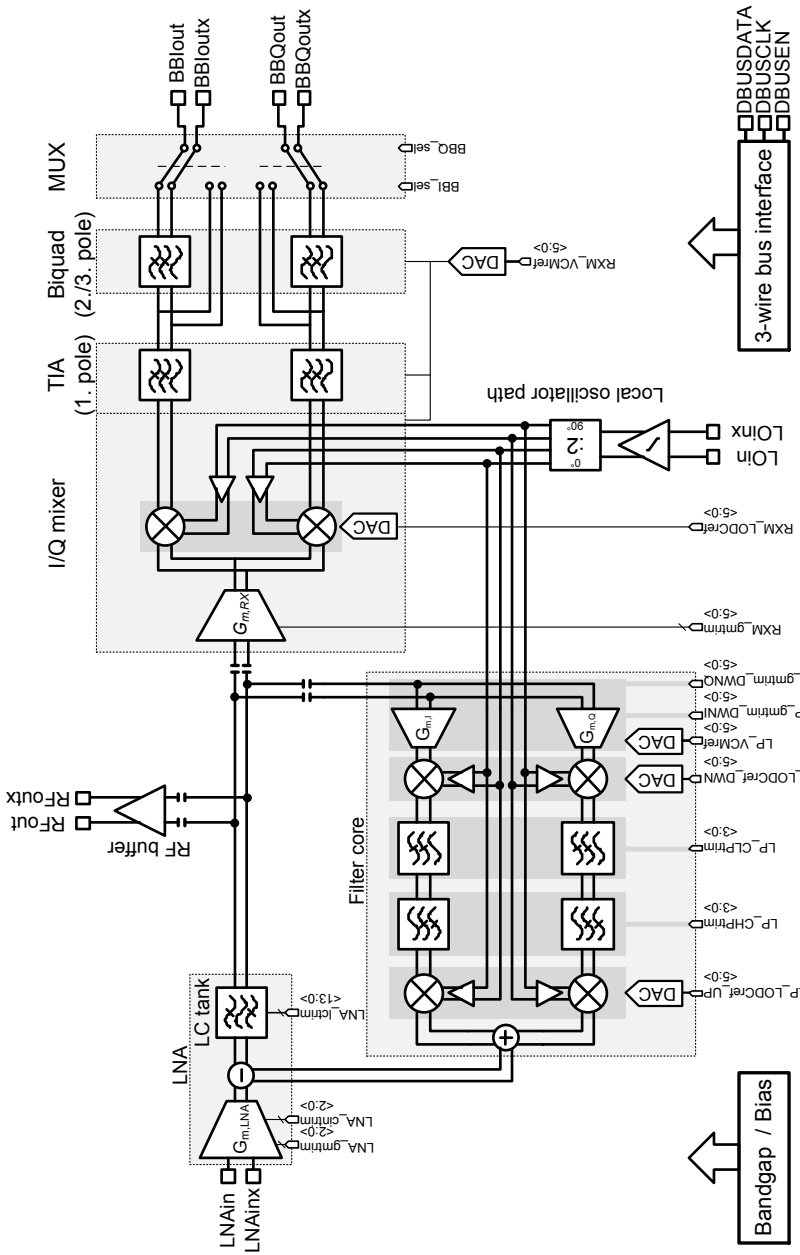


Figure 6.23.: Overview of implemented frontend.

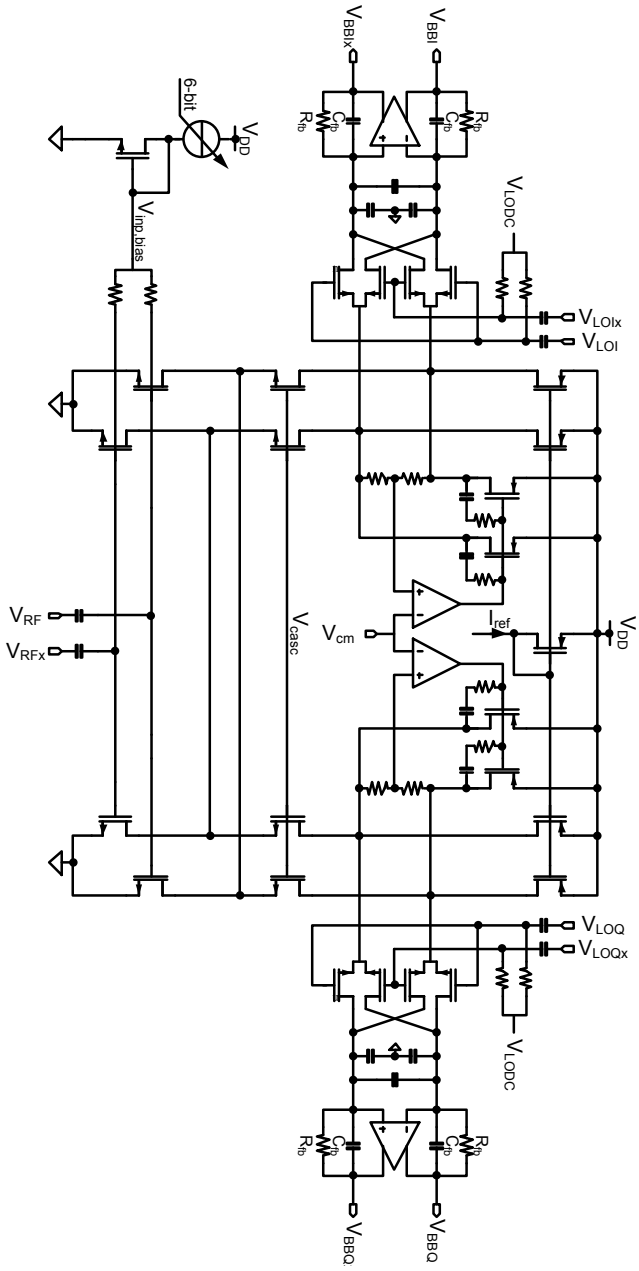


Figure 6.24.: Receive mixer circuit implementation.

is supplied by a 6-bit programmable reference current source to facilitate tuning of the input stage bias. The intention of sharing the input stage is the opportunity of better device matching between the I- and Q-paths by interdigitating the input transistors. Thus, lower I/Q imbalance is targetted. Subsequently, the current is equally split into the I- and Q-path by equally sized cascode devices.

The transconductance stage is DC-coupled to the switching quads to minimize parasitic capacitance. By this strategy, influence of the opamp input referred noise on the overall mixer noise can be minimized [63, 82]. To avoid DC current flow through the switches and its associated high flicker noise the common-modes at both ends of the switching quad must be carefully controlled. This is achieved by the split PMOS current sources on top of the cascode stages. The fixed current sources provide a constant quiescent current for the input stage. The common-mode level is set by controlled current sources. The common-mode reference voltage is applied to the mixer from a 6-bit programmable R2R-DAC to facilitate tuning of the mixer circuit. The common-mode control loop is formed by two voltage sensing resistors, an operational amplifier, and the controlled current sources with nulling Miller RC feedback [67] to ensure loop stability. At the switching quad outputs the common-mode voltage is set by the opamp's common-mode control loop. The local oscillator signals are AC-coupled to the switches by 1.8 pF MIM-capacitors. The local oscillator DC reference level is set by a 6-bit R2R-DAC to facilitate tuning.

Lowpass filtering of the switching quad output current is obtained by the RC lowpass characteristic of the transimpedance amplifier stage. A low input impedance of the transimpedance amplifier and thus reliable filtering is only maintained within the bandwidth of the opamp. Therefore, additional parallel capacitors are provided for passive filtering of interferers residing above the opamp bandwidth or LO leakage. The conversion gain is obtained from [63, 82]

$$\frac{v_{out}(\omega_{out})}{v_{in}(\omega_{in})} = \frac{\sqrt{2}}{\pi} g_m \frac{R_{fb}}{1 + \omega_{out} R_{fb} C_{fb}}, \tag{6.12}$$

where g_m is the mixer input stage transconductance and ω_{in} and ω_{out} are related to the RF input and IF output frequencies, respectively. The factor $\sqrt{2}/\pi$ is due to the first harmonic of the periodically time-varying transfer function [63] of the mixer driven by a 25 % duty cycle clock [83]. As seen in (6.12), the conversion gain is set by the transconductance g_m of the input stage and the feedback resistor R_{fb}. The baseband bandwidth is set by $\frac{1}{2\pi R_{fb} C_{fb}}$. By increasing the feedback resistor R_{fb} conversion gain is increased and the 3 dB corner frequency is decreased. Unfortunately, increased resistance results in a higher noise level thus corrupting mixer noise performance. Therefore, the approach is to design for the

maximum feedback resistor which still fulfills the noise specification. Then, the gain is set by the input stage transconductance g_m and the baseband bandwidth by the feedback capacitor C_{fb}. Depending on the required corner frequency this can result in large capacitors and high area consumption. Hence, a trade-off between area and maximum allowable noise must be sought.

In the implemented circuit the feedback resistors R_{fb} are 5.1 kΩ poly resistors. The feedback capacitors C_{fb} of 35.2 pF are implemented as a combination of MIM-capacitors, NMOS-varactors, and PMOS-capacitors to achieve a high capacitance density and minimize the required area. Additional capacitors with a total capacitance of 9.2 pF are placed in parallel with the switching quad outputs so that an overall corner frequency of 750 kHz is accomplished as specified in chapter 5.2. The simulated conversion gain including extracted parasitic is 28.8 dB, the thermal input referred double sideband noise voltage is $2.8\,\mathrm{nV}/\sqrt{\mathrm{Hz}}$, and the flicker noise corner frequency is 20 kHz. The simulated input referred $IIP3$ RMS voltage is -9 dBVrms. Total mixer current consumption is 15.6 mA from a 2.5 V supply. The input transconductance stage consumes 12.6 mA, each common-mode control opamp consumes 300 uA, and the transimpedance amplifiers consume 1.2 mA each.

Baseband Operational Amplifier

The baseband operational amplifiers are fully differential, folded-cascode operational amplifiers as depicted in Fig. 6.25. The first stage is a folded-cascode stage generating gain while output current driving capability is achieved through a class-A source follower stage. To maximize output voltage swing native NMOS devices offering almost zero threshold voltage are used in the source-follower stage as described in [84]. A rail-to-rail input stage has linearity advantages [82], particularly at high blocker levels close to the wanted channel, but has not been implemented for simplicity. The common-mode voltage is set by a common-mode control loop consisting of a pair of common-mode sense resistors at the output, a differential stage, and the controlled current sources M2A and M2B. The control loop is compensated by $C_{cm} = 0.62\,\mathrm{pF}$ and $R_{cm} = 16.2\,\mathrm{k\Omega}$. The opamp signal path itself is compensated by $C_c = 0.8\,\mathrm{pF}$ and $R_c = 8.2\,\mathrm{k\Omega}$.

As the direct conversion receiver is very sensitive to flicker noise long-channel devices are used to minimize flicker noise. Most flicker noise is contributed by the differential input stage (M1A/B) and the current source transistors (M2A/B, M3A/B, M0E-H). These devices are designed with a channel length of 5 µm and 4 µm, respectively.

The extracted simulation yields a gain of 68 dB and a unity-gain bandwidth of 70 MHz. The input referred noise voltage density is $14.5\,\mathrm{nV}/\sqrt{Hz}$ and a flicker

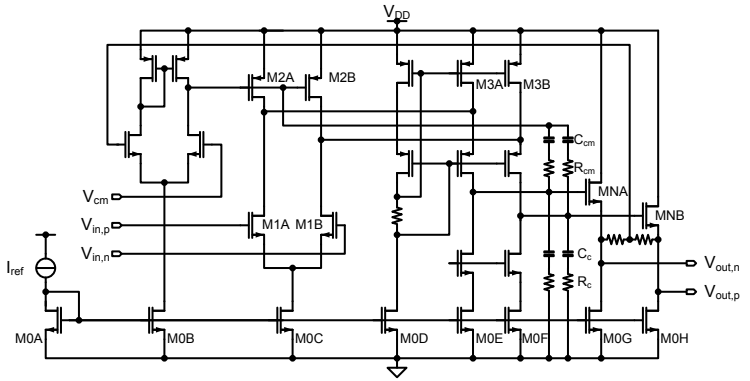


Figure 6.25.: Baseband operational amplifier.

noise corner of 8 kHz is achieved. The current consumption from a 2.5 V supply is 1.3 mA.

Baseband Biquad Filter

The baseband biquad lowpass filter which realizes the second and third filter pole is shown in Fig. 6.26. A multiple-feedback topology [67] is chosen as a -40 dB/decade roll-off can be achieved using only one single opamp. Moreover, gain and quality factor can be set independently. As laid out in chapter 5.2 the desired filter characteristic is a unity gain second order Butterworth lowpass. The design approach is very similar to the design of the mixer transimpedance amplifier. Again, the filter input referred noise is determined by the values of the resistors. Therefore, large capacitors C_1 and C_2 must be chosen to achieve the given transfer function at low noise levels. Hence, capacitor C_1 is chosen as a compromise between noise and area consumption. For a Butterworth filter with a quality factor $Q = 1/\sqrt{2}$ in unity gain configuration, the general design equations [67] simplify to

$$R_1 = R_2 = \frac{1}{2\sqrt{2}\omega_0 C_1}, \tag{6.13}$$

$$R_3 = \frac{1}{4\sqrt{2}\omega_0 C_1} = \frac{R_1}{2}, \tag{6.14}$$

$$C_2 = 2C_1. \tag{6.15}$$

Capacitor C_1 is chosen as 22.2 pF. Consequently capacitor C_2 is 44.4 pF, R1

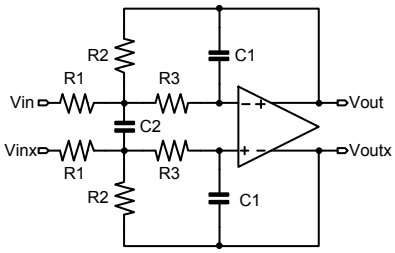


Figure 6.26.: Multiple feedback biquad filter.

and R2 are 7.2 kΩ, and R3 is 3.6 kΩ. Again, the capacitors are realized as a combination of MIM-capacitors, NMOS-varactors, and PMOS-capacitors to minimize area while the resistors are laid out as multiples of a 200 Ω poly resistor. The opamp is the same as previously described.

Using these settings, a corner frequency of 350 kHz as specified in chapter 5.2 is achieved. Moreover, circuit simulation including parasitics yields an input referred noise voltage density of 47.2 nV/$\sqrt{\text{Hz}}$ and a flicker noise corner frequency of 3 kHz which is all within the specification. The current consumption is 1.3 mA from a 2.5 V supply.

Filter Core

The implementation of the interference cancellation filter core is shown in Fig. 6.27. The filter core consists of two identical quadrature paths. Each path consists of a downconversion mixer, a programmable lowpass filter, a programmable highpass filter, and a passive upconversion mixer. The RF input of the filter core is AC-coupled to the LNA output node by two 1 pF MIM-capacitors. After signal processing the output currents of the passive upconversion mixers are summed at two common nodes and the resulting current is fed into the cascode nodes of the LNA through two 3 pF MIM-capacitors.

In contrast to the prior implementation from chapter 4, the open loop gain is completely generated in the downconversion mixers of the filter core. This eliminates excessive current consumption of the baseband buffers and avoids disturbances of the loop dynamics. As discussed in chapter 3, interference suppression is proportional to the available open loop gain around the interference cancellation loop. Since open loop gain is generated in the downconversion mixers, high transconductance is required for the input stage.

The downconversion mixer is again realized with a folded switching quad to

avoid DC current flow through the switches and the associated flicker noise problem. In the filter core, flicker noise at low frequencies is mitigated to some degree by the succeeding highpass filters. However, the downconversion mixer transconductance stage must be designed for high transconductance and high linearity resulting in high DC current levels causing excessive flicker noise. Hence, significant flicker noise can still leak across the highpass filters and is upconverted to RF severely deteriorating the noise figure in the wanted channel. Simulations reveal that Gilbert cells [85] as well as current-bleeding mixers [86] exhibit intolerably high flicker noise levels justifying the topology choice. Each input transistor of the transconductance stage is designed for a transconductance of 64 mS at a DC current of 6 mA. To maximize transconductance for a given current thin oxide transistors are used [2]. The common-mode is controlled in a similar fashion as in the receive mixer using controlled current sources and common-mode sense resistors. Moreover, the input stage bias voltage can be controlled using a 6-bit programmable current mirror circuit allowing for tuning after fabrication.

The lowpass and highpass filters are purely passive and realized using switched capacitors C_{LP} and C_{HP}, respectively. The lowpass capacitor C_{LP} can be tuned from 132.5 fF to 2.2 pF using a 4-bit control word. It is realized by MIM-capacitors. The highpass filter capacitors C_{HP} can cover a capacitance range from 8.8 pF to 70.4 pF in steps of 8.8 pF. Due to the high required capacitance it has been optimized for capacitance density using a combination of MIM-capacitors, fringe capacitors, NMOS-varactors, and PMOS capacitors.

The upconversion mixers are realized through switching quads as passive mixers whose output currents are summed in the RF domain. The switches are optimized for low LO leakage to avoid deteriorating LNA performance. Moreover, LO leakage preceding the receive mixer results in unwanted DC offsets in the baseband and its associated problems. Therefore, switches are small devices to avoid LO leakage through parasitic capacitors.

The common-mode reference voltage $V_{CM,ref}$ as well as the local oscillator reference voltages $V_{LO,dwn}$ and $V_{LO,up}$ can be programmed from 0 to 2.5 V in steps of 40 mV using a 6-bit R2R DAC. This allows for maximum circuit reconfigurability and freedom for performance optimization eliminating one of the major drawbacks of the prior implementation from chapter 4. The passive mixer is operated with 25 % duty cycle to avoid unwanted interaction between the I- and Q-paths. If the switches are driven with 50 % duty cycle I- and Q-paths are shorted for a quarter period the LO period leading to non-desired effects [54].

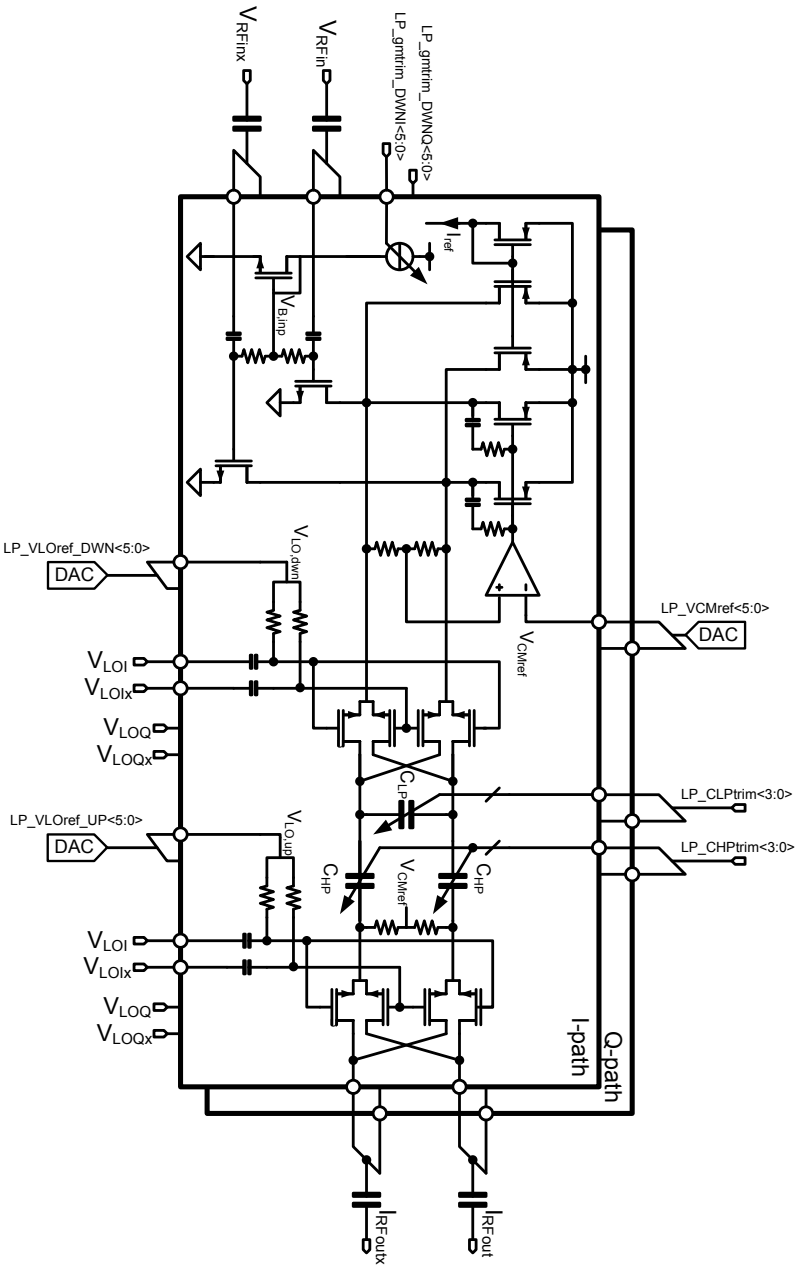


Figure 6.27.: Filter core circuit implementation.

LO Path

The local oscillator path generates a 25 % duty cycle square wave signal for driving the mixer switches as well as the parasitic capacitances associated with the signal lines. Line-up of the LO path is shown in Fig. 6.23. First, an external sinusoidal signal at twice the LO frequency is delivered to the chip. An external balun and a 100 Ω resistor in parallel with the inputs of the first differential input buffer stage depicted in Fig. 6.28(b) provide power matching to the external LO source. The differential input buffer is a self-biased inverter stage which amplifies the incident sinusoidal input signal and provides a square-wave like output signal to the frequency divider. Self-biasing using feedback resistors ensures midrail common-mode input voltage levels. The Razavi-type [87] frequency divider generates 25 % duty-cycle quadrature local oscillator signals which are delivered to the mixer switches. Full-swing CMOS inverter buffers as shown in Fig. 6.28(c) are used to drive the switch and clock line parasitic capacitances. Transistor sizes of the buffer stages and the frequency divider are optimized for low phase-noise [88, 89] to preserve low noise performance of the mixers. Therefore, phase-noise is allowed to degrade by merely 0.1 dB after passing the LO path. Hence, the phase-noise contributed by the LO path must remain 15 dB below the synthesizer phase-noise as specified in Tab. 2.3. This mandates a careful trade-off between circuit performance and power consumption. In the layout, parasitics of the differential clock lines and of different branches of the LO clock tree must be well balanced to avoid phase mismatch between the mixer stages. This is achieved by routing the clock lines in a star-like fashion thus balancing parasitic capacitances.

6.2.2. Open Loop Gain and Stability Simulation

In order to assess stability, the open loop gain is calculated in the simulation. This is achieved by breaking the loop mathematically. The transfer function of the filter core is calculated by probing the filter core output current and the LNA output voltage. Similarly, the transfer function of the LNA cascode and LC tank load can be calculated by probing the input current of the LNA cascode devices and the LNA output voltage. By cascading the LNA cascode / LC tank transfer function and the filter core transfer function, the overall open loop transfer function can be obtained without breaking the feedback loop. The correctness of this approach is verified by calculating the closed loop transfer function (3.1) from the partial transfer functions and comparison to the simulated closed loop response.

As an example, a Bode plot as well as a Nyquist plot of the open loop gain

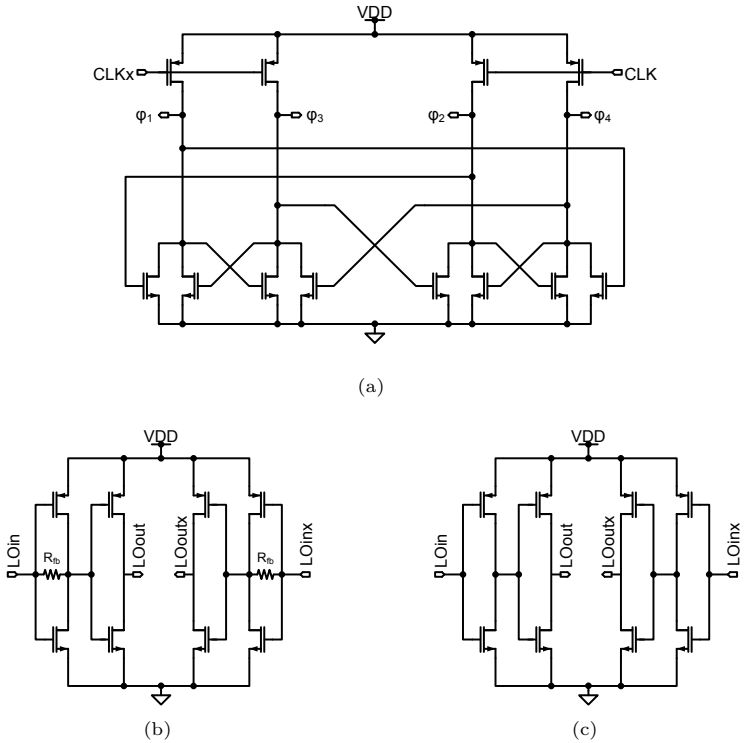
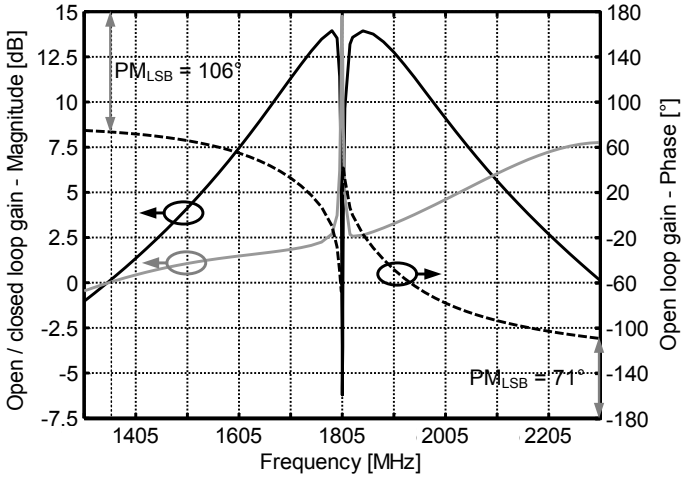


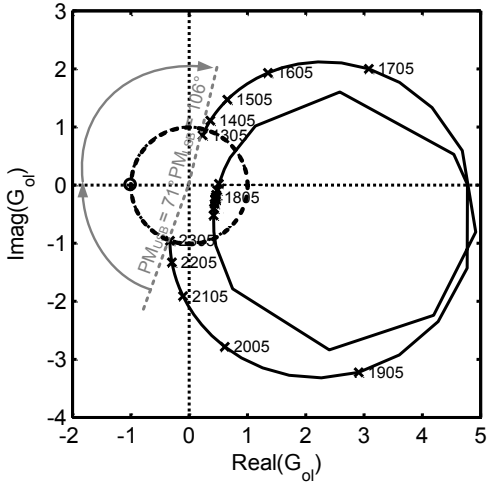
Figure 6.28.: Elements of the LO path: Razavi frequency divider with 25% duty cycle (a), self-biased input buffer (b), full-swing LO buffer (c).

for a center frequency of 1805 MHz are presented in Fig. 6.29. From the open loop Bode plot shown in Fig. 6.29(a) a maximum open loop gain of 14 dB is obtained. The lower and upper sideband unity gain frequencies are 1350 MHz and 2310 MHz, respectively. Note that the unity gain offset frequencies from the carrier are 455 MHz in the lower sideband and 505 MHz in the upper sideband. This is due to the asymmetric impedance profile of the LC tank. Correspondingly, the lower and upper sideband phase margins are 106 ° and 71 °. The associated closed loop transfer function is also displayed in Fig. 6.29(a). Due to the LC tank asymmetry and the lower phase margin in the upper sideband it exihibits a hump around the unity gain frequency.

The Nyquist plot presented in Fig. 6.29(b) is another way to conveniently



(a)



(b)

Figure 6.29.: Feedback cancellation open loop gain simulation Bode plot (a) and Nyquist plot (b).

judge on the system stability. According to Nyquits's stability criterion [90] the frequency response locus of the open loop gain must not circle the point $(-1, 0)$ of the complex plane. The frequency response locus starts at low frequencies close to the origin and traverses the complex plane clockwise as frequency is increased. First, loop gain rises and the curve departs from the origin. As the frequency approaches the carrier frequency, it gets closer to the origin again. This correlates to the dip seen in the magnitude response of the open loop transfer function from Fig. 6.29(a). Finally, loop gain increases and the frequency response locus approaches the unit circle and the origin again. The angle between the real axis and the points where the frequency response locus crosses the unit circle are the lower and upper sideband phase margins.

6.2.3. Layout Considerations

The chip has been implemented in a 1-poly, 9-metal, 90-nm CMOS process by TSMC as shown in Fig. 6.30. It covers an active area of $1.2 \times 1.5\,\mathrm{mm}^2$.

In the layout care is exercised to match the quadrature paths of the filter and the main receiver path to avoid imbalance effects. This is mainly achieved by keeping sensitive parts like the mixer input stages in close proximity and by maintaining a symmetric layout. Moreover, parasitics on sensitive circuits are minimized and balanced for differential lines. In the floorplan, the LNA input pads are placed in the pad frame for short and symmetric bondwire length. Coupling of sensitive signal lines is avoided by routing and shielding techniques. Thus, LO signals are routed orthogonally to the RF signal path to the greatest possible extent and parallel routing is avoided. Additionally, the quadrature frequency divider is placed as closely as possible to the mixer input stages to avoid spreading the LO signal across the chip. This approach also minimizes LO phase mismatch between individual mixer stages due to long LO lines and large differences in the loading. As pointed out before, the LO clock tree is laid out in a star-like fashion to balance parasitics. The input signal to the quadrature frequency divider at twice the LO frequency is routed as a long differential line on metal-6 shielded by metal-5, metal-7, and via fences. Parallel routing of the filter core input lines, which are tapped from the LNA output as indicated in Fig. 6.23, with the filter core output lines leading back to the LNA cascodes cannot be avoided. In order to minimize coupling between input and output, the differential lines are routed on different metal layers and shielded by a common shield line.

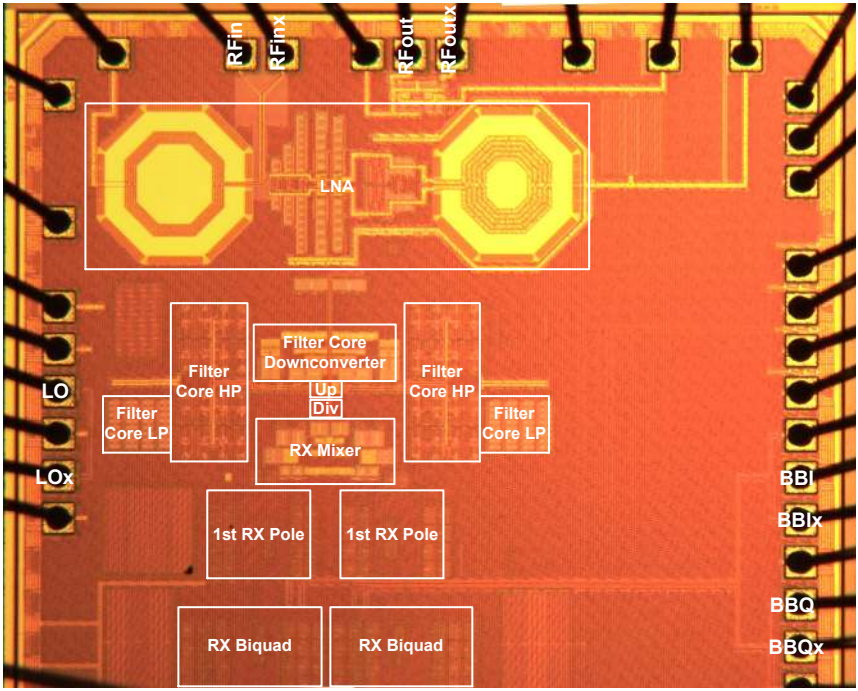


Figure 6.30.: Chip micrograph of the implemented receiver front-end.

6.2.4. Measurement Results

In this section, measurement of the implemented receiver is discussed. First, the measurement setup is described. Subsequently, measurement results are discussed.

Measurement Setup

The measurement setup is shown in Fig. 6.31. The receiver device-under-test (DUT) is soldered on a 2-layer printed circuit board. The input matching network consists of a 20 pF decoupling capacitor and the LC-balun discussed in chapter 6.1.2. The local oscillator is matched to the chip using a TDK HHM1583B1 [91] multilayer balun performing a 50 Ω to 100 Ω unbalance-to-balance conversion. The differential RF output buffer is matched to the measurement equipment by a TDK HHM1526 [91] balun. The center taps at the differential side of

both baluns are connected to RF ground by 200 pF capacitors. In order to drive the measurement equipment at baseband frequencies, the differential, high-impedance baseband outputs are connected to differential-to-single-ended line receivers MAX4444 [92] operating from a bipolar ±5 V supply. Their gain is precisely set to a factor of two so that the signal level seen at the matched 50 Ω input port of the spectrum analyzer is consistent with the differential signal at the high-impedance baseband outputs. As the spectrum analyzer input is very sensitive to DC voltages, a 500 nF blocking capacitor is mounted at the output of the line receivers for DC protection. Moreover, the baseband outputs can also be directly probed by an oscilloscope with high-impedance inputs.

The sinusoidal local oscillator signal is provided by a Rohde & Schwarz SMR40 signal generator at -10 dBm, whereas the RF input signals are delivered by SMJ100A and SMU200A vector signal generators. The DC supply voltages at 1.3 V for the LO path, 2.5 V for the receiver front-end, and at 3.3 V for the RF output buffer are applied by an Agilent N6705B DC Power Analyzer. All measurement equipment is remote-controlled via a General Purpose Interface Bus (GPIB) using a MATLAB®workstation. The serial 3-wire data bus for chip configuration is controlled by a microcontroller board [93] which interfaces to the workstation through USB.

Measurement Results

In the following, measurement results of the main receiver path and the complete system comprising the receiver and the interference cancellation loop are presented. First, small signal gain and noise measurements are reported. Then, performance under large signal interference conditions including desensitization, third, and second order intermodulation is evaluated. For brevity, exemplary results at 1805 MHz are presented and differences to other bands are mentioned when applicable. Measurement results for other frequencies and bands are shown in the appendix.

Small signal gain and noise Small signal performance has been evaluated using the setup shown in Fig. 6.31. Gain measurements are conducted by connecting the SMU200A vector signal generator to the DUT and sweeping frequency. Noise is measured using the gain method [94, 95]: The receiver input is terminated with a 50 Ω match and the output noise at the baseband ports is measured using the FSQ40 spectrum analyzer. Due to more than 40 dB gain preceding the spectrum analyzer input stage the receiver output noise floor is well above the spectrum analyzer noise floor. Hence, spectrum analyzer noise can be neglected and the

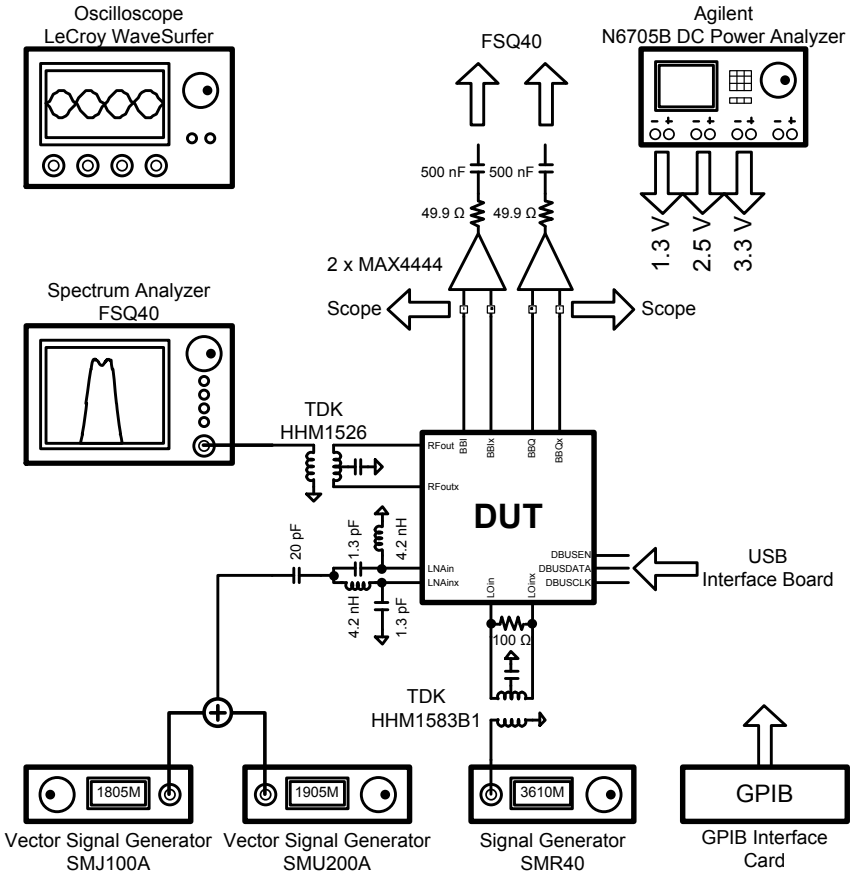


Figure 6.31.: Measurement setup.

spot noise figure is obtained by

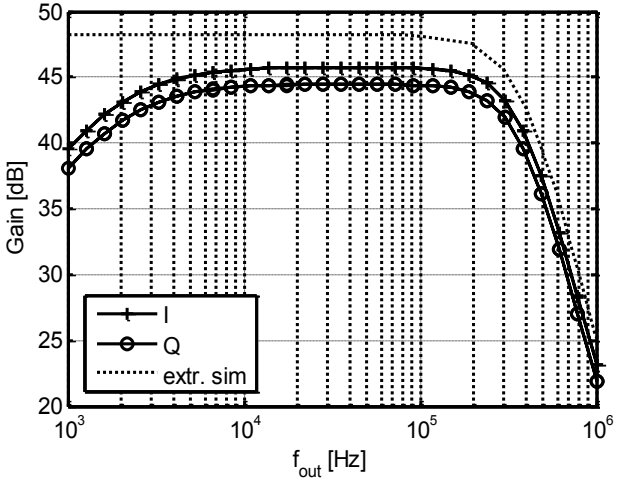
$$NF_{ssb} = dBm(P_{n,RXout}) - dB(Gain) + 174\,\text{dBm/Hz}. \tag{6.16}$$

Note that (6.16) is the single-sideband noise figure from Fig. 2.3(a) as no image reject filter is used and noise from the lower as well as the upper sideband of the carrier is translated to the baseband while gain is measured at a single frequency only. In a direct conversion receiver however, the double sideband noise figure must be used because no image band exists. Therefore, (6.16) must be corrected for the double sideband spot noise figure by 3 dB

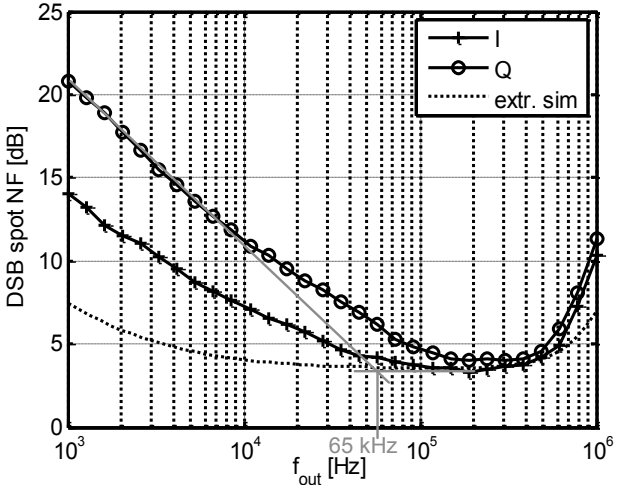
$$NF_{dsb} = NF_{ssb} - 3\,\text{dB}. \tag{6.17}$$

Receiver without interference cancellation For the measurements of the receiver path, the interference cancellation loop has been disabled by turning off the bias currents for the downconversion mixer stages of the filter core and setting the LO DC reference voltages of the filter core mixing stages to their lowest possible value to avoid toggling the mixer switches. The common-mode level of the receiver path as well as the LO DC reference voltage is set to 1.28 V. In this mode, the test chip has a current consumption of 24 mA from the 2.5 V supply for the LNA, receive mixer, baseband filters, and biasing. The LO path consumes 14.6 mA from the 1.3 V supply. The resulting gain and noise figure measurement results are shown in Fig. 6.32. For the settings at hand a gain around 45 dB with an I/Q gain mismatch of 1.5 dB is obtained. The gain drop from 1 kHz to 10 kHz is caused by the DC block capacitor which is used to protect the spectrum analyzer from DC voltages. A minimum double sideband spot noise figure of 3.3 dB in the I- and 4 dB in the Q-channel is obtained at 200 kHz. The flicker noise corner frequency is 65 kHz.

Receiver with interference cancellation The settings of the receiver path with interference cancellation are similar to the case presented above. The common-mode voltage in the filter core is set to 1.28 V and the LO DC reference voltages of the filter core downconversion and upconversion mixers are adjusted at 1.92 V. The highpass coupling capacitors are set to their maximum value to obtain a narrow RF filter characteristic while the lowpass capacitors are at the minimum setting. In this mode, the chip consumes 50.2 mA from the 2.5 V supply for the receiver path and interference cancellation blocks. The LO path has a current consumption of 14.6 mA from the 1.3 V supply. The corresponding gain and noise figure measurement results are presented in Fig. 6.33. The gain is around 40 dB for I- and Q-path. Note, that different corner frequencies are attained for the



(a)



(b)

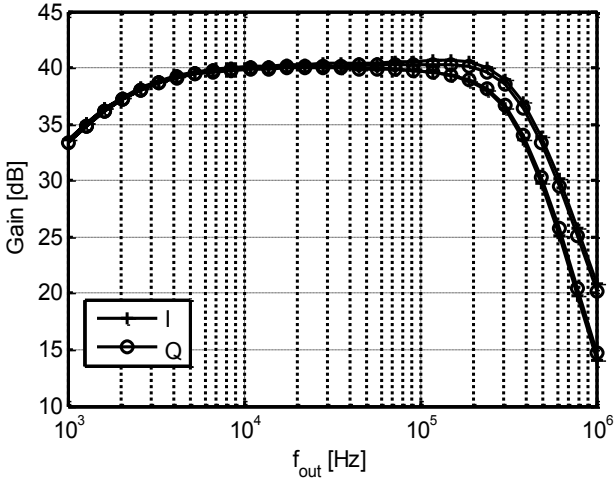
Figure 6.32.: Small signal gain (a) and noise figure (b) without interference cancellation at 1805 MHz.

upper and lower sidebands around the carrier. This is due to the asymmetric characteristic of the interference cancellation transfer function as pointed out in chapter 3.4.1 and seen in the measurement of the RF transfer function from Fig. 6.36. In comparison to the case without interference cancellation, the gain drops by approximately 5 dB. The gain drop is caused by two effects. First, the LNA gain is decreased by approximately 2 dB due to the effects lined out in chapter 3. Moreover, the local oscillator leaks into the wanted channel at the loop up-conversion mixer causing a higher DC offset in the main receiver path due to LO self-mixing which leads to reduced gain in the main receive path.

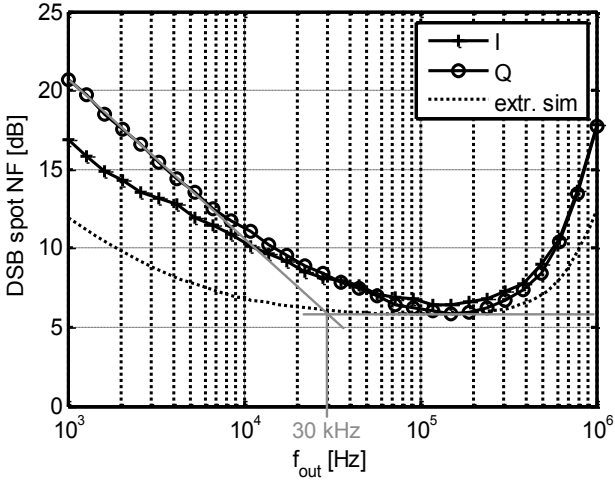
The minimum double sideband spot noise figure is 6 dB at 150 kHz. The flicker noise corner frequency is around 30 kHz.

Desensitization Gain and noise figure desensitization measurements have been conducted by sweeping the blocker power of the most critical out-of-band blockers identified in chapter 2.3.4 at 100 MHz, 20 MHz, and 3 MHz offset frequency from the wanted channel. As shown in Fig. 6.31, a power combiner is used to add the wanted signal at 1805 MHz with a power of -50 dBm from the SMU200A with the blocker signal provided by the SMJ100A. The gain at the wanted frequency and the blocker output power are measured using a FSQ40 spectrum analyzer. The noise figure is determined by connecting the SMJ100A blocker source directly to the receiver input and measuring the noise floor in the baseband using the gain method described in the preceding paragraph. As the SMJ100A vector signal generator has an output impedance of 50 Ω this is similar to connecting a match to the input which has been confirmed by prior measurements. Thus, the noise figure can be determined versus the blocker power. Again, the interference cancellation has been disabled by setting the configuration parameters appropriately for the receiver path only measurements.

Receiver without interference cancellation Desensitization results for the receiver path without interference cancellation are shown in Fig. 6.34. According to the measurements, the 1 dB desensitization points for blockers at 3 MHz and 20 MHz offset frequency are -25 dBm, while -8 dBm are obtained at 100 MHz offset frequency. The double sideband spot noise figure at 80 kHz rises from its small-signal value of 4.2 dB as the blocker power is increased. As discussed in chapter 5.2, the maximum allowable noise figure under blocking conditions is 15 dB. From Fig. 6.34(b) and Tab. 6.2 the noise figure at 3 MHz offset at -26 dBm blocker power is 10.6 dB and 11.9 dB thus fulfilling the GSM specification. The other critical blockers at 20 MHz and 100 MHz exceed the maximum allowable value but would be mitigated by the SAW-filter.

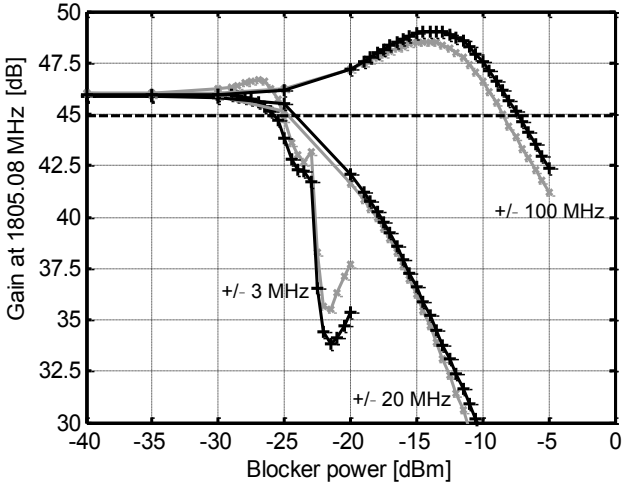


(a)

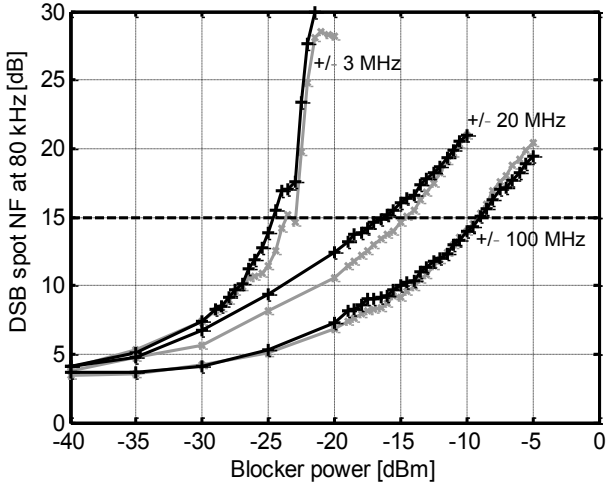


(b)

Figure 6.33.: Small signal gain (a) and noise figure (b) with interference cancellation at 1805 MHz.



(a)



(b)

Figure 6.34.: Conversion gain from 1805.08 MHz to 80 kHz vs. blocker power without interference cancellation.

Offset frequency MHz	Blocker power dBm	NF receiver dB	NF SAW-less dB
-3	-26	10.6	11.6
+3	-26	11.9	9.7
-20	-12	18.2	14.4
+20	-12	18.7	15.4
-100	-9	15	13.6
+100	-9	15	15.6

Table 6.2.: Comparison of noise figure for critical blockers.

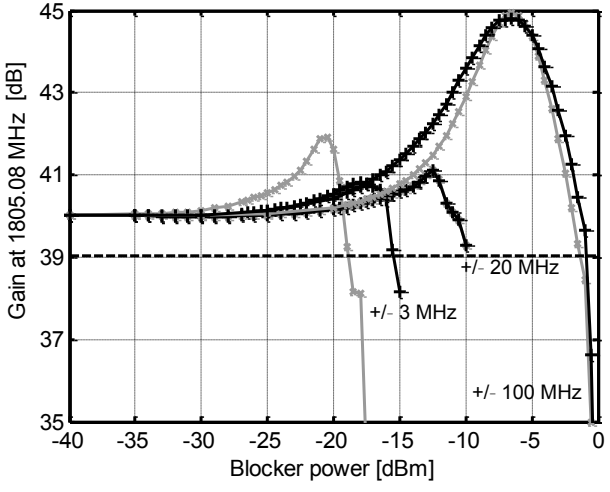
Receiver with interference cancellation Desensitization measurements for the receiver with interference cancellation are presented in Fig. 6.35. As interference cancellation is activated, the receiver desensitization points improve to -18 dBm and -16 dBm at ±3 MHz, -9.5 dBm at ±20 MHz, and -1 dBm at 100 MHz offset. Like in the previous case, noise figure rises from its small signal value of 6 dB as the blocker power is increased. In comparison (Tab. 6.2), the noise figure with critical blockers is improved by up to 3.8 dB at -20 MHz offset, while it is deteriorated by 1 dB at -3 MHz offset. The specification is not met for the 100 MHz blocker with a noise figure in excess of 20 dB.

IIP3 The input referred intercept point IIP_3 is measured in a similar setup as for the desensitization measurements. The interferer input power at 800 kHz and 1600 kHz offset frequency is swept and the intermodulation products in the wanted channel as well as the output interferer signals at 800 kHz and 1600 kHz are measured at the baseband outputs.

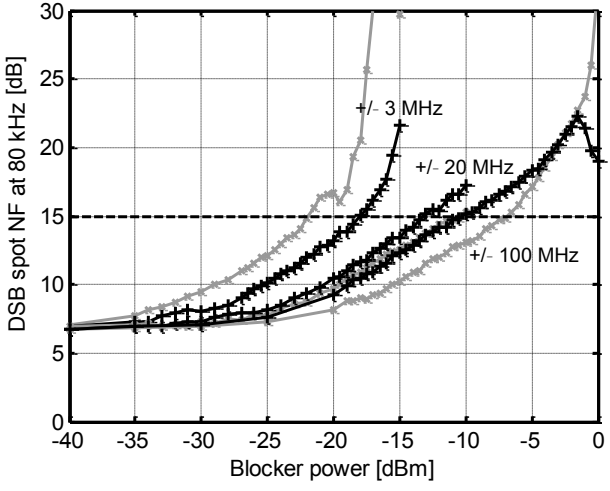
As the output test tones have different amplitude due to baseband filtering the output test tone power must be corrected by the filter selectivity. The intermodulation product resides in the wanted band and experiences no filtering. Therefore, the effective input referred $IIP3$, which can be compared to the receiver specification, is

$$IIP3_{eff} = dBm(P_{in}(\omega_1)) + \frac{1}{2}\left(dBm(P_{out,\omega_1}) + S(\omega_1) - dBm(P_{IM3})\right). \quad (6.18)$$

Measurement results for the DCS and PCS bands are shown in Fig. 6.3. As seen in the table, the receiver exceeds the $IIP3$ specification of -19 dBm from chapter 2.3 by more than 6 dB.



(a)



(b)

Figure 6.35.: Conversion gain from 1805.08 MHz to 80 kHz vs. blocker power with interference cancellation.

Frequency	IIP3 w/o interference cancellation	IIP3 /w interference cancellation
MHz	dBm	dBm
1805	-12.4	-7.2
1880	-12.8	-9.2
1930	-13.2	-8.7
1990	-13.7	-8.9

Table 6.3.: Input referred third order intercept point for the complete receiver.

Frequency	IIP2 w/o interference cancellation	IIP2 /w interference cancellation
MHz	dBm	dBm
1805	+26	+44.1
1880	+26.4	+38.7
1930	+25.4	+32.2
1990	+23.6	+30.5

Table 6.4.: Input referred second order intercept point for the complete receiver.

IIP2 The input referred second order intercept point $IIP2$ is measured with two single-tone interferers 100 kHz apart centered at +6 MHz offset frequency from the wanted channel. The intermodulation product at 100 kHz is monitored in a similar setup as described for the other intermodulation measurements and the effective $IIP2$ due to filtering is calculated correspondingly by

$$IIP2_{eff} = dBm(P_{in}(\omega_1)) + (dBm(P_{out,\omega_1}) + S(\omega_1) - dBm(P_{IM2})) \,. \quad (6.19)$$

Measurement results are listed in Tab. 6.4. As seen in the table, the receiver fails to meet the specification of 47 dBm derived in chapter 2.3.6 by more than 20 dB. It is assumed that this effect is caused by LO leakage of the filter core upconversion mixer which causes self-mixing and consequently DC offsets in the baseband of the main receiver path. A detailed analysis of the effects contributing to second order intermodulation due to self-mixing is given in [96]. When the interference cancellation is enabled the 6 MHz interferers are reduced by the loop thus leading to lower second order intermodulation and higher $IIP2$. It must also be noted that $IIP2$ is subject to device mismatch effects and hence would have to be measured for a number of samples to support these values.

Interference cancellation at LNA output The RF output signal of the LNA and interference cancellation block can be probed using the on-chip RF output buffer. The small signal transfer characteristic S_{21} from the LNA input to the RF buffer output have been measured using a ZVL3 network analyzer. Results are displayed in Fig. 6.36 showing the transfer characteristics for the LC tank centered at 1805 MHz, 1880 MHz, 1930 MHz, and 1990 MHz with interference cancellation disabled and enabled. As expected, the in-band gain drops by 1.8 dB to 2 dB as the interference cancellation is turned on. A maximum selectivity of 10.3 dB to 11.6 dB is attained 60 MHz to 80 MHz below the carrier, depending on the center frequency. Moreover, a pronounced hump is observed 200 MHz to 220 MHz above the carrier as is expected from prior work. Around these offset frequencies, selectivity degrades to 4.9 dB to 5.7 dB.

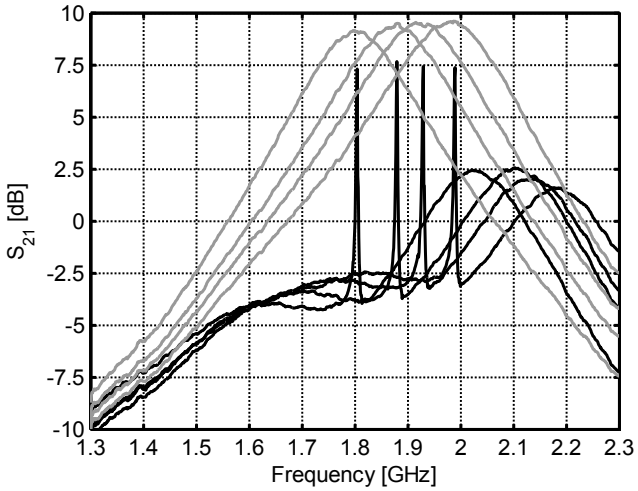


Figure 6.36.: S_{21} at RF output buffer with interference cancellation disabled (gray) and enabled (black) at 1805 MHz,1880 MHz, 1930 MHz, and 1990 MHz.

As pointed out in chapter 3.4.1, the peaking can be mitigated by lowering the LC tank center frequency below the carrier frequency. In the chip implementation at hand, this is achieved by increasing the LC trimming word. Measurements of S_{21} are shown in Fig. 6.37. As the LC tank center frequency is decreased, the hump moves to lower offset frequencies and its magnitude decreases. For the settings used in the measurements, the hump decreases by 3 dB. Below the

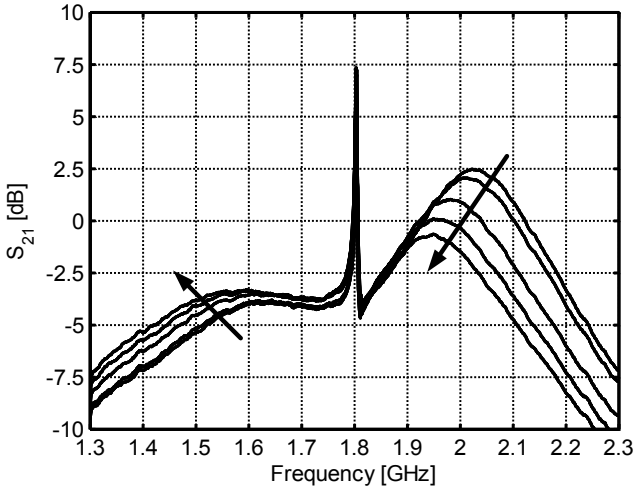


Figure 6.37.: Effect of descreasing the LC tank center frequency on closed loop transfer function.

carrier frequency, on the other hand, the selectivity degrades by 1 dB to 2.5 dB.

Desensitization measurements have been conducted by sweeping the blocker power at 1705 MHz while measuring the small signal gain from 1725 MHz to 1900 MHz. Results are depicted in Fig. 6.38. At low blocker levels, the selectivity curve of Fig. 6.36 is reproduced. As the blocker power is increased, gain at the carrier frequency is maintained but selectivity starts to decrease as revealed by Fig. 6.38. At a blocker level of 0 dBm the minimum selectivity is merely 2 dB as compared to 11.6 dB at low blocker levels. Still, the gain at the carrier frequency drops by less than 1 dB. The selectivity reduction is caused by compression of the open loop gain at high blocker levels.

Moreover, measurements of gain and noise figure around the wanted channel have been conducted for blockers at ± 20 MHz and ± 100 MHz offset using the y-factor method [95]. Results are presented in Fig. 6.39. As seen in the figure, gain is maintained even at high blocker levels in correspondence with Fig. 6.38 when interference cancellation is enabled. Still, by considering Fig. 6.39(b), the noise figure rises faster with interference cancellation enabled. This is due to the reciprocal mixing effect pointed out in chapter 5.2.2. Note that the measured RF noise figure is higher than the noise figure for the complete receiver. It is expected that the excess noise is contributed by the RF output buffer and non-idealities in

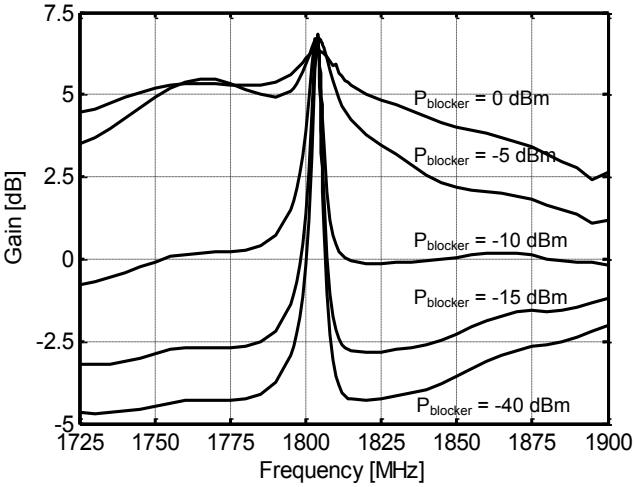


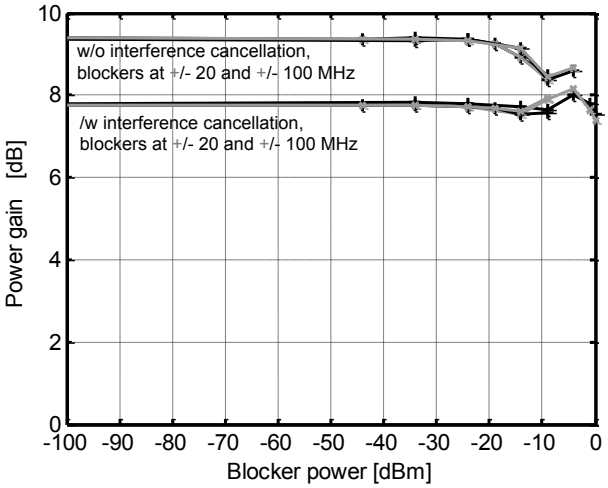
Figure 6.38.: Gain desensitization and selectivity reduction at the LNA output due to loop gain compression by blocker at 1705 MHz.

the RF path.

In addition, it has been noted in chapter 3.4.3 that phase and gain mismatch between the filter core quadrature paths leads to a blocker image. The blocker and blocker image output powers at 1705 MHz and 1905 MHz, respectively, have been measured versus the blocker input power. Results are displayed in Fig. 6.40. At low blocker levels, the blocker and its image maintain a constant ratio of 20 dB. As the input blocker power rises above -20 dBm, the image rises faster than the blocker until the image power compresses at input powers around -10 dBm.

6.3. Comparison to Published Work

Subsequently, this work is compared to published work. In [16, 97] a feedforward blocker filtering technique is proposed which uses a translational loop i.e. a downconversion, filtering, and upconversion process. In contrast to this work, only LNA and translational loop have been implemented in [16, 97]. Without filtering a gain of 23.4 dB is measured versus 20.9 dB when filtering is enabled. The noise figure is 3.9 dB without and 6.8 dB with filtering, respectively. The selectivity is better than 20 dB. For a wanted signal at 1.96 GHz and a blocker at 80 MHz offset, the 1 dB gain desensitization point stays around 0 dBm with filtering



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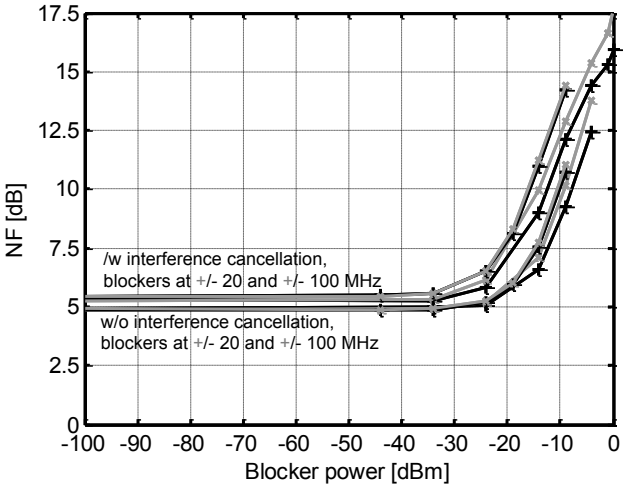

(b)

Figure 6.39.: Desensitization at 1805 MHz: Gain (a), noise figure (b).

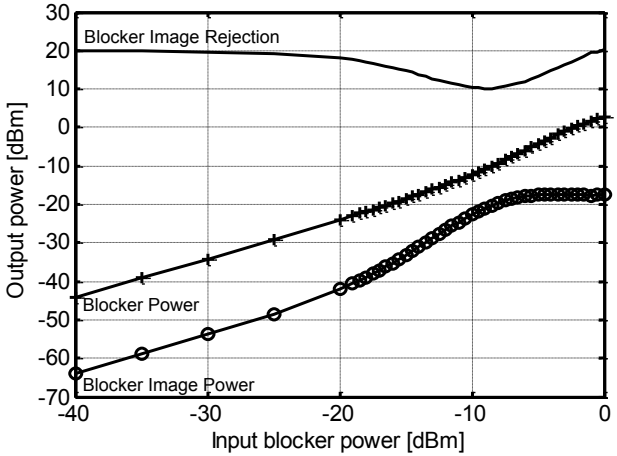

Figure 6.40.: Output blocker power and image power with $f_{LO} = 1805\,\text{MHz}$, $f_{Blocker} = 1705\,\text{MHz}$, and $f_{Image} = 1905\,\text{MHz}$.

enabled and at -12 dBm, when filtering is disabled. Noise figure desensitization measurements are not presented in the references. The current consumption from a 1.2 / 2.5 V is 29 mA and 8 mA with and without filtering, respectively.

Recently, [54] has presented a GSM compliant front-end for the PCS band employing driving point impedance translation in a passive mixer. The 1 dB gain desensitization point is above 0 dBm and the noise figure rises from 3.1 dB to 11.4 dB when the blocker is applied at 80 MHz offset. The presented front-end including receive PLL consumes 55 mA. Selectivity for a given offset frequency is not reported in the reference.

In comparison to [16, 97] the noise figure is 0.6 dB lower for the complete receive chain in this work without filtering, whereas it is comparable to the noise figure published in [54]. Also, as filtering is enabled, the noise figure of the presented receiver remains 0.8 dB below the noise figure presented in [16, 97]. In [16, 97] an RF selectivity better than 20 dB is achieved while the feedback approach at hand achieves a maximum selectivity of 10.3 dB to 11.6 dB for approximately the same current consumption. This is due to the observations made in chapter 5.2.2. In the feedback approach at hand, selectivity is limited by the maximum achievable transconductance of the filter core. Conversely, in the feedforward approach filter core transconductance needs only be high enough to

match the LNA transconductance. Hence, better selectivity can be achieved in the feedforward scheme for the same current consumption. Moreover, the filter curve in the feedforward approach does not exhibit the "humping" phenomenon in the upper sideband, as it is not affected by phase margin issues. The 1 dB gain desensitization points of the feedforward scheme as well as the feedback scheme are both around 0 dBm, whereas [54] achieves +2 dBm.

As pointed out in chapter 5.2.2, the feedback cancellation approach at hand is prone to reciprocal mixing effects. Hence, the presented receiver violates the 15 dB noise figure limit set by the GSM specification at large blockers of 0 dBm. No data on noise figure desensitization is given in [16, 97] but it is expected that it will suffer from the same issue. Conversely, the solution presented in [54] using driving point impedance translation meets the 15 dBm maximum noise figure requirement.

In conclusion, the feedforward approach [16, 97] offers higher selectivity for a given current than the feedback approach, while the implemented feedback cancellation scheme has a smaller noise figure. Still, both approaches have similar gain desensitization points around 0 dBm. The receiver employing driving point impedance translation [54] outperforms both, feedforward and feedback cancellation, in terms of noise figure, gain desensitization, and noise figure desensitization.

7. Conclusions

This work investigates feasibility of a SAW-less GSM front-end for the DCS 1800 and PCS 1900 bands based on a feedback interference cancellation technique to filter large-signal blockers on-chip.

First, the feedback interference cancellation concept is explored theoretically by a rigorous mathematical analysis. Open loop and closed loop transfer functions are derived to assess stability and system trade-offs. From the analysis, it is found that a trade-off between phase margin and inband gain degradation exists. Moreover, the mathematical analysis reveals nonidealities like an asymmetric closed transfer function which is caused by different phase margins below and above the carrier frequency and a center frequency shift. It is found that the asymmetry can be mitigated by adjusting the LC tank center frequency below the carrier frequency. A mismatch analysis of the filter core quadrature paths predicts generation of a blocker image signal. In contrast to a feedforward cancellation approach the image is reduced by the feedback loop. In addition, reciprocal mixing of the blocker replica generated by the filter core with local oscillator phase noise is identified as the most critical noise mechanism of the concept.

A first hardware demonstrator in 65-nm CMOS proofs the concept. It exhibits a noise figure of 7 dB and a gain of 25 dB. When the interference cancellation loop is activated, gain drops by 2.2 dB and noise figure rises by 0.2 dB as predicted by theory. In a desensitization scenario, gain drops by 12.6 dB when a -15 dBm blocker at 20 MHz is applied without interference cancellation. With interference cancellation gain drops by merely 3 dB. The implemented proof-of-concept chip has a current consumption of 150 mA from a 2.5 V supply which mainly originates from current buffers in the filter core feedback path which draw a current of 60 mA.

In a following step, requirements for a GSM-compliant receiver are derived from the system specification. First, a conventional direct conversion receiver line-up with SAW-filter is devised and afterwards trade-offs for SAW-less operation are discussed. In the receiver line-up, high ADC resolution is assumed allowing low gain in the front-end and filtering of adjacent channel interferers in the digital domain. This relieves analog filtering requirements and obviates the need for complex gain control and DC offset correction circuitry. Level plans for the conventional as well as the SAW-less receiver are presented and block

level specifications for the individual receiver circuit blocks are obtained. For the SAW-less receiver it is found that selectivity of the feedback interference cancellation loop is limited by the realizable open loop gain which is set by the maximum attainable transconductance of the downconversion mixer stages. From this analysis, a maximum attainable selectivity of 15 dB is estimated. Due to the reciprocal mixing process in the filter core, local oscillator phase noise plays a more pronounced role in the SAW-less front-end in contrast to a conventional front-end. This increases phase noise requirements for the local oscillator. Still, it is expected that state-of-the-art GSM frequency synthesizers can fulfill the increased requirements as they resemble the GSM transmit frequency synthesizer specification. Moreover, as no filtering is applied prior to the LNA, LNA linearity is identified as crucial for overall SAW-less receiver linearity.

Therefore, different LNA topologies are investigated for high dynamic range i.e. for high linearity and low noise figure. Moreover, a detailed analysis of LNA desensitization mechanisms including gain compression and bias noise upconversion is conducted. From a topology evaluation, the capacitor cross-coupled LNA is identified as the best candidate to achieve these goals. The capacitor cross-coupled LNA is implemented in a 90-nm CMOS process with differential inputs and as a single-ended version with an on-chip transformer balun. The differential input LNA achieves a gain of 20 dB and a noise figure of 3.3 dB to 3.5 dB. The 1 dB-desensitization point ranges between -3 dBm and 0 dBm, depending on the blocker offset frequency. The single-ended input LNA minimizes pin count, which is extremely desirable in a large multistandard, multiband transceiver SoC. Due to the transformer insertion loss it exhibits a higher noise figure of 4.2 dB and a lower gain of 18 dB compared to the differential LNA version.

Finally, a SAW-less GSM receiver prototype with interference cancellation is implemented in 90-nm CMOS according to specifications obtained from the levelplan. The main receiver path consists of a differential capacitor cross-coupled common-gate LNA, a passive quadrature downconversion mixer with a low-pass transimpedance amplifier load, which constitutes the first filter pole, and a multiple feedback biquad realizing the second and third filter pole with a single operational amplifier. The interference cancellation filter core feedback path is implemented through passive quadrature downconversion mixers with a preceding transconductance stage generating the open loop gain, programmable lowpass and highpass filters, and a passive upconversion mixer.

The implemented receiver prototype is capable of operation in the DCS band from 1805 MHz to 1880 MHz as well as in the PCS band from 1930 MHz to 1990 MHz. When operated without interference cancellation, the receiver exhibits

a noise figure of 3.3 dB and a gain of 45 dB at a current consumption of 24 mA from a 2.5 V supply. As the interference cancellation loop is activated, gain drops by 5 dB to 40 dB due to the inherent gain degradation of the interference cancellation loop and offsets in the main receiver path caused by increased local oscillator leakage and self-mixing. The noise figure rises by 2.7 dB to 6 dB. In this mode, the main receiver path and the filter core consume 50.2 mA from a 2.5 V. In both modes of operation, the local oscillator path operating from a 1.3 V supply draws a current of 14.3 mA.

Exemplary desensitization measurements of a wanted signal at 1805 MHz with a 1 dB gain desensitization point of -26 dBm and a blocker noise figure of 10.6 dB to 11.9 dB show that the main receiver path would fulfill the GSM specification if a SAW-filter is used. When the interference cancellation loop is activated, the 1 dB gain desensitization points increase between 7 dB and 15.5 dB depending on the blocker offset frequency. While gain of the front-end is well maintained over the blocker mask, noise figure desensitization fails to meet the GSM maximum noise figure specification of 15 dBm, particularly for the 0 dBm blocker at 100 MHz offset frequency which is in excess of 20 dB. This might be caused by bias noise upconversion in the receiver path as well as by reciprocal mixing of phase noise in the upconversion mixers of the interference cancellation feedback path and requires further improvement in order to meet the GSM specification.

Further measurements of the RF path from the LNA input to the LNA output reveal that the interference cancellation loop exhibits the predicted asymmetric transfer function leading to reduced filtering in the upper sideband. Thus, small signal measurements show a selectivity of more than 11 dB in the lower sideband while selectivity degrades down to 5 dB at offset frequencies of 200 MHz to 250 MHz above the carrier due to the asymmetry. Moreover, a blocker image 20 dB below the blocker is observed due to mismatch in the filter core quadrature paths, when the interference cancellation loop is activated.

While the main receiver path is capable of GSM-compliant operation, when an external SAW-filter is used, further improvements of the interference cancellation loop have to be made for SAW-less operation. The limiting factor for GSM-compliance of the proposed scheme is noise figure desensitization, particularly at high blocker levels.

Noise figure and current consumption of the proposed scheme is comparable to the feedforward cancellation approach proposed by [16]. Although the selectivity attained by feedback cancellation is lower than the selectivity obtained in [16], 1 dB gain desensitization performance is comparable. In order to obtain high selectivity in the feedforward approach, the feedforward filter path must have an effective gain close to the main LNA path. If both paths are well matched, high

selectivity can be obtained. In the proposed feedback approach, the selectivity is set by the open loop gain which tends to require more gain in the feedback path compared to [16] hence limiting selectivity. Although no image blocker measurements are presented in [16] the feedback approach proposed in this work is expected to be less susceptible to quadrature path mismatch in comparison to the feedforward approach. Noise desensitization measurements are not published in [16], but it can be assumed that the design suffers from the same issues discovered in this work, in particular reciprocal mixing of phase noise at the upconversion mixer. In contrast to [16] a complete receiver front-end is proposed in this work.

The proposed scheme has been proven for narrow-band applications, hence future work should investigate feasibility of wideband SAW-less front-ends. As selectivity is limited by the loop bandwidth, the technique presented in this work is not very amenable for wideband operation. Moreover, it might be possible to improve some issues of the proposed scheme, such as the asymmetric transfer function or the slight center frequency shift. Some work in this direction has been presented by [58] based on [59, 60] where nesting of two translational filter cores is proposed. In [98] positive feedback is proposed to improve filtering. Moreover, compatibility of the interference cancellation loop with narrow-band low-IF receivers could be investigated.

In addition, it is desirable to reduce current consumption and noise figure under blocking conditions. An approach which has gained a lot of interest in the literature during the last period of this work are N-path filtering concepts and impedance translation techniques [50] which are very promising candidates for fulfilling the GSM specification in a SAW-less receiver at moderate current consumption. Considerable research efforts for removing external SAW-filters are still ongoing in academia [58, 98, 99] as well as in industry [100, 101]. Future holds which solution will prevail.

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Curriculum Vitae

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Education and Professional Experience

since 05/2011	Mixed-signal design engineer Intel Mobile Communications GmbH, München
01/2007-04/2011	Research assistant and Ph.D. student Chair of Integrated Analog Circuits and RF Systems RWTH Aachen University
10/2005-02/2006	Analog design intern Texas Instruments Deutschland GmbH, Freising
10/2000-12/2006	Technische Universität Braunschweig Diplom-Ingenieur
08/2004-08/2005	Georgia Institute of Technology, Atlanta, USA Master of Science
09/1999-06/2000	Military service
06/1999	Gymnasium Martino-Katharineum, Braunschweig Abitur

Honors and Awards

06/2009	IEEE RFIC Symposium 2009 Best Student Paper Award – 2nd place
04/2005	Member Eta Kappa Nu Electrical Engineering Honor Society
08/2004-08/2005	DAAD Scholarship
07/2003	Philips Vordiplompreis

A. List of Publications

Peer-reviewed Journal Papers

1. T.D. Werth, C. Schmits, R. Wunderlich, and S. Heinen. An active feedback interference cancellation technique for blocker filtering in RF receiver front-ends. In *IEEE Journal of Solid-State Circuits*, 45(5):989–997, May 2010.

2. Song-Bok Kim, Tobias D. Werth, S. Joeres, R. Wunderlich, and S. Heinen. Effect of mismatched loop delay in continous-time complex sigma-delta modulators. In *IEEE Transactions on Circuits and Systems II*, 55(10):996–1000, Oct. 2008.

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1. L. Liao, T.D. Werth, S. Kaehlert, R. Wunderlich, and S. Heinen. An integrated voltage-mode PWM controlled buck converter with active compensation. In *IEEE International Conference on Electronics, Circuits, and Systems 2010*, pages 1053 – 1056, December 2010.

2. D. Bormann, S. Kaehlert, T.D. Werth, L. Liao, and S. Heinen. A novel notch filter LNA for use in multi-band, multi-standard cellular receivers. In *IEEE Latin American Symposium on Circuits and Systems 2010*, pages 64 – 67, 2010.

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4. T. D. Werth, S. Kaehlert, and S. Heinen. System design considerations for SAW-less front-ends at the example of GSM DCS1800. In *2010 IEEE International 53rd Midwest Symposium on Circuits and Systems*, pages 648 – 651, August 2010.

5. T.D. Werth, P.-F. de Sordi, and S. Heinen. A quadrature frequency divider with programmable duty-cycle. In *6th Conference on Ph.D. Research in Microelectronics and Electronics (PRIME)*, 2010.

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B. Derivation of I/Q-Mismatch Equations

Subsequently, quadrature path mismatch as discussed in chapter 3.4.3 is derived in detail.

Gain mismatch As pointed out in (3.21) the filter core output subject to gain mismatch can be expressed by

$$y(t) = \int x(\tau) \left[I \cos(\omega_{LO}\tau) \cos(\omega_{LO}t) + Q \sin(\omega_{LO}\tau) \sin(\omega_{LO}t) \right] h(t-\tau)\, d\tau. \tag{B.1}$$

Using the trigonometric identities $\cos\alpha\cos\beta = \frac{1}{2}(\cos(\alpha-\beta)+\cos(\alpha+\beta))$ and $\sin\alpha\sin\beta = \frac{1}{2}(\cos(\alpha-\beta)-\cos(\alpha+\beta))$ (3.21) can be split into an ideal and a mismatch path yielding

$$y(t) = \frac{I+Q}{2} \int x(\tau) \cos(\omega_{LO}(t-\tau)) h(t-\tau)\, d\tau + \frac{I-Q}{2} \int x(\tau) \cos(\omega_{LO}(t+\tau)) h(t-\tau)\, d\tau. \tag{B.2}$$

The second term can be expanded by applying the identity $\cos(\alpha+\beta) = \cos\alpha\cos\beta - \sin\alpha\sin\beta$

$$y(t) = \frac{I+Q}{2} \int x(\tau) \cos(\omega_{LO}(t-\tau)) h(t-\tau)\, d\tau + \frac{I-Q}{2} \int x(\tau) \left[\cos(\omega_{LO}t) \cos(\omega_{LO}\tau) - \sin(\omega_{LO}t) \sin(\omega_{LO}\tau) \right] h(t-\tau)\, d\tau, \tag{B.3}$$

yielding the equivalent block diagram depicted in Fig. 3.7(c).

The spectrum due to the mismatch path is obtained by examining the spectrum along the mismatch path by successively applying the frequency shifting property of the Laplace transform. After the first downconversion and filtering step the

spectrum in the in-phase and quadrature paths are

$$M_{G,I,BB}(s) = \frac{I-Q}{2}\frac{1}{2}\left[X(s-j\omega_{LO}) + X(s+j\omega_{LO})\right]H(s) \quad \text{(B.4)}$$

and

$$M_{G,Q,BB}(s) = \frac{I-Q}{2}\frac{1}{2j}\left[X(s-j\omega_{LO}) - X(s+j\omega_{LO})\right]H(s), \quad \text{(B.5)}$$

respectively. In the upconversion step the frequency shifting property is applied again yielding

$$M_{G,I,RF}(s) = \frac{I-Q}{2}\frac{1}{4}\left[X(s-j2\omega_{LO})H(s-j\omega_{LO}) + X(s)H(s-j\omega_{LO}) + X(s)H(s+j\omega_{LO}) + X(s+j2\omega_{LO})H(s+j\omega_{LO})\right] \quad \text{(B.6)}$$

for the in-phase path and

$$M_{G,Q,RF}(s) = -\frac{I-Q}{2}\frac{1}{4}\left[X(s-j2\omega_{LO})H(s-j\omega_{LO}) - X(s)H(s-j\omega_{LO}) - X(s)H(s+j\omega_{LO}) + X(s+j\omega_{LO})H(s+j\omega_{LO})\right] \quad \text{(B.7)}$$

for the quadrature path. Finally, subtraction of the quadrature path from the in-phase path yields

$$M_G(s) = \frac{I-Q}{2}\cdot\frac{1}{2}\left[X(s-j2\omega_{LO})H(s-j\omega_{LO}) + X(s+j2\omega_{LO})H(s+j\omega_{LO})\right] \quad \text{(B.8)}$$

which is (3.22).

Phase mismatch The filter core output with phase mismatch can be expressed by (3.23) using $\phi_I = +\Delta\phi/2$ and $\phi_Q = -\Delta\phi/2$

$$y(t) = \int x(\tau)\left[\cos(\omega\tau + \Delta\phi/2)\cos(\omega t + \Delta\phi/2) + \sin(\omega\tau - \Delta\phi/2)\sin(\omega t - \Delta\phi/2)\right]h(t-\tau)\,d\tau. \quad \text{(B.9)}$$

Using trigonometric identities the preceding equation is expanded yielding an ideal path and a path due to phase mismatch

$$y(t) = \int x(\tau)\cos(\omega(t-\tau))h(t-\tau)\,d\tau + \int x(\tau)\frac{1}{2}\left[\cos(\omega(t+\tau)+\Delta\phi) - \cos(\omega(t+\tau)-\Delta\phi)\right]h(t-\tau)\,d\tau. \quad \text{(B.10)}$$

The second term representing phase mismatch can also be expressed as

$$m_{Ph}(t) = -\sin\Delta\phi \int x(\tau)\sin(\omega(t+\tau))h(t-\tau)\,d\tau = -\sin\Delta\phi \int x(\tau)\left[\sin(\omega\tau)\cos(\omega t) + \cos(\omega\tau)\sin(\omega t)\right]h(t-\tau)\,d\tau \quad \text{(B.11)}$$

which is depicted in the block diagram of Fig. 3.7(d).

The phase mismatch spectrum is obtained by tracing the spectrum along the two parallel mismatch paths. After the first downconversion and filtering step the spectrum is

$$M_{Ph,1,BB}(s) = -\sin\Delta\phi \cdot \frac{1}{2}\left[X(s-j\omega) + X(s+j\omega)\right]H(s) \quad \text{(B.12)}$$

and

$$M_{Ph,2,BB}(s) = -\sin\Delta\phi \cdot \frac{1}{2j}\left[X(s-j\omega) - X(s+j\omega)\right]H(s), \quad \text{(B.13)}$$

respectively.

After upconversion to RF, the spectrum is

$$M_{Ph,1,RF}(s) = -\sin\Delta\phi\frac{1}{4j}\left[X(s-j2\omega)H(s-j\omega) + X(s)H(s-j\omega) - X(s)H(s+j\omega) - X(s+j2\omega)H(s+j\omega)\right] \quad \text{(B.14)}$$

and

$$M_{Ph,2,RF}(s) = -\sin\Delta\phi\frac{1}{4j}\left[X(s-j2\omega)H(s-j\omega) + X(s)H(s+j\omega) - X(s)H(s-j\omega) - X(s+j2\omega)H(s+j\omega)\right]. \quad \text{(B.15)}$$

Combining both paths yields (3.24)

$$M_{Ph}(s) = \sin\Delta\phi \cdot \frac{j}{2}\left[X(s - j2\omega_{LO})H(s - j\omega_{LO}) - X(s + j2\omega_{LO})H(s + j\omega_{LO})\right]. \quad \text{(B.16)}$$

C. Evaluation Boards

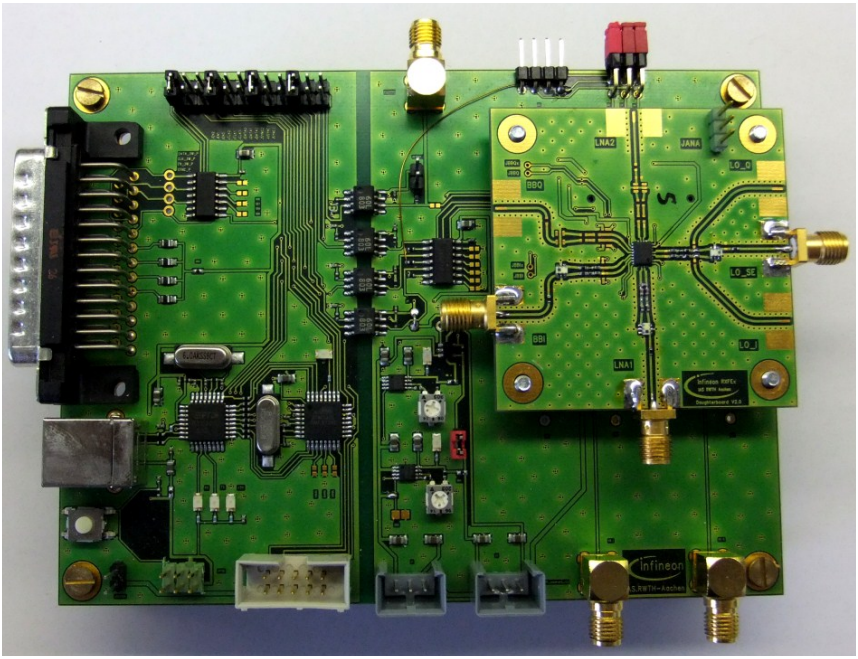


Figure C.1.: Interface board and evaluation board for the first prototype from chapter 4.

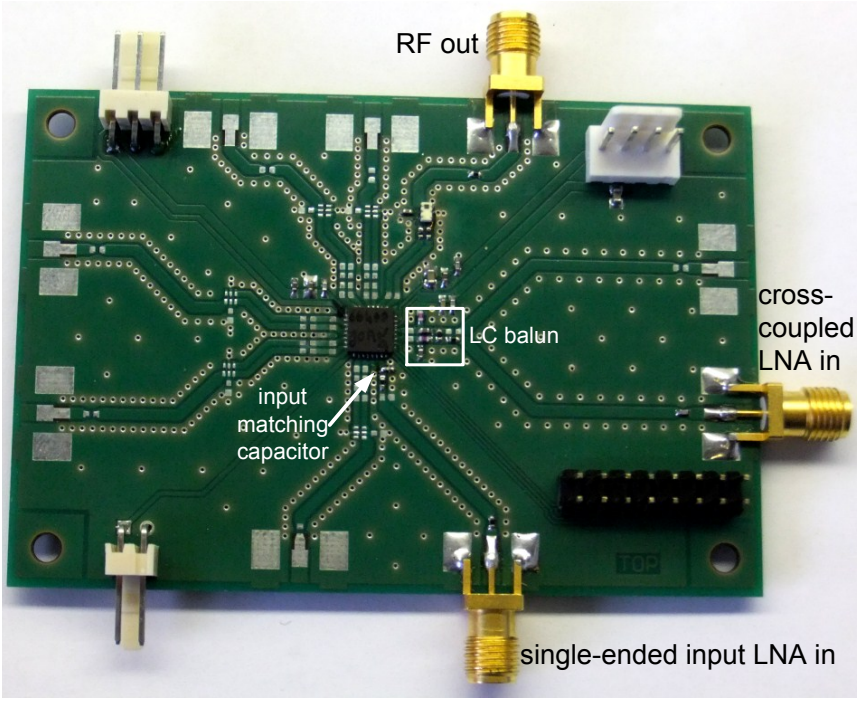


Figure C.2.: Evaluation board used for characterizing the LNAs from chapter 6.1.

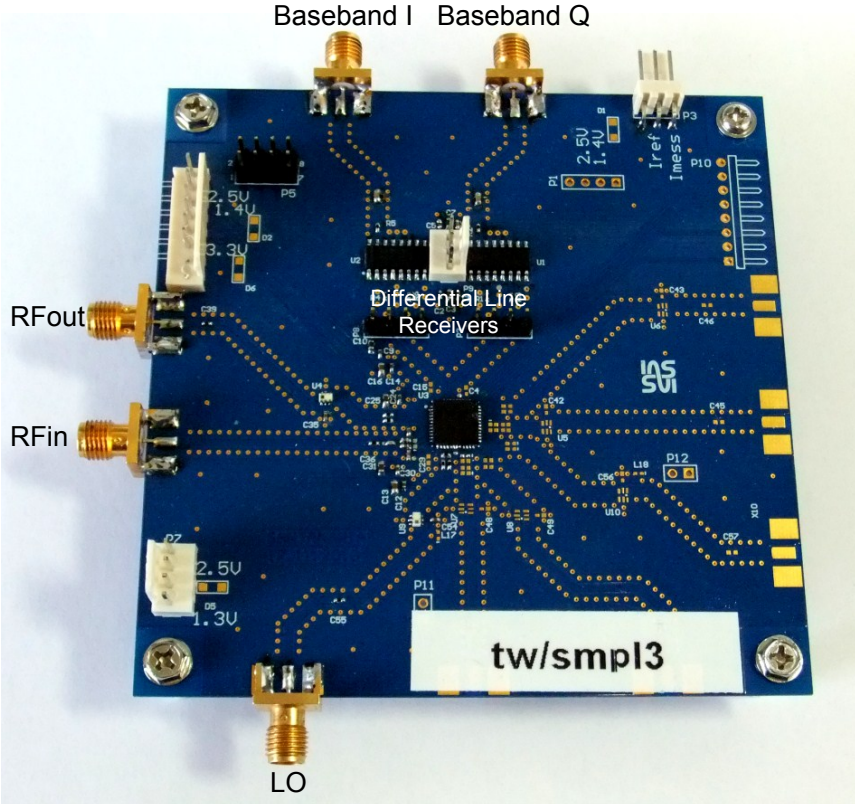
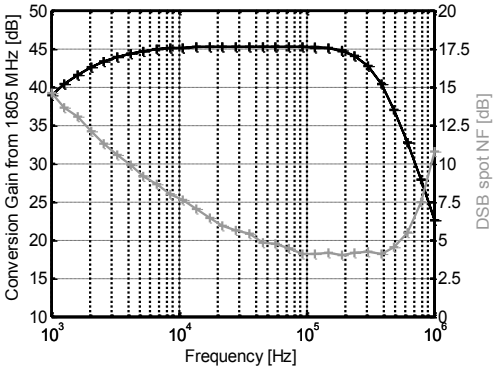


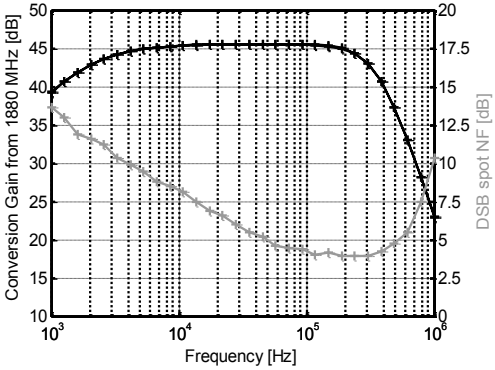
Figure C.3.: Evaluation board for the direct conversion receiver test chip from chapter 6.2.

D. Additional Measurement Results

D.1. Receiver Gain and NF for DCS and PCS bands

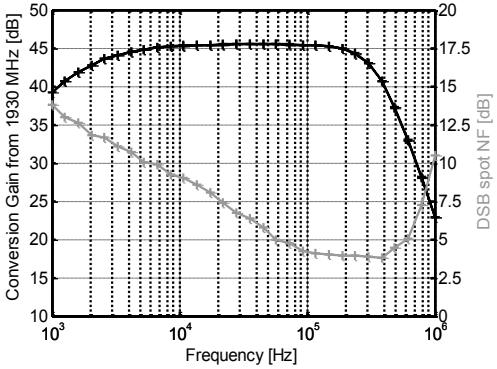


(a)

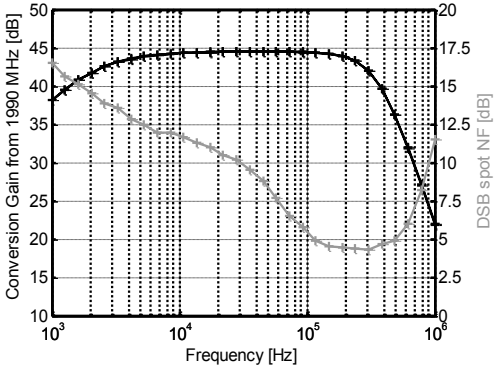


(b)

Figure D.1.: Conversion gain and DSB spot NF for RX path in DCS band.

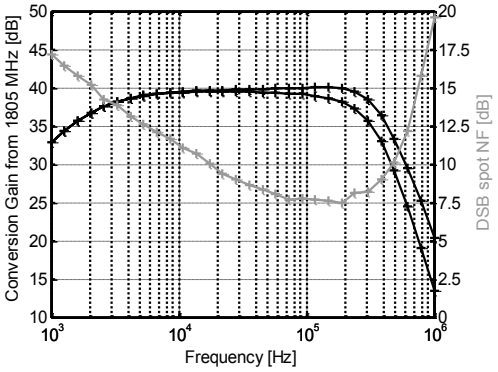


(a)

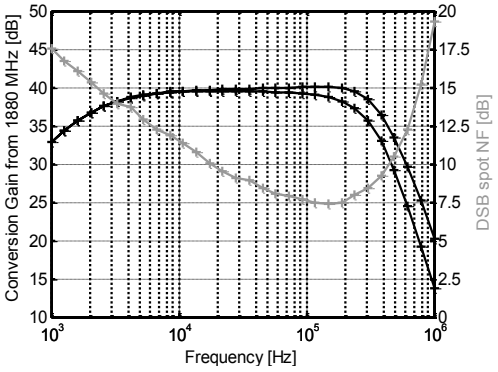


(b)

Figure D.2.: Conversion gain and DSB spot NF for RX path in PCS band.

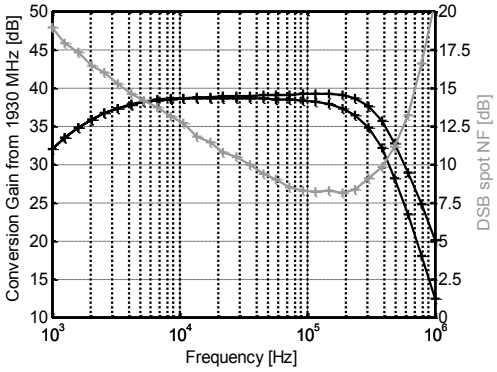


(a)

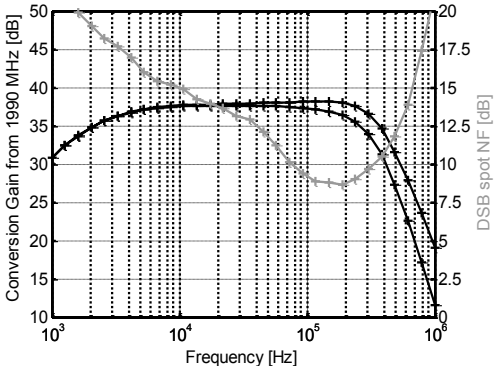


(b)

Figure D.3.: Conversion gain and DSB spot NF for RX path with interference cancellation in DCS band.



(a)



(b)

Figure D.4.: Conversion gain and DSB spot NF for RX path with interference cancellation in PCS band.