A Fixed-Frequency Pulsewidth Modulation Based Quasi-Sliding-Mode Controller for Buck Converters

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***Abstract*—This paper presents the design and analysis of a fixed-frequency pulsewidth modulation (PWM)-based quasi-sliding-mode voltage controller for buck converters from a circuit design perspective. A practical design approach that aims at systematizing the procedure for the selection of the control parameters is presented. In addition, a simple analog form of the controller for practical realization is provided. The resulting controller exhibits the same structure as a PWM proportional derivative (PD) linear controller, but with an additional component consisting of the instantaneous input voltage and the instantaneous output voltage. Simulation and experimental results show that the performance of the converter agrees with the theoretical design.**

***Index Terms*—Buck converter, fixed-frequency, hysteresis-modulation, pulsewidth modulation (PWM), quasi-sliding-mode (QSM), sliding-mode (SM) control.**

I. Introduction

SLIDING-MODE (SM) controllers are well known for their robustness and stability. The nature of the controller is to ideally operate at an infinite switching frequency such that the controlled variables can track a certain reference path to achieve the desired dynamic response and steady-state operation [1]. This requirement for operation at infinite switching frequency, however, challenges the feasibility of applying SM controllers in power converters. This is because extreme high speed switching in power converters results in excessive switching losses, inductor and transformer core losses, and electromagnetic interference (EMI) noise issues [2]. Hence, for SM controllers to be applicable to power converters, their switching frequencies must be constricted within a practical range. Nevertheless, this constriction of the SM controller's switching frequency transforms the controller into a type of quasi-sliding-mode (QSM) controller, which operates as an approximation of the ideal SM controller. The consequence of this transformation is the reduction of the system's robustness. Clearly, the proximity of QSM to the ideal SM controller will be closer as switching frequency tends toward infinity. Since all SM controllers in practical power converters are frequency-limited, they are, strictly speaking, QSM controllers. For brevity and consistency with previous publications, the term SM controller will be used in the sequel.

A review of the literature shows that most of these previously proposed SM controllers for switching power converters are hysteresis-modulation (HM) (or delta-modulation) based [3]–[8], that is, they require a bang–bang type of controller to perform the switching control. Naturally, they inherit the typical disadvantages of having variable switching frequency operation and being highly control-sensitive to noise. Possible solutions include the use of constant timer circuits into the hysteretic SM controller to ensure constant switching frequency operation [7], or the use of an adaptive hysteresis band that varies with parameter changes to control and fixate the switching frequency [8]. However, these solutions require additional components and are less suited for low cost voltage conversion applications.

An alternative solution to this is to change the modulation method of the SM controllers from HM to pulsewidth modulation (PWM), otherwise known as the duty cycle control. The technique of PWM modulation is to compare a desired analogue control signal V_c with a ramp signal, of which a pulse-like output switching signal having the same frequency as the ramp signal, will be generated [9]. The advantage is that by fixing the frequency of the ramp, the frequency of the output switching signal will be constant, regardless of how the duty cycle varies with the variation of the control signal. Thus, by employing this modulation technique in SM control, a fixed-frequency PWM-based SM controller can be obtained. Meanwhile, it should be stressed that the application of the PWM technique to SM control does not contradict the concept of classical PWM controllers used in power electronics. Both differ in the way in which their control signals V_c are formulated. SM controllers are based on the SM control law and classical PWM controllers are based on linear control law. Hence, from here on, the term PWM-based SM controller essentially refers to a pulsewidth modulator that employs an equivalent control (derived by applying the SM control technique) to generate a control signal to be compared with the fixed-frequency ramp in the modulator.

To achieve such a controller, a relationship between SM control and duty cycle control is required. The idea can be rooted back to one of the earliest papers on SM controlled power converters [3], which suggests that under SM control operation, the control signal of equivalent control approach u_{eq} in SM control is equivalent to the duty cycle control signal d of a PWM controller. However, this assumption was stated without any theoretical verification in the paper. It was some time later when Sira-Ramirez *et al.* [10] proposed a geometric framework to map the PWM feedback control onto SM control that the proof was rigourously shown in a companion paper [11]. It has been shown that as the switching frequency tends toward infinity, the averaged dynamics of an SM controlled system is equivalent to

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the averaged dynamics of a PWM controlled system, thus establishing the relationship $u_{\rm eq} = d$. On the other hand, the same correlation was derived in Martinez *et al.* [12], where the nonlinear PWM continuous control was compared with an equivalent control. In their method, an average representation of the converter model was employed. Hence, the migration of a SM controller from being HM-based to PWM-based is made possible. Unfortunately, the theory was not exploited to initiate the development of such controllers.

The first useful clue to how PWM techniques can be applied to SM control to develop fixed-frequency SM controllers is probably due to Nguyen and Lee [13], who provided a clear direction as to how such controllers may be implemented. In two other related papers [14], [15] the state space averaging technique is incorporated into the controller's modeling. By doing so, PWM duty cycle control can be directly applied to the implementation of SM controllers. However, while these papers provided encouraging evidence on the feasibility of developing such SM controllers, they failed to study the technical aspects of the implementation, which is equally important for engineering practices. For a deeper understanding of the topic, interested readers may refer to [3], [10], [11], and [13]–[15].

Hence, it may be concluded that even though the previous research on the topic provided important concepts and fundamentals for the potential implementation of such controllers, they lack practicality and concrete description on how such controllers can be developed. Consequently, circuit solutions and issues related to their practical realization have never been formally addressed.

In this paper, we present the design of a fixed-frequency PWM-based SM voltage controlled (SMVC) buck converter, with emphasis on its practical and implementation details, from a circuit design perspective, using the theoretical groundwork established in [10], [11], and [13]. In contrast to [13], the design of this controller at circuit level involves a different set of engineering considerations. Additionally, we introduce a practical approach to the design and selection of the sliding coefficients of the controller. This approach, which is based on Ackermann's Formula [16], permits the control design to be carried out systematically. It should be noted that it can also be employed for the design of other PWM-based SM power converters. Finally, an analog form of the controller that is suitable for practical realization is provided. This controller can be easily implemented from the derived mathematical expressions with only a few operational amplifiers and analog ICs. Simulations and experiments are performed on the proposed converter to validate the theoretical design.

II. Theoretical Derivation

This section covers the theoretical aspects of the SMVC converter. Complete mathematical derivations for the controller's design are presented. A practical method of designing the sliding coefficients is also introduced. Since the fixed-frequency PWM-based controller is a translated form of the HM-based controller, the model for the latter must first be derived. Therefore, the discussion in this section is valid for both the PWM and HM-based controllers.

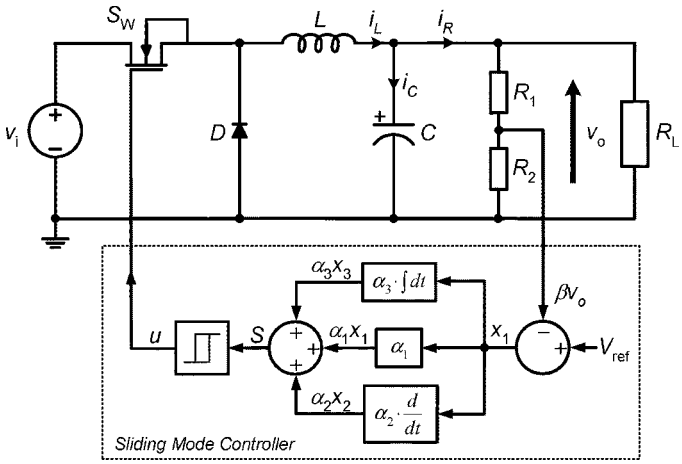


Fig. 1. Basic structure of a typical HM-based SMVC buck converter system.

A. Mathematical Model of an Ideal SM PID Voltage Controlled Buck Converter

The SM voltage controller used in this work employs a second-order PID type of control. This is different from most previously proposed SM voltage controller for buck converters which use the phase canonic form that involves only the voltage error x and its first-order derivative $\dot{x}$ as the state variables for control [7], [8], [13], [17], [19]. The additional voltage error integral term $\int x$ is included as a state variable of the controller to reduce the steady-state error of the system, since the equivalent control will be used to generate the control signal. Additionally, we have also assumed our SM to operate at a high frequency making it a close proximity to the ideal SM controller.

Fig. 1 shows a typical HM-based SMVC buck converter. Here, the voltage error x_1, the voltage error dynamics (or the rate of change of voltage error) x_2, and the integral of voltage error x_3, under continuous conduction mode (CCM) operation, can be expressed as

$$\begin{aligned} x_1 &= \mathrm{V_{ref}} - \beta \mathrm{V_o} \\ x_2 &= \dot{x_1} = \frac{\beta}{C}\left(\frac{\mathrm{V_o}}{R_\mathrm{L}} - \int \frac{u\mathrm{V_i} - \mathrm{V_o}}{L} dt\right) \\ x_3 &= \int x_1 dt \end{aligned} \tag{1}$$

where C, L, and R_L are the capacitance, inductance, and load resistance, respectively; $\mathrm{V_{ref}}$, $\mathrm{V_i}$, and $\beta \mathrm{V_o}$ are the reference, input, and sensed output voltage, respectively; and $u = 1$ or 0 is the switching state of power switch S_W. Then, the state space model of the system can be derived as

$$\dot{\boldsymbol{x}} = \boldsymbol{A}\boldsymbol{x} + \boldsymbol{B}u + \boldsymbol{D} \tag{2}$$

where

$$\boldsymbol{A} = \begin{bmatrix} 0 & 1 & 0 \\ -\frac{1}{LC} & -\frac{1}{R_\mathrm{L}C} & 0 \\ 1 & 0 & 0 \end{bmatrix}, \quad \boldsymbol{B} = \begin{bmatrix} 0 \\ -\frac{\beta \mathrm{V_i}}{LC} \\ 0 \end{bmatrix}$$

$$\boldsymbol{D} = \begin{bmatrix} 0 \\ \frac{\mathrm{V_{ref}}}{LC} \\ 0 \end{bmatrix}, \quad \text{and} \quad \boldsymbol{x} = \begin{bmatrix} x_1 \\ x_2 \\ x_3 \end{bmatrix}.$$

The basic idea of SM control is to design a certain sliding surface in its control law that will direct the trajectory of the state variables toward a desired origin when coincided. For our system's model, it is appropriate to have a control law, which is based on satisfying the hitting condition[1] [17], to adopt a switching function such as

$$u = \frac{1}{2}(1 + \text{ sign}(S)) \tag{3}$$

where S is the instantaneous state variable's trajectory, and is described as

$$S = \alpha_1 x_1 + \alpha_2 x_2 + \alpha_3 x_3 = \boldsymbol{J}^{\mathrm{T}} \boldsymbol{x} \tag{4}$$

with $\boldsymbol{J}^{\mathrm{T}} = [\alpha_1 \ \alpha_2 \ \alpha_3]$ and α_1, α_2, and α_3 representing the control parameters termed as sliding coefficients. By enforcing $S = 0$, a sliding surface (plane) can be obtained. The graphical representation of the sliding plane in three-dimensional (3-D) space is illustrated in Fig. 2.

A detailed discussion of the SM control principle can be found in [1]. In brief, the entire SM control process can be divided into two phases. In the first phase, regardless of the starting position, the controller will perform a control decision that will drive the trajectory of the state variables to converge to the sliding surface [see Fig. 3(a)]. When the trajectory is within a small vicinity of the sliding surface, it is said to be in SM operation, which is the second phase of the control process. The controller will give a series of control actions via switching, such that the trajectory is maintained within a small vicinity of the sliding surface, and is concurrently directed toward the desired reference at origin O [see Fig. 3(b)]. In other words, the SM controller is performing its control decision by utilizing the sliding plane as a reference path, on which the trajectory will track and eventually converge to the origin to achieve steady-state operation. Hence, when the system enters into SM operation, its equivalent trajectory can be ideally described as $S = 0$.

It is worth mentioning that the realization of the aforementioned SM operation can easily be achieved by imposing control equations (3) and (4) into a controller. The main difficulty, however, lies on the design and selection of the control parameters (sliding coefficients). It is important to note that such issues have been well addressed in the area of SM control [16]. Here, we aim to present a more coherent design and selection approach in the context of power electronics.

B. Existence Condition in Circuit Terms

As in all other SM control schemes, the determination of the ranges of employable sliding coefficients for the SMVC converter must go through the process of analyzing the existence condition[2] of the controller/converter system using the

[1]Satisfaction of the hitting condition assures that regardless of the initial condition, the state trajectory of the system will always be directed toward the sliding surface.

[2]Satisfaction of the existence condition ensures that the state trajectory at locations near the sliding surface will always be directed toward the sliding surface.

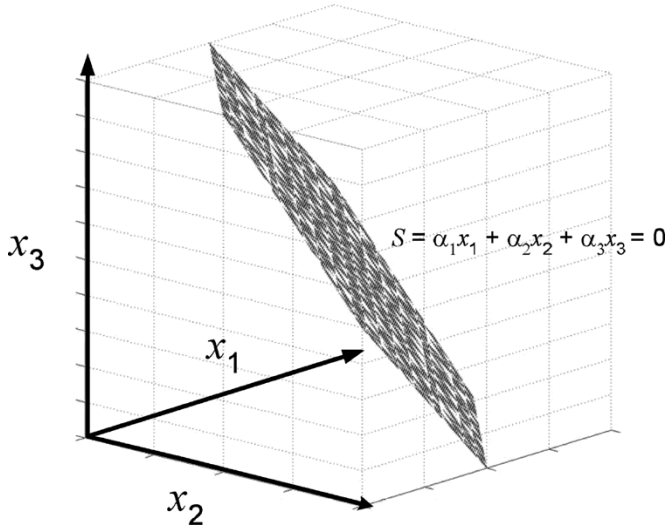
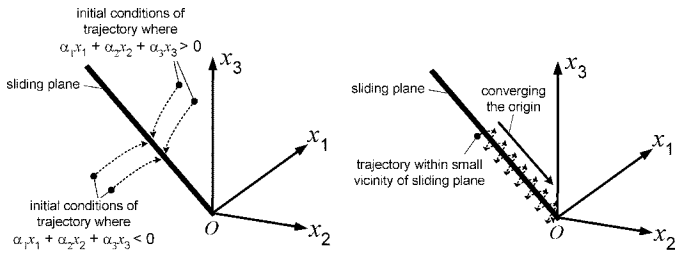


Fig. 2. Graphical representation of the sliding plane in 3-D space.



(a) Phase 1 (b) Phase 2

Fig. 3. Graphical representations of state variables' trajectory's behavior in SM control process: (a) Phase 1—illustrating trajectory converging the sliding plane irrespective of its initial condition and (b) Phase 2—illustrating trajectory being maintained within a small vicinity from the sliding plane, and concurrently being directed to converge to the origin O.

Lyapunov's direct method [18]. This is performed by first combining (2), (3), and the time derivative of (4) to give

$$\dot{S} = \boldsymbol{J}^{\mathrm{T}} \boldsymbol{A} \boldsymbol{x} + \frac{1}{2} \boldsymbol{J}^{\mathrm{T}} \boldsymbol{B} + \frac{1}{2} \boldsymbol{J}^{\mathrm{T}} \boldsymbol{B} \text{ sign}(S) + \boldsymbol{J}^{\mathrm{T}} \boldsymbol{D}. \tag{5}$$

Multiplying (5) by (4) gives

$$\begin{aligned} S\dot{S} &= S\left[\boldsymbol{J}^{\mathrm{T}} \boldsymbol{A} \boldsymbol{x} + \frac{1}{2} \boldsymbol{J}^{\mathrm{T}} \boldsymbol{B} + \frac{1}{2} \boldsymbol{J}^{\mathrm{T}} \boldsymbol{B} \text{ sign}(S) + \boldsymbol{J}^{\mathrm{T}} \boldsymbol{D}\right] \\ &= S\left(\boldsymbol{J}^{\mathrm{T}} \boldsymbol{A} \boldsymbol{x} + \frac{1}{2} \boldsymbol{J}^{\mathrm{T}} \boldsymbol{B} + \boldsymbol{J}^{\mathrm{T}} \boldsymbol{D}\right) + \frac{1}{2} |S| \boldsymbol{J}^{\mathrm{T}} \boldsymbol{B}. \end{aligned} \tag{6}$$

To achieve local reachability, (6) is evaluated as

$$\lim_{S \to 0} S \cdot \dot{S} < 0 \tag{7}$$

which can be written as

$$\begin{cases} \dot{S}_{S \to 0^+} = \boldsymbol{J}^{\mathrm{T}} \boldsymbol{A} \boldsymbol{x} + \boldsymbol{J}^{\mathrm{T}} \boldsymbol{B} + \boldsymbol{J}^{\mathrm{T}} \boldsymbol{D} < 0 \\ \dot{S}_{S \to 0^-} = \boldsymbol{J}^{\mathrm{T}} \boldsymbol{A} \boldsymbol{x} + \boldsymbol{J}^{\mathrm{T}} \boldsymbol{D} > 0 \end{cases} \tag{8}$$

i.e.,

$$\boldsymbol{J}^{\mathrm{T}} \boldsymbol{A} \boldsymbol{x} + \boldsymbol{J}^{\mathrm{T}} \boldsymbol{B} + \boldsymbol{J}^{\mathrm{T}} \boldsymbol{D} < 0 < \boldsymbol{J}^{\mathrm{T}} \boldsymbol{A} \boldsymbol{x} + \boldsymbol{J}^{\mathrm{T}} \boldsymbol{D} \tag{9}$$

or rearranged in scalar representation

$$0 < LC\frac{\alpha_3}{\alpha_2}(\mathrm{V_{ref}}-\beta\mathrm{V_o})-\beta L\left(\frac{\alpha_1}{\alpha_2}-\frac{1}{R_\mathrm{L}C}\right)i_C+\beta\mathrm{V_o} < \beta\mathrm{V_i}. \tag{10}$$

The above inequalities give the conditions for existence and therefore provide a range of employable sliding coefficients that will ensure that the converter stays in SM operation when its state trajectory is near the sliding surface. However, other than the existence of SM, no information relating the sliding coefficients to the converter performance can be derived.

C. Existence Condition With Design Parameters Consideration

To alleviate the above problem, we propose to first tighten the design constraints by absorbing the actual operating parameters into the inequality. This is done by decomposing (10) into two inequalities and considering them as individual cases with respect to the polarity of the capacitor current flow. Since in practice $(\alpha_1/\alpha_2) > (1/R_\mathrm{L}C)$, the left inequality of (10) is implied by

$$0 < LC\frac{\alpha_3}{\alpha_2}(\mathrm{V_{ref}}-\beta\mathrm{V_o})-\beta L\left(\frac{\alpha_1}{\alpha_2}-\frac{1}{R_\mathrm{L}C}\right)|\hat{i_C}|+\beta\mathrm{V_o} \tag{11}$$

which can be rearranged to give

$$\frac{\alpha_1}{\alpha_2} < \frac{\beta\mathrm{V_o}+LC\frac{\alpha_3}{\alpha_2}(\mathrm{V_{ref}}-\beta\mathrm{V_o})}{\beta L|\hat{i_C}|}+\frac{1}{R_\mathrm{L}C} \tag{12}$$

and the right inequality of (10) is implied by

$$LC\frac{\alpha_3}{\alpha_2}(\mathrm{V_{ref}}-\beta\mathrm{V_o})+\beta L\left(\frac{\alpha_1}{\alpha_2}-\frac{1}{R_\mathrm{L}C}\right)|\hat{i_C}|+\beta\mathrm{V_o} < \beta\mathrm{V_i} \tag{13}$$

which can be rearranged to give

$$\frac{\alpha_1}{\alpha_2} < \frac{\beta\mathrm{V_i}}{\beta L|\hat{i_C}|}-\frac{\beta\mathrm{V_o}+LC\frac{\alpha_3}{\alpha_2}(\mathrm{V_{ref}}-\beta\mathrm{V_o})}{\beta L|\hat{i_C}|}+\frac{1}{R_\mathrm{L}C} \tag{14}$$

where $\hat{i_C}$ is the peak magnitude of the bidirectional capacitor current flow. Next, (12) and (14) can be recombined and further tightened by considering the range of input and loading conditions of the converter to give

$$\begin{aligned}
&\frac{\alpha_1}{\alpha_2} < \frac{\mathrm{V_o}+LC\frac{\alpha_3}{\alpha_2}\left(\frac{\mathrm{V_{ref}}}{\beta}-\mathrm{V_o}\right)}{L|\hat{i_C}|}+\frac{1}{R_{\mathrm{L(max)}}C} \quad \text{for}\\
&\mathrm{V_{i(min)}} \geq 2\left[\mathrm{V_o}+LC\frac{\alpha_3}{\alpha_2}\left(\frac{\mathrm{V_{ref}}}{\beta}-\mathrm{V_o}\right)\right]\\
&\frac{\alpha_1}{\alpha_2} < \frac{\mathrm{V_{i(min)}}}{L|\hat{i_C}|}-\frac{\mathrm{V_o}+LC\frac{\alpha_3}{\alpha_2}\left(\frac{\mathrm{V_{ref}}}{\beta}-\mathrm{V_o}\right)}{L|\hat{i_C}|}\\
&\qquad +\frac{1}{R_{\mathrm{L(max)}}C} \quad \text{for}\\
&\mathrm{V_{i(min)}} < 2\left[\mathrm{V_o}+LC\frac{\alpha_3}{\alpha_2}\left(\frac{\mathrm{V_{ref}}}{\beta}-\mathrm{V_o}\right)\right]
\end{aligned} \tag{15}$$

where $R_{\mathrm{L(max)}}$ is the maximum load resistance and $\mathrm{V_{i(min)}}$ is the minimum input voltage, which the converter is designed for. Additionally, the peak capacitor current $|\hat{i_C}|$ is the maximum inductor current ripple during steady-state operation.

Theoretically, one may assume that at steady-state operation, the actual output voltage $\mathrm{V_o}$ is ideally a pure dc waveform whose magnitude is equal to the desired output voltage $\mathrm{V_{od}} \equiv \mathrm{V_{ref}}/\beta$. However, this is not true in practice. Due to the limitation of finite switching frequency and imperfect feedback loop, there will always be some steady-state dc error between $\mathrm{V_o}$ and $\mathrm{V_{od}}$, even with the error-reducing integral controllers (i.e., PI, PID). It is important to take this error into consideration for the design of the controller since the factor $LC(\alpha_3/\alpha_2)((\mathrm{V_{ref}}/\beta)-\mathrm{V_o})$ is relatively large in comparison to $\mathrm{V_o}$.

Now, considering that

a) in controllers with integral control function, the difference between $\mathrm{V_o}$ and $\mathrm{V_{od}}$ is small, and when optimally designed, is normally limited to a range of within $\pm$ 5% of $\mathrm{V_{od}}$;[3]

and in our particular controller arrangement where voltage error is denoted as $\mathrm{V_{ref}}-\beta\mathrm{V_o}$

b) the dc average of $\mathrm{V_o}$ is always lower than $\mathrm{V_{od}}$ for PWM-based SMVC converters (as shown in the results later in the paper);
c) the dc average of $\mathrm{V_o}$ is always higher than $\mathrm{V_{od}}$ for HM-based SMVC converters (as illustrated from the results in [19]); and
d) the term $LC(\alpha_3/\alpha_2)$ is always positive;

we can rewrite the existence condition (15) for PWM-based SMVC converter as

$$\begin{aligned}
&\frac{\alpha_1}{\alpha_2} < \frac{0.95\ \mathrm{V_{od}}}{L|\hat{i_C}|}+\frac{1}{R_{\mathrm{L(max)}}C} \quad \text{for}\\
&\mathrm{V_{i(min)}} \geq \left(1.95+0.05\ LC\frac{\alpha_3}{\alpha_2}\right)\mathrm{V_{od}}\\
&\frac{\alpha_1}{\alpha_2} < \frac{\mathrm{V_{i(min)}}}{L|\hat{i_C}|}-\frac{\left(1+0.05\ LC\frac{\alpha_3}{\alpha_2}\right)\mathrm{V_{od}}}{L|\hat{i_C}|}\\
&\qquad +\frac{1}{R_{\mathrm{L(max)}}C} \quad \text{for}\\
&\mathrm{V_{i(min)}} < \left(1.95+0.05\ LC\frac{\alpha_3}{\alpha_2}\right)\mathrm{V_{od}}
\end{aligned} \tag{16}$$

by substituting $\mathrm{V_o} = 0.95\ \mathrm{V_{od}}$ or $\mathrm{V_o} = \mathrm{V_{od}}$ into the appropriate parts. For HM-based SMVC converter, the existence condition can be expressed as

$$\begin{aligned}
&\frac{\alpha_1}{\alpha_2} < \frac{\left(1-0.05\ LC\frac{\alpha_3}{\alpha_2}\right)\mathrm{V_{od}}}{L|\hat{i_C}|}+\frac{1}{R_{\mathrm{L(max)}}C} \quad \text{for}\\
&\mathrm{V_{i(min)}} \geq \left(2.05-0.05\ LC\frac{\alpha_3}{\alpha_2}\right)\mathrm{V_{od}}\\
&\frac{\alpha_1}{\alpha_2} < \frac{\mathrm{V_{i(min)}}-1.05\ \mathrm{V_{od}}}{L|\hat{i_C}|}+\frac{1}{R_{\mathrm{L(max)}}C} \quad \text{for}\\
&\mathrm{V_{i(min)}} < \left(2.05-0.05\ LC\frac{\alpha_3}{\alpha_2}\right)\mathrm{V_{od}}
\end{aligned} \tag{17}$$

[3]This is a conservative value to be adopted for output voltage accuracy. Many switching regulators available have errors of less than $\pm$ 1%.

by substituting $V_o = 1.05\ V_{od}$ or $V_o = V_{od}$ into the appropriate parts. Thus, the control parameters α_1, α_2, and α_3 are now bounded by inequalities that have more stringent constraints than in (10).

D. Selection of Sliding Coefficients

Clearly, inequalities (16) and (17) provide only the general information for the existence of SM, but give no details on the selection of the parameters. For this purpose, we employ the Ackermann's Formula for designing static controllers [16]. This is basically the selection of sliding coefficients based on the desired dynamic properties. In this way, by designing the SM controller/converter system to respond to our intention, the stability condition[4] of the system is therefore satisfied.

In our example, the equation relating sliding coefficients to the dynamic response of the converter during SM operation (i.e., Phase 2 of the control process) can be easily found by substituting $S = 0$ into (4), i.e.,

$$\alpha_1 x_1 + \alpha_2 \frac{dx_1}{dt} + \alpha_3 \int x_1 dt = 0. \tag{18}$$

Rearranging the time differentiation of (18) into a standard second-order system form, we have

$$\frac{d^2x_1}{dt^2} + 2\zeta\omega_n \frac{dx_1}{dt} + \omega_n^2 x_1 = 0 \tag{19}$$

where $\omega_n = \sqrt{(\alpha_3/\alpha_2)}$ is the undamped natural frequency and $\zeta = (\alpha_1/2\sqrt{\alpha_2\alpha_3})$ is the damping ratio. Recall that there are three possible types of response in a linear second-order system: under-damped ($0 \le \zeta < 1$), critically-damped ($\zeta = 1$), and over-damped ($\zeta > 1$). For ease of discussion, we choose to design the controller for critically-damped response,[5] i.e.,

$$x_1(t) = (A_1 + A_2 t)e^{-\omega_n t}, \quad \text{for } t \ge 0 \tag{20}$$

where A_1 and A_2 are determined by the initial conditions of the system. In a critically-damped system, the bandwidth of the controller's response f_{BW} is

$$f_{BW} = \frac{\omega_n}{2\pi} = \frac{1}{2\pi}\sqrt{\frac{\alpha_3}{\alpha_2}}. \tag{21}$$

By rearranging (21) and substituting $\zeta = 1$ into the damping ratio, the following design equations are obtained:

$$\frac{\alpha_1}{\alpha_2} = 4\pi f_{BW} \quad \text{and} \quad \frac{\alpha_3}{\alpha_2} = 4\pi^2 f_{BW}^2. \tag{22}$$

Thus, the design of the sliding coefficients is now dependent on the bandwidth of the desired frequency response in conjunction with the existence condition (17) for HM-based controllers or (16) for PWM-based controllers. It is worth mentioning that the design equations in (22) for the SMVC controller are applicable to all other types of second-order converters.

[4]Satisfaction of the stability condition ensures that the state trajectory of the system under SM operation will always reach a stable equilibrium point.

[5]The design for an under-damped controller can be performed using a similar procedure as discussed hereafter.

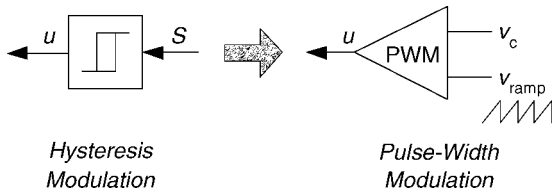


Fig. 4. Simplified hysteresis modulation (HM) and PWM structure.

III. Implementation of PWM Based SMVC Buck Converter

This section details the implementation of PWM-based SMVC buck converter.

A. Derivation of PWM-Based SM Control Law

The migration of the modulation technique in SM control from HM to PWM (see Fig. 4) requires the relationship of the two control technique to be established. This is possible by first considering the two theorems. First, in SM control, the discrete control input (gate signal) u can be theoretically replaced by a smooth function known as the equivalent control signal u_{eq} [1]. Second, at a high switching frequency, the equivalent control is effectively a duty cycle control [11]. Since a duty cycle is basically also a smooth analytic function of the discrete control pulses in PWM, we can obtain a PWM-based SM control system by mapping the equivalent control function onto the duty cycle function of the pulsewidth modulator.

1) Equivalent Control: From [1], the equivalent control signal u_{eq} can be formulated using the invariance conditions by setting the time differentiation of (4) as $\dot{S} = 0$, i.e.,

$$\boldsymbol{J}^T \boldsymbol{A}\boldsymbol{x} + \boldsymbol{J}^T \boldsymbol{B} u_{eq} + \boldsymbol{J}^T \boldsymbol{D} = 0. \tag{23}$$

Now, solving for equivalent control function yields

$$\begin{aligned} u_{eq} &= [\boldsymbol{J}^T \boldsymbol{B}]^{-1} \boldsymbol{J}^T [\boldsymbol{A}\boldsymbol{x} + \boldsymbol{D}] \\ &= \frac{LC}{\beta V_i}\left(\frac{\alpha_1}{\alpha_2} - \frac{1}{R_L C}\right) x_2 + \frac{V_o}{V_i} + \frac{\alpha_3 LC}{\alpha_2 \beta V_i} x_1 \end{aligned} \tag{24}$$

where u_{eq} is continuous and $0 < u_{eq} < 1$. Substituting (24) into the inequality and multiplying by βV_i gives

$$\begin{aligned} 0 &< {u_{eq}}^* \\ &= \beta L\left(\frac{1}{R_L C} - \frac{\alpha_1}{\alpha_2}\right) i_C + \beta V_o + \frac{\alpha_3}{\alpha_2} LC(V_{ref} - \beta V_o) \\ &< \beta V_i \end{aligned} \tag{25}$$

which will provide the ideal average sliding motion on the manifold $S = 0$.

2) Duty Cycle Control: In terms of PWM-based controlled system, the instantaneous duty cycle d is expressed as

$$d = \frac{V_c}{\hat{v}_{ramp}} \tag{26}$$

where V_c is the control signal to the pulsewidth modulator and $\hat{v}_{ramp}$ is the peak magnitude of the constant frequency ramp

signal. Since d is also continuous and bounded by $0 < d < 1$, it may also be written in the form

$$0 < \mathrm{V_c} < \hat{v}_{\mathrm{ramp}}. \tag{27}$$

3) Comparing Equivalent Control and Duty Cycle Control: Comparing the equivalent control and the duty ratio control [11], the following relationships can be established:

$$\mathrm{V_c} = u_{\mathrm{eq}}^{*} = \beta L\left(\frac{1}{R_{\mathrm{L}}C} - \frac{\alpha_1}{\alpha_2}\right) i_C + \beta \mathrm{V_o} + \frac{\alpha_3}{\alpha_2} LC(\mathrm{V_{ref}} - \beta \mathrm{V_o}) \tag{28}$$

and

$$\hat{v}_{\mathrm{ramp}} = \beta \mathrm{V_i} \tag{29}$$

for the practical implementation of PWM-based SMVC controller.

A close inspection of (28) reveals that the control signal $\mathrm{V_c}$ is actually load dependent. Thus, for the controller to be regulation-robust to load changes for a particular switching frequency, the instantaneous value of R_{L} should be fed back. However, this would require additional sensors and cumbersome computations, which complicate the controller. On the other hand, the dependence and sensitivity of $\mathrm{V_c}$ on the load can be minimized by a proper design of α_1, α_2, and α_3 such that $(\alpha_1/\alpha_2) \gg (1/R_{\mathrm{L}}C)$. In such circumstance, the design value of load resistance can be made a constant parameter $R_{\mathrm{L(nom)}}$. If this is adopted, the real system's dynamics at SM operation will be changed from being ideal

$$\frac{d^2x_1}{dt^2} + \frac{\alpha_1}{\alpha_2} \cdot \frac{dx_1}{dt} + \frac{\alpha_3}{\alpha_2} \cdot x_1 = 0 \tag{30}$$

to the actual case of

$$\frac{d^2x_1}{dt^2} + \left(\frac{\alpha_1}{\alpha_2} + \frac{1}{r_{\mathrm{L}}(t)C} - \frac{1}{R_{\mathrm{L(nom)}}(t)C}\right) \cdot \frac{dx_1}{dt} + \frac{\alpha_3}{\alpha_2} \cdot x_1 = 0 \tag{31}$$

where $r_{\mathrm{L}}(t) \neq R_{\mathrm{L(nom)}}$ is the instantaneous load resistance, when the load differs the design value.

As for (29), it can be seen that the line-regulation robustness can be maintained by varying the peak magnitude of the ramp signal with the input voltage. The implementation of this condition can be easily achieved with simple circuitries.

Finally, it should also be noted that this controller is not of absolute robustness to line and load variations. Its robustness improves with switching frequency. Full robustness of any controller can only be achieved when switching frequency is infinite.

B. Implementation of Controller

Fig. 5 shows the schematic diagram of the proposed PWM-based SMVC buck converter. The controller design is based on (28) and (29). Careful examination of the circuit also reveals that it basically adopts the same structure as the PWM proportional derivative (PD) linear control, but with an additional component consisting of the instantaneous input voltage $\beta \mathrm{V_i}$ and the instantaneous output voltage $\beta \mathrm{V_o}$. This is the only component contributing to the nonlinearity of the feedback control. It

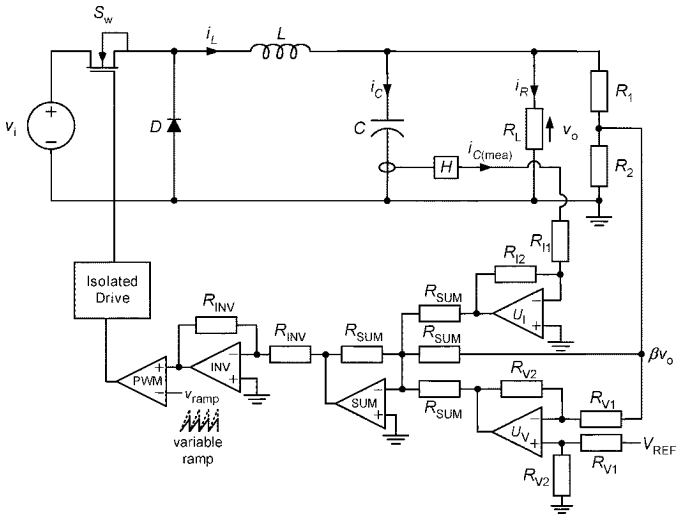


Fig. 5. Schematic diagram of the proposed PWM-based SMVC buck converter.

should also be noted that the integral term of the control variable x_3 is implicitly hidden in the control variable $\mathrm{V_o}$. In case of large disturbance, this component is highly influential in the control. However, when the steady state is reached, $\mathrm{V_o}$ actually becomes a fixed point, thereby destroying the integral control. The equation then transpires to the PWM PD linear controller form.

Interestingly, the PWM-based SM controller also inherits the adaptive feed-forward voltage control property of classical PWM voltage mode control in its operation since the modulation signal $\mathrm{V_{ramp}}$ is a constant frequency ramp with variable peak magnitude proportional to the input voltage $\mathrm{V_i}$ [refer to (29)]. As mentioned, this is in fact the main design feature keeping the line regulation robustness of this controller with respect to input voltage variations.

Briefly, the design of this controller can be summarized as follows: selection of the desired frequency response's bandwidth, calculation of the corresponding sliding coefficients using (22); inspection of the sliding coefficients's appropriateness using existence condition (16); and formulation of the control equations by substituting the calculated parameters into (28) and (29). For a detailed design procedure, refer to Appendix I.

IV. Simulation and Experimental Results

The proposed design approach and analog controller for the PWM-based SMVC buck converter are verified through simulations[6] and experiments. The specification of the converter is given in Table I. The converter is designed to operate in continuous conduction mode for $\mathrm{V_i} = 16$ V to 30 V and $i_R = 0.5$ A to 4 A. The calculated critical inductance is $L_{\mathrm{crit}} = 36\ \mu$H. The minimum required capacitance is $C_{\mathrm{min}} = 9\ \mu$F. The maximum allowable peak-to-peak ripple voltage is 50 mV.

To study the compliance of the design equations with the performance and their relationships with the transient

[6]The simulation is performed using Matlab/Simulink. The step size taken for all simulations is 10 ns.

TABLE I
SPECIFICATION OF BUCK CONVERTER

Description	Parameter	Nominal Value
Input voltage	$v_{\rm i}$	24 V
Capacitance	C	150 μF
Capacitor ESR	r_C	21 mΩ
Inductance	L	100 μH
Inductor resistance	r_L	0.12 Ω
Switching frequency	$f_{\rm S}$	200 kHz
Minimum load resistance	$R_{\rm L(min)}$	3 Ω
Maximum load resistance	$R_{\rm L(max)}$	24 Ω
Desired output voltage	$V_{\rm od}$	12 V

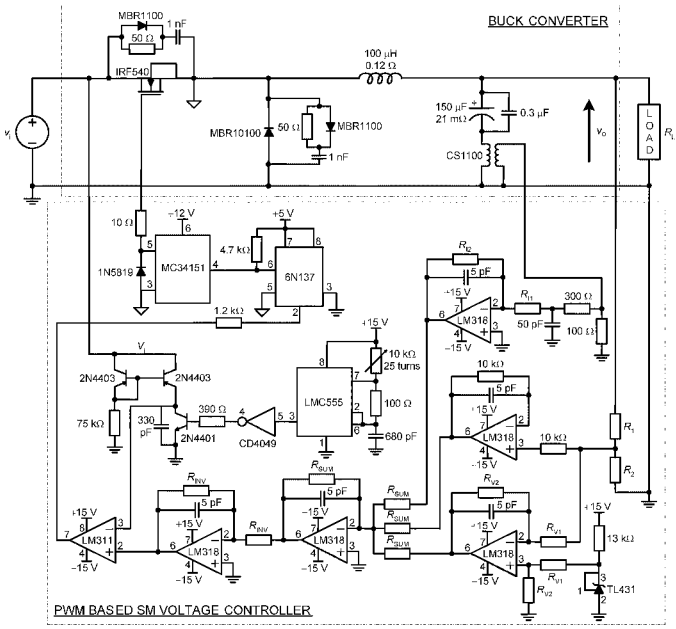


Fig. 6. Full schematic diagram of the PWM-based SMVC buck converter prototype.

response, the controller is designed for two different bandwidths: at one twentieth and at one tenth of the switching frequency $f_{\rm S}$, i.e., $f_{\rm BW} = 10$ kHz (i.e., first-order response time constant $\tau_{10\,\rm kHz} = 15.915$ μs) and $f_{\rm BW} = 20$ kHz (i.e., $\tau_{20\,\rm kHz} = 7.956$ μ s). The parameters of the controllers are given in Appendix II. Fig. 6 shows the full schematic diagram of the experimental prototype.

A. Steady-State Performance

Figs. 7 and 8 show the simulated (left) and experimental (right) waveforms during steady-state operation, for the SMVC converter with the 20-kHz bandwidth controller operating at full load (i.e., $R_{\rm L} = 3$ Ω). It can be seen that except for some ringing noise in the experimentally captured $\rm V_c$ and $\widetilde{\rm V_o}$ waveforms, the simulated and experimental waveforms are in good agreement. The main difference is that for the simulation, output voltage ripple $\widetilde{\rm V_o} \approx \pm 4$ mV (i.e., <0.035% of $\rm V_{od}$), and for the experiment, $\widetilde{\rm V_o} \approx \pm 8$ mV (i.e., <0.07% of $\rm V_{od}$). This discrepancy is mainly due to the presence of parasitic resistance and equivalent series inductance (ESL) of the capacitor in the practical converter, which are not modeled in the simulation program.

Fig. 9 shows the corresponding set of experimental waveforms for the SMVC converter with the 10-kHz bandwidth controller operating at full load (i.e., $R_{\rm L} = 3$ Ω). Except for $\rm V_c$, there is no major difference between these waveforms and the experimental waveforms in Figs. 7 and 8. Due to the higher magnitude of the sliding coefficients, $\rm V_c$ of the 20-kHz bandwidth controller has a higher peak-to-peak value than $\rm V_c$ of the 10-kHz bandwidth controller.

B. Load Variation Analysis

Fig. 10 shows a plot of the measured dc output voltage against the different operating load resistances. At full load operation (i.e., $R_{\rm L} = 3$ Ω), the converter employing the 20-kHz bandwidth controller has a steady-state dc output voltage $\overline{\rm V}_{\rm o}$ of 11.661 V, which corresponds to a -2.825% deviation from $\rm V_{od}$. The plot also shows that even though $\overline{\rm V}_{\rm o}$ increases with $R_{\rm L}$, $\overline{\rm V}_{\rm o}$ is always less than $\rm V_{od}$. This agrees with the previous assumption that the output voltage of PWM-based system is always below the desired voltage. Furthermore, it also shows that the converter has satisfactory load regulation, having only a 0.151 V deviation in $\overline{\rm V}_{\rm o}$ for the entire load range of $3\ \Omega \le R_{\rm L} \le 24\ \Omega$, i.e., the load regulation is only 1.29% of $\overline{\rm V}_{\rm o(full\ load)}$ from full load to minimum load.

For the converter employing the 10-kHz bandwidth controller, the steady-state dc output voltage at full load operation is 11.633 V, which corresponds to a -3.058% deviation from $\rm V_{od}$. For the entire load range of $3\ \Omega \le R_{\rm L} \le 24\ \Omega$, $\overline{\rm V}_{\rm o}$ has a deviation of 0.189 V, i.e., the load regulation is 1.62% of $\overline{\rm V}_{\rm o(full\ load)}$ from full load to minimum load. Thus, it can be concluded that the 20-kHz bandwidth controller has better load variation property than the 10-kHz bandwidth controller.

C. Line Variation Analysis

Fig. 11 shows the experimental waveforms of the SMVC buck converter that is operated with minimum and maximum input voltage of $\rm V_i = 16$ V and $\rm V_i = 30$ V. As shown in the figures, the controller operates effectively for both operating conditions.

Additionally, to investigate the effectiveness of the adaptive feed-forward control property, experiments are performed for both the cases where the peak of the input ramp signal to the comparator is set as a constant (i.e., $\hat{v}_{\rm ramp} = 5$ V) and where it is adaptive (i.e., $\hat{v}_{\rm ramp} = \beta \rm V_i$).

Fig. 12(a)–(d) and Fig. 13(a)–(d) show, respectively, the experimental waveforms of the converter under minimum and maximum input voltage. The waveforms with and without the adaptive feed-forward control property can be differentiated in terms of their ramp signals [$\hat{v}_{\rm ramp} = 5.00$ V in Figs. 12(b) and (c) and 13(a) and (c); $\hat{v}_{\rm ramp} = 3.33$ V in Fig. 12(b) and (d); and $\hat{v}_{\rm ramp} = 6.25$ V in Fig. 13(b) and (d)]. The other difference between the adaptive and nonadaptive controllers' waveforms is the control signal $\rm V_c$. In the case where $\rm V_i = 16$ V, with a lower $\hat{v}_{\rm ramp}$, and in the attempt to accommodate the operation to a constant duty ratio $d = (\rm V_o/V_i)$, the magnitude of $\rm V_c$ signal is automatically reduced by the adaptive feed-forward

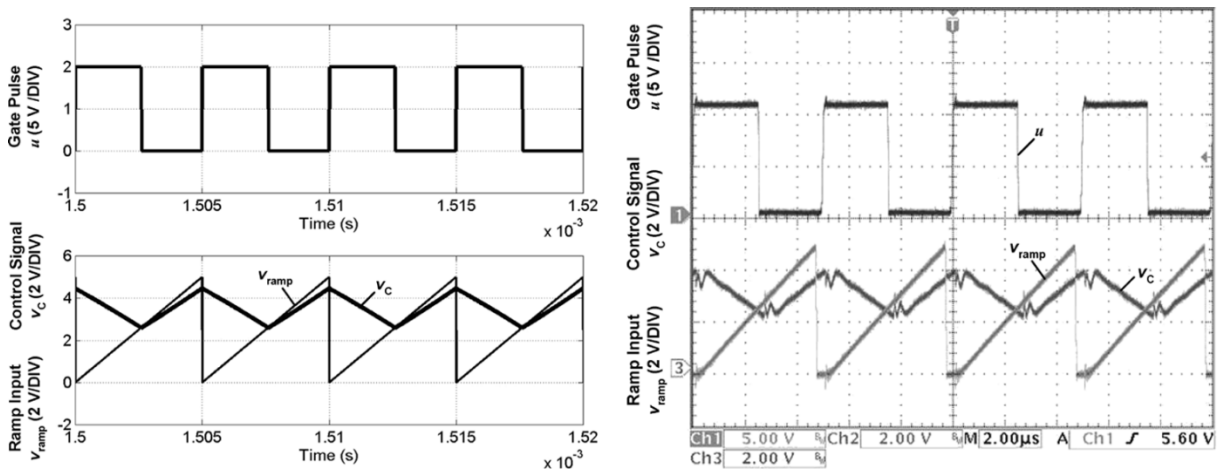
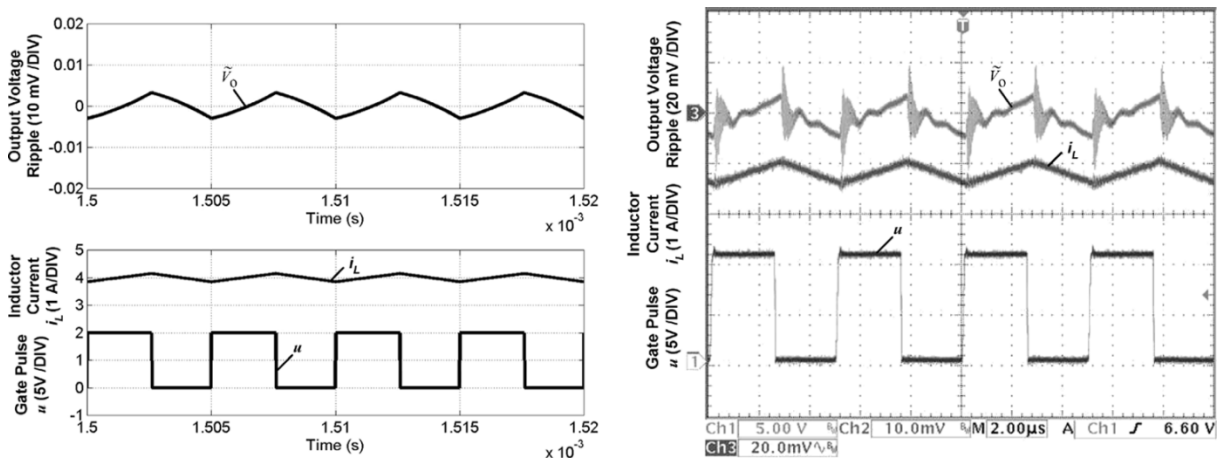
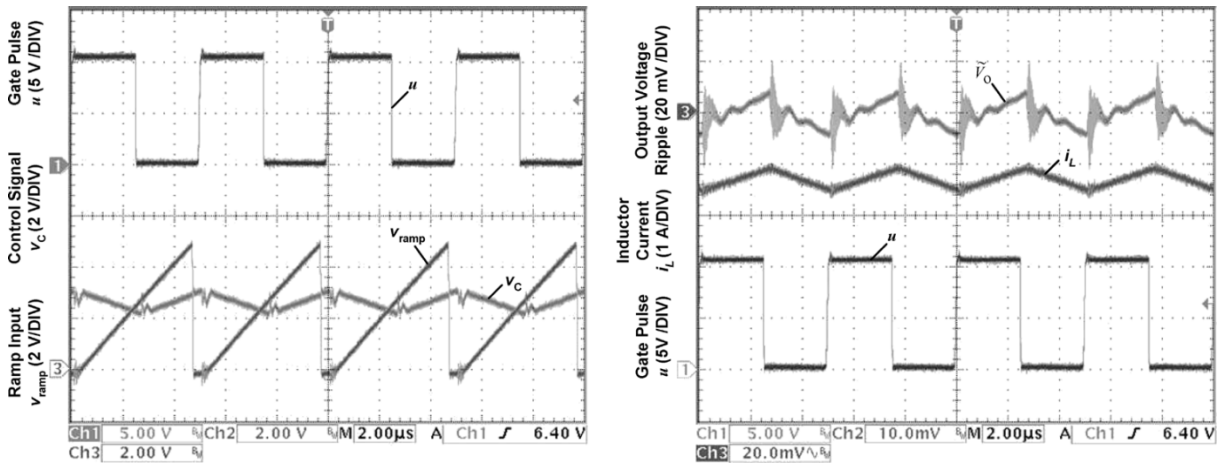


Fig. 7. (a) Simulated and (b) experimental waveforms of control signal V_c, input ramp V_{ramp}, and generated gate pulse u for SMVC converter with the 20-kHz bandwidth controller operating at constant load resistance $R_L = 3\ \Omega$.



(a) (b)

Fig. 8. (a) Simulated and (b) experimental waveforms of gate pulse u, and the corresponding inductor current i_L and output voltage ripple $\widetilde{V_o}$ for SMVC converter with the 20-kHz bandwidth controller operating at constant load resistance $R_L = 3\ \Omega$.



(a) (b)

Fig. 9. Experimental waveforms of (a) control signal V_c input ramp V_{ramp}, and generated gate pulse u and waveforms of (b) gate pulse u and the corresponding inductor current i_L and output voltage ripple $\widetilde{V_o}$, for the SMVC converter with the 10-kHz bandwidth controller operating at load resistance $R_L = 3\ \Omega$.

control [compare Fig. 12(a) and (c) with Fig. 12(b) and (d)]. This effectively tightens the voltage regulation relative to the controller without adaptive feed-forward control. In contrast, when the converter operates at $V_i = 30$ V, the magnitude of

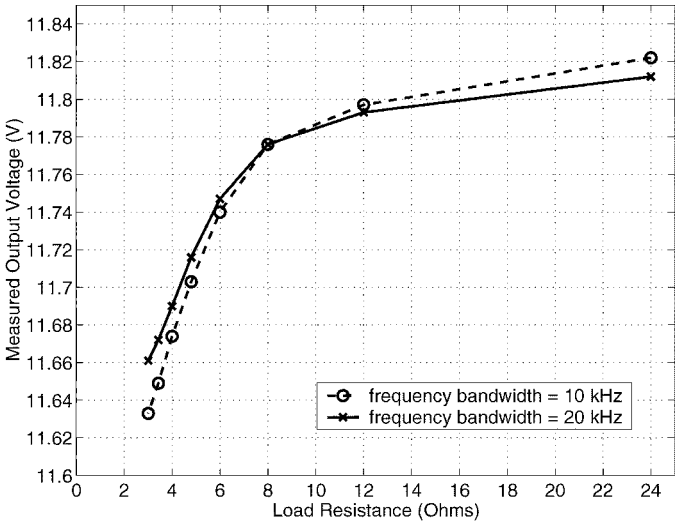


Fig. 10. Plot of measured dc output voltage $\overline{V}_o$ against load resistance R_L for SMVC buck converter with both the 10-kHz and 20-kHz bandwidth controllers.

V_c signal is automatically increased for the controller with the adaptive feed-forward control [compare Fig. 13(a) and (c) with Fig. 13(b) and (d)]. This, on the other hand, loosens the voltage regulation. Surprisingly, such control actions of tightening and loosening the voltage regulation as input voltage varies, are actually the inherited virtues of the adaptive feed-forward control. This is evident as shown in Fig. 14 that the line regulation from minimum to maximum input voltage is corrected from 1.38% of $\overline{V}_{o(V_i=24V)}$ (10-kHz bandwidth controller without adaptive feed-forward control) and 0.43% of $\overline{V}_{o(V_i=24\ V)}$ (20-kHz bandwidth controller without adaptive feed-forward control), to a perfect regulation of 0% for both controllers with the adaptive feed-forward control.

D. Dynamic Performance

The dynamic performance of the controllers is studied using a load resistance that alternates between quarter load (12 Ω) and full load (3 Ω) at a constant frequency of 5 kHz. Figs. 15 and 16 show, respectively, the simulated and experimental output voltage ripple (top) and inductor current (bottom) waveforms of the converter for both the 10-kHz bandwidth controller (left) and the 20-kHz bandwidth controller (right). As illustrated in Fig. 15, the simulated output voltage has an overshoot ripple of 220 mV (1.83% of V_{od}) and a steady-state settling time of 120 μs for the 10-kHz bandwidth controller, and an overshoot ripple of 232 mV (1.93% of V_{od}) and a steady-state settling time of 83 μs for the 20-kHz bandwidth controller, during the load transients. As shown in Fig. 16, the output voltage has an overshoot ripple of 200 mV (1.67% of V_{od}) and a steady-state settling time of 104 μs for the 10-kHz bandwidth controller, and an overshoot ripple of 250 mV (2.08% of V_{od}) and a steady-state settling time of 73 μs for the 20-kHz bandwidth controller, during the load transients. Furthermore, consistent with a critically-damped response, there is no ringing or oscillations in transience. However, it should also be mentioned that there are some slight disagreements between the experimental and simulation results in terms of the overshoot ripple magnitudes and the settling times. These are mainly due to the modeling imperfection of the simulation program, and the parameters' deviation of the actual experimental circuits from the simulation program due to the variation of the actual components used in the setup. Additionally, it should be clarified that the settling time measured in this case is the total time taken to complete both Phase 1 and Phase 2 of the control process, which has been described and illustrated in Fig. 3. Hence, this explains why the steady-state settling time exceeds 5τ, where $\tau = \tau_{10\ \mathrm{kHz}}$ for the 10-kHz bandwidth controller and $\tau = \tau_{20\ \mathrm{kHz}}$ for the 20-kHz bandwidth controller.

E. A Comparison With Classical PWM Voltage Mode Controller

The dynamic behavior of the PWM-based SMVC buck converter is compared to that of the classical type of PWM voltage mode controlled buck converter. In the experiment, the former employs a 20-kHz bandwidth PWM-based SM controller and the latter employs a PID PWM voltage mode controller that is optimally tuned to operate at a step load change that alternates between $R_L = 3\,\Omega$ and $R_L = 12\,\Omega$. Fig. 17(a)–(f) show the experimental waveforms with both converters operating at 5-kHz step load change.

With the classical PWM voltage mode controller, the dynamic behavior of the system is dissimilar at different operating settings. Specifically, the response becomes more oscillatory at lower currents, i.e. the output voltage ripple waveform in Fig. 17(a) has most oscillation, Fig. 17(b) with some oscillation, and Fig. 17(c) with no oscillation (when entered momentarily into discontinuous conduction mode). This is expected since the PWM controller is designed for a specific operating condition, which leads to changes in the response behavior when a different operating condition is engaged.

On the other hand, with the PWM-based SM controller, the dynamic behavior of output voltage ripple are basically similar (i.e., critically damped) for all three operating load conditions, even when it enters momentarily into discontinuous conduction mode and experiencing a change in converter's description. This demonstrates the strength of the SM controller in terms of robustness in the dynamic behavior at different operating conditions and uncertainties. Additionally, the example also illustrates a major difference between a large-signal controlled system (SM) and a small-signal controlled system (PWM), that is, the former complies to the design with a similar response for all operating conditions, while the response of the latter will only comply to the design at a specific operating condition.

V. Conclusion

A fixed-frequency PWM-based SMVC buck converter is presented from a circuit design perspective. The description of the design methodology takes into account the different aspects of converter's operating conditions. A practical approach to the design of the sliding coefficients is also proposed in this paper. This approach uses an equation that is derived from analyzing the dynamic behavior of the converter during SM operation, in

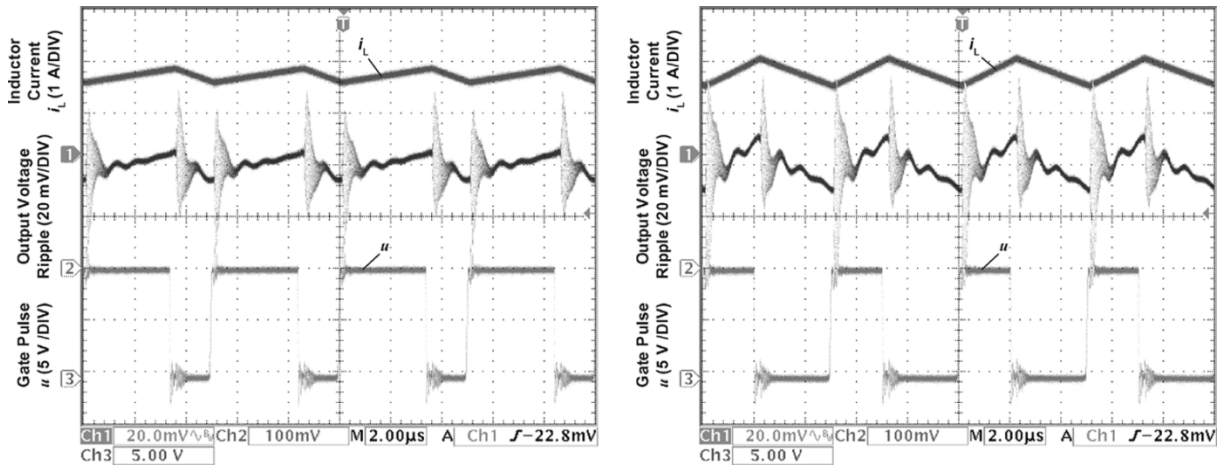


Fig. 11. Experimental waveforms of gate pulse u, and the corresponding inductor current i_L and output voltage ripple $\widetilde{V_o}$, for the SMVC converter with the 10-kHz bandwidth controller operating at (a) input voltage $V_i = 16$ V and (b) $V_i = 30$ V, at load resistance $R_L = 3\ \Omega$.

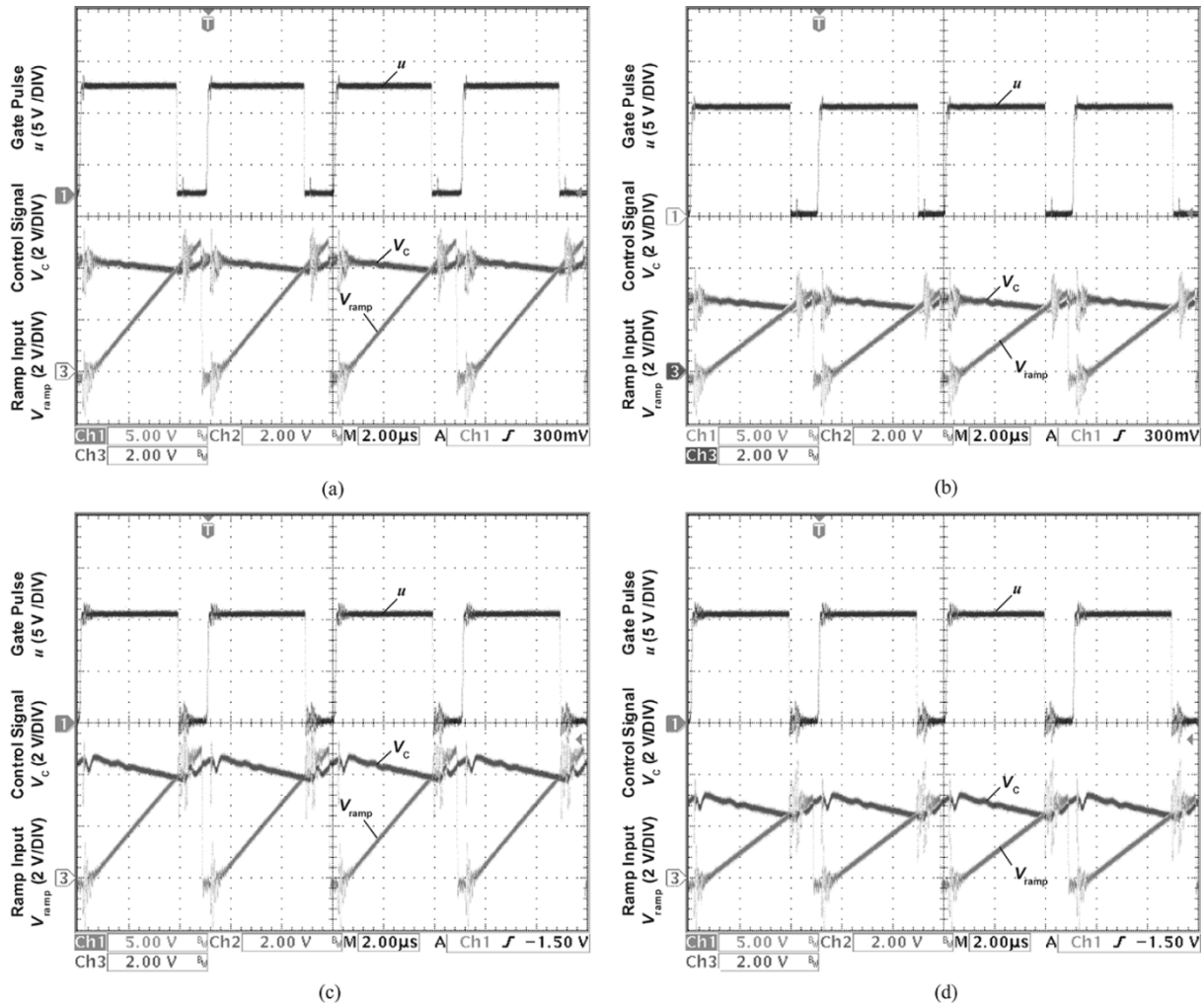


Fig. 12. Experimental waveforms of control signal V_c, input ramp V_{ramp}, and generated gate pulse u for the SMVC converter with both the 10-kHz and 20-kHz bandwidth controllers, with and without the adaptive feed-forward control property, operating at input voltage $V_i = 16$ V and load resistance $R_L = 3\ \Omega$. (a) 10-kHz bandwidth controller without adaptive feed-forward control. (b) 10-kHz bandwidth controller with adaptive feed-forward control. (c) 20-kHz bandwidth controller without adaptive feed-forward control. (d) 20-kHz bandwidth controller with adaptive feed-forward control.

addition to the existence conditions of the system. An analog form of the controller is also presented. It is found that the PWM-based SM controller adopts a similar structure to that of a classical PWM PD linear voltage mode controller. The simulation and experimental results show that the response of the converter agrees with the theoretical design.

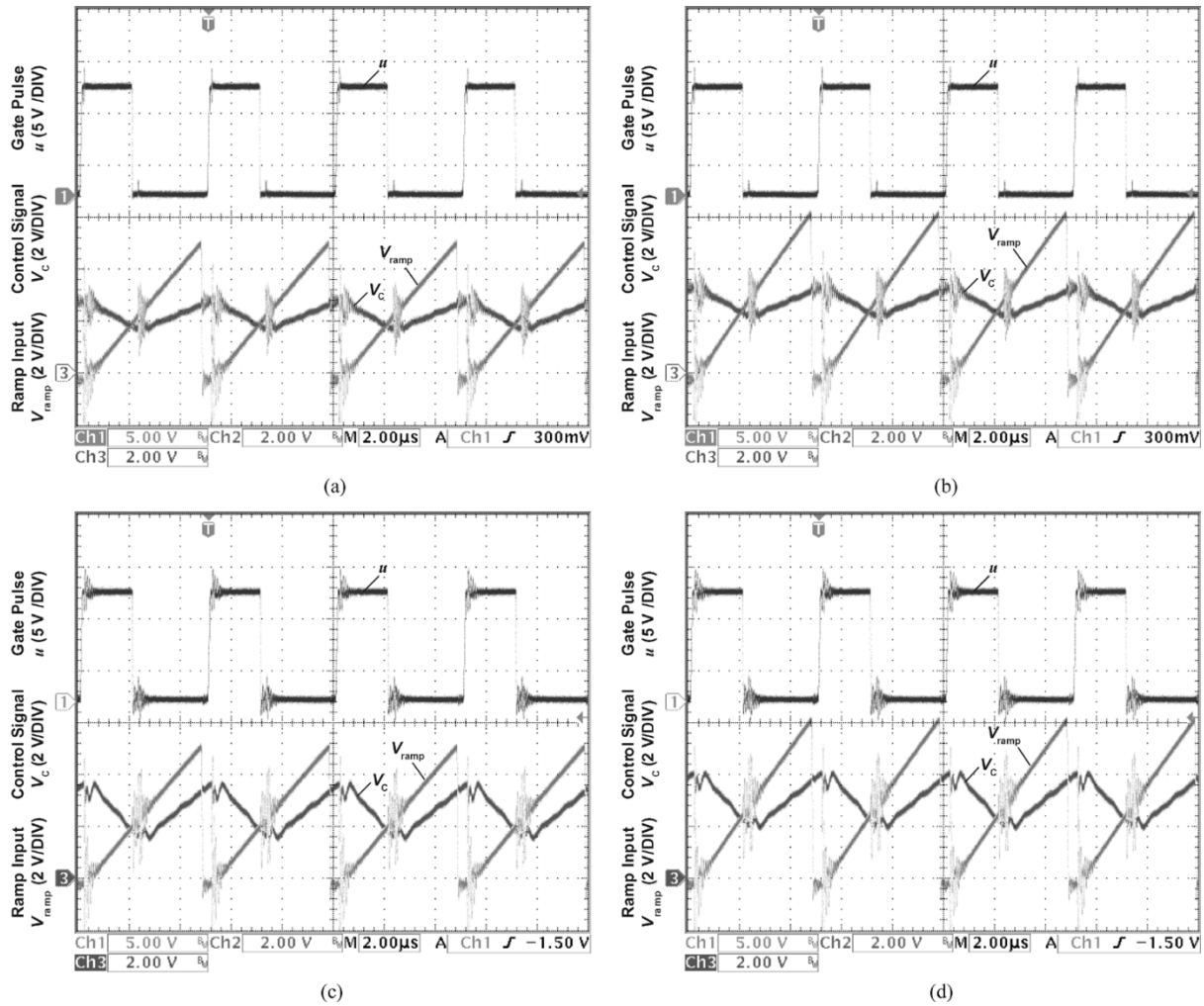


Fig. 13. Experimental waveforms of control signal V_c, input ramp V_{ramp}, and generated gate pulse u for the SMVC converter with both the 10-kHz and 20-kHz bandwidth controllers, with and without the adaptive feed-forward control scheme, operating at input voltage $V_i = 30$ V and load resistance $R_L = 3\ \Omega$. (a) 10-kHz bandwidth controller without adaptive feed-forward control. (b) 10-kHz bandwidth controller with adaptive feed-forward control. (c) 20-kHz bandwidth controller without adaptive feed-forward control. (d) 20-kHz bandwidth controller with adaptive feed-forward control.

APPENDIX I
DESIGN PROCEDURE FOR THE PROPOSED PWM BASED SMVC BUCK CONVERTER

Step1: Choosing a desired bandwidth, the control parameters can be calculated using (22), i.e., $(\alpha_1/\alpha_2) = 4\pi f_{\rm BW}$ and $(\alpha_3/\alpha_2) = 4\pi^2 f_{\rm BW}^2$. Substitute these parameters along with the converter's parameters into (16) to ensure that the existence condition is met.

Step2: Choosing a certain reference voltage $V_{\rm ref}$, β is calculated using the expression

$$\beta = \frac{V_{\rm ref}}{V_{\rm od}}. \tag{32}$$

Also, R_1 and R_2 are related by

$$R_2 = \frac{\beta}{1-\beta} R_1. \tag{33}$$

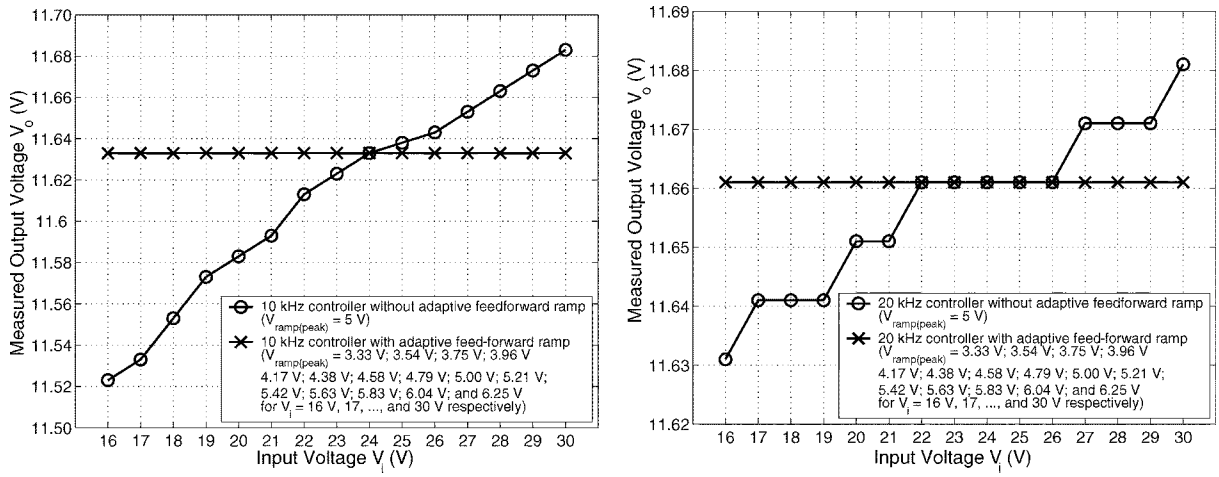
Step3: From (28), the gain required for the amplification of the signal $(V_{\rm ref} - \beta V_{\rm o})$ is $(\alpha_3/\alpha_2)LC$. Hence, with known converter's parameters, $R_{\rm V1}$ and $R_{\rm V2}$ are be determined using

$$R_{\rm V2} = \left(\frac{\alpha_3}{\alpha_2} LC\right) R_{\rm V1}. \tag{34}$$

Step4: Setting the current sensing gain H at a value such that the measured capacitor current $i_{\rm C(mea)}$ is equal to the actual capacitor current $i_{\rm C}$, and considering that the controller is designed for maximum load current (i.e. minimum load resistance $R_{\rm L(min)}$), the gain required for the amplification of the signal $i_{\rm C(mea)}$ is $\beta L((1/R_{\rm L(min)}C) - (\alpha_1/\alpha_2))$. Hence, with known converter's parameters, $R_{\rm I1}$ and $R_{\rm I2}$ can be determined using

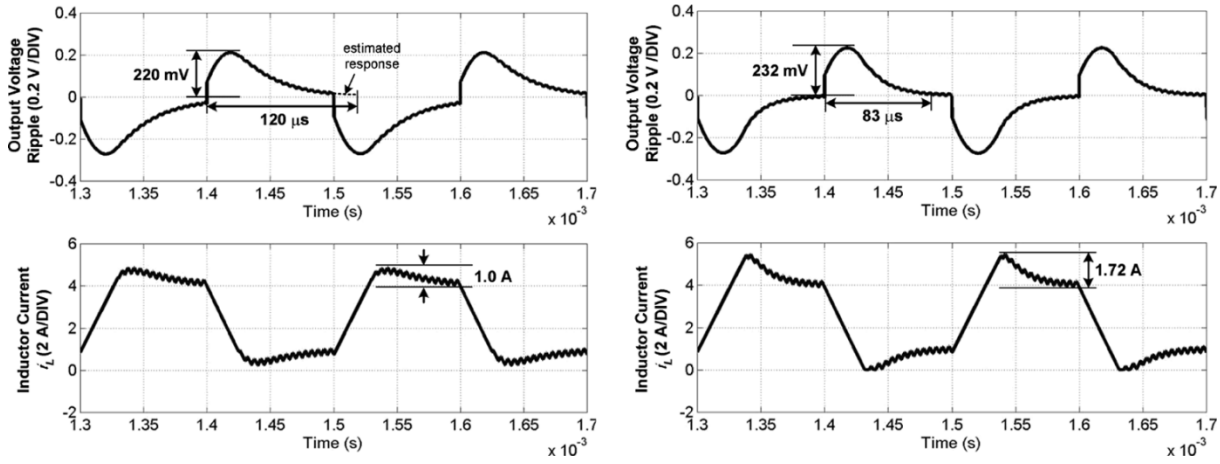
$$R_{\rm I2} = \beta L \left(\frac{1}{R_{\rm L(min)}C} - \frac{\alpha_1}{\alpha_2}\right) R_{\rm I1}. \tag{35}$$

Step5: Fig. 18 shows the schematic diagram of the adaptive feed-forward variable ramp generator adopted in our controller design.



(a) (b)

Fig. 14. Plots of measured dc output voltage $\overline{V}_o$ against input voltage V_i for SMVC buck converter with both the (a) 10-kHz and (b) 20-kHz bandwidth controllers, with and without the adaptive feed-forward control property.



(a) (b)

Fig. 15. Simulated waveforms of output voltage ripple $\widetilde{V_o}$ and inductor current i_L of the SMVC converter with the (a) 10-kHz bandwidth controller and the (b) 20-kHz bandwidth controller, operating at 5-kHz step load change between $R_L = 3\ \Omega$ and $R_L = 12\ \Omega$.

According to the figure, the rate of change of voltage in the capacitor $C_{\rm ramp}$ is

$$\frac{d\mathrm{V}_{\rm ramp}}{dt} = \frac{\mathrm{V_i}}{R_{\rm ramp}C_{\rm ramp}}. \tag{36}$$

For one complete ramp cycle of T_S duration, $\mathrm{V}_{\rm ramp}$ is linearly varied from 0 V to $\hat{v}_{\rm ramp}$ V. Hence,

$$\hat{v}_{\rm ramp} = \frac{\mathrm{V_i}}{R_{\rm ramp}C_{\rm ramp}}T_{\rm S}. \tag{37}$$

Since $\hat{\mathrm{V}}_{\rm ramp} = \beta \mathrm{V_i}$ and $T_{\rm S} = (1/f_{\rm S})$, the equation can be arranged as

$$R_{\rm ramp} = \frac{1}{\beta C_{\rm ramp} f_{\rm S}} \tag{38}$$

APPENDIX II
PARAMETERS OF CONTROLLERS

The reference voltage is chosen as $\mathrm{V}_{\rm ref} = 2.5$ V and the ratio of the voltage divider network β =0.208. The current sensing ratio is set at H =1 so that $i_C = i_{C(\rm mea)}$.

A. Parameters of the 10-kHz Bandwidth Controller

For the 10-kHz bandwidth controller, the ideal control equation calculated from the design equations is

$$\mathrm{V_c} = -2.572\, i_C + 0.208\ \mathrm{V_o} + 59.218(\mathrm{V_{ref}} - \beta \mathrm{V_o}). \tag{39}$$

The values of the components used in the controller for both the simulation and experiment are

$$\begin{aligned} R_1 &= 950\ \Omega, \quad R_2 = 250\ \Omega \\ R_{\rm I1} &= 2.16\ \mathrm{k}\Omega, \quad R_{\rm I2} = 5.6\ \mathrm{k}\Omega \\ R_{\rm V1} &= 2.2\ \mathrm{k}\Omega, \quad R_{\rm V2} = 130\ \mathrm{k}\Omega \\ R_{\rm INV} &= 10\ \mathrm{k}\Omega, \quad R_{\rm SUM} = 10\ \mathrm{k}\Omega. \end{aligned} \tag{40}$$

Hence, the implemented control equation is

$$\mathrm{V_c} = -2.593\, i_C + 0.208\ \mathrm{V_o} + 59.100(\mathrm{V_{ref}} - \beta \mathrm{V_o}). \tag{41}$$

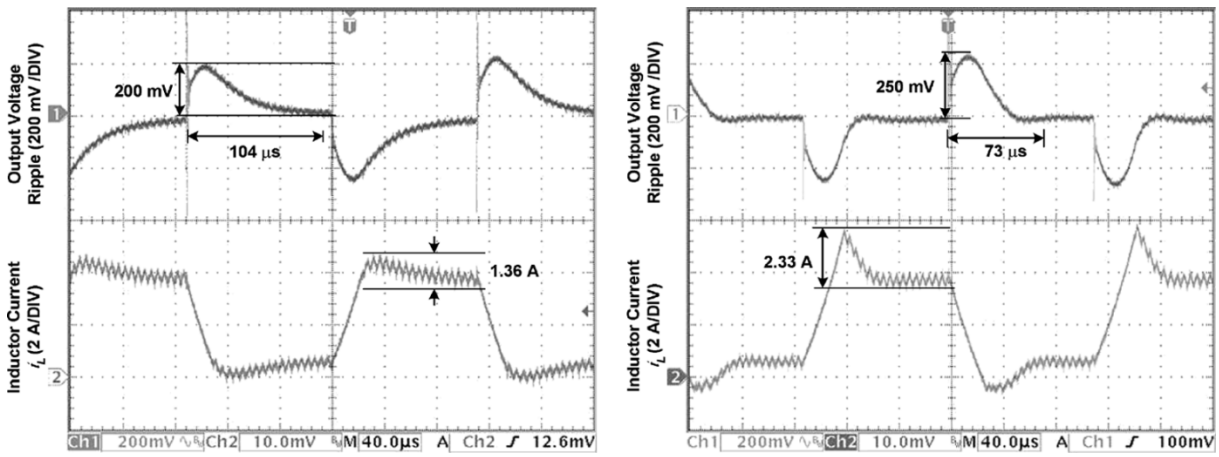


Fig. 16. Experimental waveforms of output voltage ripple $\widetilde{V_o}$ and inductor current i_L of the SMVC converter with the (a) 10-kHz bandwidth controller and the (b) 20-kHz bandwidth controller, operating at 5-kHz step load change between $R_L = 3\ \Omega$ and $R_L = 12\ \Omega$.

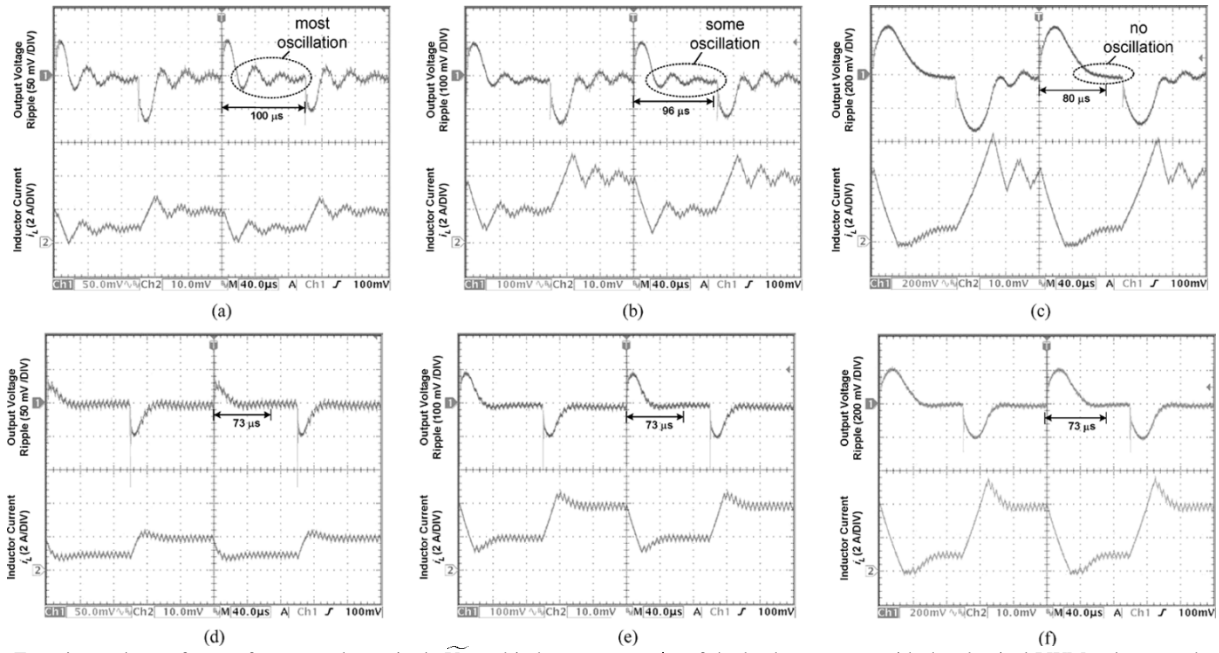


Fig. 17. Experimental waveforms of output voltage ripple $\widetilde{V_o}$ and inductor current i_L of the buck converter, with the classical PWM voltage mode controller (a)–(c) and the 20-kHz bandwidth PWM-based SM controller (d)–(f), operating at 5-kHz step load resistance change. (a) R_L between 6 Ω and 12 Ω (PWM controller). (b) R_L between 3 and 6 Ω (PWM controller). (c) R_L between 3 and 12 Ω (PWM controller). (d) R_L between 6 and 12 Ω (SM controller). (e) R_L 3 and 6 Ω (SM controller). (f) R_L between 3 and 12 Ω (SM controller).

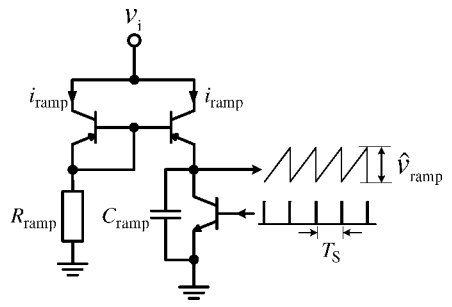


Fig. 18. Schematic diagram of the adaptive feed-forward ramp signal generator.

B. Parameters of the 20-kHz Bandwidth Controller

For the 20-kHz bandwidth controller, the ideal control equation calculated from the design equations is

$$V_c = -5.190\, i_C + 0.208\, V_o + 236.875(V_{ref} - \beta V_o). \quad (42)$$

The values of the components used in the controller for both the simulation and experiment are

$$\begin{aligned} R_1 &= 950\ \Omega, \quad R_2 = 250\ \Omega \\ R_{I1} &= 2.16\ \text{k}\Omega, \quad R_{I2} = 11.2\ \text{k}\Omega \\ R_{V1} &= 3.6\ \text{k}\Omega, \quad R_{V2} = 910\ \text{k}\Omega \\ R_{INV} &= 10\ \text{k}\Omega, \quad R_{SUM} = 10\ \text{k}\Omega. \end{aligned} \quad (43)$$

Hence, the implemented control equation is

$$V_c = -5.185\, i_C + 0.208\, V_o + 252.780(V_{ref} - \beta V_o). \quad (44)$$

C. Parameters of the Adaptive Feed-Forward Ramp Generator

The input ramp signal for both the controllers is a sawtooth signal that varies from 0 V to its peak magnitude $\hat{v}_{ramp} =$

0.208 V_i V at a constant frequency $f_S = 200$ kHz. Setting $C_{ramp} = 330$ pF, and by using (38), R_{ramp} is calculated as 72.7 kΩ. A 75-kΩ resistor is chosen.

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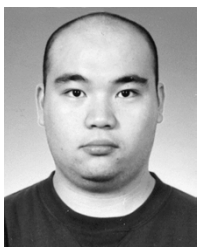

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