A Flexible Low-Latency DC-to-4 Gbit/s Link Operating From -40 to +200°C in 28nm CMOS for Galvanically Isolated Applications

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***Abstract*— This paper presents a communication link for galvanically isolated (GI) applications. The proposed link employs a 120 GHz OOK transmitter and receiver with a PTFE fiber as directive channel to reduce transmission losses. The receiver is implemented with a replica temperature compensation loop to provide operation from −40 to +200 °C and thereby overcome the limitations of existing optical and magnetically coupled solutions. The presented work reports an isolated communication link with a data rate of 4 Gbit/s and reports the lowest latency of 1 ns with less than 4.5% variation over the entire measured temperature range. The power consumption of the entire link is only 52.4 mW and achieves 13.1 pJ/bit efficiency.**

***Index Terms*— Galvanic Isolation, mm-Wave, OOK, polymer fiber, temperature compensation, replica biasing**

I. Introduction

With the increasing interest in high voltage (HV) electronics (wind turbines, trains, electric vehicles …), the need for communication links that can provide galvanic isolation emerges. These isolated links are key to communicate between microcontroller and HV electronics and are required to work from DC up to a set data rate. An important specification for these links is low latency when used for power converters in motor control. A low latency link is a crucial component to increase switching efficiency in Zero-Voltage-Switching (ZVS) operation by reducing the dead time control delay. A high data rate isolated link on the other hand is required in medical applications, where isolation is needed between human and medical equipment [1].

Fig. 1 summarizes and compares reported topologies for GI communication links. Optocouplers are the proven choice for isolated communication, because of their high isolation capabilities. However, optocouplers suffer from a limited operational temperature range, due to the decrease in output power of the VCSEL/LED and the increase in dark currents in the photodiode at higher temperatures [2]. Other galvanically isolated topologies, such as magnetic and capacitive coupled isolators [1], [3]–[6] overcome the temperature issue but suffer from limited isolation capability, as their link efficiency is greatly dependent on the isolation distance.

To overcome the problems mentioned above, this work demonstrates a low-latency link operating over a wide temperature range, based on guided mm-wave communication. The presented work achieves a higher temperature range than optocouplers and has a lower latency than magnetic/capacitive solutions. The demonstrated link uses a 120 GHz transmitter (TX) and receiver (RX) with temperature compensation in 28 nm CMOS together with a 100 mm PTFE fiber as a directive channel to decrease path loss and to act as an isolation barrier. With this technique, 4 Gbit/s communication with an operating temperature range from −40 to +200 °C is achieved. For this distance a maximum latency, as low as 1.03 ns is measured over temperature with a total power consumption of only 52.4 mW.

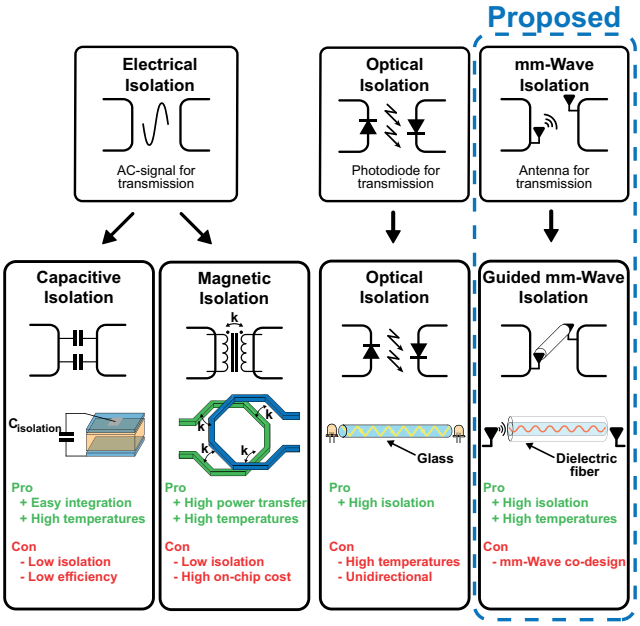


Fig. 1. Comparison of galvanic isolation topologies.

II. Proposed Low-Latency Link

Fig. 2 shows the architecture of the proposed low-latency link for galvanically isolated applications. An OOK transmitter modulates the incoming data of an on-chip generated 120 GHz carrier. A simple OOK modulation scheme is chosen as it will result in low latency, minimal chip area and low power consumption. The modulated signal is radiated into a foam-cladded PTFE fiber through

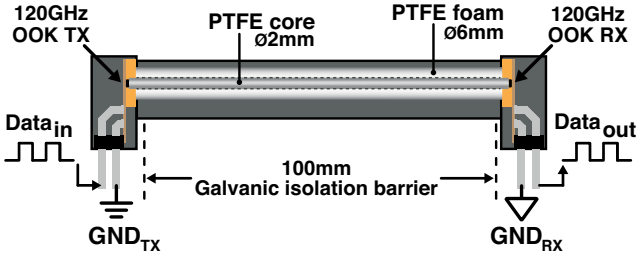


Fig. 2. Proposed low-latency link for galvanically isolated applications.

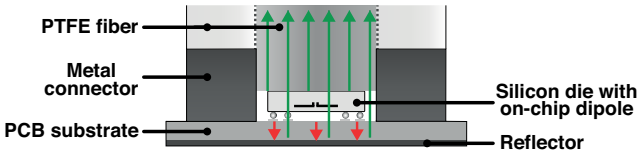


Fig. 3. Coupling between on-chip dipole antenna and fiber. A reflector is added to increase coupling efficiency.

an on-chip dipole antenna. A dipole antenna is chosen because of its small area. The antenna is produced in the top metal and radiates through the backside of the silicon, as illustrated in fig. 3. The chip is flip-chip bonded on a high-frequency PCB substrate with a metal shield at the bottom acting as a reflector for the front side radiation. The simulated coupling loss between chip and fiber is 4.5 dB.

The PTFE fiber consists of a 2 mm core, which confines the propagating signal and a 6 mm PTFE foam cladding with lower dielectric constant, which prevents any outside objects to interfere with the propagating signal inside the fiber core. The loss of 100 mm cladded fiber is only 0.5 dB at 120 GHz. Multiple links and fibers with cladding can be placed next to each other in the same package, to increase I/O throughput per area.

A link with 100 mm fiber can easily provide high isolation as the dielectric strength of PTFE is around 20 kV/mm, which is six times higher than air and comparable with borosilicate glass. Owing to the flexible properties of the PTFE fiber, bends can easily be applied if required. If lower latency, fewer isolation or reduced area is required, the fiber length can easily be shortened to fulfil specifications.

III. Circuit Implementation

A. 120 GHz *OOK Transmitter*

The architecture of the proposed OOK TX is shown in fig. 4. A LC-VCO generates a 120 GHz fundamental carrier and has a 2-bit, sized capacitor bank to compensate for possible process variation and increase robustness. The VCO is directly followed by an OOK modulator, which is implemented as a capacitive neutralized common-source amplifier with two modulation switches, as highlighted in fig. 4. An extra pMOS switch is added between the

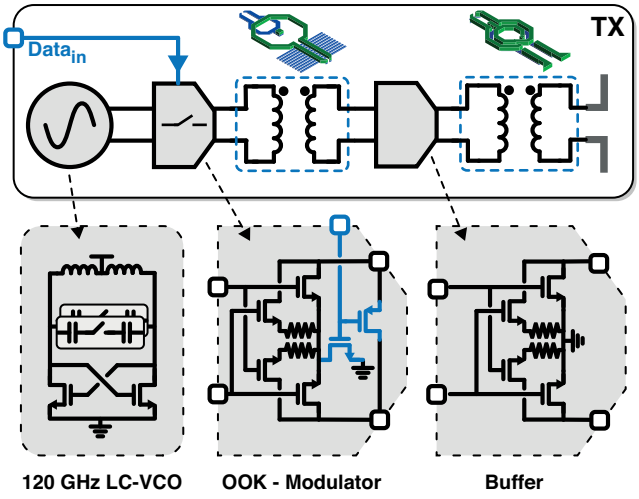


Fig. 4. Architecture of the proposed 120 GHz OOK transmitter.

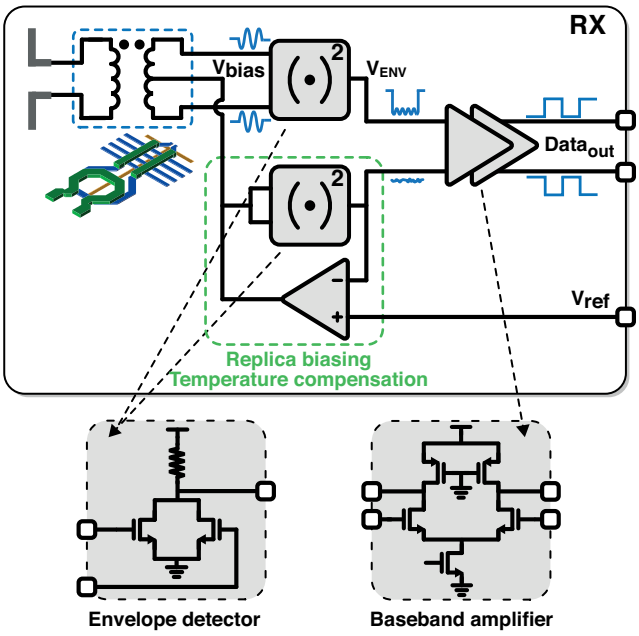


Fig. 5. Architecture of the proposed 120 GHz OOK receiver with replica biasing feedback loop for temperature compensation.

drains to increase the modulation index. A buffer stage, implemented as a neutralized common-source amplifier, buffers the modulated signal with the on-chip dipole antenna. The output matching network is designed with a 2-turn transformer to achieve a high k-factor and reduce the insertion loss of the network, thereby maximizing power efficiency. The output power of the transmitter, measured after 100 mm PTFE fiber, is −7.9 dBm, including both coupling and fiber losses. The total power consumption of the TX is 27.3 mW. The proposed TX is fabricated in 28 nm CMOS with 0.082 mm^2 active area, including the antenna, with die micrograph shown in fig. 6.

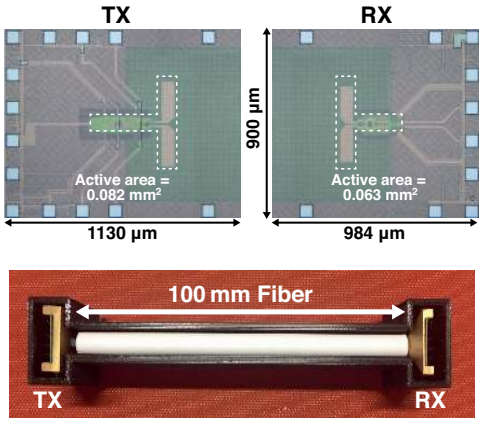


Fig. 6. Die micrograph of the proposed TX and RX (top). Photograph of the communication link inside a 3D-printed package for galvanically isolated applications (bottom).

B. 120 GHz *Temperature Compensated OOK Receiver*

The proposed 120 GHz OOK receiver, as shown in fig. 5, incorporates an on-chip dipole antenna, OOK demodulator and a temperature compensation feedback loop. The on-chip antenna is coupled to an envelope detector (ED) through a high-k transformer-based matching network. Due to the low-loss dielectric fiber there is no need for a power hungry LNA-stage, thereby reducing the overall power consumption.

The ED is implemented as a common-source differential pair, loaded with a resistor and extracts the envelope of the incoming 120 GHz OOK modulated signal, as shown in fig. 5. Together with the wanted envelope, unwanted even harmonics are also present at the output of the envelope detector. However these are located at high frequencies (240 GHz) and will be filtered by the baseband amplifiers. To achieve higher conversion gain the ED is biased towards weak inversion, which increases the non-linear transistor properties. Biasing is achieved with a replica ED in feedback with an amplifier to make the RX robust over temperature. The amplifier output is fed back to the centertap of the transformer in the matching network and sets the biasing voltage of the main ED. The main and replica ED both experience the same temperature conditions, thereby adjusting the bias voltage accordingly, making the RX robust over a wide temperature range.

Another advantage of this technique is that no feedback is applied directly on the main ED, thus ensuring that the link works down to DC. In addition to provide biasing, the replica-biasing network also provides a stable reference voltage for comparison with the demodulated data signal. The RX chip is implemented in 28 nm CMOS. Die micrograph is shown in fig. 6 and has an active area of 0.063 mm^2, including the on-chip dipole antenna. The 120 GHz RX consumes 25.1 mW from a 0.9 V supply.

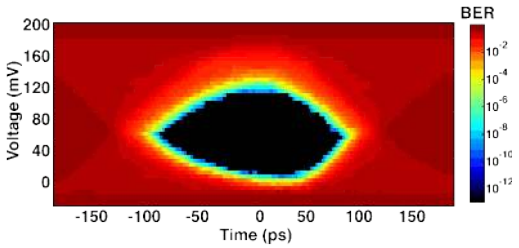
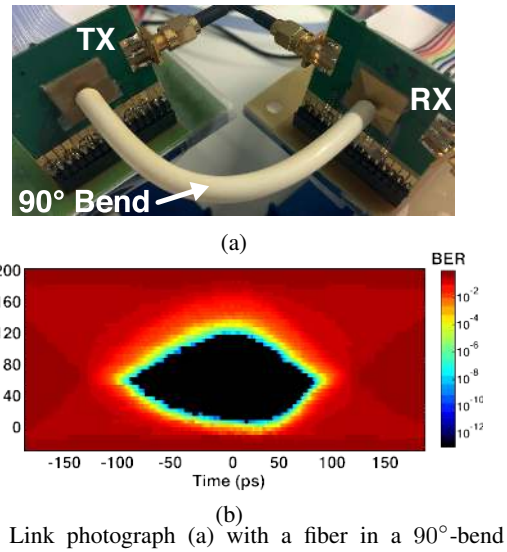


Fig. 7. Eye diagram and BER for a 4 Gbit/s PRBS13 signal.



(a)

(b)

Fig. 8. Link photograph (a) with a fiber in a 90°-bend and corresponding eye diagram and BER for a 4 Gbit/s PRBS13 signal (b).

IV. Measurement Results

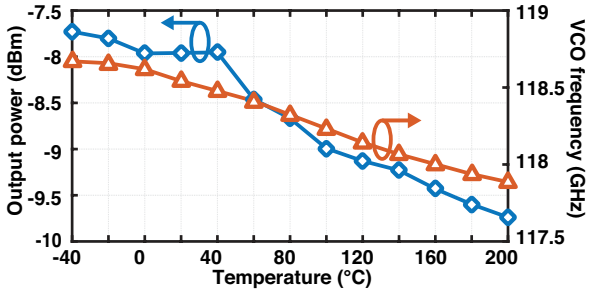
Fig. 6 shows the implementation of the proposed isolated link inside a 3D-printed package. The measured latency of the link for 0-to-1 and 1-0 transition is respectively 1.008 ns and 1.004 ns at 25 °C. This can be lowered to 778 ps when the fiber length is shortened to 50 mm.

The eye diagram and BER for 4 Gbit/s, is shown in fig. 7 for 100 mm communication distance. When a 90°-bend, with a radius of 63.7 mm, is applied to fiber it can be concluded, from the corresponding eye diagram from fig. 8b, that a bend has no effect on the link performance, proving the flexible properties.

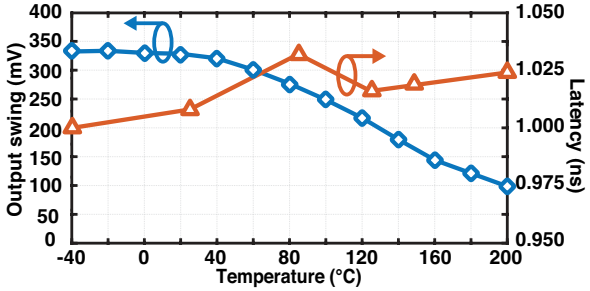
The robustness, of both TX and communication link, over temperature is measured from −40 to +200 °C and shown in fig. 9. The measured variation of transmitted output power and carrier frequency over temperature can be seen in 9a. The output power drops less than 2.5 dB, while the carrier frequency only varies with 750 MHz. This is less than 1% variation with respect to the nominal carrier frequency, showing the robustness of the VCO against temperature variation. Fig. 9b shows the measured robustness from −40 to +200 °C of the entire link. The maximum measured variation of the latency over the entire operating temperature range for 100 mm fiber is 1.03 ns,

TABLE I
COMPARISON WITH STATE-OF-THE-ART GI LINKS

	This work (TX/RX)	AVAGO AFBR3950xxRZ	ISSCC17 [4]	RFIC17 [3]	ISSCC16 [5]	VLSI15 [1]	TI ISO7821
Isolation topology	**Guided mm-wave**	Optical	Magnetic	Magnetic	Magnetic	Magnetic/ mm-wave	Capacitive
Isolation distance (mm)	**100**	100	0.5	0.012	Oxide layer	2	<7.6
Data rate (Mbit/s)	**DC-4000**	DC-50	DC-500	2-80	0.1-40	f_c-2500	DC-100
Latency (ns)	**1.03**	50	NA	17.6	NA	2	11
Operating range (°C)	**-40..+200**	-40..+85	NA	NA	NA	NA	-40..+125
Power consumption (mW)	**27.3 / 25.1**	155 / 135	57.5	322 / 9.45	228	NA	100
Efficiency (pJ/bit)	**13.1**	6100	175	4143	5700	20	1000
Technology	**28 nm CMOS**	NA	180 nm CMOS	350 nm BCD	350 nm BCD	65 nm CMOS	NA



(a)



(b)

Fig. 9. Measured oscillation frequency and output power of the implemented TX from −40 to +200 °C (a). Measured robustness of the entire 100 mm link and latency variation from −40 to +200 °C (b)

resulting in a variation of just 4.3%. Performance of the proposed low-latency link for GI applications is summarized and compared to state-of-the-art designs in table I. This work is the first to achieve and demonstrate an operational temperature range from −40 to +200 °C. With a maximum latency of only 1.03 ns, the link outperforms both magnetic and optically coupled links. With 4 Gbit/s the proposed link has a 60% increase in data rate compared with other state-of-the-art implementations. Due to the low power consumption of 52.4 mW, the link achieves the best efficiency of 13.1 pJ/bit.

V. CONCLUSION

A low-latency, flexible isolated link is presented based on mm-wave and a PTFE fiber as channel to reduce transmission losses. By using the proposed topology the presented link breaks with the temperature and isolation limitations from both optical and magnetically coupled isolated links. A record data rate of 4 Gbit/s for isolated links is achieved with the lowest reported latency of less than 1.03 ns. This work is the first to report a measured operating range from −40 to +200 °C and consumes only 52.4 mW.

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