This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI10.1109/TNB.2022.3152228,

A Flexible Memristor Model with Electronic Resistive Switching Memory Behavior and its Application in Spiking Neural Network

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***Abstract*—Memristive technologies are attractive due to their non-volatility, high-density, low-power and compatibility with CMOS. For memristive devices, a model corresponding to practical behavioral characteristics is highly favorable for the realization of its neuromorphic system and applications. This paper presents a novel flexible memristor model with electronic resistive switching memory behavior. Firstly, the Ag-Au/$MoSe_2$-doped Se/Au-Ag memristor is prepared using hydrothermal synthesis method and magnetron sputtering method, and its performance test is conducted on an electrochemical workstation. Then, the mathematical model and SPICE circuit model of the Ag-Au/$MoSe_2$-doped Se/Au-Ag memristor are constructed. The model accuracy is verified by using the electrochemical data derived from the performance test. Furthermore, the proposed model is applied to the circuit implementation of spiking neural network with biological mechanism. Finally, computer simulations and analysis are carried out to verify the validity and effectiveness of the entire scheme.**

***Index Terms*—Electronic resistive switching memory behavior, memristor, performance test, spiking neural network**

I. Introduction

With the advent of Internet of Things, cloud computing, and big data; the in-depth analysis and processing of massive unstructured data require higher computational speed and energy efficiency [1]. However, the computing system under Von Neumann architecture appears to be less capable, and at the same time, Moore's Law is greatly challenged [2]. In contrast, the human brain consumes about 20W of power but it does well in versatile tasks including working memory, pattern recognition, vision processing and adaptive learning, which impose huge challenges for computers to perform [3]. Therefore, developing new electronic components and intelligent information processing systems closer to the structure and functions of human brains are currently the research focus.

Memristor possesses numerous unique properties such as high-density, low-power, nanoscale geometry, non-linearity, binary/multiple memory and capacity compatibility with complementary metal-oxide-semiconductor (CMOS), which makes it a powerful candidate in the field of neuromorphic computing [4]–[6]. Electronic resistive switching memory (ERSM) is one important kind of resistive random-access memory (RRAM) [1], with asymmetric I–V curves in the positive and negative voltage regions and no obvious current jump, which has been widely concerned by researchers. [7]–[12]. In 2013, reference [7] successfully fabricated a Pt/$BiFeO_3$ nano-islands/SRO memristor. The detailed electrochemical analysis indicated that the ERSM behavior could be attributed to the asymmetric Schottky barrier and the interfacial polarization charge. In [8], the devices with Pt/MoS_2-$MoO_{x<3}$/Ag structures were fabricated by spin-coating at room temperature. The ERSM phenomenon should be attributed to the polar charges at the two ends and the space charges in the bulk of the composite MoS_2-$MoO_{x<3}$ nanobelts. A highly flexible ERSM was fabricated in the Al/TiO_2/Al/polyimide structure using a simple and cost-effective method. The detailed electrical analysis indicated that the ERSM behavior could be attributed to the electronic switching mechanism mediated by the electron trapping/detrapping [9]. A polymer memristor with buffer layer was prepared in [10], and its specific working mechanism indicated that the device also belonged to ERSM. In [11], the design and fabrication of an asymmetrical Al/TiO_2/FTO sandwiched nanostructure was reported by using simple spin-coating and vacuum deposition techniques. The Al/TiO_2/FTO memristor presents the ERSM behavior mode by trapping and detrapping of carriers. In [12], the

Manuscript revised February 15, 2022.

This work was supported in part by the National Natural Science Foundation of China under Grant U1909201, Grant 62001149, and Natural Science Foundation of Zhejiang Province under Grant LQ21F010009 *(Corresponding authors: Donglian Qi and Zhekang Dong)*.

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TABLE I
THE COMPARATIVE INFORMATION OF DIFFERENT MEMRISTOR MODELS

Literature	[18, 19]	[20]	[21, 22]	[23]	[24-26]	**This work**
Physical support	No	Yes	No	No	No	Yes
Physical mechanism	Ion migration theory	Quantum tunneling theory	No	Ion migration theory	No	Defect state filling theory
Model complexity	Easy	Complex	Medium	Medium	Complex	Medium
Applied range	Wide	Narrow	Wide	Wide	Narrow	Wide

$Ag/BaTiO_3/LaNiO_3$ memristor was prepared using sol-gel method, and its performance test indicated that ERSM behavior was led by the light-assisted Schottky tunneling mechanism.

However, current memristive devices have been suffering from geometry variation and process variation, thus leading change of performance parameters and restricting their device integration and application [13]. The modeling of a memristor aims to correlate the electrical properties with the underlying physical mechanisms [14]. Once the memristor model is constructed the performance parameters of the memristor model remain constant. As a result, most applied research on memristors always using their mathematical models [15]–[17]. A simple linear memristor model based on ion migration theory was proposed by D. Strukov's team in HP Laboratory in 2008 [18]. On this basis, a nonlinear memristor model considering the boundary effect was proposed in [19]. A more accurate physical model based on quantum tunneling theory was proposed in [20]. This model is however quite complicated, without an explicit relationship between current and voltage, and is also computational inefficient. Inspired by [20], a new memristive device model was presented—TEAM (ThrEshold Adaptive Memristor model) [21]. Notably, this model is flexible and can be fit to any practical memristive device. Since a voltage-controlled memristor was more suitable in parallel memristor-based application circuits, a Voltage ThrEshold Adaptive Memristor (VTEAM) model extending the previously proposed TEAM model was proposed [22]. In 2017, a novel experiment-based memristive model considering the drifting effect, the diffusing effect, and the negative differential resistance (NDR) behavior was presented [23]. In addition, some researchers [24]–[26], based on the Chua theory, used traditional analog circuit components to build a memristor simulation circuit, to simulate the basic characteristics of memristor.

For clarity, the comparative information of different memristor models is collected and summarized in Table I. It can be concluded that although all these above-mentioned models can reflect the basic characteristics of the memristor, the physical mechanism between the model and the real memristor is still a knowledge gap. Meanwhile, the electrochemical characteristics of the real memristor cannot be fully characterized.

In this paper, a flexible memristor model with electronic resistive switching memory behavior is constructed. The main contributions are as follows:

1) The Ag-Au/$MoSe_2$-doped Se/Au-Ag memristor is prepared using hydrothermal synthesis method and magnetron sputtering method. Meanwhile, the corresponding performance test via electrochemical workstation is conducted to explore the ERSM behavior, which serves as a frame of reference for the subsequent model construction.

2) Unlike many existing memristor modeling techniques, the mathematical model and SPICE circuit model of the Ag-Au/$MoSe_2$-doped Se/Au-Ag memristor are built up, based on the electrochemical data derived from the performance test. It opens up a novel path for the deep integration of physical memristors into neuromorphic computing systems and energy-efficient integrated circuits.

3) Based on the constructed memristor model, a circuit implementation of spiking neural network with long/short term synaptic plasticity is presented and verified by the handwritten digits recognition task, which provides a practical case study for the development of neuromorphic computing systems.

The rest of the paper is organized as follows. In Section II, an Ag-Au/$MoSe_2$-doped Se/Au-Ag memristor is fabricated and the performance of which is tested by the electrochemical workstation CHI-600D. In Section III, the mathematical and circuit models are established by analyzing the physical mechanism of memristors, and the simulation experiments show that the proposed models can have high accuracy. Section IV designs a compact spiking neural network circuit with memristor-based synapse and neuronal cells to classify the MNIST dataset. Section V concludes the work and future work will be provided.

II. FABRICATION AND EXPERIMENT

A. Preparation of Ag-Au/$MoSe_2$-doped Se/Au-Ag Memristor

In this paper, Ag-Au/$MoSe_2$-doped Se/Au-Ag memristor is prepared based on hydrothermal synthesis and magnetron sputtering methods, in which hydrothermal synthesis method is

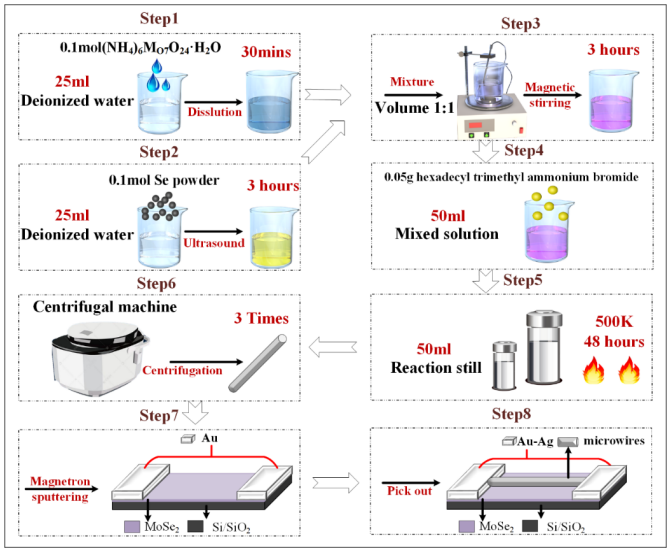

Fig. 1. Flow chart for the preparation of Ag-Au/$MoSe_2$-doped Se/Au-Ag memristor.

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used to prepare $MoSe_2$-doped Se microwires and magnetron sputtering method is used to prepare Ag-Au electrodes, with details as shown in Fig. 1.

Step 1: 0.1moL ammonium molybdate $(NH_4)_6Mo_7O_{24}\cdot H_2O$ is dissolved in 25mL deionized water, stirred for 30 minutes at room temperature until it is completely dissolved.

Step 2: 0.1moL Se powder is dispersed in 25mL deionized water and sonicates continuously for 3 hours.

Step 3: Sonicated Se powder dispersed liquid and ammonium molybdate solution are mixed in a 1:1 ratio by volume and stirred continuously for 3 hours with a magnetic stirrer, until the mixture is completely mixed.

Step 4: 0.05g hexadecyl trimethyl ammonium bromide (i.e., the surfactant) is added to the stirred solution.

Step 5: The mixture is transferred to a 50mL Teflon-lined container, fixed by a still reactor with a corresponding size, heated at 500K for 48 hours in a blast oven, and then cooled to room temperature.

Step 6: $MoSe_2$-doped Se microwire is obtained by centrifugation at room temperature for 3 times.

Step 7: Magnetron sputtering is used to fabricate Au electrodes with a spacing of 400μm and an area of $50\times50\mu m^2$ pre-deposited on the Si/SiO_2 substrate.

Step 8: A single microwire is picked out using a four-probe test system, the ends of which are lapped onto the Au electrode and covered with a layer of Ag adhesive to form an Ag-Au/ $MoSe_2$-doped Se/Au-Ag memristor.

B. Performance Test of Ag-Au/$MoSe_2$-doped Se/Au-Ag Memristor

An electrochemical workstation CHI-600D is used to test the I–V and resistance curves of Ag-Au/$MoSe_2$-doped Se/Au-Ag memristor at room temperature. Fig. 2(a) shows the measured I–V curve of Ag-Au/$MoSe_2$-doped Se/Au-Ag memristor with a ±3V bias voltage scan rate of 0.05V/s, and the inset is a structural representation of the prepared memristor. The overall I–V curve shows that the characteristics of memristors are asymmetrical in the positive and negative voltage regions, and there is no current jump. That is, the prepared memristor exhibits ERSM behavior. In the first stage, the memristor is in the high resistance state (HRS). As the scan voltage increases from 0V to 1.5V, there is very little change in the device current and when the applied voltage exceeds 1.5V, the current starts to increase with the scan voltage and reaches a maximum at 3V, meaning that the memristor changes from HRS to low resistance state (LRS), and the "SET" process is completed. In the second stage, the memristor remains in LRS while the scan voltage decreases from 3V to 0V. In the third stage, LRS of the memristor remains unchanged as the scan voltage is reversed from 0V to −3V. In the fourth stage, the current gradually decreases from a negative maximum as the scan voltage changes from −3V to 0V. When the scan voltage is higher than −1.5V, the memristor changes from LRS to HRS, meaning that the "RESET" process is completed. Reference [6] suggests that the asymmetric contact between the interface of Ag-Au and $MoSe_2$ doped Se microwires, mainly caused by the asymmetric distribution of free defects Mo^{4+} in the microwires and the

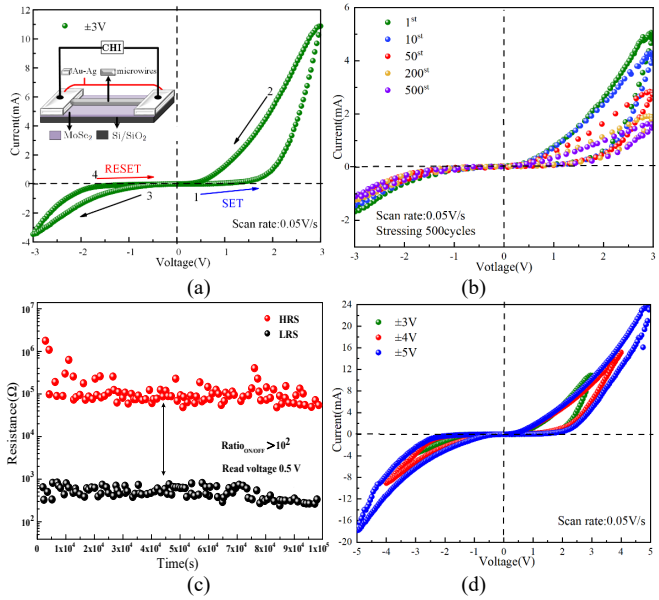

Fig. 2. (a) I-V curve of Ag-Au/$MoSe_2$-doped Se/Au-Ag memristor. The inset is a structural representation of the prepared memristor; (b) Measurements of cyclic scan for the I-V curves; (c) The stability of HRS and LRS of the prepared memristor over time at 0.5V; (d) I-V curves of the memristor with different amplitudes of voltages.

asymmetric distribution of other impurity defects in the Se microwires themselves, may lead to the ERSM behavior in memristor. The I–V curves for the 1st, 10th, 50th, 200th and 500th cycles are shown in Fig. 2(b). It can be seen that this continuously varying asymmetry in the positive and negative voltage regions is well maintained, although the corresponding curves decay from 50th cycle onwards, indicating that the dominant ERSM mechanism remains unchanged. To study the stability of the device, a 0.5 V reading voltage is applied both in the high resistive state and low resistive state for 10^5 seconds, as shown in Fig. 2(c). A resistance ratio between the high resistive state and low resistive state of over 10^2 can be maintained during the retention time indicating that the prepared memristor has good stability. The I–V curves of the device at different scan voltages are shown in Fig. 2(d). The continuity and asymmetry of the I–V curve at different scan voltages is unchanged, which indicates that the variations of voltage only change the degree of filling of electrons in the microwire with deep and shallow trappings.

III. Memristor Modeling

A. Analysis of the Physical Mechanism of the Memristor

The ERSM behavior observed in Ag-Au/$MoSe_2$-doped Se/Au-Ag memristors is dominated by trapping and detrapping of charges in the empty state, satisfying space-charge limited current (SCLC) mechanism [27] with the following mathematical expressions:

$$J \propto \frac{V^{m+1}}{L^{2m+1}} \tag{1}$$

where J is the current density, V is the external voltage, L is the microwire's length and m is the fitting parameter. In particular, when $m = 0$, the current is linearly related to the voltage, meaning that it satisfies Ohmic or Ohmic-like Conduction.

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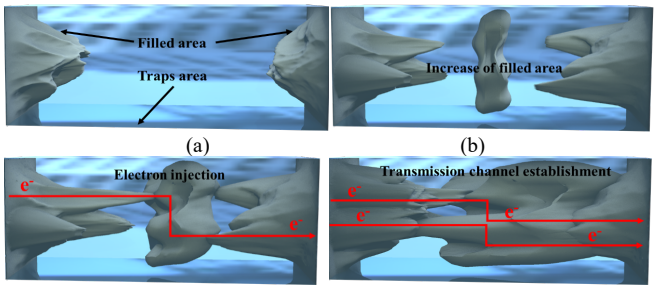

Fig. 3. (a) Traps being empty; (b) Traps being gradually filled; (c) Traps just being filled with charge; (d) A transport channel is established through injected electrons in the empty traps in the microwire.

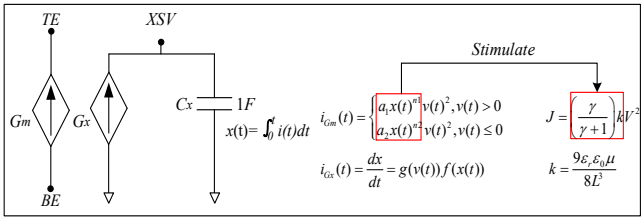

Fig. 4. An equivalent circuit for the memristor model.

The structure of the SCLC mechanism for trapping and detrapping of charges is shown schematically in Fig. 3, where the blue region indicates the empty traps, and the grey region indicates that the empty traps have been filled with electrons.

In the initial state, the traps are empty (as shown in Fig. 3(a)); after the external voltage is applied to the memristor, the traps are gradually filled (as shown in Fig. 3(b)); as the applied voltage increases, the traps are fully filled (as shown in Fig. 3(c)); after which electrons are injected from the Ag-Au side and a transport channel is established through the electrons in the empty traps (as shown in Fig. 3(d)).

According to the SCLC mechanism, when the fitting factor m = 1, (1) can be rewritten as:

$$J=\left(\frac{\gamma}{\gamma+1}\right)kV^2 \tag{2}$$

$$k=\frac{9\varepsilon_r\varepsilon_0\mu}{8L^3} \tag{3}$$

where J is the density of the current, γ is the ratio of the number of free electrons in the microwire to the number of electrons captured in the empty traps, ε_r and ε_0 are the relativity permittivity and vacuum permittivity respectively, μ is the carrier mobility, and L is the length of the microwire.

In the initial state, as the applied voltage is very low, most of the traps are empty. When γ<<1, (2) can be expressed as $J=\gamma kV^2$, the memristor is in HRS. When the applied voltage exceeds the forward threshold voltage, all the empty traps are filled with electrons injected from the electrodes, and the memristor transforms into LRS, which means that the device completes the SET process. When the empty traps are filled, the electrons in the empty traps have less influence on the subsequently injected electrons and the current increases rapidly. When the reverse voltage is applied to the memristor, the conductive channel formed by the filled empty traps still exists and the device remains LRS until the applied voltage is less than the negative threshold voltage. When the conductive channel formed in the empty traps is broken and the device is transformed into HRS, indicating that the device completes the RESET process.

TABLE II
SUB-CIRCUIT DESCRIPTION OF THE MEMRISTOR MODEL

```
* Memristor model
**XSV-External connection to plot state variable that is not used otherwise**
.SUBCKT Memristor model TE BE XSV PARAMS:
+a1=0.0015 a2=−1.709E−4 n1=1.696 n2=−0.12 Vth1=1.5 Vth2=−1.5
+x0=0.01 Ap=1 An=−0.117 xp=0.3 xn=0.5 Alphap=1 Alphan=5
**********Function dx/dt=F(x(t),v(t))**********
.func wp(x,xp)={(xp-x)/(1-xp)+1}
.func wn(x,xn)={x/(1-xn)}
.func G(v,Vth1,Vth2,An,Ap)={if(v>=Vth1,Ap*(exp(v)-exp(Vth1)),
+if(v<=Vth2, -An*(exp(Vth2)-exp(-v)),0))}
.func f1(x,xp,Alphap)={if(x>=xp,exp(-Alphap*(x-xp))*wp(x,xp),1)}
.func f2(x,xn,Alphan)={if(x<=(1-xn),exp(Alphan*(x+xn-1))*wn(x,xn),1)}
.func F(x,v,xp,xn,Alphap,Alphan)={if(v>=0,f1(x,xp,Alphap),
+f2(x,xn,Alphan))}
**********IV Response – Hyperbolic sine due to MIN structure********
.func IVRel(x,v,a1,a2,n1,n2)={if(v>=0,a1*(x^n1)*v^2,a2*(x^n2)*v^2)}
Gm Plus Minus value={IVRel(V(x),V(Plus,Minus),a1,a2,n1,n2)}
**********Circuit to determine state variable**********
Gx 0 x value={F(V(x),V(Plus,Minus),xp,xn,Alphap,Alphan)*
+G(V(Plus,Minus),Vth1,Vth2,An,Ap)}
Cx x 0 1 IC={x0}
Raux x 0 1T
ENDS Memristor model
```

B. *Demonstration of PSpice Analysis*

Based on the above analysis, an equivalent circuit for the memristor model is proposed in this paper, including G_m, G_x, two current sources and C_x, a capacitor with a capacitance of 1F. The terminals TE and BE represent the top and bottom electrodes of the memristor, where the model would be connected in a circuit schematic. The equivalent circuit is shown in Fig. 4.

From the circuit, the current and voltage relationship can be described by:

$$i_{Gm}(t)=\begin{cases}a_1x(t)^{n1}v(t)^2, v(t)>0\\ a_2x(t)^{n2}v(t)^2, v(t)\le 0\end{cases} \tag{4}$$

where $v(t)$ denotes the applied voltage, $i_{Gm}(t)$ denotes the current passing through the memristor, a_1, a_2, n_1, and n_2 are the fitting parameters of the model so that the I–V curve of this mathematical model approximates the actual physical model. $x(t)$ with the range of [0,1] is the state variable, characterizing the conductivity of the device. The value of the state variable $x(t)$ is derived from the integration of the current $i_{Gx}(t)$ over time, and such an integration process is accomplished in the equivalent circuit through the capacitor C_x. The $a_1x(t)^{n1}$ and $a_2x(t)^{n2}$ terms are used to stimulate the dynamics of the $k\gamma/(\gamma+1)$ term in the SCLC mechanism with respect to the applied voltage.

The change of the state variable depending on two different functions $g(v)$ and $f(x)$ can be mathematically expressed by:

$$i_{Gx}(t)=\frac{dx}{dt}=g(v)f(x) \tag{5}$$

where $g(v)$ is used to model the voltage threshold behavior of the memristor. $f(x)$ is the window function mainly used to ensure that the state variable $x(t)$ is always in the range of [0,1].

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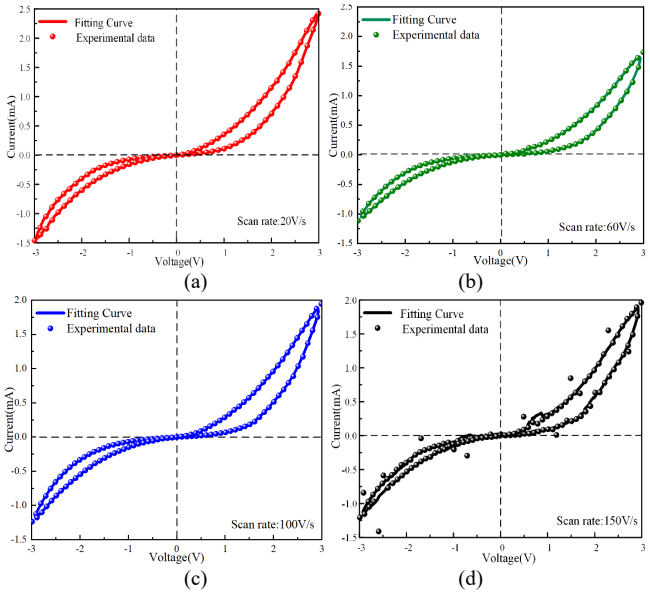

Fig. 5. Simulation and fitting results of measured data of different voltage scanning rates of memristor (a) scanning rate of 20V/s; (b) Scanning rate 60V/s; (c) Scanning rate 100V/s; (d) Scanning rate: 150V/s.

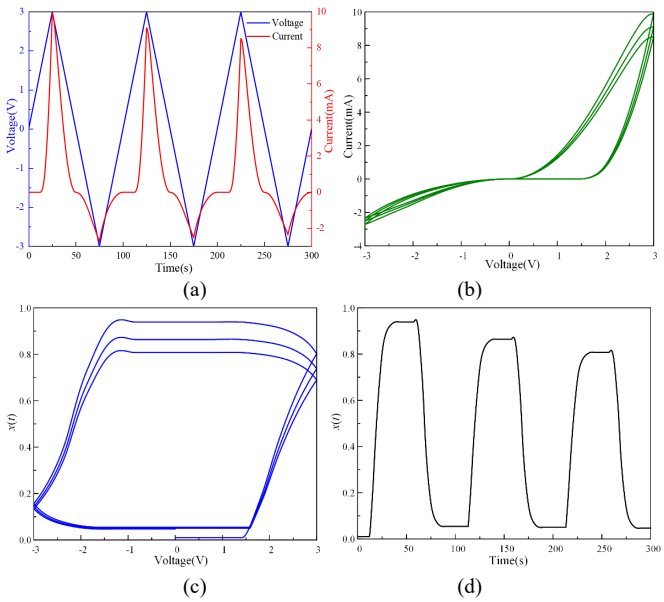

Fig. 6. The simulation results of proposed memristor model (a) V&I–t; (b) I–V; (c) x–V; (d) x–t.

Specifically, $g(v)$ is expressed as follows:

$$g(v)=\begin{cases} A_p\left(e^{v(t)}-e^{v_{th1}}\right), v(t)>v_{th1} \\ -A_n\left(e^{v_{th2}}-e^{v(t)}\right), v(t)<v_{th2} \\ 0, \quad v_{th2}\leqslant v(t)\leqslant v_{th1} \end{cases} \tag{6}$$

where v_{th1} and v_{th2} denote the forward threshold voltage and reverse threshold voltage of the memristor respectively, and the state variable only changes when the voltage applied to the memristor is greater than the threshold voltage. A_p and A_n are the fitting parameters, and the larger their magnitude, the faster the rate of change of the state variable of the memristor when the change conditions are met.

It should be noted that in (5), a totally different window function [28] is used, with $f(x)$ being expressed specifically as follows:

$$f_+(x)=\begin{cases} \omega_p\left(x,x_p\right)e^{-\alpha_p(x-x_p)}, x\geqslant x_p \\ 1, \quad x<x_p \end{cases} \tag{7}$$

$$f_-(x)=\begin{cases} \omega_n\left(x,x_p\right)e^{-\alpha_n(x+x_n-1)}, x\leqslant 1-x_n \\ 1, \quad x>1-x_n \end{cases} \tag{8}$$

where x_p and x_n are the upper and lower boundary thresholds for the state variables respectively. Notably, when the applied voltage is positive, the state variable is limited by an exponential function decaying with a rate of α_p. On the other hand, when the applied voltage is negative, the state variable is limited by an exponential function decaying with a rate of α_n. In particular, when the values of the state variables do not reach the threshold values x_p and x_n, the value of the window function is a constant term of 1, that is, the window function does not affect the rate of change of the state variables.

$\omega_p(x, x_p)$ and $\omega_n(x, x_n)$ are the two boundary functions to ensure that the value of the state variable does not exceed the upper and lower limits.

$$\omega_p\left(x,x_p\right)=\frac{x_p-x}{1-x_p}+1 \tag{9}$$

$$\omega_n\left(x,x_n\right)=\frac{x}{1-x_n} \tag{10}$$

Based on the above theoretical description and mathematical derivation, a SPICE model of the memristor is proposed with its corresponding sub-circuit description, as shown in Table II.

C. Simulation Analysis of the Memristor Model

In order to measure how the experimental data of the Ag-Au/$MoSe_2$-doped Se/Au-Ag memristor fits to the constructed circuit model in this paper, we use Gradient Descent to minimize the relative error function value [29]. The error function is selected as relative root mean squared error (RRMSE):

$$E_{rms}=\sqrt{\frac{1}{N}\cdot\left(\frac{\sum_{k=1}^{N}\left(V_k-V_{ref,k}\right)^2}{V_{ref}^2}+\frac{\sum_{k=1}^{N}\left(I_k-I_{ref,k}\right)^2}{I_{ref}^2}\right)} \tag{11}$$

where N is the total number of samples, V_k and $V_{ref,k}$ denote the k_{th} voltage applied to the real memristor and its circuit model, respectively. I_k and $I_{ref,k}$ present the k_{th} current through the real memristor and its circuit model, respectively. V_{ref} and I_{ref} are the Euclidean norm of the voltage and current of the circuit model, respectively.

The fitting results of the memristor are shown in Fig. 5, where the solid spheres represent the experimental data obtained from the Ag-Au/$MoSe_2$-doped Se/Au-Ag memristor at different scan voltages, while the solid lines represent the I–V curves of the constructed circuit model with a scan voltage at the amplitude of 3V. In this paper, sequential model-based global optimization (SMBO) [30] is used to obtain the following parameters of the circuit model: a_1=1.500×10^{-3}, a_2=−1.709×10^{-4}, n_1=1.696, n_2=−0.121, A_p=1, A_n=−0.117, x_p=0.3, x_n=0.5, α_p=1, α_n=5, v_{th1}=−v_{th2}=1.5V. Fig. 5(a) shows the

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TABLE III
COMPARATIVE SUMMARY OF DIFFERENT MEMRISTIVE MODELS

Model	Linear ion model [18]	Nonlinear ion model [19]	Simmons model [20]	TEAM model [21]	VTEAM model [22]	Fang model [23]	**This work**
State variable	$0\leqslant x\leq D$ Doped region physical width	$0\leqslant x\leq 1$ Doped region physical width	$a_{off}\leqslant x\leq a_{on}$ Undoped region width	$a_{off}\leqslant x\leq a_{on}$ Undoped region width	$a_{off}\leqslant x\leq a_{on}$ Undoped region width	$0\leqslant x\leq 1$ No physical explanation	$0\leqslant x\leq 1$ Conductivity of the device
Control mechanism	Current	Voltage	Current	Current	Voltage	Voltage	Voltage
I-V relationship	Explicit	Explicit	Ambiguous	Explicit	Explicit	Explicit	Explicit
Physical mechanism	IMT	IMT	QTT	Ambiguous	Ambiguous	Ambiguous	DSFT
Model Complexity	Easy	Medium	Complex	Medium	Medium	Medium	Medium
Boundary effects	Unsolved	Solved	Solved	Solved	Solved	Unsolved	Solved
Threshold effects	No	No	Yes	Yes	Yes	No	Yes
Fitting accuracy	Lowest	Low	Highest	Moderate	Moderate	Moderate	High

Note: IMT→Ion migration theory; QTT→Quantum tunneling theory; DSFT→Defect state filling theory.

simulation results of the device at a scan rate of 20 V/s. The RRMSE obtained after fitting to the experimental data is 0.14%. Compared with the I–V curve in Fig. 2(a), the device at 20 V/s does not change significantly, in terms of the curve's shape and the maximum current. When the voltage scan rate increases to 60V/s and 100V/s, the asymmetry of the I–V curve and the continuous current variation can be both maintained, with the exception of a slight reduction in the maximum current, from 2.5mA to 1.9mA, as shown in Fig. 5(b) and Fig. 5(c). These fitted curves are matched to the target data, and the RRMSEs are calculated as 0.26%. When the scan rate is added to 150 V/s, RRMSE rises to 4.26% and the shape of I–V curve is basically fitted except for some noise points, as shown in Fig. 5(d). The scan rate mainly reflects the response of the interface defect state to the voltage polarity variation. From the experimental data, the interface defect state makes a relatively small contribution to the ERSM behavior of the microwire device, and only when the scan rate reaches 150V/s or more does it have a significant effect on the device.

In Fig. 6(a), when a triangular-wave voltage is applied to the memristor, the overall current through the memristor gradually decreases, because of the charge at deep traps which influences the scattering of injected electrons. From Fig. 6(b), the I–V relationship are hysteresis loops with overlap between adjacent loops, which are asymmetrical in the positive and negative voltage regions, and the memristor exhibits ERSM characteristics. Meanwhile, the state variable $x(t)$ of the memristor is changed with the external excitation voltage, as shown in Fig. 6(c). When the external excitation voltage is less than the threshold voltage ($v_{th2}<v<v_{th1}$), the memristor remains in HRS. Until the threshold condition is satisfied, the memristor changes from HRS to LRS, and the state variable gradually increases (decreases) influenced by the positive (negative) voltage. From Fig. 6(d), it can be seen that the state variable $x(t)$ is in a decreasing trend, which is consistent with the change of the current and is in line with the characteristics of the physical memristor.

D. Comparison with Previously Proposed Models

A comparative summary of different memristive models is given in Table III. From Table III, different memristor models (e.g., Linear ion model[18], Nonlinear ion model [19], Simmons model[20], TEAM model[21], VTEAM moddel[22], and Fang model [23]) are used to reflect the characteristic of the physical memristive device. However, these models seldom consider the physical mechanism of the real memristor and the physical phenomena including the ERMS behavior. Compared with other works, the proposed model is a simple, flexible and convenient model that can be used to characterize a practical memristive devices. The proposed model exhibits a voltage threshold and nonlinear dependences on the state variable which alleviates the boundary effects and shows a ERSM behavior. While the simplicity of this model improves the efficiency of the simulation process, the model is sufficiently accurate, exhibiting a relative root mean squared error of only 0.14% as compared to the other memristive device models. This model fits practical memristive devices better than previously proposed models.

IV. THE APPLICATION OF AG-AU/MOSE2-DOPED SE/AU-AG MEMRISTOR MODEL

A. Memristor Synapse Circuit

Synapses are biological junctions through which the signals of neurons can be exchanged with each other and with non-neuronal cells [31]. The memristors can be programmed into different conductance states and can be used to modulate signals in either forward or backward directions [32]. This property makes the memristor a favorable candidate for achieving electronic synapses and helps obtaining different weighting parameters of a neural network, simply by generating different modulated signals without changing the circuit structure. Based on the proposed memristor circuit model in this paper, a memristor synapse circuit is designed as shown in Fig. 7, where the synapse circuit consists of a pair of memristors and diodes that are connected with a reversed polarity.

For the synapse circuit, the input voltage is added into the connection point of two memristors, and according to Kirchhoff's Current Law [33] the branch current is obtained as follows:

$$\begin{cases} I_A = G_A V_{input} \\ I_B = G_B V_{input} \end{cases} \tag{12}$$

The output current I_{output} equals to the difference between the branch currents I_A and I_B:

$$I_{\text{output}} = I_A - I_B = \left(G_A - G_B\right) V_{\text{input}} = W_G V_{\text{input}} \tag{13}$$

where $W_G=G_A-G_B$.

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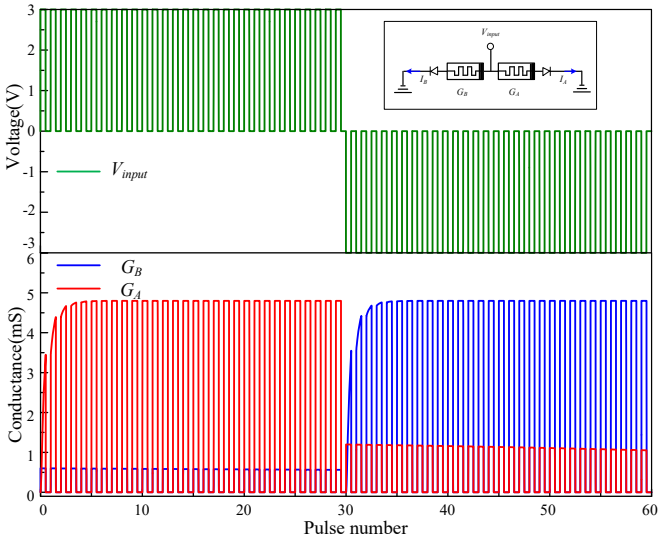

Fig. 7. Simulation results of the memristor synapse circuit.

In this paper, PSpice simulations of the memristor synapse circuit are performed based on the proposed memristor model. The threshold voltage of the memristor is v_{th1}=−v_{th2}=1.5V, the resistance range is from R_{on}=206Ω to R_{off}=325kΩ, and the corresponding conductance range is from G_{on}=4.85mS to G_{off}=3.08μS. The simulation results of the synapse circuit are shown in Fig. 7. When a positive programming signal is applied, the conductance G_B decreases while G_A increases, the corresponding synapse weights change from zero to a positive maximum. When a negative programming signal is applied, the conductance G_A decreases while G_B increases, the corresponding synapse weights change from zero to a negative maximum. Thus, the proposed memristor synapse circuit can be programmed for both positive and negative weights. The range of W_G can be calculated as follows.

$$-4.85\text{mS} = G_{\text{off}} - G_{\text{on}} \le W_G \le G_{\text{on}} - G_{\text{off}} = 4.85\text{mS} \quad (14)$$

In the above synapse operation, when the input voltage is less than the voltage threshold of the memristor, the state of the memristor does not change. Conversely, when the applied voltage is greater than the voltage threshold, the synapse weights can be programmed. When a positive programming voltage is applied, conductance G_B decreases while G_A increases, resulting in an increase in the synapse weight. However, when a negative programming voltage is used, the synapse weight decreases. In the above programming process, since the polarity of the two memristors is reversed, the change in memristors is always reversed, regardless of whether the applied signal is positive or negative. This not only accelerates the weight programming operation, but also ensures that the positive, zero and negative synapse weights can be obtained during successive programming without setting in advance.

The modulation of synapse is the process of applying an electrical signal to update the conductance of memristors from the initial to the target state, so that the synapse weights can meet the requirements. In practice, in order to obtain the high accuracy, pulse-based modulation is usually adopted, changing only a small amount of synapse weights at a time. In this paper, the relationship between memristors' conductance and pulses

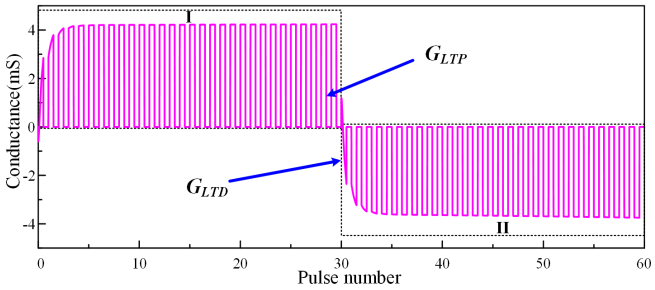

Fig. 8. Modulation process of the weights of the memristor synapse circuit.

obtained from [32] is used, its mathematical expression can be described by:

$$G_{LTP} = B\left(1 - e^{\left(-\frac{P}{A}\right)}\right) + G_{\min} \quad (15)$$

$$G_{LTD} = -B\left(1 - e^{\left(-\frac{P-P_{\max}}{A}\right)}\right) + G_{\min} \quad (16)$$

$$B = \frac{G_{\max} - G_{\min}}{1 - e^{\frac{-P_{\max}}{A}}} \quad (17)$$

where P is the number of pulses required for synapse modulation and A is the fitting parameter of the device. As for LTP and LTD, they represent long-term potentiation and long-term depression, respectively. G_{LTP} denotes the increasing process of conductance (SET process) while G_{LTD} means the opposite (RESET process). G_{max}, G_{min} and P_{max} indicate the maximum conductance, the minimum conductance and the maximum number of pulses corresponding to the processes from SET to RESET.

Fig. 8 shows the modulation process of the designed memristor synapse. Part I and Part II correspond to the increase (G_{LTP}) and decrease (G_{LTD}) of memristor weights, respectively. According to (15) – (17), the parameters of the synapse modulation process can be obtained as follows: G_{max}=4.85mS, G_{min} =3.08μS and P_{max}=60, A=0.42.

B. Neuron Circuit Based on Memristor Synapse

Artificial neurons contain three basic processing units: multiplication, summation, and activation [34]. How to combine the weighted signals from multiple synapses and activate the output is the key to neuron circuit design. In this paper, a memristor neuron circuit is illustrated in Fig. 9(a). It's worth noting that two diodes at the memristor synapse circuit can effectively avoid "snake current" in neuron circuit.

In this circuit, the input voltages can be converted directly into currents by means of the memristor. These weighted currents are then collected directly into the negative terminals of amplifiers A_1 and A_2, and the output voltages V_1 and V_2 are expressed as:

$$\begin{cases} V_1 = -R_f\left(I_{A1} + I_{A2} \ldots + I_{Ai} \ldots + I_{An}\right) \\ V_2 = -R_f\left(I_{B1} + I_{B2} \ldots + I_{Bi} \ldots + I_{Bn}\right) \end{cases} \quad (18)$$

where the signal of branch currents can be expressed as:

$$\begin{cases} I_{Ai} = G_{Ai} V_{\text{input}} \\ I_{Bi} = G_{Bi} V_{\text{input}} \end{cases} \quad (19)$$

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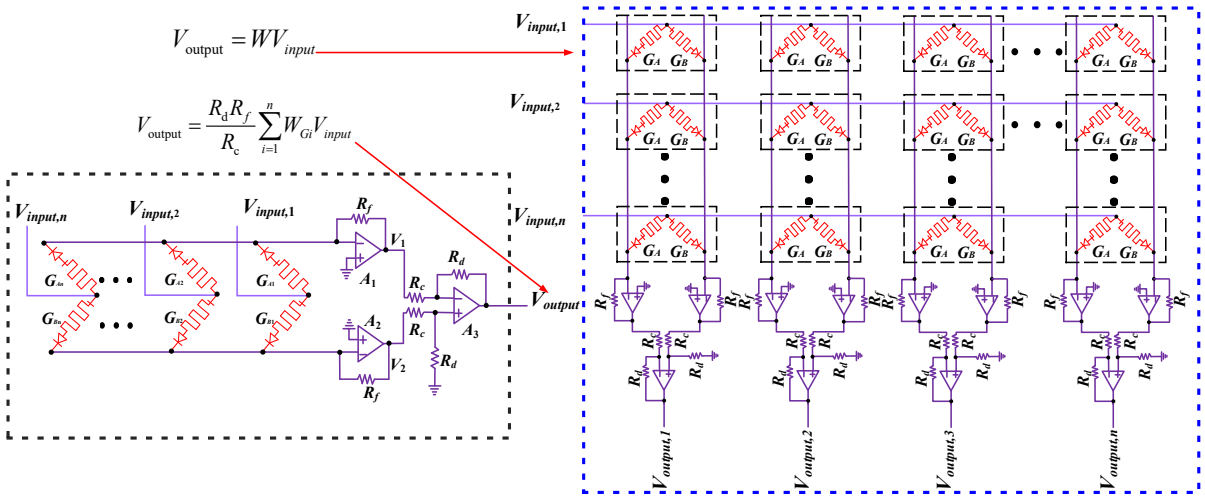

(a) (b)

Fig. 9. (a) Memristor neuron circuit; (b) Memristor crossbar array.

The output voltage of this neuron circuit can be computed by the difference of amplifier voltage V_1 and V_2:

$$V_{output} = \frac{R_d}{R_c}(V_2 - V_1)$$
$$= \frac{R_d R_f}{R_c}\left[\left(G_{A1}V_{input} - G_{B1}V_{input}\right) + \ldots \left(G_{An}V_{input} - G_{Bn}V_{input}\right)\right] \quad (20)$$
$$= \frac{R_d R_f}{R_c}\sum_{i=1}^{n} W_{Gi}V_{input}$$

where W_{Gi}=G_{Ai} –G_{Bi}.

Notably, if the number of synapse arrays and operational amplifiers is further increased, as shown in Fig. 9(b), the multiplication of the input vector and the weight matrix, V_{output}=WV_{input}, can be achieved in one go, which is the most basic and resource-intensive operation in a neural network. In a digital circuit system, parameters are repeatedly read from memory for computation, but in a memristor network, the mapping of input vectors to output vectors can be also done in one go, combining memory and computation in a unit, which is much more efficient. In addition, during the synapse modulation process, the same memristor array can be updated into an arbitrary W parameter matrix, which can be applied to a pulse-based neural network for online learning.

C. Memristor-based Spiking Neural Network for digital handwritten recognition

In fact, a complete memristor-based spiking neural network

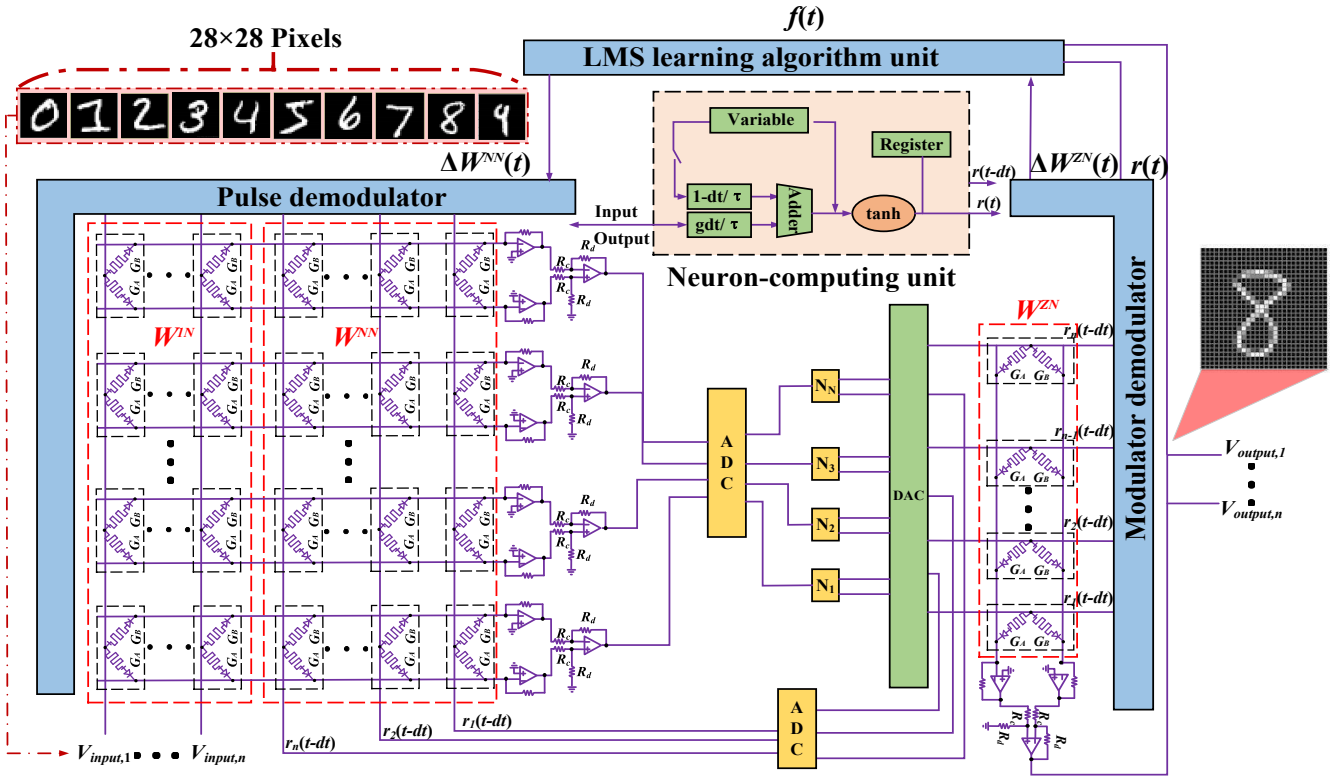

Fig. 10. Memristor-based spiking neural network for digital handwritten recognition.

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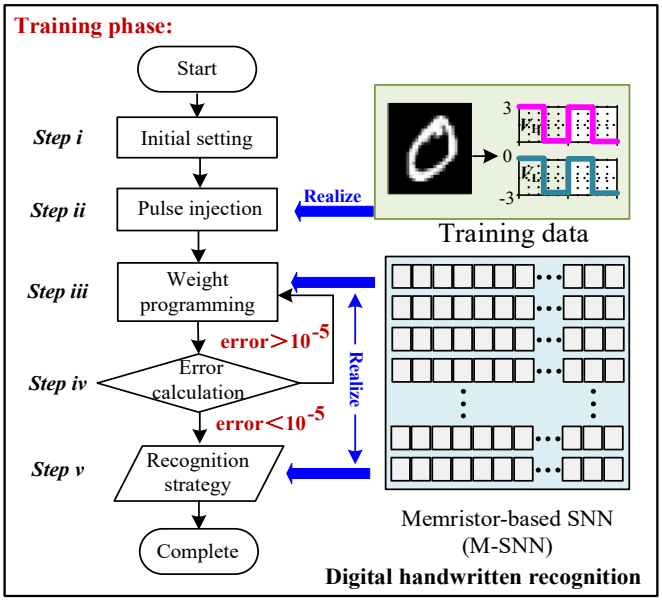

Fig. 11. The flow chart of training phase.

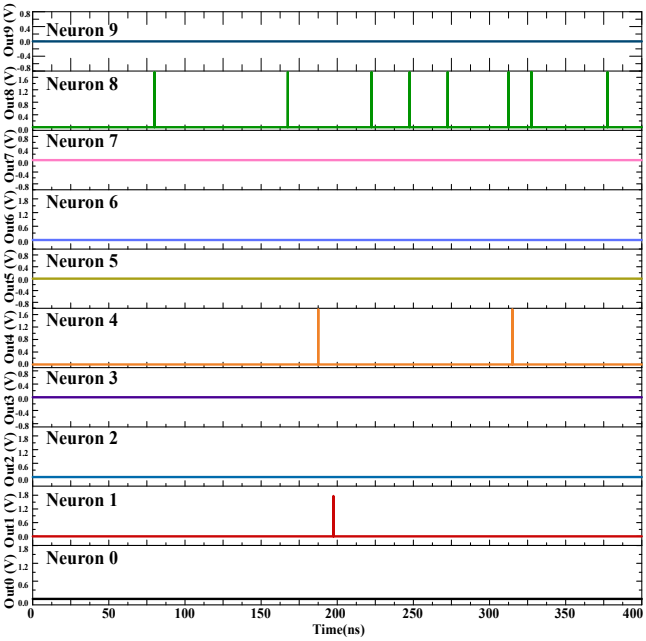

Fig. 12. Simulation results of the generated pulses of the memristor neuron.

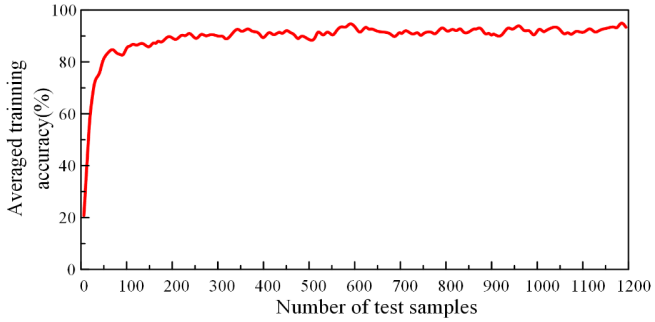

Fig. 13. Variation of network recognition rates with the increased number of samples tested.

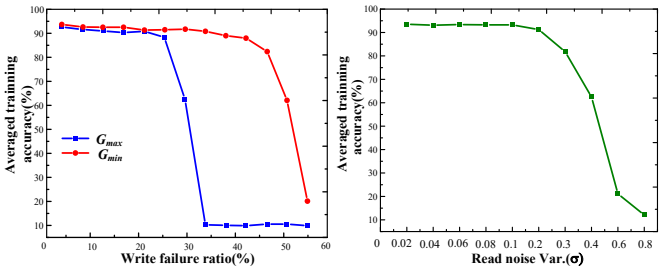

Fig. 14. (a) Effect of the failed device ratio in the array on the network recognition rate; (b) Effect of the read noise on the network recognition rate.

contains extra components (i.e., peripheral circuits). As shown in Fig. 10, besides the memristor array and input/output circuits, memristor-based spiking neural network consists of analog-to-digital converters (ADCs), digital-to-analog converters (DACs), neuron-computing unit, pulse modulator, learning algorithm unit and weight modulator. Specifically, the memristor array implements the vector-matrix multiplication of weight value and input value, neuron-computing unit describes the dynamics of the neurons, the learning algorithm unit calculates the error between the target weight and the actual outputs, and the pulse-based modulator generates the modulated pulses of each memristor to update its state. To improve the energy efficiency for the circuit implementation of spiking neural network, the simplified neuron-computing model proposed in [35] is used. Notably, the circuit implementation of neural network algorithms is still a difficult task, which may be affected by factors such as the scale of circuits and the interaction between circuit components. Hence, the realization of a self-learning neuron circuit designed in [36] is taken to perform online least mean squares (LMS) algorithms. Furthermore, the memristor synapse adopts a pair of reversely-connected memristors, as illustrated in Section IV-A, and the modulation of synapse is based on the relationship between the memristor conductance and pulse introduced in (15) – (17).

The whole circuit is finally completed in PSpice. For the sake of verification, the memristor-based spiking neural network is applied for digital handwritten recognition, and the recognition process is illustrated (as show in Fig. 11).

Step i: Initial setting. This includes the setting of the network parameters as well as the component parameters in the memristor array. The memristor is initialized to a very low conductance by applying voltage pulses to each column of the array.

Step ii: Pulse injection. Each digital image of the MNIST dataset is in 28 × 28 pixels. The grey-scale value of each pixel is encoded as the pulse sequence $V_{input,i}$ and further injected into 10 neurons numbered from 0 to 9.

Step iii: Weight programming. The target weights are programmed by applying different intensity of pulses corresponding to the encoded grey-scale values to each column. The state of each memristor synapse is updated according to (15) – (17), and the programming is performed row by row until all memristors on each selected row have been programmed to the target value. Once the target conductance is achieved, the synapse weights remain constant, and the training of the neural network is completed, at which the network output is

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TABLE IV
COMPARISON OF DIFFERENT MEMRISTOR-BASED NEURAL NETWORK FOR DIGITAL HANDWRITTEN RECOGNITION

Literature	[30]	[35]	[36]	[37]	[17]	**This work**
Memristor model	Ta/TaO_x/Pt memristor	Ta/HfO_2/Pd memristor	Pt/Cu:ZnO/Nb:STO memristor model	Linear ion model	Pt/VO_2/TaO_x/Si memristor	Ag-Au/$MoSe_2$-doped Se/Au-Ag memristor model
Preparation process	✓	✓	✓	×	✓	✓
Number of memristors in a weight	1	1	1	1	1	2
Hardware-based design	Totally	Totally	Partially	Partially	Partially	Totally
Robustness	Not mentioned	Not mentioned	Not mentioned	Not mentioned	Not mentioned	Good
Recognition rate	92.1%	89.9%	91.07%	92.5%	95.2%	95.6%

represented as $V_{output,i}$.

Step iv: Corresponding error calculation:

$$error = \frac{1}{n}\sum_{i=1}^{i=n}\left|V_{input,i} - V_{output,i}\right| \tag{21}$$

Notably, if the error converges to a sufficiently small value (the *error* is previously set as 10^{-5} in this paper), *Step v* is executed. Otherwise, return to *Step iii*.

Step v: Recognition strategy. The output pulses generated by each neuron is counted, and the final recognition result depends on the largest number of the output pulses.

In our experiments, the MNIST dataset contains 6000 samples, where 4800 samples are used for training and the remaining 1200 samples are used for testing. After executing *Step i* - *Step iv*, the training phase is completed. When the 12th test sample (handwritten digit 8) is injected into the well-trained memristor-based spiking neural network, the generated pulses of the output-layer neuron are shown in Fig. 12. It can be seen that Neuron 1, Neuron 4 and Neuron 8 generate one, two and eight pulses respectively, while the remaining seven neurons do not generate any pulses. Since the recognition result is determined by the largest number of pulses generated by the neuron, the recognition result is number 8.

The variation of the recognition rate with the number of test samples is exhibited in Fig. 13. It can be seen that when the number of samples is 200, the recognition rate is approximately 92.4% and when 1200 samples are tested, the recognition rate becomes 95.6%.

To verify the robustness of the proposed neural network, this paper sets a certain ratio of failed devices (assuming in the lowest or highest conductance state) in the array. As shown in Fig. 14(a), when the device is in a low conductivity state and its failure rate is less than 25%, the recognition rate still greater than 90%; when the device is in a high conductivity state and its failure rate is less than 10%, the recognition rate also maintains over 90%. It can be concluded that the proposed memristor -based spiking neural network has a better tolerance to the failed memristor in a low conductivity state. The main reason may be that high conductance failure tends to produce large error current, which can significantly affect the output of the weighted summation. Conversely, low conductance failure does not produce large current and can be adjusted by the non-failed devices to improve the output of the weighted summation, thus maintaining a good recognition rate despite the large failure rate of the devices.

The read noise always occurs during the period of weight gain. From Fig. 14(b), when the variance of read noise is less than 0.2, the memristor-based spiking neural network maintains a high recognition rate, indicating that the proposed neural network performs well in terms of robustness to noise. Only when the variance of read noise is larger than 0.2, the recognition rate decreases sharply with the noise increasing.

D. Comparison with Previously Proposed memristor-based neural networks

A comparison between different memristor-based spiking neural networks are provided in Table IV.

From Table IV, different memristor models (e.g., Ta/TaO_x/Pt memristor [30], Ta/HfO_2/Pd memristor [35], Pt/Cu:ZnO/Nb:STO memristor model [36], Linear ion model [37], Pt/VO_2/TaO_x/Si memristor [17], and Ag-Au/$MoSe_2$-doped Se/Au-Ag memristor model) are used to realize the circuit design of neural networks for handwritten recngnition. According to [37], Linear ion model cannot accurately characterize the nonlinear behaviors of emerging memristors, which may lead to the instability and inaccuracy. In particular, unlike the other memristor-based neural network implementations, this work provides the specific preparation process of the Ag-Au/$MoSe_2$-doped Se/Au-Ag memristor, which makes the entire circuit design more convincing. Meanwhile, in order to realize the positive, negative and zero weights, almost all the memristor-based neural network implementations use a single memristor to represent a weight and some additional circuit elements are used to realize the negative and zero weights. Compared with other works, this paper uses dual-memristor configuration to represent a weight, which can be obtained during successive programming without setting in advance. Last but not least, compared with the other competitors, this work provides a robust scheme that can perform well in terms of robustness to failed devices and noise, indicating the proposed network achieves similar or even higher recognition rate compared to other works.

V. CONCLUSION

In this paper, a flexible memristor model based on electronic resistive switching memory is investigated. Specifically, the Ag-Au/$MoSe_2$-doped Se/Au-Ag memristor is prepared using hydrothermal synthesis method and magnetron sputtering method, and its performance testing is conducted by electrochemical workstation. Correspondingly, a novel Ag-Au/$MoSe_2$-doped Se/Au-Ag memristor model (including mathematical model and circuit model) derived, based on the electrochemical data obtained from the performance test. The sufficient accuracy of the proposed model as compared with the

experimental data is achieved by tuning the fitting parameters, exhibiting a root mean squared error of 0.14%. Meanwhile, a compact spiking neural network circuit realized by memristor-based synaptic and neuronal circuits is designed with high degree of accuracy. Compared with the existing methods, the proposed memristor-based spiking neural network offers benefits in terms of robustness and hardware friendly. For verification, the proposed method is applied to the handwritten digits recognition. The experimental results demonstrate that the memristor-based spiking neural network has good performance (i.e., accuracy and tolerance) in pattern recognition, achieving a recognition rate of 92.4% considering device failure and external noise.

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