# A Forward Converter Topology With Independently and Precisely Regulated Multiple Outputs

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***Abstract*—A forward converter topology with independently and precisely regulated multiple outputs is presented in this paper. In this topology, each regulated output has its own feedback control circuit that controls the appropriate synchronous rectifiers in the pertinent output stage. All output circuits are voltage-decoupled from each other, and the cross-regulation between the outputs is eliminated. Steady state analysis as well as small signal modeling is performed to understand the topology and to provide design guidance. A prototype circuit with two outputs is built, and experimental results are presented for proof-of-concept.**

***Index Terms*—Cross regulation, distributed power supply, forward converter topology, multiple outputs, soft switching, zero voltage switching.**

## I. Introduction

FORWARD converter topology has been widely used in telecom and computer systems as the distributed power supply, because of its simple circuitry, low output ripple voltage and high output current capability. However, one of its major drawbacks is the poor regulation in multiple output applications. As advanced telecom systems now require more than one tightly regulated supply voltage for different critical electronic loads on a single circuit board, the standard forward topology is no longer suitable for such advanced applications.

A conventional solution to obtain multiple output regulation in forward topology is to employ a magnetic amplifier (magamp) in each slave output [1]–[3]. It is cost effective when the output voltage is above 5 V. Unfortunately, it is not efficient for very low voltage (e.g., 2 V and lower) applications, because the magamp cannot be used along with synchronous rectifiers. In addition, the saturable core of the magamp brings nonlinear properties into design. The bandwidth of the magamp loop must be kept lower than the main loop to avoid loop interaction [3], and this limits its speed of dynamic response.

In recent years, other post regulation techniques of multiple output forward topologies have been developed [4]–[10]. However, precise regulation in each slave output is hardly obtainable owing to exacting matching and coupling of the magnetics. Moreover, they are rather complicated in analysis and difficult to design due to complex cross regulation. Their small signal models [11]–[13] are complicated and make the loop design hard [14].

There are some precisely regulated multiple-output forward-type topologies using the pre-regulator-post-regulator approach. The post-regulator can be a linear regulator [1], a buck converter [15], or a synchronous switch post regulator (SSPR) [16], [17]. The linear regulator option is cheap but lossy [1], and the output current is limited below 1.5 A. The buck converter post-regulator is more efficient than the linear one. However, it involves an additional stage of power conversion, and this sacrifices the overall efficiency. The additional second-stage converter spoils the natural simplicity of forward topology, and increases the costs. The SSPR is basically a simplified version of a buck converter in which the buck switch is placed directly in series with the pre-regulator rectifier, and this will reduce the costs. But, the two-component rectifier of SSPR reduces the efficiency as the load current increases. Above all, all these post regulators will lose output regulation when the main output runs into discontinuous mode.

A frequent practice in industry is to use several converter modules, the so-called point-of-use-power-supplies (PUPS)—each independently producing a well-regulated supply voltage. This approach is nevertheless bulky and costly because of the high costs of PUPSs and much of the precious on-board space taken by multi-modules.

This paper presents an improved multiple-output forward converter topology that can overcome the aforementioned drawbacks. The major features of the proposed topology include:

i) independent and precise regulation of each output voltage by an independent feedback control circuit for each output;
ii) elimination of cross regulation by voltage decoupling between the outputs, and inherent immunity to short circuit conditions;
iii) instantaneous response in regulation of the output voltages against the input voltage variations by using feed-forward control of the main switch;
iv) single stage conversion to maintain the simplicity of forward topology;
v) soft switching operation when employing the resonant auxiliary circuit.

Steady state and small signal analyses are performed to understand the topology and its performance. Based on the analyses, a design procedure of the power circuit is generated, and implementation of the feed-forward and feedback controls is addressed. A prototype converter is built with two outputs

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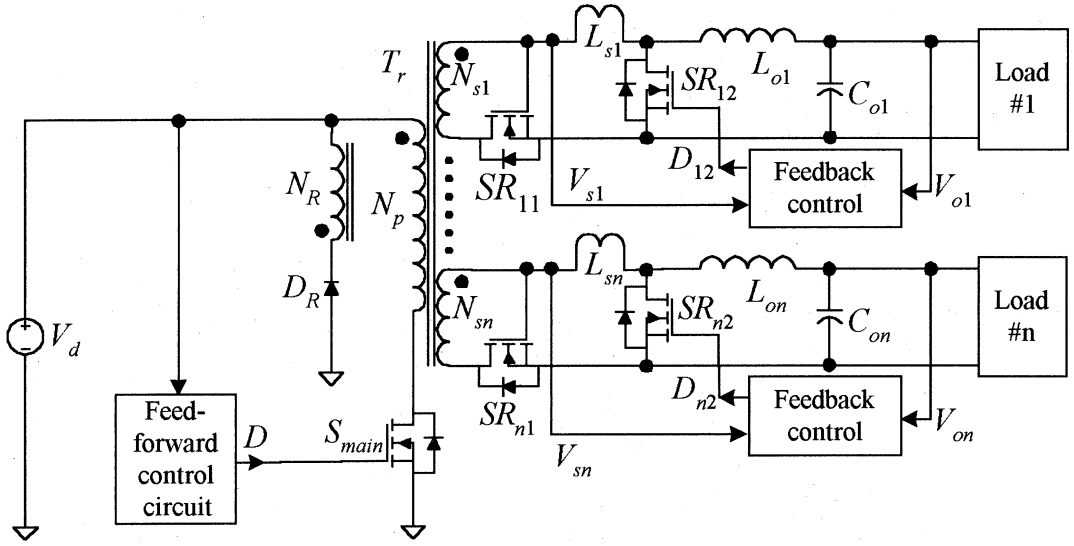



Fig. 1. Proposed independently regulated multiple output forward converter topology.

(5.0 V 30 W and 2.0 V 24 W) operating under the input voltage range from 35 V to 75 V dc and running at a switching frequency of 200 kHz. Experimental results are given for proof-of-concept.

## II. Description of the Proposed Topology

Fig. 1 shows the proposed multiple-output forward converter topology. It consists of the following blocks:

i) power transformer $T_r$;
ii) main switch $S_{\rm main}$;
iii) multiple output sub-circuits;
iv) feed-forward control circuit controlling $S_{\rm main}$.

All the output sub-circuits have identical structures and are parallel-connected to $T_r$. For the arbitrary $k^{th}$ output ($k = 1$ or $2, \ldots$), it consists of the following:

i) an output filter formed by $L_{ok}$ and $C_{ok}$;
ii) a pair of Synchronous Rectifiers (SRs), $SR_{k1}$ and $SR_{k2}$;
iii) a small voltage decoupling inductor $L_{sk}$;
iv) a feedback circuit controlling the shunt SR, namely $SR_{k2}$.

Basically, on the primary side, the feed-forward control circuit generates PWM signal for the main switch in such a way that constant volt-second unidirectional pulses are produced. Therefore, the converter can achieve instantaneous output regulation against the input dc bus voltage variations. On the secondary side, all output circuits are voltage-decoupled from each other by the decoupling inductors in order to eliminate cross-regulation, and each pair of SRs acts as a chopper that chops the said unidirectional voltage pulses. For each output circuit, the pertinent feedback circuit modulates the chopping interval, or the simultaneous conduction interval of the pair SRs, to obtain the output voltage regulation against its load variations.

## III. Operating Principle and Steady State Analysis

Fig. 2 shows key waveforms of the steady state operation of a two-output converter of the proposed topology in Fig. 1. It can easily be extended to more outputs. For the generic steady state analysis (for arbitrary $k_{th}$ output circuit), the following assumptions are made.

i) The input dc voltage $V_d$ and output voltage $V_{ok}$ are constant.
ii) The load current $I_{ok}$ is constant.
iii) The switching frequency is $f_s$.
iv) The circuit is in the continuous conduction mode.
v) The components have linear properties.
vi) The leakage inductances of $T_r$ are negligible.
vii) $L_{ok}$ and $C_{ok}$ make an ideal output filter.

In steady state, each output circuit goes through five modes per cycle. Fig. 3 shows the active current paths in these five modes.

### A. Main Switch ON (Duty-Ratio D)

As soon as $S_{main}$ is ON, the front SR that is driven by a transformer winding is also turned on. The circuit goes through the following three modes.

*Mode 1 ($SR_{k1}$ is ON, $SR_{K2}$ is OFF but its Body Diode Conducts.):* At the beginning of this mode, $S_{main}$ and $SR_{k1}$ are turned ON, and $SR_{k2}$ is OFF. Due to the series voltage decoupling inductor $L_{sk}$, the secondary current $i_{sk}$ rises gradually from zero. Fig. 3(a) shows the active current paths in this interval.

Since the current through the output inductor is nearly constant, the body diode of $SR_{k2}$ is forced to conduct until $i_{sk}$ rises to take over all the output inductor current. In this mode, $L_{sk}$ sees a constant voltage and $i_{sk}$ is governed by

$$i_{sk}(t) = \frac{N_{sk} V_d}{N_p L_{sk}} (t - t_1). \tag{1}$$

This mode terminates when $i_{sk}$ reaches the value of the output inductor current, or approximately the $k^{th}$ output current $I_{ok}$ if

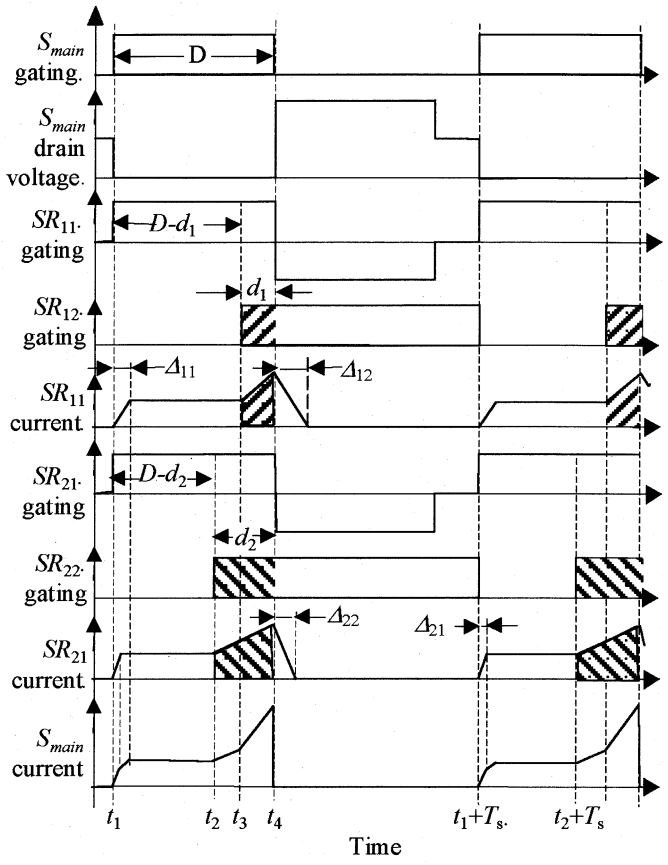



Fig. 2. Key waveforms of a two-output converter of the proposed topology of Fig. 1.

the inductor is very large. Therefore, the duration of this mode, expressed in a fraction of a switching period, is determined by

$$\Delta_{k1} = \frac{N_p f_s L_{sk}}{N_{sk} V_d} I_{ok}. \tag{2}$$

*Mode 2 ($SR_{k1}$ is ON, $SR_{k2}$ is OFF.):* At the beginning of this mode, $i_{sk}$ reaches $I_{ok}$, and the body diode of $SR_{k2}$ becomes reverse biased. The total output inductor current now flows through $SR_{k1}$, and the power is transferred from the input to the load as in a conventional forward converter. Fig. 3(b) shows the active current paths in this interval.

This mode terminates when $SR_{k2}$ is turned ON to regulate the output voltage by the feedback circuit at some time ahead of the end of the ON state of $SR_{k1}$. The duration of this mode is determined by $(D - \Delta_{k1} - d_k)$, where $d_k$ is the duration of the next mode.

*Mode 3 ($SR_{k1}$ is ON, $SR_{k2}$ is ON.):* At the beginning of this mode, $SR_{k2}$ is turned ON ahead of the end of $D$ by an interval $d_k$. Because $SR_{k1}$ is still ON, both SRs now conduct simultaneously, and this creates a short-circuit. Fig. 3(c) shows the active current paths in this interval.

This short-circuit condition chops off the excessive portion from the voltage pulse seen on the secondary side, and in this way the output voltage is regulated. Hence, the effective pulse width, or effective duty-ratio, is governed by

$$D_{eff\_k} = D - d_k - \Delta_{k1}. \tag{3}$$

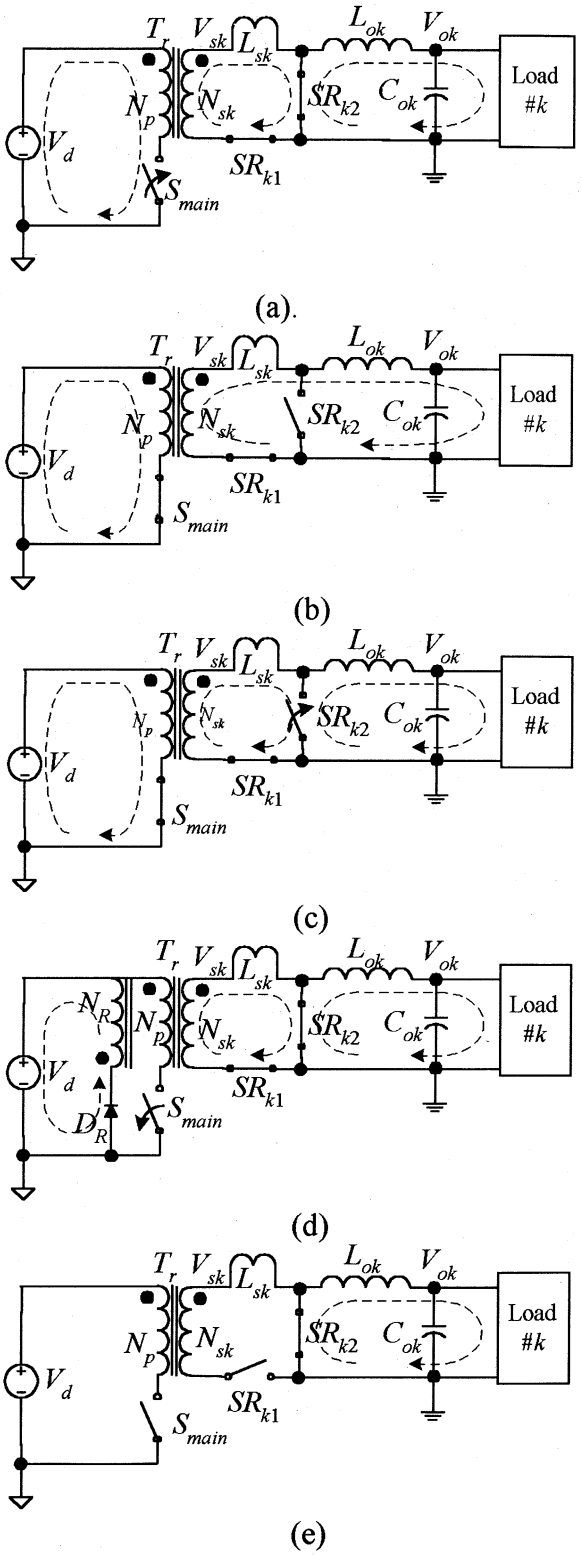



Fig. 3. Active current paths in the five steady state operation modes of the $k^{th}$ output circuit, (a) Mode 1 (Duration: $\Delta_{k1} = f_s L_{sk} I_{ok} / n_k V_d$), (b) Mode 2 (Duration: $D - \Delta_{k1} - d_k$), (c) Mode 3 (Duration: $d_k$), (d) Mode 4 (Duration: $\Delta_{k2}$), and (e) Mode 5 (Duration: $1 - D - \Delta_{k2}$).

Thanks to the inductor $L_{sk}$, this short circuit condition is decoupled from the power transformer $T_r$, and the voltages across all windings do not collapse. Therefore, the cross-regulation between different outputs is eliminated.

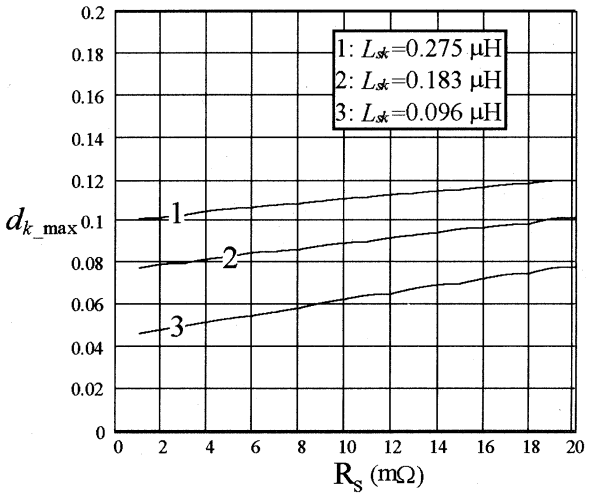



Fig. 4. Maximum simultaneous conduction interval $d_k$ of the pair SRs in the 2 V 24 W output circuit versus the Thevenin equivalent source resistance $R_{sk}$ and the decoupling inductor $L_{sk}$.

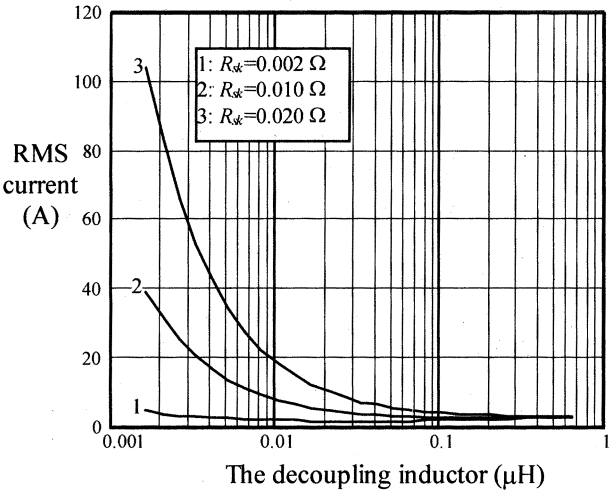



Fig. 5. Rms current through the pair SRs of 2 V output circuit under no load condition.

$L_{sk}$ now sees the pertinent secondary voltage, the secondary current will rise again as governed by

$$i_{sk}(t) = \frac{N_{sk}}{N_p}\frac{V_d}{L_{sk}}\left(t - \frac{D - d_k}{f_s}\right) + I_{ok}. \tag{4}$$

This mode is terminated by turning off the main switch. The duration of this mode is $d_k$. At the end of this mode, $i_{sk}$ reaches a peak value given by

$$I_{peak} = I_{ok} + \frac{N_{sk}}{N_p}\frac{V_d}{L_{sk}}\frac{d_k}{f_s}. \tag{5}$$

### B. Main Switch OFF

*Mode 4 ($SR_{k1}$ is OFF but its Body Diode Conducts, $SR_{k2}$ is ON.):* At the beginning of this mode, $S_{main}$ is turned OFF by the feed-forward control circuit, then the voltage polarity of each windings of the power transformer reverses. Thus, the front SR in each output circuit is also turned off. Fig. 3(d) shows the active current paths in this interval.

However, due to $L_{sk}$, the secondary current can not stop instantaneously, and the body diode of the front SR ($SR_{k1}$) is forced to conduct the residual current in $L_{sk}$. As the shunt SR ($SR_{k2}$) is already ON, $L_{sk}$ starts to see the negative secondary voltage. Hence, $i_{sk}$ starts to decrease.

This mode finishes when the residual current drops to zero, and the duration of this mode can be found approximately to be $\Delta_{k1} = (\Delta_{k2} + d_k)$..

*Mode 5 ($SR_{k1}$ is OFF, $SR_{k2}$ is ON.):* This is the last mode of one switching cycle. In this mode, the shunt SR is in freewheeling of the total output inductor current. Fig. 3(e) shows the active current paths in this interval. The duration of this mode is $(1 - D - \Delta_{k1} + d_k)$.

### C. Steady State Characteristics

Each output circuit can be represented by a Thevenin equivalent circuit, and the output voltage as the function of the load current can be expressed as

$$V_{ok} = V_{sk} - R_{sk}I_{ok} \tag{6}$$

where $V_{sk}$ and $R_{sk}$ are the Thevenin equivalent source voltage and resistance of the $k^{th}$ output circuit, respectively, and

$$V_{sk} = \frac{N_{sk}}{N_p}V_d(D - d_k - \Delta_{k1}). \tag{7}$$

Seen from (6) and (7), the output voltage can be regulated against load variations by modulating $d_k$, or the simultaneous conduction interval of the pair of SRs.

Solving from (2), (6) and (7), it is found that the simultaneous conduction interval shall be governed by the following equation in order to regulate the output voltage

$$d_k = D - \frac{N_p}{N_{sk}}\frac{V_{ok}}{V_d} - \frac{N_p(f_sL_{sk} + R_{sk})}{N_{sk}V_d}I_{ok}. \tag{8}$$

$d_k$ represents the duration of the short-circuit condition. Because a large current may be produced in this condition, it is important to minimize the maximum $d_k$ in design. If the main switch duty ratio is programmed to satisfy

$$D = \frac{N_p}{N_{sk}}\frac{V_{ok} + (R_{sk} + f_sL_{sk})I_{ok\_max}}{V_d} \tag{9}$$

where $I_{ok\_max}$ is the maximum load current, then (8) becomes

$$d_k = \frac{N_p(f_sL_{sk} + R_{sk})}{N_{sk}V_d}(I_{ok\_max} - I_{ok}) \tag{10}$$

and this sets $d_k$ at zero under the full load condition. Hence, the conduction losses can are minimized.

Also seen from (10) is that $d_k$ increases with the equivalent source resistance $R_{sk}$. Because $R_{sk}$ is mainly determined by the Rds(ON) of the SR MOSFETs, to minimize $d_k$ requires the use of low Rds(ON) MOSFETs for the SRs.

To illustrate these characteristics, the 2 V 24 W output circuit of the example circuit given below is used. Fig. 4 shows maximum simultaneous-conduction-interval of the pair SRs as a function of the circuit parameters. When $R_{sk}$ selecting the lowest Rds(ON) MOSFETs, the maximum $d_k$ that occurs at no load can be kept lower than 5% of a switching cycle.

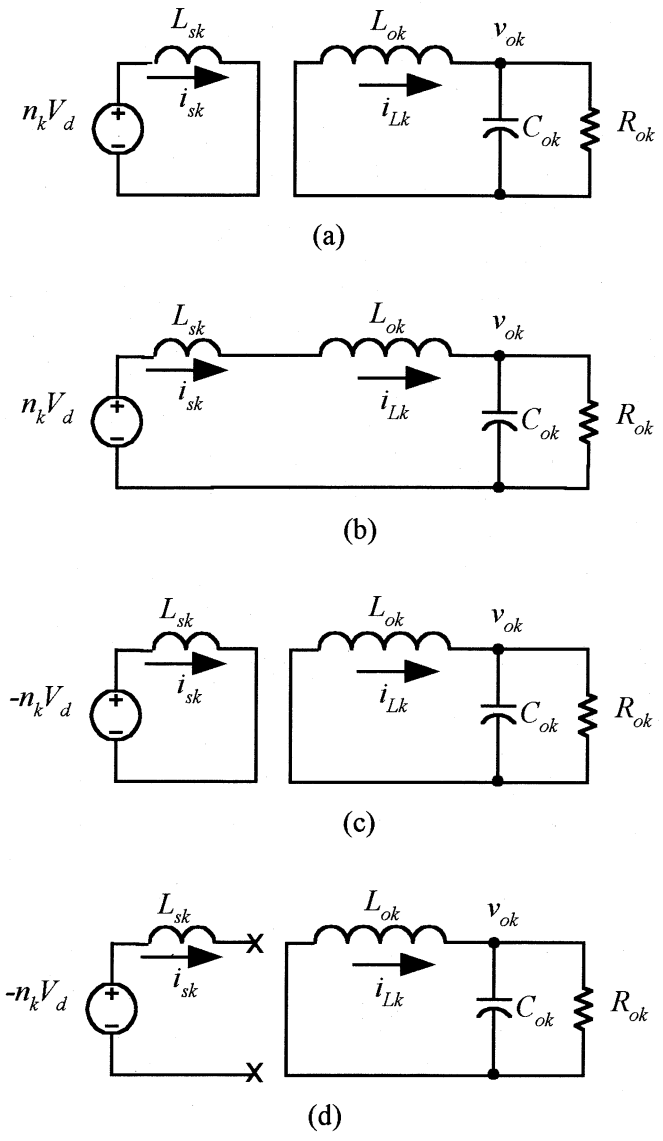



Fig. 6. Four equivalent circuits of the five modes in the k$^{th}$ output circuit (k = 1 or 2 in the two-output example). (a) Modes 1 and 3 (Duration: $\Delta_{k1} + d_k$). (b) Mode 2 (Duration: $D - \Delta_{k1} - d_k$. (c) Mode 4 (Duration: $\Delta_{k2}$). (d) Mode 5 (Duration: $1 - D - \Delta_{k2}$).

However, a minimized $d_k$ alone does not guarantee a minimized conduction losses. The decoupling inductor $L_{sk}$ is another critical factor determining the peak current or conduction losses. A decrement in $L_{sk}$ will reduce $d_k$ as seen in (10), on the other hand, a decrement in $L_{sk}$ will increase the peak current and also the conduction losses as seen in (5). A better way to show the influence of $L_{sk}$ on the conduction losses is to observe the rms current resulted from the simultaneous conduction losses. To highlight this influence, the rms current through the SRs under no load condition is investigated. Fig. 5 shows the rms current in the SRs as a function of $L_{sk}$ and $R_{sk}$ under no load condition. It is seen that $L_{sk}$ shall not be too small, otherwise excessive rms current would be resulted from the simultaneous conduction interval.

In summary, when the circuit is designed properly, the short circuit interval can be limited, and excessive rms current or conduction losses can be prevented.

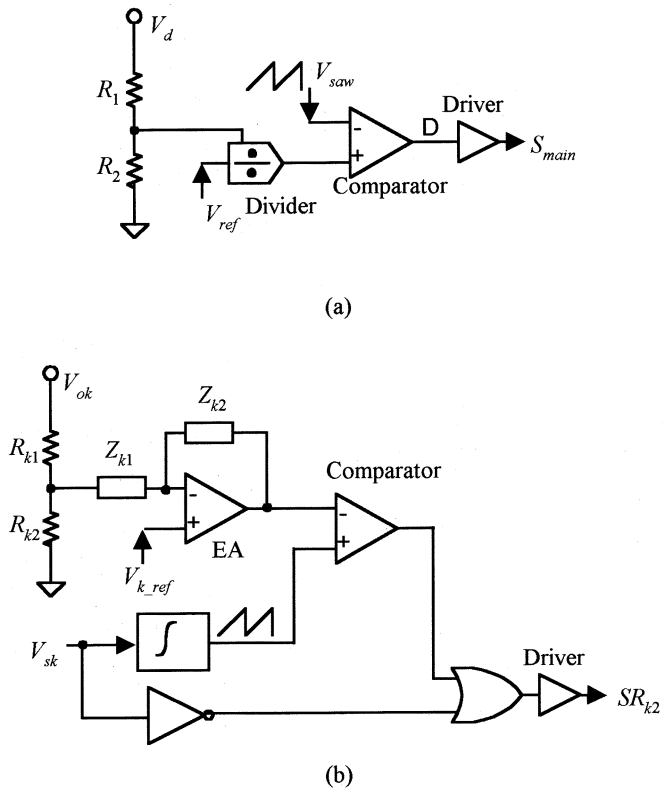



Fig. 7. Control implementations. (a) The feed-forward control. (b) The feedback control.

## IV. Small Signal Analysis

Fig. 6 shows the four equivalent circuits representing the five modes. Based on the equivalent circuits, and noting the duty-ratio of $SR_{k2}$ is $D_{k2} = 1 - D + d_k$, one can obtain the averaged state space model of the $k^{th}$ output circuit as

$$\begin{cases} L_{ok}\frac{di_{Lk}}{dt} = -\nu_{ok} + \left(1 - D_{k2} - \frac{n_k f_s L_{sk} I_{ok}}{V_d}\right)\frac{V_d}{N_k} \\ C_{ok}\frac{d\nu_{ok}}{dt} = \frac{\nu_{ok}}{R_{ok}} - i_{Lk} \end{cases} \tag{11}$$

where $n_k$ is the transformer turns ratio, i.e., $n_k = N_p/N_{sk}$.

From (11), the small signal transfer function from the control of $SR_{k2}$ to the output is found to be as

$$\frac{\hat{\nu}_{ok}(s)}{\hat{d}_k(s)} = \frac{\frac{-V_d}{n_k}}{s^2 L_{ok}C_{ok} + s\frac{L_{ok}}{R_{ok}} + \left(1 + \frac{f_s L_{sk}}{R_{ok}}\right)}. \tag{12}$$

Similarly, when the ESR of the output capacitor $C_{ok}$, namely $R_{kESR}$, is considered, the transfer function becomes

$$\frac{\hat{\nu}_{ok}(s)}{\hat{d}_k(s)} = \frac{-(1+sR_{kESR}C_{ok})\frac{V_d}{n_k}}{s^2 L_{ok}C_{ok}\left(1+\frac{R_{kESR}}{R_{ok}}\right) + s\left[\frac{L_{ok}}{R_{ok}} + R_{kESR}C_{ok}\left(1+\frac{f_s L_{sk}}{R_{ok}}\right)\right] + \left(1+\frac{f_s L_{sk}}{R_{ok}}\right)}. \tag{13}$$

## V. Design Procedure and Control Implementation

A design procedure can be generated based on above analyses.

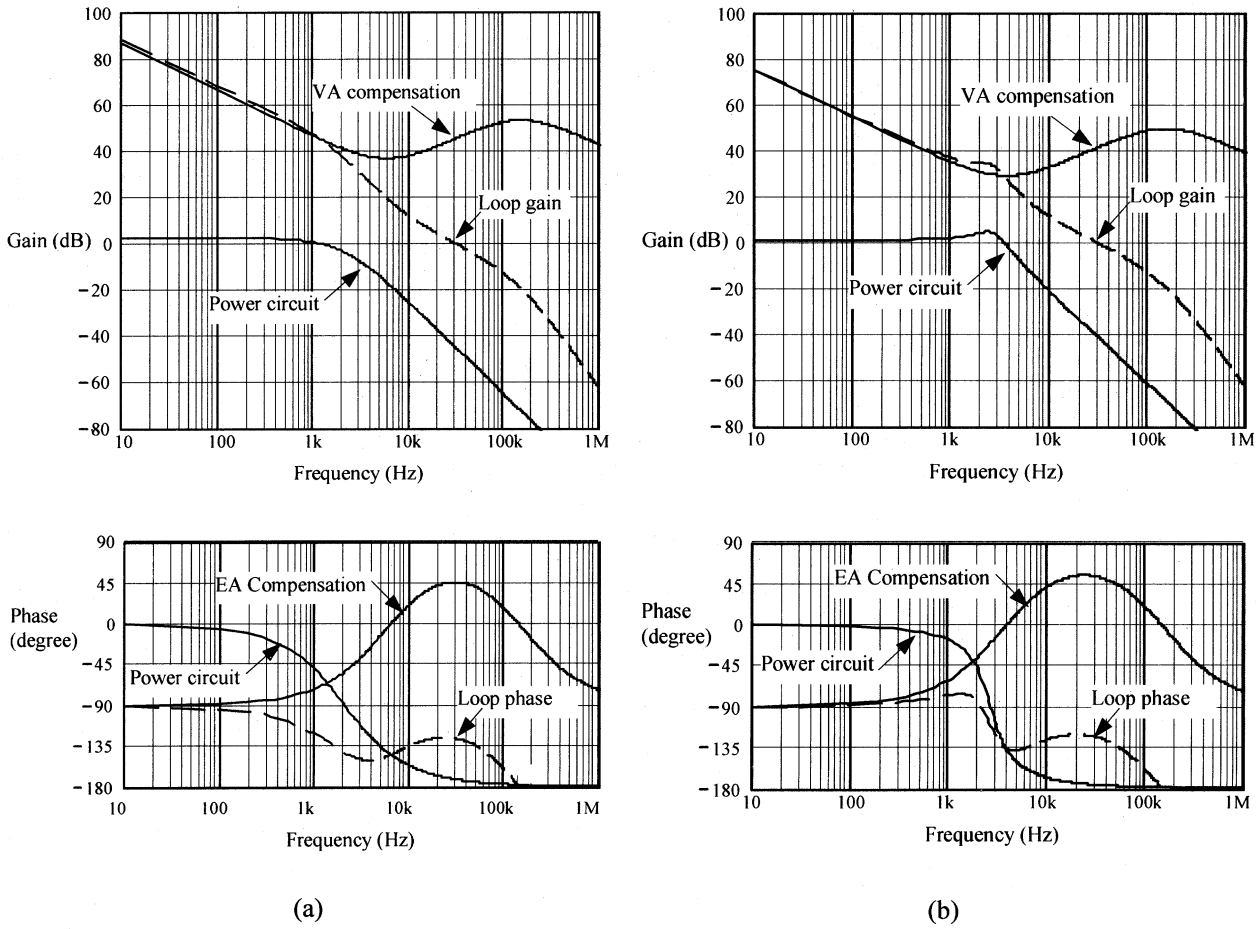



Fig. 8. Bode plots of the open loop transfer functions of both output circuits. a-2 V output circuit, b- 5 V output circuit.

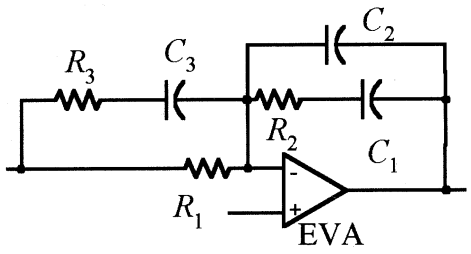



Fig. 9. Type-III error amplifier.

TABLE I
PRINCIPAL PARAMETERS OF THE PROTOTYPE CONVERTER

| Components | Selection | Components | Selections |
|---|---|---|---|
| $T_r$ core | PQ2625-3FC1 | $S_{main}$ | IRF640 |
| $T_a$ core | Gapped SP41408 | $S_{aux}$ | IRF643 |
| $N_p/N_{s1}$ (2V) | 15:2 | $L_a/C_a$ | 1 μH/66 nF |
| $N_p/N_{s2}$ (5V) | 15:5 | $C_{snb}$ | 10 nF |
| SRs (2V) | MTP75N05 (9mΩ) | $D_{a1}/D_{a2}$ | HFA08TB |
| SRs (5V) | IRFZ44 (28mΩ) | $L_{o1}/C_{o1}$ | 12 μH/400 μF |
| $L_{s1}/L_{s2}$ | 0.3 μH/0.9μH | $L_{o2}/C_{o2}$ | 32 μH/100 μF |

### A. Main Switch Duty-Ratio $D$

The main switch duty-ratio determines the magnetizing of the power transformer. In steady state, the magnetizing and demagnetizing intervals of the transformer must maintain volt-second balance. Thus, the maximum $D$ should be limited below 0.5, otherwise the main switch would suffer from excessive voltage stress owing to the resultant high voltage from a short demagnetizing interval.

On the other hand, $D$ shall not be too small, or larger output filter may be required to meet the output voltage ripple specifications. It is a good practice to set the maximum $D$ about 0.45.

### B. $S_{main}$, $SR_{k1}$ and $SR_{k2}$

They should be low Rds(ON) MOSFEFs and meet the power rating requirements.

### C. Transformer Turns Ratio $N_p/N_{sk}$

The selection of a proper turns ratio shall let the secondary winding produce enough voltage. From (6) and (7), one can find that the turns ratio shall satisfy the following inequality:

$$\frac{N_p}{N_{sk}} \le \frac{D_{\max} V_{d\min}}{V_{ok} + (R_{sk} + fsL_{sk})I_{ok}}. \tag{14}$$

Selection of the power transformer core and magnetizing inductance can follow the conventional design procedure.

### D. Decoupling Inductor $L_{sk}$

In a practical circuit, $L_{sk}$ can just be the $T_r$ leakage inductance. The stray inductance seen by the pair SRs can also contribute to $L_{sk}$ total effective value, although it is normally

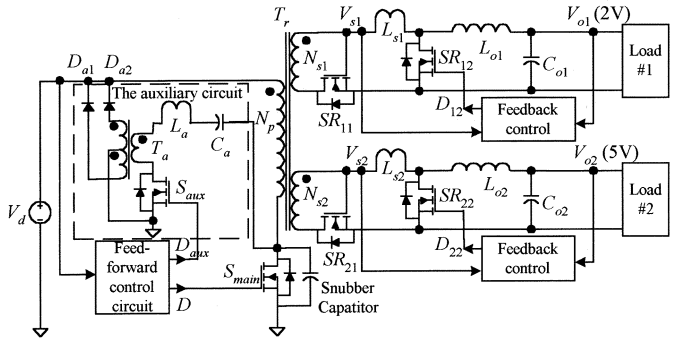



Fig. 10. Prototype converter employing a resonant auxiliary circuit to achieve soft switching.

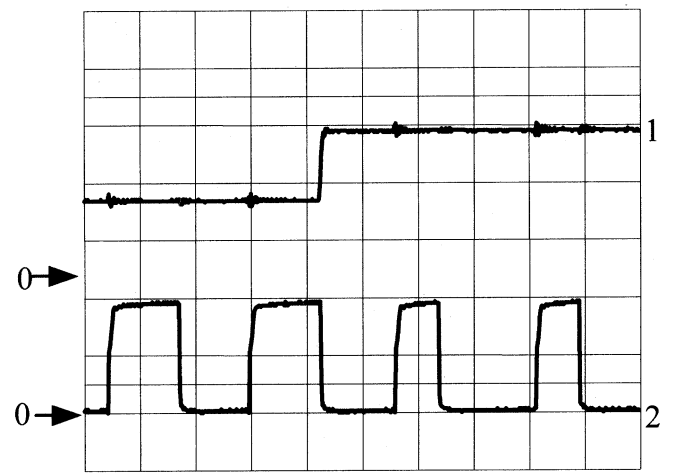



Fig. 11. Main switch duty ratio response to $V_d$ steps from 35 V up to 55 V. $f_s = 200$ kHz. Traces: 1-input voltage (20 V/div.); 2-feed-forward gating command (5 V/div.). Timing-2 $\mu$s/div.

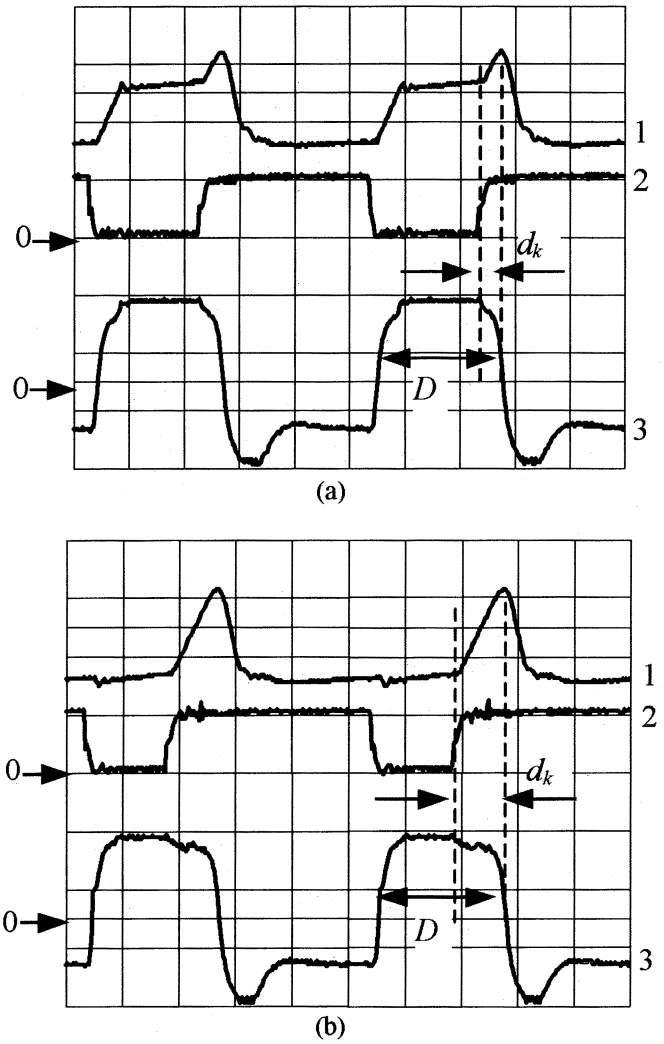



Fig. 12. Front SR current waveform in the 2 V output circuit under different load conditions. $V_d = 55$ V, $f_s = 200$ kHz. Traces:1-front SR current (10 A/div.); 2-gating of the shunt SR (10 V/div); 3-gating of the front SR (10 V/div). Timing-1$\mu$s/div. (a) At full load (12 A). (b) No load (0 A).

negligible. When these parasites are not large enough, an additional inductor shall be added.

Seen from (2) and (3), $L_{sk}$ reduces the effective duty-ratio by $\Delta_{k1}$. Thus, $L_{sk}$ shall not be too big in order to avoid excessive duty-ratio reduction, otherwise a larger output inductor must be employed to meet the output ripples specifications. On the other hand, as seen from (5) and Fig. 5, $L_{sk}$ should not be too small, or excessive rms current and hence excessive conduction losses would be resulted. Therefore, a reasonable tradeoff is to set $\Delta_{k1}$ between 0.05 and 0.1. This determines the inductor to be as

$$L_{sk} = \frac{N_{sk} V_d}{N_p f_s I_{ok}} \Delta_{k1}. \tag{15}$$

Assuming $L_k$ is $T_r$ leakage inductance seen by the pair SRs in the $k^{th}$ output, then the required additional inductor is given by

$$L_{sk\_additional} = \frac{N_{sk} V_d}{N_p f_s I_{ok}} \Delta_{k1} - L_k. \tag{16}$$

It is important to point out that $L_{sk}$ must be prevented from saturation, otherwise it would lose the voltage decoupling function and failure of whole circuit could happen.

### *E. Others*

Design of the output filter can follow the conventional design procedure. The auxiliary circuits used in [19], [20] can be used in the proposed topology to achieve soft switching of the main switch and self-reset of the power transformer, hence improving the converter's overall efficiency at high switching frequency, and simplifying the power transformer.

### *F. Implementation of the Voltage Feed-Forward Control*

As mentioned previously, the feed-forward control circuit shall be programmed to generate gating pulse for the main switch with a duty-ratio satisfying (9).

Fig. 7(a) shows an implementation of the feed-forward control circuit. In the prototype converter, an Analog Device multiplier/divider AD734 is used to perform the inverse function of the input voltage. The output of AD734 is set according to (9) by defining a reference voltage $V_{ref}$, and it is compared with a 200 kHz, 5 V pk-pk saw-tooth signal to generate the PWM signal for the main switch, and a IR2110 driver is used to drive the switch.

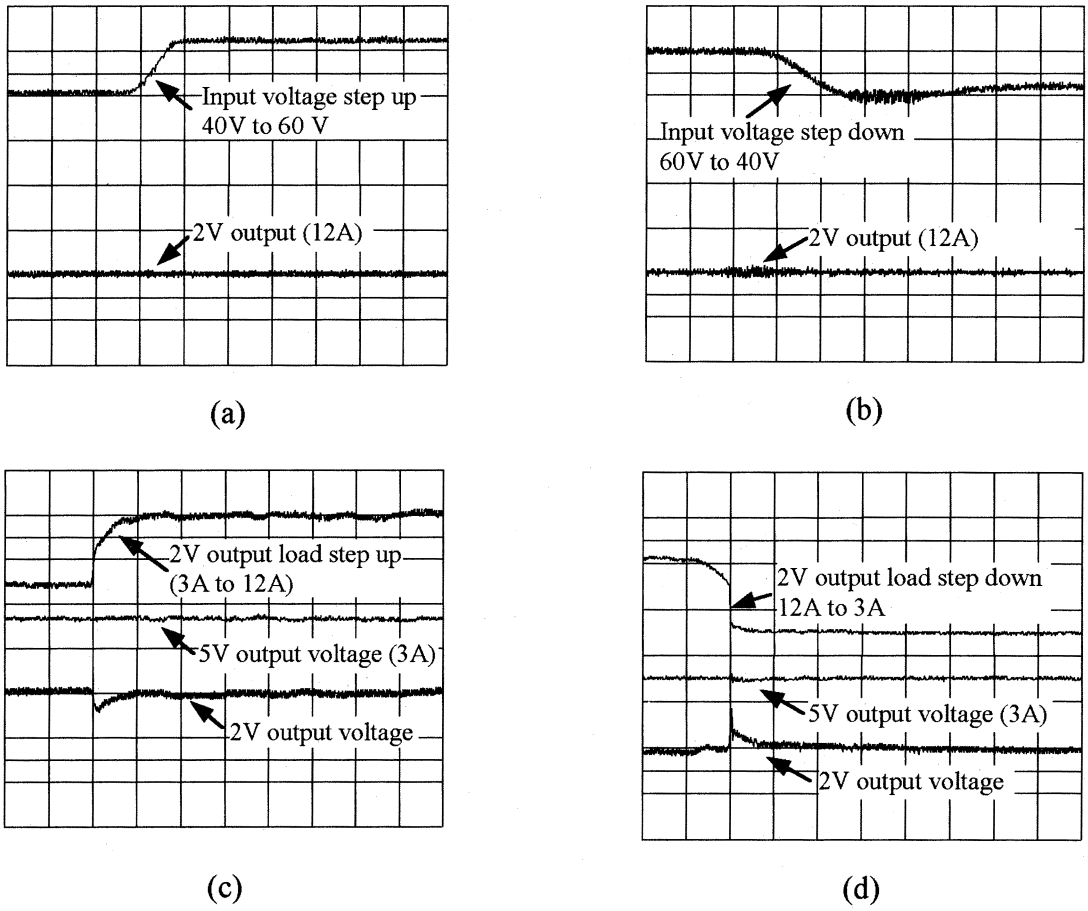



Fig. 13. Output voltage dynamic responses. The time scale: 0.1 ms/div. Vertical scales: 20 V/div. for the input voltage trace, 1 V/div. for the 2 V output voltage trace, and 2 V/div. for the 5 V output voltage trace: (a) input voltage step up, (b) input voltage step down, (c) load step up, and (d) load step down.

### *G. Implementation of Controls of the SRs*

$SR_{k1}$ can be directly driven by the secondary winding as shown in Fig. 1, or be driven by a separate winding if the secondary winding does not produce proper voltage level.

$SR_{k2}$, the shunt SR, is controlled by the feedback circuit. The feedback circuit must modulate the gating of the shunt SR in order to obtained output regulation. In addition, it shall also be synchronized by sensing the transformer secondary voltage, or by sensing the main switch's gating through a pulse transformer.

Fig.7 (b) shows an implementation of the voltage-mode feedback control circuit. It senses the secondary voltage for synchronization, and uses an integrator to generate a triangle or ramped signal for the PWM block.

### *H. Implementation of Closed Loop Compensation*

It is seen from (12) and (13) that, each output circuit of the proposed topology has dynamic properties similar to an ordinary single output dc to dc converter. Thus, the loop compensation for stabilization becomes straightforward [18].

Specifically, for the 2 V 24 W output circuit of the prototype converter, $V_{o1} = 2.0$ V, $R_{o1} = 0.1\ \Omega$, $L_{o1} = 12\ \mu$H, $C_{o1} = 400\ \mu$F, $L_{s1} = 0.3\ \mu$H, $N_p/N_{s1} = 15/2$. For the 5 V 30 W output circuit, $V_{o2} = 5.0$ V, $R_{o2} = 0.83\,\Omega$, $L_{o2} = 32\,\mu$H, $C_{o2} = 100\ \mu$F, $L_{s2} = 0.9\ \mu$H and $N_p/N_{s2} = 15/5$. It is found from (12) that both output circuits have double (conjugated) poles. The double poles of the 2 V circuit are located at 2.05 kHz, and those of the 5 V circuit are at 2.16 kHz. Fig. 8 shows the Bode Plot of the transfer functions of the two-output circuits from their error amplifier outputs to their power circuit outputs.

Selecting the crossover frequency $f_c$ at one sixth of the switching frequency, namely 30 kHz. For the loop stability, the total open loop gain can be tailored having a -20 dB/dec. slope around $f_c$ and an optimal phase margin of 45° with a Type-III error amplifier for the loop compensation. Fig. 9 shows a Type III error amplifier. For the 2 V output circuit, selecting $R_1 = 1$ kΩ, $R_2 = 34$ kΩ, $R_3 = 40.2\ \Omega$, $C_1 = 820$ pF, $C_2 = 27$ pF, and $C_3 = 27$ nF, and this will tailor the total open loop to have a phase margin of 53° and gain margin of about 20 dB. For the 5 V output circuit, selecting $R_1 = 1$ kΩ, $R_2 = 14$ kΩ, $R_3 = 25.5\ \Omega$, $C_1 = 1.5$ nF, $C_2 = 47$ pF, and $C_3 = 33$ nF, and this will tailor the total open loop to have a phase margin of 57° and gain margin of about 18 dB. The Bode Plots of the compensation and total open loop are also shown in Fig. 8.

When ESR of $C_{ok}$ is not negligible, the compensation must be adjusted accordingly. In any case, the proper loop compensation can be readily found in the references like [18], which will not be repeated in this paper.

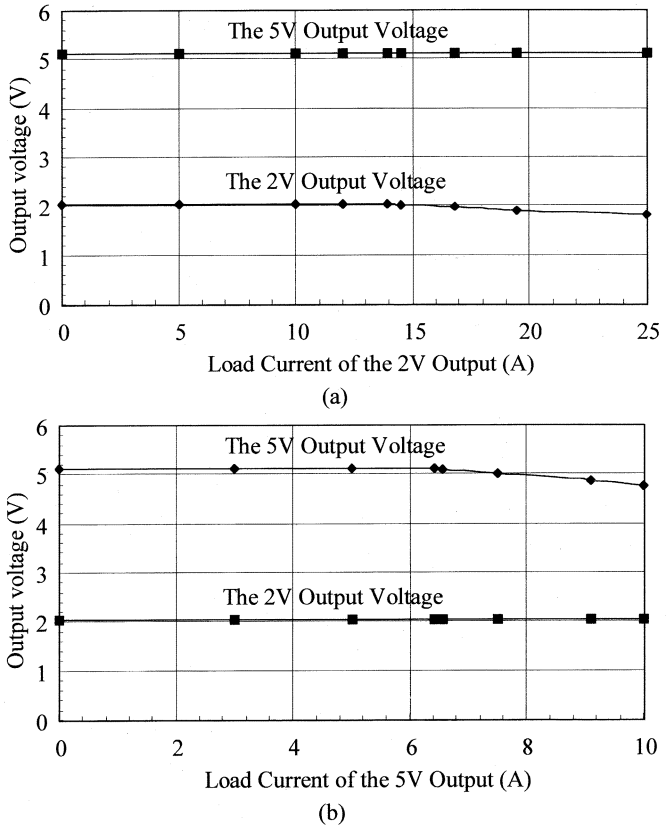



Fig. 14. Experimental results showing the elimination of cross-regulation between the two outputs. (a) Output voltages versus the 2 V output current (the 5 V output current is at 6 A constant). (b) Output voltages versus the 5 V output current (the 2 V output current is at 12 A constant).

## VI. Experimental Results

To prove the concept of the proposed topology, prototype converter is built on the breadboard designed according to above design criteria. The prototype has two outputs, 2 V 24 W and 5 V 30 W, and it is operated at 200 kHz under a input dc voltage ranging between 35 and 75 V. Table I lists all the principle parameters and components of this prototype circuit.

Experiment is carried out based on the breadboard prototype converter.

Fig. 10 shows the prototype converter that employs the resonant auxiliary circuit reported in [19], [20] to achieve soft switching and self-reset of the power transformer. Table I shows key components/devices of the power converter. Fig. 11 shows the main switch gating signal under input voltage step change. It is seen that the feed-forward control circuit reacts instantaneously. This verifies the implementation of the feed-forward circuit.

Fig. 12 shows the gating and drain current of the SRs in the 2 V output circuit under different load conditions. It is seen that the simultaneous conduction interval of the pair SRs increases as the load decreases, confirming with (8). However, despite this simultaneous conduction interval, the peak drain current does not go excessive even at no load thanks to the current limiting by the decoupling inductor.

Fig. 13 shows output voltage under dynamic line and load conditions. It is seen in Fig. 13(a) and 13(b) that the output voltage is simply immune to the disturbance in the input voltage, and this verifies the instantaneous regulation against the input with the feed-forward control.

In Fig. 13(c) and 13(d), it is seen that the load step changes in one output circuit does not affect the other output voltage, experimentally proving the independent regulation of each output and the elimination of cross-regulation.

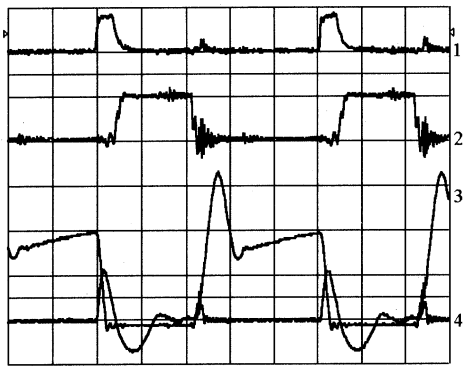
Fig. 14 shows the output voltage regulation against the load currents. It is seen that the voltage regulation of one output is totally independent of the load condition of the other output, indicating the elimination of cross regulation in the proposed topology.

The loss of regulation of the relevant output at very large load current (as shown in Fig. 14) can be explained as follows. Refer to (6) and (7), and note that D is only feed-forward controlled and does not react to the load changes. When the load current increases, the output regulation is achieved by decreasing $d_k$ accordingly to compensate the internal voltage drops. However, when the load current keeps increasing, $d_k$ will decreases to zero and cannot further compensate the internal voltage drops at these excessive load currents. Thus, the output voltage will lose regulation and starts to decrease as the load current increases. The advantage of the loss of regulation in this condition is the inherent overload protection. On the other hand, this does not affect the regulation of the other output because of the elimination of cross regulation.

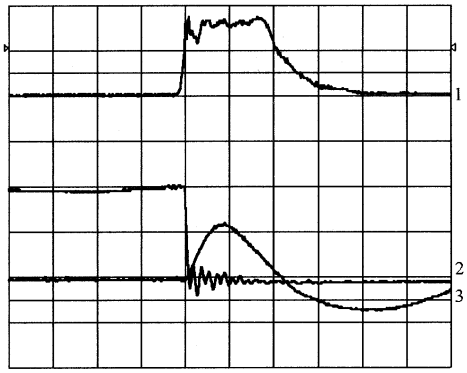
Also obtainable from Fig. 14 is the output resistor of each output circuit, which gives 23.4 m$\Omega$ for the 2 V output and 99.6 m$\Omega$ for the 5 V output, and it reflects the losses on all parts along the secondary current paths, including the SRs, output filters, decoupling inductors, transformer windings, and output inductor, and the circuit tracks. These output resistors are much higher than the SRs Rds(ON) (see Table I). The reasons for this are the poor layout of the breadboard circuit, lack-of copper on the power tracks, and non-optimal magnetics. This also explains the reasons for the tested efficiency given below.

Fig. 15 shows the soft switching being achieved in the main and auxiliary switches. In Fig. 15(a), it is seen that the current of the auxiliary circuit discharges the main switch snubber capacitor before the main switch is turned on, and the gating of the main switch comes after the drain voltage drops to zero, indicating a ZVS turn-on. At turn-off, due to the snubber capacitor, the drain voltage rise after the gating has already tripped to low level, indicating a ZVS turn-off. The main switch drain current is not recorded, because a long wire loop must be added to admit the current probe and this long wire loop will interfere with the nominal operation. Seen in Fig. 15(b), a zero current switching (ZCS) is achieved on the auxiliary switch at turn on. At turn-off, due the reversed resonant current in the auxiliary circuit, the drain of the auxiliary switch is clamped at zero, achieving ZVS turn-off. In summary, the prototype converter achieves soft switching.

Fig. 16 shows the overall efficiency versus total output power. The prototype converter only yields a maximum efficiency of about 83% at full load. Seen from Fig. 16, the efficiency stays almost constant over the range from 100% to 70% of the full power, and it drops as the output power decreases further. This can be explained as follows. Because the prototype achieves




a. ZVS turn-on and turn-off of the main switch.
Traces: 1-gating of the aux. sw. (10V/div.);
2- gating of the main sw.(10V/div.);
3- drain voltage of main sw.(20V/div.);
4- auxiliary circuit current (5A/div.)
Timing: 1μs/div.




b. ZCS turn-on and ZVS turn-off of the auxiliary switch.
Traces: 1-gating of the aux. sw. (5V/div.);
2- drain voltage of aux. sw.(20V/div.);
3- auxiliary circuit current (5A/div.).
Timing: 0.2μs/div.

Fig. 15. Soft switching of the main and auxiliary switches.

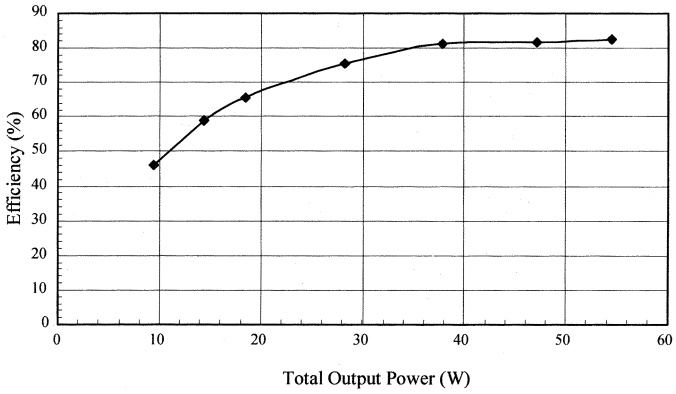



Fig. 16. Overall efficiency of the prototype converter. Each output has 50% of the total output power.

soft-switching, the major losses are the conduction losses. When the loads decrease from the full power, the conduction losses also decrease, therefore the overall efficiency can be kept almost constant. However, as the power decreases further, the simultaneous conduction interval $d_k$ of the pair SRs in each output circuit becomes greater, as shown in (10). Then, the conduction losses arising from the increased $d_k$ become more dominant, and hence the overall efficiency drops more and more rapidly as the output power become lower and lower. If the internal resistance $R_{sk}$ is minimized by employing optimal magnetics and low Rds(ON) MOSFETs and building a neat PCB converter, the interval $d_k$ can be minimized, and thus a better efficiency can be achieved.

## VII. Conclusion

In the proposed topology, the feed-forward control of the main switch allows instantaneous response in regulation against input voltage variations. The decoupling inductors between the power transformer and each output circuit eliminate cross regulation between the outputs. Each output circuit has an independent feedback control circuit that regulates the output voltage by controlling the synchronous rectifiers, thus independent and precise output voltage regulation can be obtained in each output. Verified with experimental results, the proposed topology provides a promising solution of on-board power supplies for advance telecom and computer systems.

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