A FOUR-QUADRANT CMOS ANALOG MULTIPLIER

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ABSTRACT

A new circuit configuration for an MOS four-quadrant analog multiplier circuit is presented. It is based on the square-law I-V characteristics of the MOS transistor. Linearity is better then 0.14 % for an output swing of 36 % of the supply current. The bandwidth is from dc to above 1 MHz.

INTRODUCTION

Four-quadrant analog multipliers are very useful building blocks in many circuits such as adaptive filters, frequency-shifters and modulators. Analog multipliers have got severe attention in bipolar technology [1].Even in CMOS technology, multipliers using (lateral) bipolar transistors have been reported [2]. Until now only a few CMOS multiplier designs have been published. Single-quadrant multipliers have been reported in [3] and [4]. In [5] and [6] four-quadrant multipliers using switched capacitor techniques have been described. A continuous-time CMOS multiplier has been presented by Soo and Meyer [7]. Basically their circuit approach is a translation of the well-known bipolar circuit concept described by B. Gilbert [1]. In this paper we report a new approach for a four-quadrant analog multiplier which is realised in CMOS technology. This multiplier relies on the quadratic drain current-gate voltage characteristics of MOS transistors operated in saturation. First a novel voltage controlled linear V-I convertor is explained. Combining two of these circuits results in a two-quadrant multiplier, while again duplicating this circuit yields a four-quadrant multiplier circuit.

BASIC VOLTAGE CONTROLLED V-I CONVERTOR

Consider the circuit of fig. 1. Although the circuit has been realised in PMOS as is also shown in the circuit schemes, the derivation below uses the NMOS equations for reasons of simplicity. All devices have the same geometry and operate in the saturation region. Using the simple square-law characteristic:

$$I_d = K (V_{gs} - V_t)^2 \qquad (1)$$

the current difference $(I_l - I_r)$ can be written as

$$I_l - I_r = K (V_{gs3} + V_{gs1} - 2V_t) (V_{gs3} - V_{gs1}) . \qquad (2)$$

Under the condition of

$$(V_{gs3} + V_{gs1} - 2V_t) = \text{constant} , \qquad (3)$$

equation (2) describes a linear relation between (I_1-I_r) and $(V_{gs3}-V_{gs1})$. As will be clear from fig. 1:

$$I_{d1} = I_{d2}$$

and it follows

$$V_1 \equiv V_{gs1} = V_{gs2} \ .$$

So

$$(V_{gs3} + V_{gs1} - 2V_t) = (V_{gs3}+V_{gs2} - 2V_t) = V_2 - 2V_t \ , \qquad (4)$$

where

$$V_2 \equiv V_{g2} = V_{gs3} + V_{gs2} \quad \text{(see fig. 1).}$$

By keeping the gate voltage of M_2 at a constant voltage V_2 with respect to ground, condition (3) is fulfilled. Equation (2) can now be rewritten as

$$(I_1-I_r) = K \{V_2^2 - 2V_t V_2 + 2V_1 (2V_t - V_2)\} \ . \qquad (5)$$

Apart from the term $K (V_2-2V_t) V_2$, equation (5) shows a linear relationship between (I_1-I_r) and V_1. The conversion factor can be controlled by V_2. For proper operation it is required that

$$V_1 > V_t \quad \text{and} \quad V_2 > V_1 + (V_1-V_t)/A \ , \qquad (6)$$

with A a constant accounting for the body-effect (A=1.1 to 1.3).

THE MULTIPLIER

Duplication of the circuit of fig. 1 and cross-coupling the output currents results in the circuit of fig. 2 in which the same voltage is applied to the V_2 terminals. We may now write for the output current difference:

$$I_1 - I_r = 2K (V_2 - 2V_t) (V_1' - V_1) \ . \qquad (7)$$

This represents a two-quadrant multiplier. Note that the nonlinear quadratic term from the V_2 input has disappeared. By again duplicating this circuit and cross-coupling the output currents (fig. 3) a four-quadrant multiplier is obtained. The output current difference is now described by

$$I_1 - I_r = 2K (V_2-V_2') (V_1' - V_1) \ . \qquad (8)$$

PERFORMANCE ANALYSIS

For simplicity the analysis above assumes first order MOST theory. SPICE simulations of the circuit of fig. 3 showed a total harmonic distortion of less then 0.1% at 90% of full scale input swing. Although such simulation results have to be considered with ample wariness, they justified realisation of a prototype circuit.

The current efficiency has been estimated along the following line. For properly biasing the condition (6) has to be fulfilled. If V_{i1m} and V_{i2m} are the maximum peak to peak signal voltages at the V_1 and the V_2 input then the minimum bias voltage at these terminals are:

$$V_{1dc} = V_t + 0.5\ V_{i1m}\ ,$$

$$V_{2dc} = 0.5\ V_{i2m} + V_t + V_{i1m} + (V_t+V_{i1m})/A - V_t/A =$$

$$0.5\ V_{i2m} + V_t + (1+1/A)\ V_{i1m}\ .$$

Then the total supply current is given by

$$I_{sup} = 4K\ \{(0.5\ V_{i1m})^2+(0.5\ V_{i2m}+\ (0.5+1/A)\ V_{i1m}-V_t)^2\ .$$

If the maximum input voltages are applied, the output current is:

$$I_{out,pp} = 2(I_1-I_r) = 4K\ V_{i1m}\ V_{i2m}) \qquad (10)$$

The current efficiency $I_{out,pp}/I_{sup}$ is optimal for $V_{i1m}=V_{i2m}=V_t$ and in that case $I_{out,pp}/I_{sup}=40\%$.

EXPERIMENTAL RESULTS

Fig. 4 shows the die photograph of the four-quadrant multiplier. This IC was fabricated in the IC processing facility of Twente University of Technology, using a retrograde twin well CMOS proces. As this proces has isolated n-wells, the circuit has been realised in PMOS because now the body-effect could be reduced by connecting the well-substrate to the source. The threshold voltage is -0.6 V. All devices have the same geometry: W=120 µm, L=10 µm.

Fig. 5 shows the performance of the multiplier as a frequency doubler; the input signals are two in-phase sine waves of 3.5 V p-p. The output is a sine wave of twice the input signal frequency and has a magnitude of 44 mV p-p measured over a 100 Ω load resistor, i.e. an output current of 0.44 mA p-p. The total supply-current was 2.0 mA.

Fig. 6 shows the multiplier performance as a modulator. A 3.5 V_{p-p} triangle wave was applied to the V_1 inputs and a 3.8 V_{p-p} sine wave was applied to the V_2 input. The output current amplitude measured in a 100 Ω load resistor was 0.9 mA p-p. The total supply-current was 1.0 mA.

With a 3 V dc voltage applied to the V_1 input the multiplier was used as a linear gain control circuit. The total harmonic distortion was measured as a function of the current-efficiency $I_{out,pp}/I_{sup}$, by varying the magnitude of a 1 kHz sine wave applied to the V_2 input. Fig. 7 shows the result. Fig. 8 shows the spectrum of the output signal with a 1 kHz sine wave of magnitude 1.7 V_{p-p}. The output current was 0.6 mA p-p in a 100 Ω load resistor. The second and third harmonic are both 60 dB below the fundamental.

The frequency response measured with a load resistor of 100 Ω and a load capacitor of 50 pF was from dc to above 1 MHz.

CONCLUSIONS

An extremely simple and compact design for a CMOS four-quadrant multiplier circuit is presented. The circuit is based on the square-law characteristic of the MOS transistor in saturation. The measured total harmonic distortion was 0.14% at a current efficiency I_{out}/I_{sup} of 36%. The bandwidth of the circuit with a load resistor of 100 Ω and a load capacitor of 50 pF was 1 MHz.

ACKNOWLEDGEMENT

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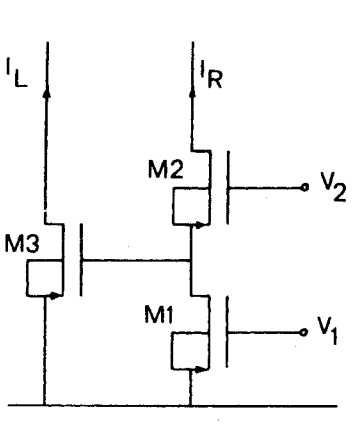

Fig. 1 The voltage controlled V-I converter.

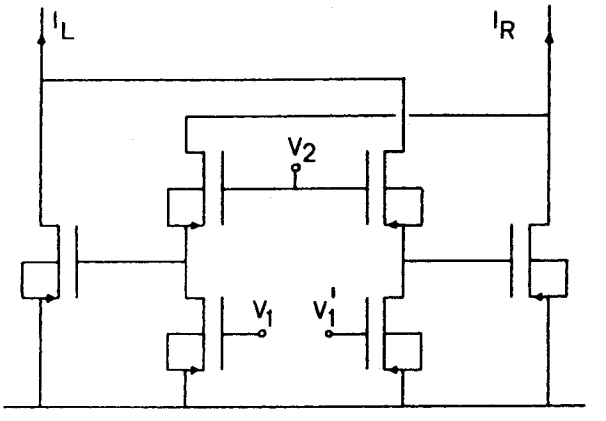

Fig. 2 Two-quadrant multiplier.

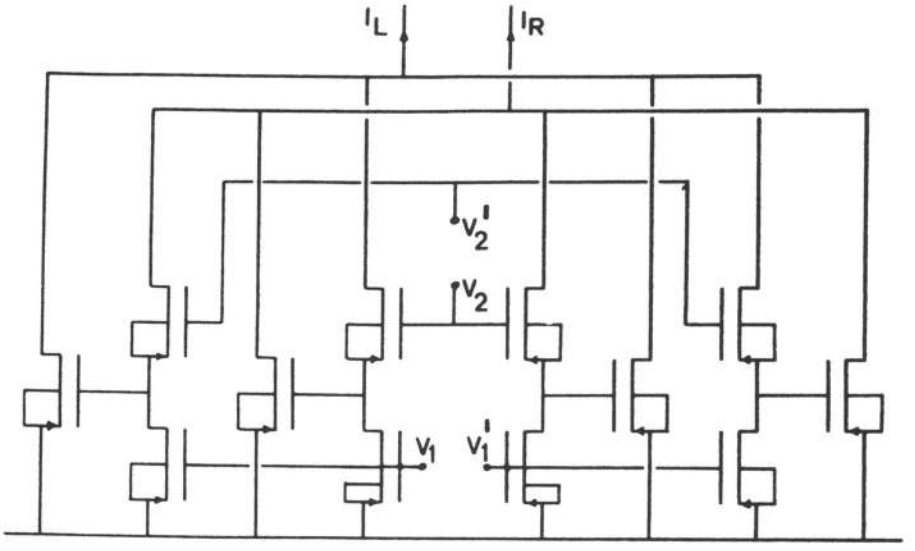

Fig. 3 Four-quadrant multiplier.

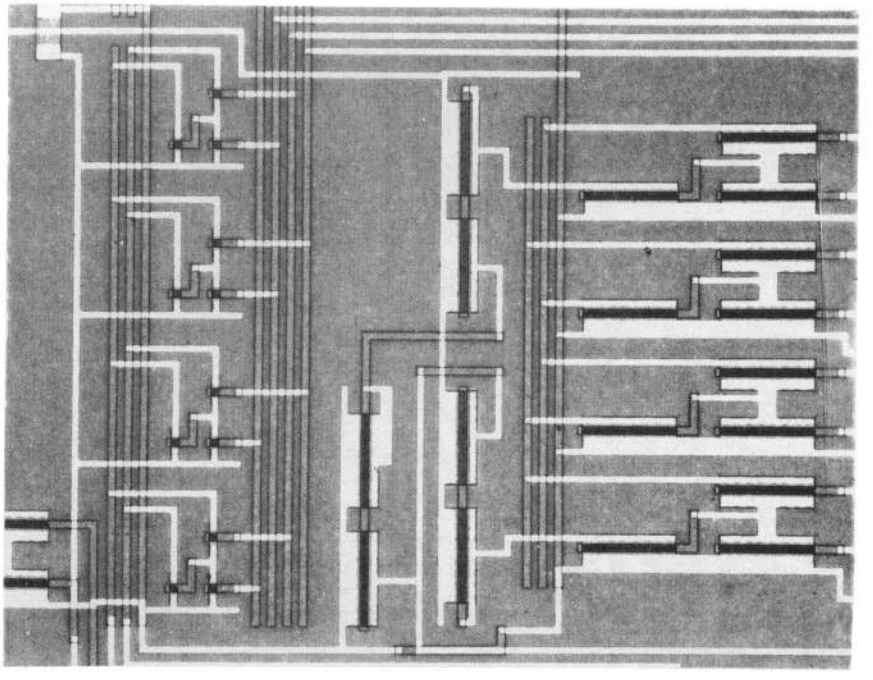

Fig. 4 Microphotograph of the circuits, showing two circuit realisations of the circuit of fig. 3. On the right hand the MOST's of the circuit have W/L = 120/10, on the left hand the circuit is realised with W/L = 10/10. In the middle are some transistors for test purpose.

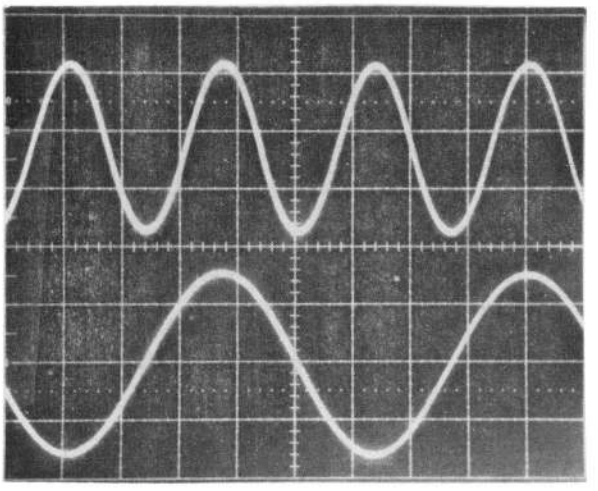

Fig. 5 Multiplication of two sine waves of the same frequency.

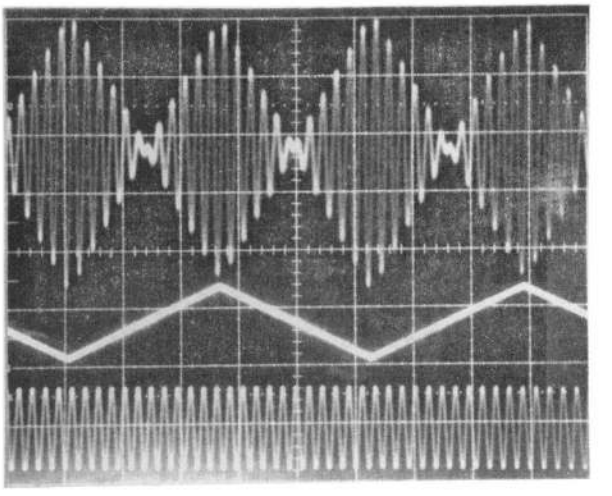

Fig. 6. Modulated triangle wave.

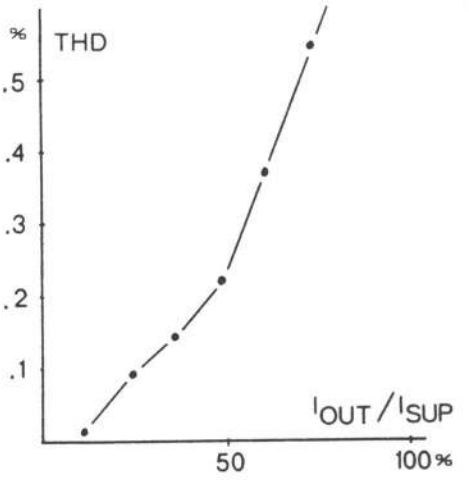

Fig. 7 The total harmonic distortion as a function of the current efficiency I_{out}/I_{supply}.

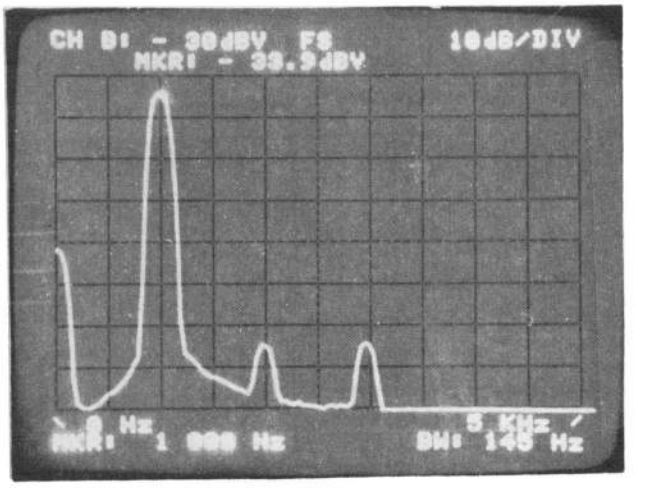

Fig. 8 Spectral content of a sine wave at the output of the multiplier.