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A Fourth-Order Single-Bit Switched-Capacitor Σ–Δ Modulator for Distributed Sensor Applications

Simona Brigati, *Member, IEEE*, Fabrizio Francesconi, *Member, IEEE*, Piero Malcovati, *Member, IEEE*, and Franco Maloberti, *Fellow, IEEE*

***Abstract*—In this paper, we present a switched-capacitor sigma–delta (Σ–Δ) modulator for high resolution applications. In particular, this Σ–Δ modulator is well suited for distributed sensor networks. The circuit, implemented in a double-poly, double-metal 0.6 μm CMOS technology, is based on a fourth-order single-loop architecture with a sampling frequency of 256 kHz. The chip consumes 50 mW from a single 5-V supply and achieves a signal-to-noise ratio of 104.9 dB over a bandwidth of 400 Hz, corresponding to a resolution of 17.1 bits.**

***Index Terms*—CMOS integrated circuits, detectors, intelligent sensors, measurement system data handling, sigma–delta (Σ–Δ) modulation, switched capacitor circuits.**

I. Introduction

HIGH-ORDER sigma–delta (Σ–Δ) modulators are the most suitable A/D converters for low-frequency, high-resolution applications, in view of their inherent linearity, reduced antialiasing filtering requirements, and robust analog implementation. Moreover, by trading accuracy with speed, Σ–Δ modulators allow excellent performance to be achieved with high tolerance to analog component imperfections without requiring component trimming. Σ–Δ modulators are, therefore, the best candidates for implementing the A/D converters in sensor applications, where the signal bandwidth is typically small, the required resolution is high and the environment where the circuit has to operate can be quite harsh. In particular, in distributed sensor applications, such as in seismic detectors for oil search, a resolution as high as 18 bits over a 400-Hz bandwidth is required. So far, complex mash, multiloop or multibit architectures with dynamic element matching have been used to achieve resolutions higher than 16 bits [1]–[3]. These solutions, however, are quite critical and the power consumption, the power supply voltage or the silicon area are large. For distributed sensor applications, therefore, a single-loop, single-bit Σ–Δ modulator seems to be the best suited, since the area and the power consumption are intrinsically lower and the single-bit output can be easily transmitted without any digital post-processing. The signal-to-noise ratio (SNR) due to quantization noise, assumed white and additive, for such a Σ–Δ, a modulator is approximately given by [4], [5]

$$\text{SNR} = \frac{6(2L+1)M^{2L+1}}{\pi^{2L}} \tag{1}$$

where L is the order of the modulator and M the oversampling ratio ($M = f_s/(2B)$, with f_s denoting the sampling frequency and B the signal bandwidth). Considering the resolution required in seismic detectors for oil search (SNR $>$ 100 dB) with $f_s = 256$ kHz and $B = 400$ Hz, (1) leads us to the choice of the fourth-order Σ–Δ modulator ($L = 4$) presented in this paper, whose specifications are summarized in Table I.

TABLE I
MOST IMPORTANT FEATURES OF THE PROPOSED FOURTH-ORDER, SINGLE-LOOP, SINGLE-BIT Σ–Δ MODULATOR

Parameter	*Value*
Order of the modulator (L)	4
Sampling frequency (f_s)	256 kHz
Signal bandwidth (B)	400 Hz
Oversampling ratio (M)	320
Signal-to-noise ratio (*SNR*)	> 100 dB

II. Σ–Δ Architecture

The general block diagram of a fourth-order, single-loop, single-bit Σ–Δ modulator is shown in Fig. 1. In order to approach, as much as possible, the theoretical limit for the SNR, the general structure has to be optimized. Moreover, the stability of the modulator has to be ensured under any operating conditions.

The noise and the signal transfer functions, NTF(z) and STF(z), for the modulator architecture shown in Fig. 1 are

$$\text{NTF}(z) = \frac{(1-z^{-1})^2[-1+2z^{-1}-(1+gc_3)z^{-2}]}{D(z)} \tag{2}$$

and (3), as shown at the bottom of the next page, respectively, where

$$\begin{aligned} D(z) = &-1+(4-a_1b)z^{-1}+(-6+3a_1b-a_2bc_1-c_3g)z^{-2} \\ &+(4-3a_1b+2a_2bc_1-a_4bc_1c_2+2c_3g-a_1bc_3g)z^{-3} \\ &+(-1+a_1b-a_2bc_1-a_4bc_1c_2 \\ &-a_3bc_1c_2c_3-c_3g+a_1bc_3g-a_2bc_1c_3g)z^{-4}. \end{aligned} \tag{4}$$

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S. Brigati and F. Francesconi are with the Acco Microelettronica S.r.l., 27100 Pavia, Italy (e-mail: s.brigati@acco-ic.it, f.francesconi@acco-ic.it).

P. Malcovati is with the Department of Electrical Engineering, University of Pavia, 27100 Pavia, Italy (e-mail: p.malcovati@ele.unipv.it).

F. Maloberti is with the Department of Electrical Engineering, University of Pavia, 27100 Pavia, Italy, and also with the Department of Electrical Engineering, University of Texas, Dallas, TX 75083-0688 USA (e-mail: franco.maloberti@utdallas.edu).

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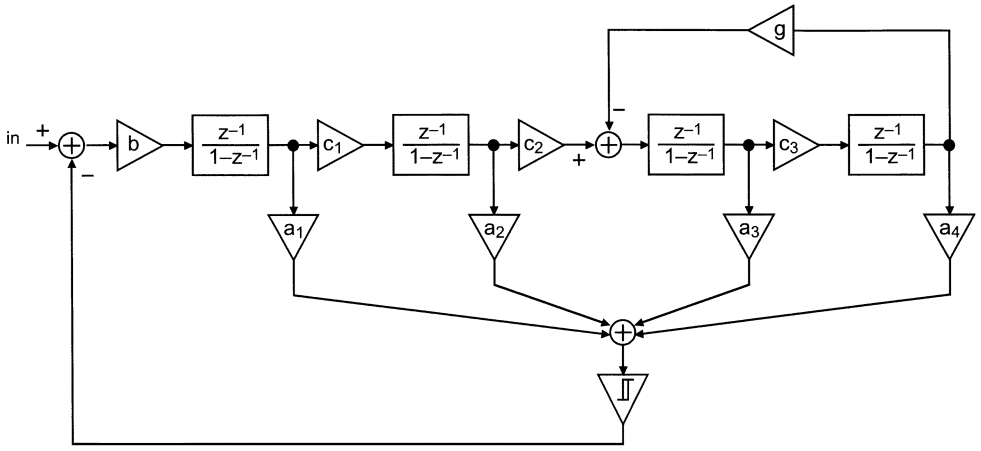


Fig. 1. Fourth-order, single-loop, single-bit Σ–Δ modulator architecture.

In order to determine the optimal values of the modulator coefficients, we followed a few basic guidelines.

- To improve the stability and the SNR of the modulator, it is useful to split the four transmission zeroes in two couples of zeros placed at dc and at the edge of the signal bandwidth (f_z), respectively. With behavioral simulation, we determined that the value of f_z, which maximizes the SNR, is 650 Hz, i.e., two zeroes are placed just outside the signal band ($B = 400$ Hz).
- To avoid instability of the modulator for large signals, the maximum amplitude of NTF(z), according to Lee's criterion, has to be lower than 1.5 [5].
- To ensure proper operation of the modulator with 5-V power supply, we scaled the coefficients in order to limit the output swing of all the integrators within ± 1 V under any operating conditions [5]. An output swing of ± 1 V at a 5-V supply, indeed, can be achieved with high linearity with conventional operational amplifier topologies.

The equations derived by applying these guidelines are not sufficient to ensure that the modulator is stable and achieves the required performance, because of the intrinsic nonlinearity of the system. Therefore, starting from a coarse sizing obtained from the linear model, we performed a number of simulations, using SIMULINK toolboxes dedicated to Σ–Δ modulators [6]–[8], to verify the behavior of the system and consequently optimize the values of the coefficients. The optimal values obtained are summarized in Table II, while a typical noise power spectral density of the modulator with ideal building blocks is shown in Fig. 2(a).

Unfortunately, the quantization noise is not the only parameter which determines the SNR of a Σ–Δ modulator, since the thermal noise and the building block nonidealities are in many cases quite significant, if not dominant. Considering a switched-capacitor implementation, therefore, we simulated the proposed sigma delta modulator, using the mentioned SIMULINK toolbox, which takes into account the most important nonideal effects (kT/C noise, operational amplifier finite gain, bandwidth, noise, and slew rate, as well as clock jitter). A typical noise power spectral density of the Σ–Δ modulator with nonideal building blocks is shown in Fig. 2(b). The power-spectral density has been obtained by the fast Fourier transform (FFT) on 65 536 samples with Hanning window and no averages. The SNR has been calculated using the procedure described in [8]. From these simulations, we derived the specifications of the building blocks and in particular of the first integrator (summarized in Table III). It can be observed that, with the chosen parameters, the thermal noise is dominant with respect to the quantization noise, leading to a total noise power of −128.2 dB, which corresponds to a SNR with full scale signal of 116.2 dB (19-bit resolution). Moreover, no spur tones are visible in the baseband, although no dithering is used.

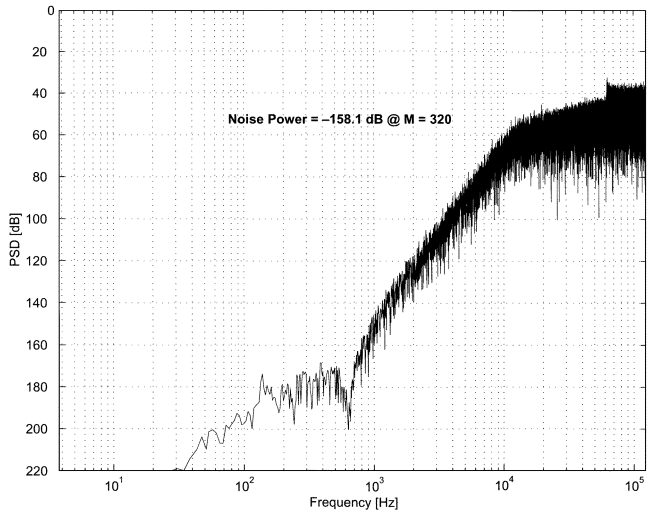
TABLE II
VALUES OF THE COEFFICIENTS FOR THE PROPOSED Σ–Δ MODULATOR

Parameter	*Value*
Coefficients b, c_1	0.4
Coefficient c_2	0.3
Coefficient c_3	0.1
Coefficients a_1, a_2	2
Coefficients a_3, a_4	1.5
Coefficient g	0.0025

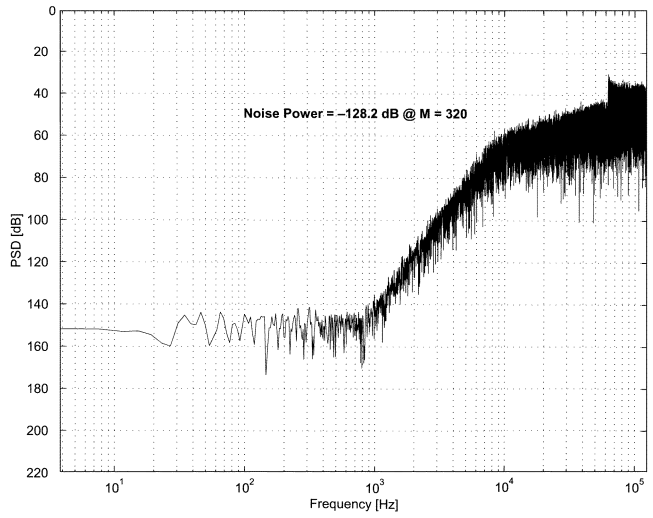
III. SWITCHED-CAPACITOR IMPLEMENTATION

The switched capacitor implementation of the proposed fourth-order, single-loop, single-bit Σ–Δ modulator is illustrated in Fig. 3. The circuit, based on a fully-differential architecture, reflects the block diagram shown in Fig. 1. The integrating and sampling capacitances of the first integrator are 500 pF and 200 pF, respectively, while the capacitances in the subsequent integrators are smaller (few tens of picofarads), since the thermal noise constraints become less stringent. The

$$\mathrm{STF}(z)=\frac{[a_1bz^{-1}+(3a_1b-a_2bc_1)z^{-2}+(-3a_1b+2a_2bc_1-a_4bc_1c_2-a_1bc_3g)z^{-3}+(a_1b-a_2bc_1-a_4bc_1c_2-a_3bc_1c_2c_3+a_1bc_3g-a_2bc_1c_3g)z^{-4}]}{D(z)} \tag{3}$$



(a)



(b)

Fig. 2. Typical noise power spectral density of the proposed Σ–Δ modulator with (a) ideal and (b) nonideal building blocks.

TABLE III
MOST IMPORTANT SPECIFICATIONS OF THE FIRST INTEGRATOR OF PROPOSED Σ–Δ MODULATOR

Parameter	*Value*
Sampling capacitance (for kT/C noise)	200 pF
Operational amplifier gain	80 dB
Operational amplifier bandwidth with feedback and load capacitors	5 MHz
Operational amplifier slew-rate with feedback and load capacitors	20 V/μs
Operational amplifier input-referred noise	7.5 μV_{rms}
Clock jitter	10 ns
Operational amplifier output swing	> ±1 V

operational amplifiers used are based on a folded cascode topology. The tail currents of the operational amplifiers in the different integrators are scaled together with the capacitance values in order to achieve the required bandwidth and slew-rate, while minimizing the power consumption. A switched-capacitor common-mode feedback is used in all the stages. In the first integrator, we exploited the autozero technique to reduce the effect of offset and flicker noise.

IV. OPERATIONAL AMPLIFIERS AND COMPARATOR

The main requirement for the operational amplifiers used in a switched capacitor Σ–Δ modulator is speed. Indeed, in a switched capacitor circuit, if the operational amplifier is fast enough to allow the circuit to settle completely within half of the clock period, the nature of settling will not impact the overall circuit performance. Therefore, in the proposed Σ–Δ modulator, we used the fully-differential folded-cascode operational amplifier, whose schematic is shown in Fig. 4. This architecture allows us to drive large capacitive loads with high dc gain and high speed without the need for frequency compensation. Moreover, the use of a fully differential structure removes the poles associated to the current mirrors required in a single-ended architecture, which would slow down the settling phase. Transistors $M_{\rm SR}1$ and $M_{\rm SR}2$ have been introduced to improve the slew-rate of the operational amplifier. They are switched on during the slewing phase and increase dynamically the available output currents, thus making the operation faster. A large output voltage swing is achieved with the use of high-swing cascode current sources and active loads. All transistor sizes have been also optimized to minimize the overall input referred noise. Table IV summarizes the simulated performance of the operational amplifier used in the first integrator. The operational amplifiers used in the subsequent integrators are based on the same architecture, but, as already mentioned, the bias currents and, hence, the performances are scaled.

The schematic of the latched comparator used [9] is shown in Fig. 5. The circuit consists of a *p*-channel input differential pair ($M_{\rm IP}$ and $M_{\rm IN}$), two bistable regenerative loops (M_4, M_8, M_9, and M_{10}) and an output latch ($M_{12} - M_{19}$). During clock phase Φ_R (reset phase), the comparator is reset by means of switches M_3, M_{11}, and M_7. On the falling edge of Φ_R, then, the comparator is latched and, depending on the input signal ($V_{\rm IP} - V_{\rm IN}$), the regenerative loops reach one of the two stable states ("one" or "zero"). This state is then maintained by the output latch till the end of the next reset phase, independently of the input signal. Due to the regenerative effect, this comparator allow very fast transients (in the order of 100 ns) and high resolution (around 40 μV) to be achieved.

V. EXPERIMENTAL RESULTS

The proposed high-resolution Σ–Δ modulator has been integrated using a 0.6-μm double-metal, double-poly CMOS process. The micrograph of the chip is shown in Fig. 6. The chip area, including pads, is 3.2 × 3.8 mm.

The measured noise power spectral density of the proposed Σ–Δ modulator, obtained by fast FFT on 65 536 samples with Hanning window and no averages, is shown in Fig. 7. We achieved an in-band noise floor of −140 dB, which is about 10-dB higher than in the simulations. This is due to additional noise sources, mainly related to the test setup, which were not taken into account in the simulations, such as the noise of the reference voltages and of the signal source as well as the noise coupled through the substrate. Nevertheless, the achieved noise power in the signal band is as low as −116.9 dB, thus leading to

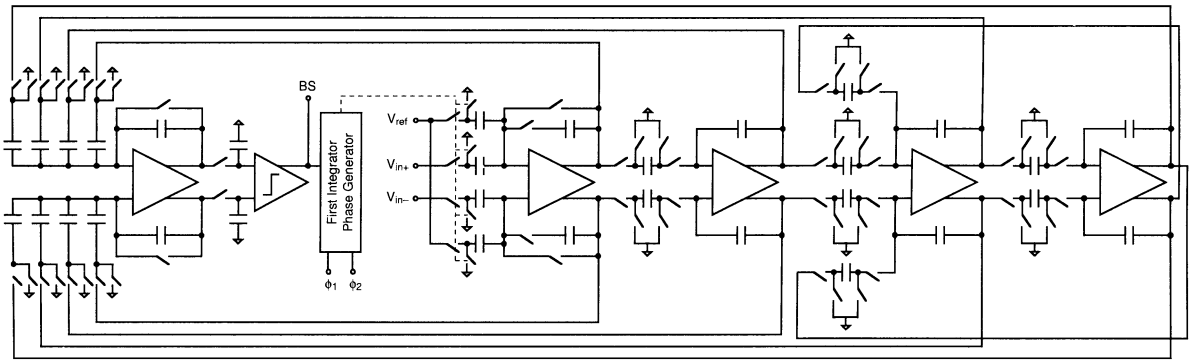


Fig. 3. Switched-capacitor implementation of the proposed fourth-order, single-loop, single-bit Σ–Δ modulator.

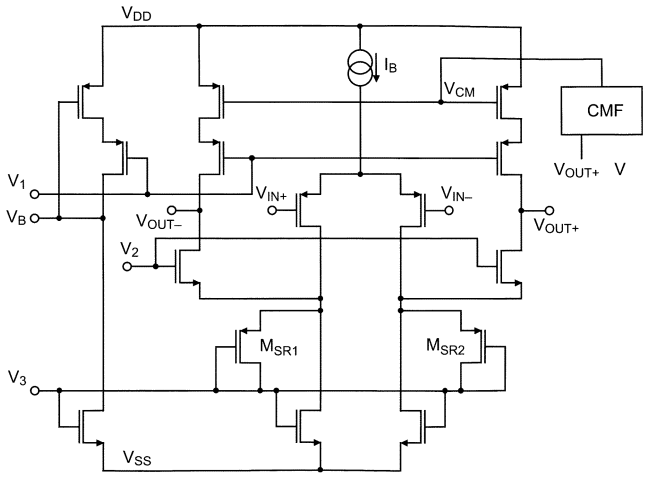


Fig. 4. Schematic of the operational amplifier used in the proposed Σ–Δ modulator.

TABLE IV
SIMULATED PERFORMANCE OF THE OPERATIONAL AMPLIFIER USED IN THE FIRST INTEGRATOR OF THE PROPOSED Σ–Δ MODULATOR

Parameter	*Value*
DC Gain	83 dB
Gain-bandwidth product (*GBW*) @ C_L = 500 pF	5.2 MHz
Phase margin @ C_L = 500 pF	90°
Output swing (differential)	±2.65 V
Settling time @ 0.1 ppm	582 ns
Slew-rate @ C_L = 500 pF	20 V/μs
Input referred noise	7.5 μV_{rms}
Current consumption	6.3 mA

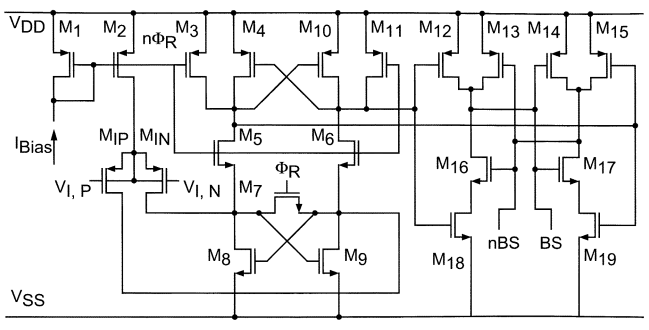


Fig. 5. Schematic of the comparator used in the proposed Σ–Δ modulator.

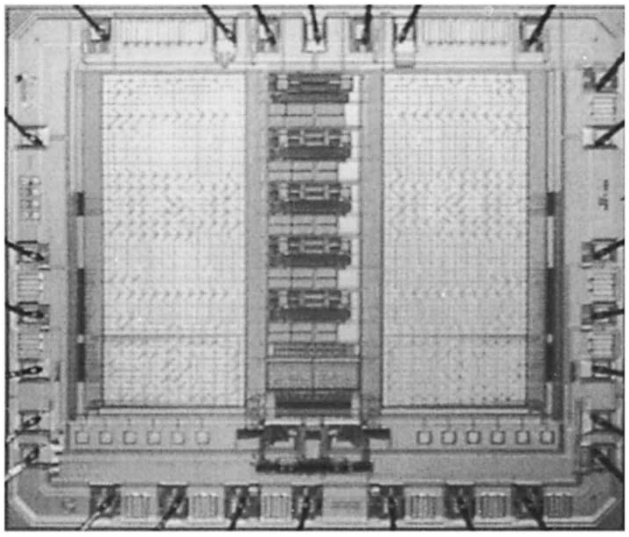


Fig. 6. Chip micrograph of the proposed Σ–Δ modulator.

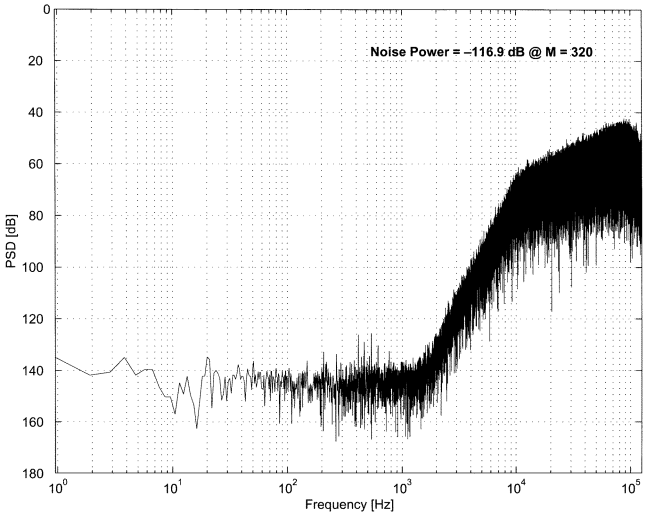


Fig. 7. Measured noise power spectral density of the proposed Σ–Δ modulator.

a maximum SNR, calculated using the procedure described in [8], of 104.9 dB, corresponding to 17.1 bits of resolution, which is sufficient for the considered application.

The proposed Σ–Δ modulator consumes 50 mW from a single 5-V power supply. The most important features of the circuit are summarized in Table V.

TABLE V
FEATURES OF THE PROPOSED Σ–Δ MODULATOR

Parameter	*Value*
Technology	0.6 μm CMOS
Power supply voltage	5 V
Power consumption	50 mW
Input voltage range (peak-to-peak, differential)	2 V
Input signal bandwidth (B)	400 Hz
Sampling rate (f_s)	256 kHz
Noise power in band	–116.9 dB
Signal-to-noise ratio @ Full scale signal	104.9 dB
Resolution	17.1 bits
Chip Size (including pads)	3.2 mm × 3.8 mm

VI. CONCLUSION

In this paper, we presented a fourth-order single-bit single-loop switched-capacitor Σ–Δ modulator designed for seismic oil search applications. The circuit operates with a sampling frequency of 256 kHz and an oversampling ratio of 320. A prototype of the proposed modulator has been fabricated in a double-poly, double-metal 0.6-μm CMOS technology. The 3.2×3.8 mm chip consumes 50 mW from a single 5-V supply and achieves a peak signal-to-noise ratio of 104.9 dB over a bandwidth of 400 Hz, corresponding to a resolution of 17.1 bits. The achieved performance is suitable for the considered application, although slightly worse than expected.

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Simona Brigati (M'96) was born in Castelsangiovanni (PC), Italy, in 1966. She received the degree in electronic engineering (summa cum laude) and the Ph.D. degree in electronic and computer engineering, for an activity on the design of high-speed A/D and D/A converters, from the University of Pavia, Pavia, Italy, in 1991 and 1995, respectively.

She joined the Integrated Microsystems Group, University of Pavia, in 1991. From 1996 to 2000, she was with Micronova Sistemi S.r.l., Italy. In 2001, she joined Acco Microelettronica S.r.l, Pavia, where she is involved in the design of mixed analog-digital ASICs. Her research interests are in the field of high-speed CMOS data converters, high resolution Σ–Δ modulators, and high-performance analog and mixed ICs.

Fabrizio Francesconi (M'00) was born in Mortara (PV), Italy, in 1965. He received the Laurea degree in electronics and the Ph.D. degree in electronic and computer engineering, for an activity on the design of bandpass Σ–Δ A/D converters, from the University of Pavia, Pavia, Italy, in 1991 and 1996, respectively.

From 1996 to 2000, he was with Micronova Sistemi S.r.l., Italy. In 2001, he joined Acco Microelettronica S.r.l, Pavia, where he is responsible for the development of mixed analog-digital integrated circuits. His main interests ares in the area of audio integrated circuits, SC filters, A/D and D/A converters, and Σ–Δ converters.

Piero Malcovati (M'95) was born in Milano, Italy, in 1968. He received the Laurea degree (summa cum laude) in electronic engineering from the University of Pavia, Pavia, Italy in 1991 and the Ph. D. degree in electrical engineering from the Swiss Federal Institute of Technology Zurich (ETHZ), Zurich, Switzerland, in 1996.

In 1991, he received a one-year grant from SGS-Thomson, Italy. In 1992, he joined the Physical Electronics Laboratory, ETHZ, as a Ph.D. candidate. From 1996 to 2001, he was an Assistant Professor with the Department of Electrical Engineering, University of Pavia, Pavia, Italy, where he has been Associate Professor of electrical measurements since 2002. He has authored or coauthored more than 20 papers in international journals, more than 60 presentations at international conferences (with published proceedings), two book chapters, and he holds three industrial patents. He was the Guest Editor of the *Journal of Analog Integrated and Signal Processing* for the special issue on IEEE ICECS 1999. His research activities are focused on microsensor interfaces and high performance data converters.

Dr. Malcovati was the Special Session Chairman of IEEE ICECS 2001. He was the Technical Program Committee Secretary of ESSCIRC 2002.

Franco Maloberti (F'96) received the Laurea degree in physics (summa cum laude) from the University of Parma, Parma, Italy, in 1968 and the Dr. Honoris Causa Ph.D. in electronics from the Instituto Nacional de Astrofisica, Optica y Electronica (Inaoe), Puebla, Mexico, in 1996.

In 1993, he was a Visiting Professor at the Swiss Federal Institute of Technology Zurich (ETHZ), Zurich, Switzerland. He was Professor of microelectronics and Head of the Micro Integrated Systems Group, University of Pavia, Pavia, Italy, and the TI/J.Kilby Analog Engineering Chair Professor, Texas A&M University, College Station. He is currently the Distinguished Microelectronic Chair Professor at the University of Texas, Dallas, and part-time Professor at the University of Pavia. He has written more than 250 published papers, three books, and holds 15 patents. He has been responsible, at both technical and management levels, for many research programs, including 10 ESPRIT projects, and has served the European Commission as ESPRIT Projects' Evaluator, Reviewer, and as European Union Expert in many European initiatives. He served the Academy of Finland and the Portuguese Research Council in the assessment of electronic research in academic institutions and on the research programs' evaluations. He is also a member of the Editorial Board of *Analog Integrated Circuits and Signal Processing*. His professional expertise is in the design, analysis, and characterization of integrated circuits and analog digital applications, mainly in the areas of switched capacitor circuits, data converters, interfaces for telecommunication and sensor systems, and CAD for analog and mixed A-D design.

Dr. Maloberti is a member of the Italian Electrothecnical and Electronic Society (AEI). He is the President of the IEEE Sensor Council. He was Vice-President, Region 8, of the IEEE Circuits and Systems Society from 1995 to 1997 and an Associate Editor of IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—PART II: ANALOG AND DIGITAL SIGNAL PROCESSING. In 1992, he was the recipient of the XII Pedriali Prize for his technical and scientific contributions to national industrial production. He was co-recipient of the 1996 Institute of Electrical Engineers (U.K.) Fleming Premium for the paper "CMOS Triode Transistor Transconductor for high-frequency continuous time filters." He also received the 1999 IEEE CAS Society Meritorious Service Award, the 2000 CAS Society Golden Jubilee Medal, and the 2000 IEEE Millenium Medal.