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A frequency-scalable 15-bit incremental ADC for low power sensor applications

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Published on: 03 Aug 2010 - International Symposium on Circuits and Systems

Topics: Low-power electronics, Delta-sigma modulation and CMOS

A Frequency-Scalable 15-bit Incremental ADC for Low Power Sensor Applications

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***Abstract*— A 15-bit low-power incremental ADC is designed for sensor applications. The ADC is designed to be frequency-scalable by 1000 times from 1.67S/s to 1.67kS/s. To reduce power, an opamp with class AB characteristics is used. The design was fabricated in 0.18μm CMOS and occupies an area of 0.35mm^2. Configured to operate at full-rate as a Delta-Sigma modulator, the ADC achieves 91.8dB peak SNDR while consuming 83μW from a 1.8-V supply. Operating as an incremental converter, the ADC powers off periodically to achieve frequency scalability, maintaining 84.7dB to 88.9dB peak SNDR while operating from 1.67S/s to 1.67kS/s and scaling analog power by up to 500 times.**

I. Introduction

Micromachined MEMS sensors have been applied increasingly in the automotive industry. Crucial to the development of power-efficient sensor solutions, is the development of lower-power interfaces including ADCs. This work addresses a class of piezoresistive pressure sensor devices applied in devices ranging from altimeters to tire pressure monitors. To reduce design costs, it was desired that a single ADC be capable of scaling its signal bandwidth by 1000 times from Hz to kHz operation. A power efficient solution would also have to scale its power by the same factor of 1000.

Scaling the power and bandwidth of analog circuits by 1000 times can be quite difficult. For example, by varying the bias current of circuits, their power consumption can be scaled. However, it is not easy to maintain correct circuit operation over a wide range of bias conditions. The alternative, used in [1] and [2] and chosen in this design is to always operate the circuits with the same bandwidth and sample rate, and power down circuits between conversions. In this way, analog circuits always operate at a consistent operating point. This scheme does however require a finite state machine to power circuits on and off. This controller must always remain on, consuming some static power.

The relatively high (15-bit) resolution and low bandwidth required for this application are amenable to the use of oversampled (delta-sigma) ADCs. Implementing this power-scaling scheme is not straight-forward with oversampled ADCs. Delta-sigma modulators rely on integrator circuits which accumulate charge in capacitors. To power down circuits between samples, these integrator circuits would have to maintain their charge while circuits are shut down. Due to leakage and startup issues, this is impractical. It was therefore decided to use a subset of delta-sigma modulators, the incremental ADC, which uses OSR back-to-back conversion steps (where OSR is the oversampling ratio) to produce each output and is then reset. Due to their simple post-filters, incremental converters may achieve lower SNR than equivalent delta-sigma ADCs, but their resettable operation makes them suitable for power-scaled operation.

This paper presents an incremental converter that can scale its bandwidth from 1.67Hz to 1.67kHz while maintaining 84.7-88.9dB peak SNDR. Power consumption at full-rate is 83μW for the ADC and 42μW for the on-chip post-filter. Section II and III summarize the system and circuit-level design of the ADC. Section IV describes the experimental results.

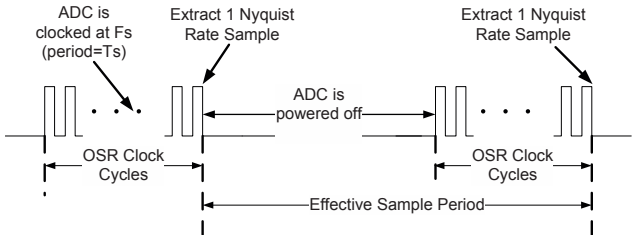

Fig. 1. Illustration of Frequency-Scaled Operation

II. System Design

A. Incremental Converter Design

Incremental converters combine a delta-sigma modulator with a digital post-filter to form a Nyquist rate ADC [3]. The system operates for OSR cycles, before both the delta-sigma modulator and filter are reset. The output of the post-filter is sampled after every OSR cycles, providing a Nyquist rate data output. Although more advanced filtering might be used, at a minimum, post-filters consist of a cascade of digital integrators.

The required order of delta-sigma modulator is determined in part by the desired OSR. In this design, to reduce loading on the sensor device and ease the requirements of any input buffer that might be used, the input sampling capacitor sizes were reduced to 550fF. To achieve sufficiently low thermal noise, an OSR of 1500 was required. At this OSR, a 2nd order incremental converter offered sufficiently low quantization noise to obtain a thermal noise-limited design with the desired 15-bit accuracy. Therefore, a 2nd order incremental converter was designed, consisting of a 2nd order delta-sigma modulator, followed by 2 digital post-integrators.

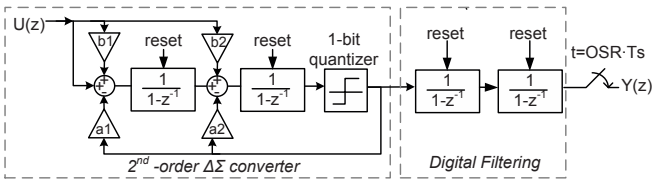

Fig. 2. 2nd Order Incremental Converter

B. 2nd Order Delta-Sigma Modulator

The delta-sigma modulator uses a cascade of integrators feedback (CIFB) topology [4] as shown in Fig. 2. The input feed-in to the

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input of the second stage integrator reduces input signal content in the power-hungry first integrator stage and potentially suppresses non-linearities in that stage. The lack of an input feed-in to the quantizer eliminates the need for an additional summation before the quantizer. This leads to a low-pass, as opposed to an all-pass signal transfer function (STF), but it was found not to impact performance significantly. Due to the high OSR used, optimized zeros were impractical to implement so the zeros of the noise transfer function (NTF) were left at DC (z=1). Filter coefficients were selected using the Delta-Sigma Toolbox [4]. Also due to the high OSR, the opamps used required relatively high gains of 50dB or more.

A single-bit quantizer was used to avoid the need for additional digital circuits to suppress non-linearities in the feedback DAC. This is also desirable in incremental converters since it allows the first post-filter stage to be a simple counter.

III. Circuit Implementation

A. Delta-Sigma Modulator

The delta-sigma modulator was implemented using switched-capacitor circuits as shown in Fig. 3. Capacitors were shared between the input and feedback DAC to prevent additional thermal noise. Using a full 1.8V supply, clock-boosting was not required. The

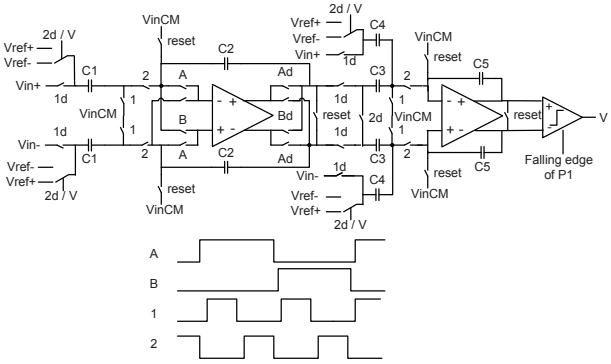

Fig. 3. Switched-Capacitor Implementation of $\Delta\Sigma$

first stage integrator was chopped [5] at half of the sample rate to suppress flicker noise, permitting operation at low frequencies. The chopper clock phases A and B were generated identically to the non-overlapping clocks 1 and 2 using a second clock generator, driven by an on-chip clock divider.

B. Opamp Design

To minimize power and noise, it was desired to maximize the input transconductance of the opamps. This can be accomplished using class-AB techniques ([6],[7]) which combine the gm of complementary NMOS and PMOS devices. However such circuits often require additional biasing networks such as level shifters, or complicate common mode feedback. To avoid this, a solution was chosen that achieves much of the performance advantages of class-AB designs (see Fig. 4).

The design consists of a Folded-Cascode opamp in which both the PMOS input differential pair (M1/M2) and NMOS current sources (M3/M4) are driven. The design combines the gm of both pairs of devices. By allocating more of the current to the differential pair than the folding network, the improvement in gm is significant. To enhance the opamp's slew rate, a current mirror network, which turns on to provide additional current was added. The network is controlled by the diode-connected devices M12 & M13, which only turn on under large signal conditions. An increased slew rate reduces the duration of slewing as the opamp output settles. This can relax the opamp's bandwidth requirements as more time is available for linear settling.

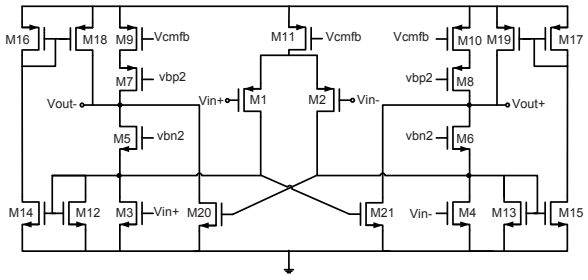

Fig. 4. Pseudo Class-AB Opamp

Since thermal noise from the second stage integrator is suppressed by the first stage integrator gain, its capacitor sizes were reduced requiring less power from the second stage opamp. Since potential power savings were lower in the second stage, a simple NMOS-input telescopic opamp was used. The NMOS tail current source was removed to lower the input common mode and ease the use of NMOS switches at the opamp input.

C. Power-Down Control

As mentioned, in power-scaled operation, circuits (including bias circuits) are disabled between conversions to reduce power. The cascode devices in the opamps were used as switches to switch the opamps on and off. By disabling the clock input to the clock generators, digital circuits could be similarly powered down.

To reduce transients in analog circuits as they are powered on, bias circuits were powered on and allowed to settle for several clock periods before powering on the amplifier circuits [1]. Allowing this startup time increased overall power consumption by less than 10%.

D. Digital Circuits

The digital post-filter was synthesized using standard library cells. A shift-register was used to provide the digital output serially. An on-chip controller was also synthesized to control the power-scaled/reseting operation of the incremental converter. The controller was programmable to accommodate different sampling rates and additional options such as the duration of startup phases. To reduce its power, an on-chip divider was used to reduce the clock rate entering the controller.

IV. Experimental Results

The complete design was fabricated in 1P6M 0.18μm CMOS with a 1.8-V supply. Fig. 5 shows the ADC integrated with a previously designed programmable gain amplifier [2]. The ADC itself, including digital filter and controller occupy an active area of 0.5mm×0.7mm=0.35mm^2.

A. Delta-Sigma Modulator

The ADC was configured to operate as a traditional delta-sigma modulator to evaluate its performance. A fully differential, low-distortion signal generator was used as the signal source. In this case, the filtering and resetting operations were disabled and the output of the delta-sigma modulator was sampled directly. In this configuration, the ADC achieves 91.8dB peak SNDR at an input level of 990mVpp differential (-3.6dBFS) over its 1.67kHz bandwidth. (SNDR values

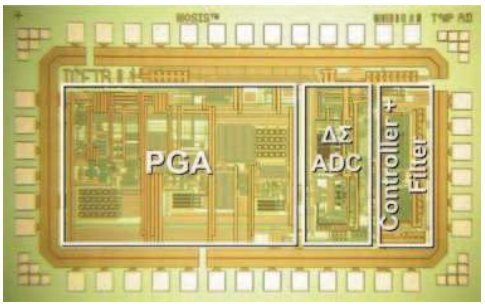

Fig. 5. Die Photo

include tones up to the 7th harmonic.) Fig. 6 shows the ADC's output spectrum. Several 60Hz harmonics seen in the ADC output were present in the signal source output when viewed with a spectrum analyzer. Since they are were not caused by the ADC, they were discounted from SNR calculations. From Fig. 6, the delta-sigma ADC actually has a usable bandwidth of up to 10kHz. Reducing the OSR from 1500 to 250, the delta-sigma still achieves 85.8dB peak SNDR over 10kHz of bandwidth. This was however traded off to increase SNR over a reduced bandwidth required in this application.

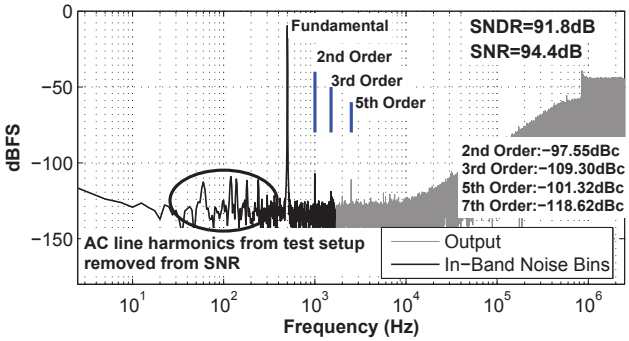

Fig. 6. Output Spectrum From Delta-Sigma Modulator

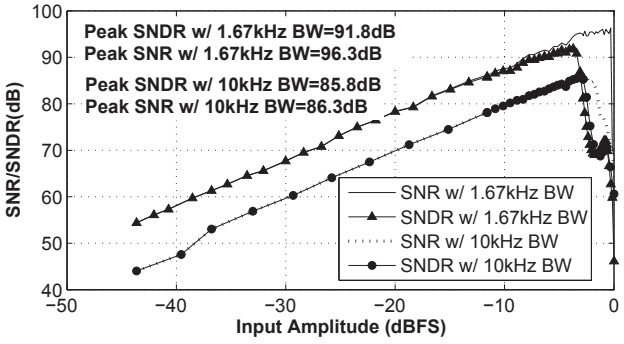

Fig. 7. SNR vs. Amplitude for Input @500Hz

ADCs can be compared in terms of bandwidth and accuracy (measured here in SNDR) using the following Figure-of-Merit (FOM) [8]:

$$FOM1 = \frac{4kT \times Bandwidth \times SNDR}{Power} \quad (1)$$

where k is Boltzmann's constant and T is the temperature in Kelvin. This FOM compares the number of conversion steps achieved relative to the power consumed and thermal noise level. Inverting the FOM and assuming all comparisons are made at room temperature, leads

TABLE I
MEASUREMENT RESULTS FOR DELTA-SIGMA MODULATOR

	Configuration 1	Configuration 2
Supply Voltage	1.8V	1.8V
Maximum Input Swing	1.5Vpp diff.	1.5Vpp diff.
Clock Rate	5MHz	5MHz
OSR	1500	250
Signal Bandwidth	1.67kHz	10kHz
Total Analog Power	33μW	33μW
Digital Clock Power	50μW	50μW
Peak SNDR	91.8dB @ 990mVpp	85.8dB @ 1.06Vpp
Peak SNR	96.3dB @ 1.44Vpp	86.3dB @ 1.10Vpp
DR	96.5dB	89.1dB

to an adjusted FOM of:

$$FOM2 = \frac{Power}{Bandwidth \times SNDR} \quad (2)$$

which measures relative power consumption and has units of J/(step)^2.

Fig. 8 compares this work to several recent low-power discrete-time delta-sigma modulators using FOM2 described above. This design has performance comparable with other recent work but does consume more power due to its relatively high supply voltage. Digital clock power in particular, is quite high. The other designs all use supply voltages of 1V or less. [6] achieves the lowest FOM to date using inverters and a 0.7V supply. It should also be noted that [8] has a larger 3V input swing, allowing it to achieve a higher SNR. However, as mentioned, a conventional delta-sigma modulator cannot easily be power-scaled, necessitating the use of an incremental converter.

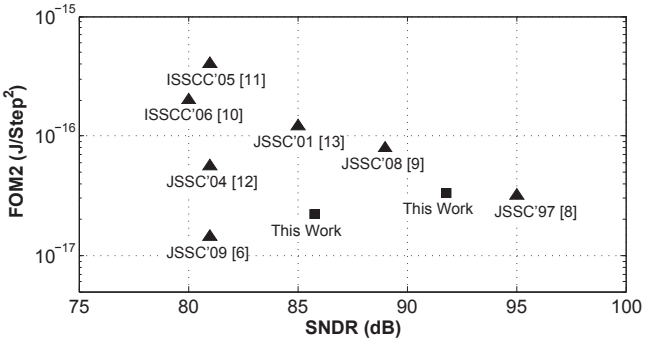

Fig. 8. FOM2 vs. SNDR for Various Discrete-Time $\Delta\Sigma$ Modulators

B. Power-Scalable Incremental Converter

Operating as an incremental converter, the delta-sigma modulator is periodically reset and powered on and off by the on-board controller. The digital post-filter outputs digital data serially at the Nyquist rate. The peak SNR achievable from the on-chip filter is expected to be roughly 1.25dB [3] lower than can be achieved with a delta-sigma modulator using an ideal decimation filter. The measured difference was 2dB. As a result, if power scaling is not required, it is advantageous to operate the ADC simply as a delta-sigma. Fig. 10 shows the peak SNR/SNDR for the incremental ADC as its bandwidth is scaled. At lower frequencies, the SNR drops off due to increased noise at low frequencies.

Operating at full-rate, the incremental converter consumes 83μW for the delta-sigma and 42μW for the post-filter. When power-scaled, measurements confirmed that the analog power of the delta-sigma ADC could scale from 33μW down to 67nW at the lowest bandwidth

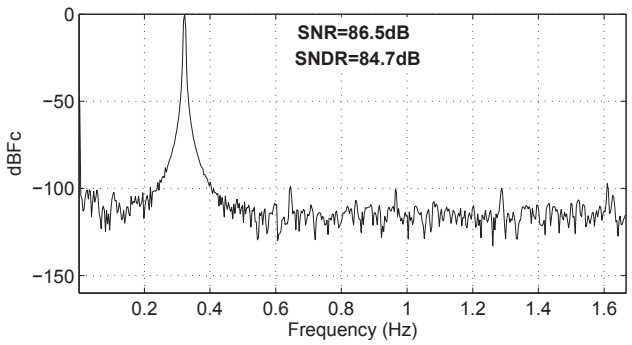

Fig. 9. Output Spectrum of Incremental Converter (Power-Scaled by 1000)

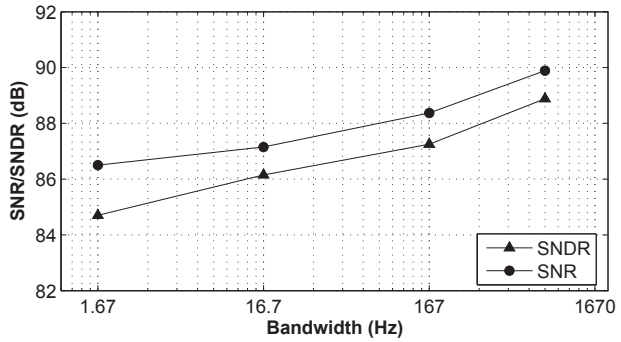

Fig. 10. Peak SNR/SNDR vs. Signal Bandwidth

due to the varying duty cycle (see Fig. 11). Power scaling of digital clock circuits was limited to roughly 50 times in measurements. This is because several stages of on-chip clock buffers always remain active, leading to a fixed minimum power consumption. This could be remedied by disabling the clock before any buffering is used.

For testing purposes, the on-chip controller was designed with wide programmability and consumed 4.3μW. This power could be reduced using a simplified, less flexible controller. In addition, although the presence of the controller limits the minimum power of the ADC to 4.3μW, in the intended application, combined with a variable gain amplifier, the controller would account for only a small portion of the interface's total power.

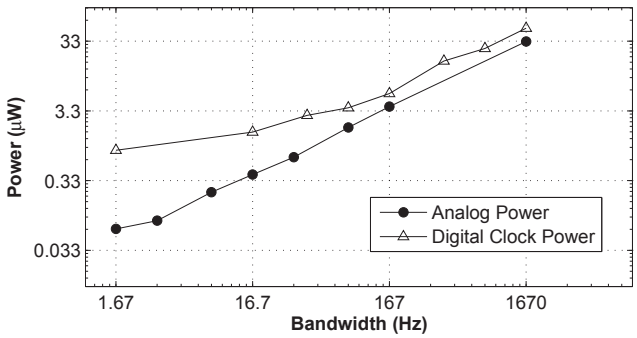

Fig. 11. ADC Power vs. Signal Bandwidth

V. Conclusion

A power-scalable incremental ADC has been presented which can scale its bandwidth by 1000 times from 1.67Hz to 1.67kHz while achieving 84.7-88.9dB SNDR. Operating at full-rate, power consumption is 83μW for the ADC and 42μW for the on-chip post-filter. Analog power was confirmed to scale as desired, but several clock buffers which always remain active limited digital power scaling to roughly 50 times.

TABLE II
Specifications of Power-Scalable Incremental Converter

Technology	0.18μm CMOS
Supply Voltage	1.8V
Maximum Input Swing	1.5Vpp diff.
Signal Bandwidth	1.67Hz - 1.67kHz
Total Analog Power	67nW - 33μW
Digital Clock Power	0.9μW - 50μW
Digital Filter Power (full-rate)	42μW
Peak SNDR	84.7dB - 88.9dB
Peak SNR	86.5dB - 89.9dB
Active Area	$0.35mm^2$

Acknowledgement

The authors would like to thank Bosch Research and Technology Center and the National Sciences and Engineering Council of Canada (NSERC) for research funding and Canadian Microelectronics Corporation (CMC) for fabrication services.

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