A Full-Range Drain Current Model for Double-Gate Junctionless Transistors

Juan Pablo Duarte, Sung-Jin Choi, and Yang-Kyu Choi

***Abstract*—A drain current model available for full-range operation is derived for long-channel double-gate junctionless transistors. Including dopant and mobile carrier charges, a continuous 1-D charge model is derived by extending the concept of parabolic potential approximation for the subthreshold and the linear regions. Based on the continuous charge model, the Pao–Sah integral is analytically carried out to obtain a continuous drain current model. The proposed model is appropriate for compact modeling, because it continuously captures the phenomenon of the bulk conduction mechanism in all regions of device operation, including the subthreshold, linear, and saturation regions. It is shown that the model is in complete agreement with the numerical simulations for crucial device parameters and all operational voltage ranges.**

***Index Terms*—Bulk current, double gate (DG), junctionless (JL) transistor, semiconductor device modeling.**

I. Introduction

A CONVENTIONAL metal–oxide–semiconductor field-effect transistor (MOSFET) consists of two p-n junctions at the source and drain regions. As devices are scaled further, the formation of such junctions requires a large doping concentration gradient and careful fabrication, considering a low thermal budget. These stringent demands push the scaling of MOSFETs to their fundamental limits. Hence, a new device, called a junctionless (JL) transistor [1], has been proposed to alleviate the aforementioned problems. Its structure is similar to a conventional MOSFET; however, with homogeneous doping polarity and a uniform doping concentration across the channel, source, and drain, the device requires no junctions, e.g., n^+ source–n^+ channel–n^+ drain for an n-channel metal–oxide–semiconductor field-effect transistor (NMOS). The main conduction mechanism in a junctionless field-effect transistor (JLFET) relies not on the surface but on the bulk current; moreover, it turns off by making the channel fully depleted [2]. Utilizing a single gate, it is rather difficult to fully deplete the channel, and acceptable threshold voltages are also difficult to obtain under such a condition [3]. Therefore, a double-gate (DG) structure is a promising candidate for JLFETs due to its good electrostatic control of the channel [4].

Due to the interesting characteristics of DG-JLFETs, analytic compact current–voltage models are needed for circuit simulators and to understand the fundamentals of device characteristics. Recently, an analytic model for DG-JLFETs has been proposed [5]. It represents the main physical characteristics of the device in a simple form; however, its piecewise approach may cause convergence problems in compact modeling applications [6]. In addition, a hybrid model has been proposed for DG-JLFETs [7]; nevertheless, its hybrid approach may also cause convergence problems [6]. One model that continuously covers every operation region would overcome these difficulties. The Pao–Sah integral [8], which is based on Poisson and current continuity equations with gradual channel approximation, can be used to describe all regions of operation (subthreshold, linear, and saturation), because it includes the drift and diffusion current components through the use of a quasi-Fermi potential. In this paper, by extending the parabolic potential approximation above the subthreshold region and using Pao–Sah electrostatic assumptions [8], a 1-D continuous charge model is developed for a symmetric long-channel DG-JLFET, considering the dopant and mobile carrier charges. With the derived charge model, the Pao–Sah integral is analytically obtained, which leads to a continuous drain current model. The proposed model does not use fitting parameters, and it captures the phenomenon of the bulk conduction mechanism [2] in all regions of device operation. Depending on the bias condition, the model reduces to simple expressions that compressively explain the working principle and device parameter dependence of DG-JLFETs. These expressions have not been shown by the hybrid model proposed in the previous report [7].

II. Device Working Principle

The working principle of a DG-JLFET differs from a conventional inversion-mode DGFET. A transversal view of a DG-JLFET with corresponding schematic band diagrams for different gate voltages is depicted in Fig. 1. Both p^+ polysilicon gates have the same work function, and the same voltage is also applied to each gate. The electron quasi-Fermi level of the source–drain is taken as a reference for the other energy levels. The work function difference between the gate and the channel is approximately given as $E_g/2 + qv_T \ln(N_{\rm si}/n_i)$, where E_g is the band gap of silicon, v_T is the thermal voltage (kT/q), $N_{\rm si}$ is the doping concentration of the channel, and n_i is the intrinsic carrier density. At a gate voltage lower than the threshold

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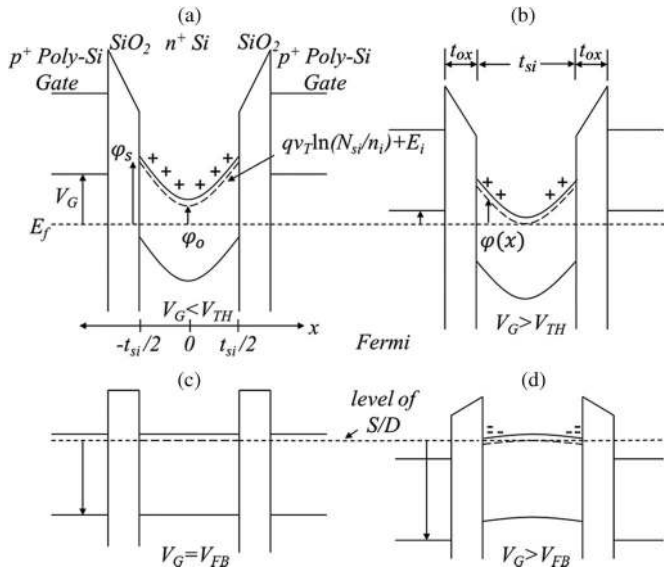

Fig. 1. Schematic band diagrams for a symmetric DG-JLFET. (a) Fully depleted and downwardly bent channel in the subthreshold mode. (b) Partially depleted and downwardly bent channel in the bulk current mode. (c) Flattened channel in the flatband mode. (d) Upwardly bent channel in the accumulation mode.

voltage ($V_{\rm TH}$), the channel is fully depleted, and the device is under a subthreshold state [see Fig. 1(a)]. For a voltage higher than $V_{\rm TH}$, the channel is partially depleted, and the current can flow through the center of the channel by the bulk conduction mechanism [see Fig. 1(b)]. When the gate voltage is equal to the flatband voltage ($V_{\rm FB}$), a completely neutral channel is created, and the current can flow through the entire channel [see Fig. 1(c)]. In DG-JLFETs, $N_{\rm si}(\sim 1\times 10^{19}\ {\rm cm}^{-3})$ is relatively high compared to a conventional inversion-mode FET. This condition makes the work function difference approximately equal to E_g, i.e., 1.1 eV. At a gate voltage larger than $V_{\rm FB}$, the mobile carrier (electrons in NMOS) density is increased at the surfaces, and the surface current conduction is governed by the mobile carriers that accumulate at the channel interface [see Fig. 1(d)]. This way, in the linear and subthreshold regions, the DG-JLFET current mechanism is primarily composed of the bulk current [2]. In contrast, electrons in conventional inversion-mode DGFETs are distinctively confined near the interface (surface inversion) in the linear region producing the surface current, whereas they are concentrated at the center of the channel (volume inversion) in the subthreshold region [6].

III. Charge Model

Considering only mobile charges (electrons for NMOS) and using the Pao–Sah gradual channel approximation [8], the Poisson equation in the silicon channel region can be written as

$$\frac{d^2\varphi}{dx^2} = -\frac{qN_{\rm si}}{\varepsilon_{\rm si}}\left(1-e^{(\varphi-V)/v_T}\right) \tag{1}$$

where φ is the channel potential, $\varepsilon_{\rm si}$ is the permittivity of silicon, and V is the electron quasi-Fermi potential. Note the defined coordinate and brief sketch of the potential in Fig. 1. Unfortunately, an analytical solution for φ cannot directly be integrated from (1) [9], [10]. To obtain an analytical expression of the channel potential, parabolic potential approximation has been used [11], [12]. Thus, the channel potential is represented by

$$\varphi(x) = \left(4x^2/t_{\rm si}^2\right)\times(\varphi_s-\varphi_o)+\varphi_o \tag{2}$$

where φ_s and φ_o are the potential at the surface and the center of the channel, respectively. Parabolic potential approximation is commonly used in the subthreshold region [11], where mobile carrier charges are neglected. Therefore, to implement parabolic potential approximation in the subthreshold and linear regions, a different approach is needed to obtain expressions for φ_s and φ_o. Using the Gauss law and a boundary condition at the interface, it is possible to determine the relationships among φ_s, φ_o, and the gate voltage (V_G) as

$$-\frac{\varepsilon_{\rm ox}}{t_{\rm ox}}(V_G-V_{\rm FB}-\varphi_s) = -\varepsilon_{\rm si}\left.\frac{d\varphi}{dx}\right|_{x=t_{\rm si}/2} = \frac{4\varepsilon_{\rm si}}{t_{\rm si}}\Delta\varphi. \tag{3}$$

Here, $\varepsilon_{\rm ox}$ is the permittivity of the oxide, and $\Delta\varphi=\varphi_o-\varphi_s$. Note that the right part of (3) is equivalent to the assumption of a uniform charge distribution in the channel [13], i.e., $\Delta\varphi\approx(t_{\rm si}/8\varepsilon_{\rm si})\times(Q_{\rm mobile}+qN_{\rm si}t_{\rm si})$. In addition, a threshold criterion can directly be obtained from (3) by assuming a fully depleted channel and approximating φ_o to zero at $V_{\rm TH}$, i.e.,

$$V_{\rm TH} = V_{\rm FB} - qN_{\rm si}t_{\rm si}t_{\rm ox}/2\varepsilon_{\rm ox} - qN_{\rm si}t_{\rm si}^2/8\varepsilon_{\rm si}. \tag{4}$$

Equation (4) shows that $V_{\rm TH}$ increases as $t_{\rm si}$ or $t_{\rm ox}$ decreases.

An additional equation is necessary to relate φ_s and φ_o, because (3) alone cannot directly be applicable to determine those values. The left and right terms in (3) are related to the half-channel charge of the device. The total charge can also be obtained by integrating the charge density over the entire channel using the channel potential given by (2) as

$$\begin{aligned} Q_{\rm total} &= qN_{\rm si}t_{\rm si} - qN_{\rm si}\int_{-t_{\rm si}/2}^{t_{\rm si}/2} e^{(\varphi-V)/v_T}dx \\ &= qN_{\rm si}t_{\rm si}\times\left[1-\frac{e^{(\varphi_o-V)/v_T}}{2}\sqrt{\frac{\pi v_T}{\Delta\varphi}}\times{\rm Erf}\left(\sqrt{\frac{\Delta\varphi}{v_T}}\right)\right]. \end{aligned} \tag{5}$$

Equation (5) is not an analytical expression at this point; however, if $\Delta\varphi/v_T$ is equal to or greater than one, the error function tends to be unity. This condition is always valid, except when the applied gate voltage is approximately equal to $V_{\rm FB}$. Therefore, a new expression relating to φ_s and φ_o can be formulated as

$$2\frac{4\varepsilon_{\rm si}}{t_{\rm si}}\Delta\varphi = qN_{\rm si}t_{\rm si}\times\left(1-\frac{e^{(\varphi_o-V)/v_T}}{2}\sqrt{\frac{\pi v_T}{\Delta\varphi}}\right). \tag{6}$$

The aforementioned expression is formulated by equating the simplified expression of (5) and the left-hand side (although the

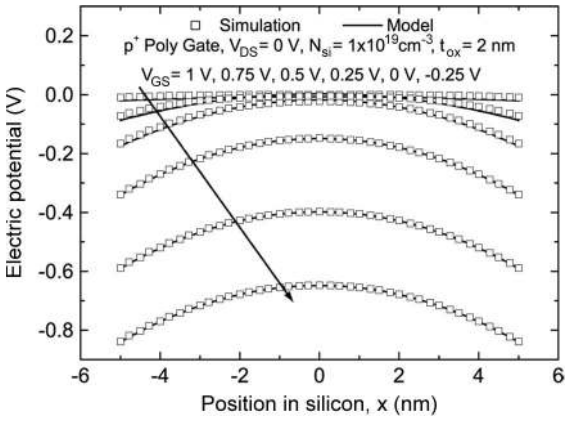

Fig. 2. Electric channel potential φ as a function of the position in the silicon channel for different gate voltages.

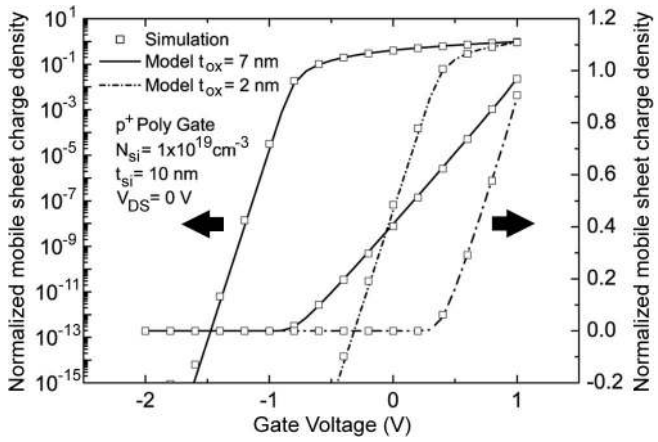

Fig. 3. Normalized sheet charge density of the mobile carriers obtained from (7) $-Q_{\rm mobile}/qN_{\rm si}t_{\rm si}$ as a function of the gate bias for dielectric thicknesses of $t_{\rm ox} = 7$ and 2 nm.

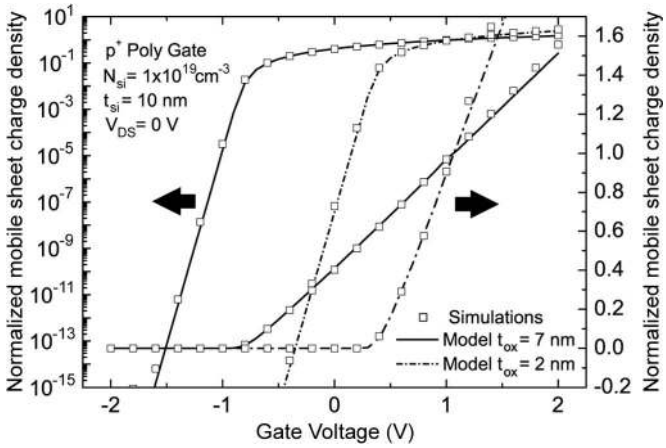

Fig. 4. Normalized sheet charge density of the mobile carriers obtained from (8) $-Q_{\rm mobile}/qN_{\rm si}t_{\rm si}$ as a function of the gate bias for dielectric thicknesses of $t_{\rm ox} = 7$ and 2 nm.

right-hand side is also possible) of (3) with an additional factor of two to account for the charge of the entire channel. Equations (3) and (6) form a self-consistent equation that can be used to determine φ_s and φ_o.

Fig. 2 shows a numerical example calculated from the aforementioned equations. It compares the electric potential in the channel for different gate voltages calculated from the proposed model and the value extracted from simulations. The simulated data were extracted through the Silvaco tool [14]. The Fermi–Dirac carrier statistics was employed in the simulation. At a lower voltage, the potential profile is bent, and its shape does not show gate–voltage dependence, given that the channel is fully depleted and the mobile charge density is much smaller than the doping charge density. This condition implies that $\Delta\varphi$ is a positive constant. For this gate bias, the device is in the subthreshold region. As the gate voltage increases, the potential profile becomes flatter; thus, $\Delta\varphi$ tends to be smaller. In this region, the channel is partially depleted, i.e., above the subthreshold region. When the gate voltage approaches $V_{\rm FB}$, φ_s and φ_o tend to be equal, and the potential is constant through the channel.

Based on the results of φ_s and φ_o, it is possible to extract the sheet charge density of the mobile carriers by subtracting the dopant charge term $(qN_{\rm si}t_{\rm si})$ from (5). However, after replacing $\Delta\varphi$ with $(t_{\rm si}/8\varepsilon_{\rm si}) \times (Q_{\rm mobile} + qN_{\rm si}t_{\rm si})$ and with simple subsequent algebraic manipulations of (3) and (6), it is possible to obtain a closed form of the expression for the mobile charge within the channel as

$$-\frac{2\varepsilon_{\rm ox}}{\beta t_{\rm ox}}(V_G - V_{\rm TH} - V) = Q_{\rm mobile} - \frac{2\varepsilon_{\rm ox}v_T}{\beta t_{\rm ox}} \ln\left(-Q_{\rm mobile}\sqrt{\frac{qN_{\rm si}t_{\rm si} + Q_{\rm mobile}}{2\varepsilon_{\rm si}\pi v_T q^2 N_{\rm si}^2 t_{\rm si}}}\right). \quad (7)$$

Here, $\beta = 1 + \varepsilon_{\rm ox}t_{\rm si}/4\varepsilon_{\rm si}t_{\rm ox}$, and $V_{\rm TH}$ is given by (4). Fig. 3 shows the normalized sheet charge density of the mobile carriers $-Q_{\rm mobile}/qN_{\rm si}t_{\rm si}$, as obtained from (7). The modeled data are compared with the simulated data. In the subthreshold and linear regions, the modeled data show good agreement with the simulated data. There is no notable difference in the behavior of the mobile carriers at different dielectric thicknesses, except that a thinner gate oxide shows a higher $V_{\rm TH}$ value due to the improved electrostatic control of the channel. In other words, a lower gate voltage with respect to $V_{\rm FB}$ is required to deplete the channel for a thicker gate dielectric, which is expected from (4). As the gate voltage approaches $V_{\rm FB}$, the sheet charge density of the mobile carriers tends to be $qN_{\rm si}t_{\rm si}$. This condition always occurs at $V_{\rm FB}$ and is independent of the gate dielectric and the channel thickness. This case is clearly different from the behavior of conventional inversion-mode DGFETs, where the mobile carrier density is sensitively affected by the gate dielectric thickness at any gate voltage.

Equation (7) can be simplified to

$$-\frac{2\varepsilon_{\rm ox}}{\beta t_{\rm ox}}(V_G - V_{\rm TH} - V) = Q_{\rm mobile} - \frac{2\varepsilon_{\rm ox}v_T}{\beta t_{\rm ox}} \ln\left(\frac{-Q_{\rm mobile}}{\sqrt{2\varepsilon_{\rm si}\pi v_T q N_{\rm si}}}\right) \quad (8)$$

because in the subthreshold region, $Q_{\rm mobile} \ll qN_{\rm si}t_{\rm si}$. Equation (8) is approximately equivalent to (7), because above the subthreshold region, (7) and (8) are dominated by the first term; thus, the aforementioned approximation does not affect

the relationship between the charge and voltages in this region. Fig. 4 shows the normalized sheet charge density of the mobile carriers obtained from (8). Equation (8) can be evaluated above $V_{\rm FB}$, where mobile charges accumulate on the surface of the channel. It is an accurate approximation in this region for $\beta < 1.1$, i.e., $t_{\rm si} < 12t_{\rm ox}$, which is the common case for thin channels used in JLFETs [1].

IV. Drain Current Model

A drain current expression can be derived by integrating the current continuity equation $I_{\rm DS}dy = -\mu W Q_{\rm mobile}dV$ from the source–drain region [6] and expressing dV as $(dV/dQ_{\rm mobile}) \times dQ_{\rm mobile}$. Here, μ is the effective mobility, and W is the device width. This approach gives the following form of the Pao–Sah integral, which includes the diffusion and drift current components

$$I_{\rm DS} = -\mu \frac{W}{L} \int_0^{V_{\rm DS}} Q_{\rm mobile} dV = -\mu \frac{W}{L} \int_{\rm Qs}^{Q_D} Q_{\rm mobile} \frac{dV}{dQ_{\rm mobile}} dQ_{\rm mobile}. \quad (9)$$

Here, L is the gate length of the device. Utilizing (8) to obtain (9), integration can analytically be performed to yield

$$I_{\rm DS} = -\mu \frac{W}{L} \left(\frac{\beta t_{\rm ox}}{4\varepsilon_{\rm ox}} Q_{\rm mobile}^2 - v_T Q_{\rm mobile} \right) \Bigg|_{\rm Qs}^{Q_D}. \quad (10)$$

Q_D and Q_S are obtained from (8) by replacing V by $V_{\rm DS}$ and 0, respectively.

V. Results and Discussion

To validate the proposed model, a 2-D numerical simulation using ATLAS [14] was carried out. The Lombardi mobility model is employed; it accounts for the temperature, doping, and field-dependence effects. The Fermi–Dirac carrier statistics, along with standard recombination models, is used in the simulation. Through the simulations, the channel length and the device width are equal to 1 μm. In addition, the source and drain length (L_S and L_D) are assumed to be small (10 nm) compared to the channel length. This way, parasitic resistance effects can be neglected. The parameters used for the modeled data are identical to the parameters used in the simulations. The effective mobility values used in the model were extracted from the simulations in the linear region, and their approximated values are 110 cm^2/Vs and 130 cm^2/Vs for devices with doping concentrations of 1×10^{19} cm^{-3} and 5×10^{18} cm^{-3}, respectively. Fig. 5 shows the drain current versus the drain voltage of a DG-JLFET. Figs. 6–9 show the drain current versus the gate voltage of DG-JLFETs for different drain voltages, oxide thicknesses, channel doping concentrations, and channel thicknesses, respectively. In addition, Fig. 10 shows the transconductance (g_m) versus the gate voltage for different

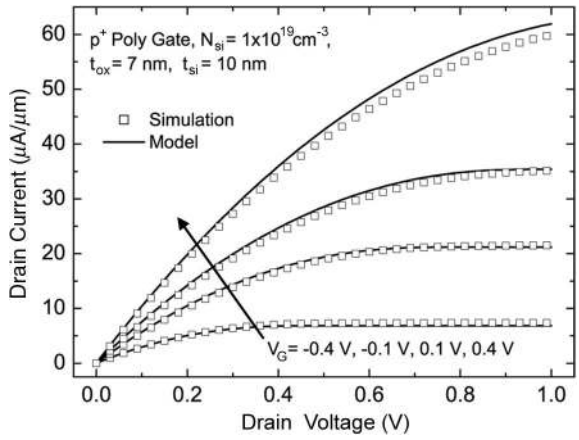

Fig. 5. Drain current versus drain voltage of a DG-JLFET for different gate voltages.

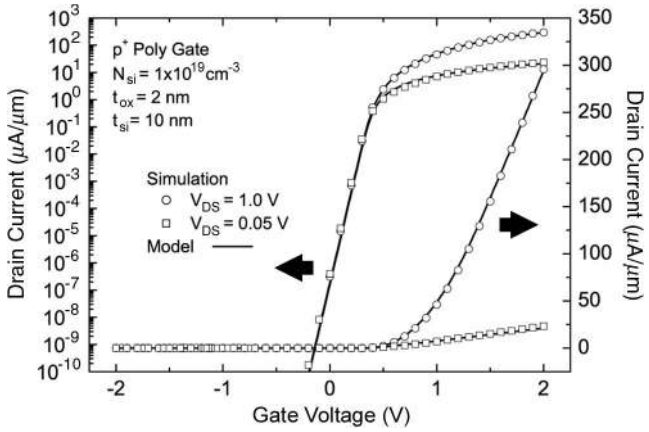

Fig. 6. Drain current versus gate voltage of a DG-JLFET for different drain voltages.

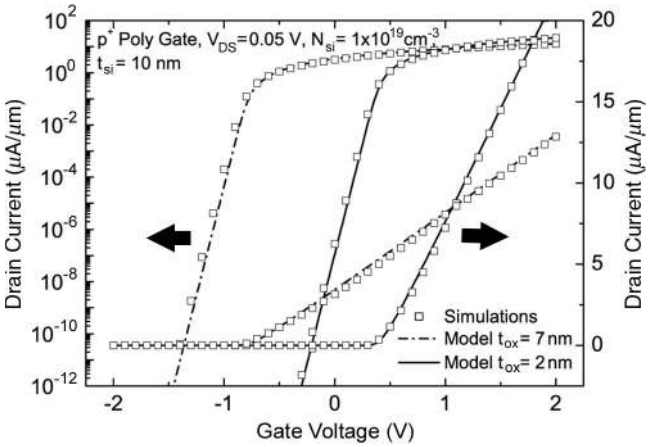

Fig. 7. Drain current versus gate voltage of a DG-JLFET for different oxide thicknesses.

devices, and Fig. 11 shows the output conductance $(g_{\rm DS})$ versus the drain voltage for different gate biases. Good correlation between the model and the simulation results validate the proposed model. It continuously predicts the characteristics of DG-JLFETs in all regions of operation (in this case, the linear, saturation, and subthreshold regions). For example, in the linear region, the first term on the right-hand side of (8) and the first

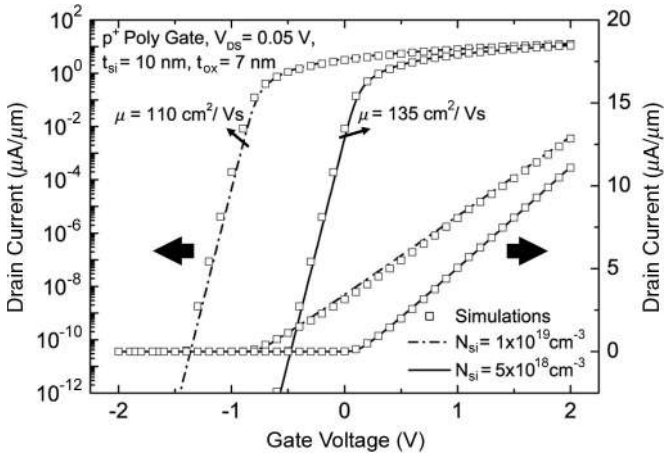

Fig. 8. Drain current versus gate voltage of a DG-JLFET for different channel doping concentrations.

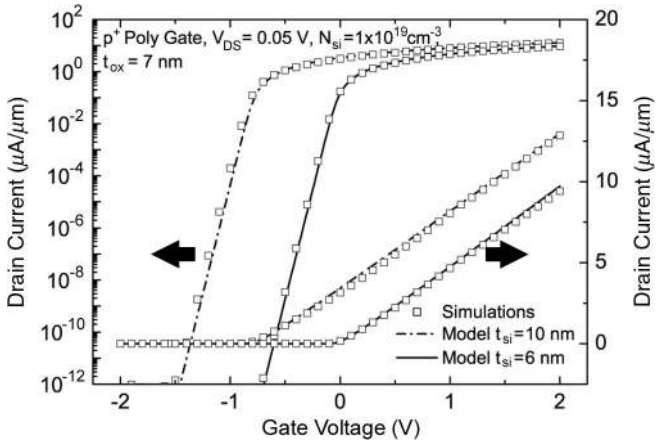

Fig. 9. Drain current versus gate voltage of a DG-JLFET for different channel thicknesses.

term of (10) are dominant; therefore, in this region, the drain current is given as

$$I_{\rm DS} \approx 2\mu \frac{\varepsilon_{\rm ox}}{\beta t_{\rm ox}} \frac{W}{L} \left(V_G - V_{\rm TH} - \frac{V_{\rm DS}}{2} \right) V_{\rm DS}. \qquad (11)$$

Equation (11) has the same form as the linear current expression for conventional inversion-mode DGFETs [6]; however, the total capacitance is reduced by $\beta = 1 + \varepsilon_{\rm ox} t_{\rm si} / 4 \varepsilon_{\rm si} t_{\rm ox}$. In addition, it has the same form as a recent piecewise model proposed for DG-JLFETs [5], which also accounts for the reduction in the gate capacitance. This reduction in the capacitance comes from the bulk current mechanism of JL transistors. When mobile carriers are confined at the center of the channel, additional capacitance appears in a series connection with the gate capacitance due to the depletion formed between the gate dielectric and the mobile charges, reducing the total capacitance that drives the current in JL transistors. Fig. 7 shows how the oxide thickness affects the device characteristics in the linear region. In the case of a thinner oxide, the current slope increases according to (11). When the doping concentration is reduced, the threshold voltage increases, as shown in Fig. 8. The current slope also increases due to the increment of the carrier mobility resulting from the reduction of impurity scattering in the channel. Although β depends on $t_{\rm si}$, its dependence is rather small. This condition is shown in Fig. 9, which shows two devices with different channel thicknesses. In this case, the current slope is similar in both devices. Utilizing (11), for a gate voltage equal to $V_{\rm FB}$, the drain current in the linear region can be expressed as follows:

$$I_{\rm DS} \approx \mu \frac{W}{L} q N_{\rm si} t_{\rm si} V_{\rm DS}. \qquad (12)$$

This equation is the common current expression for a resistor ($I = V/R$), which is also expected for JL transistors [1]. It shows that, in the linear region and for a gate voltage equal to $V_{\rm FB}$, the current does not depend on the dielectric thickness. This condition can be observed in Fig. 7, where both drain current curves meet at $V_{\rm FB}$, although their gate dielectric thicknesses are different.

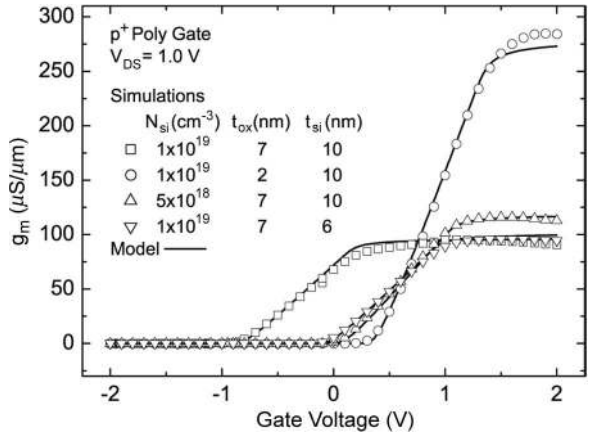

Fig. 10. Transconductance versus gate voltage for different DG-JLFETs.

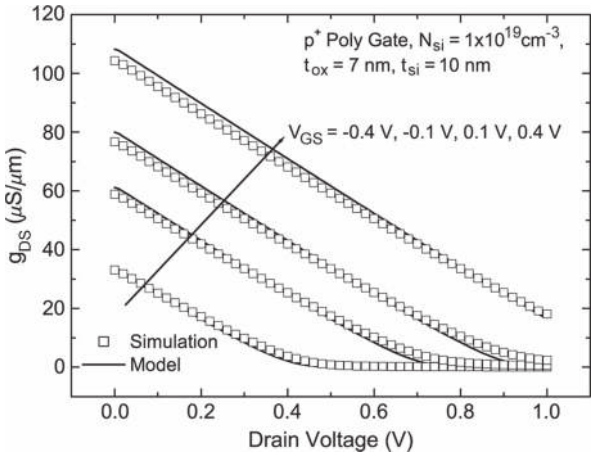

Fig. 11. Output conductance versus drain voltage of a DG-JLFET for different gate biases.

In the saturation region, the device experiences a pinchoff at the center of the channel on the drain side [2], [5]. In this operation region, for the drain charge and the source charge, the second and first terms of the right-hand side of (8) are dominant, respectively. Hence, the second term of (10) is dominant for the drain charge Q_D, and the first term is dominant for the source

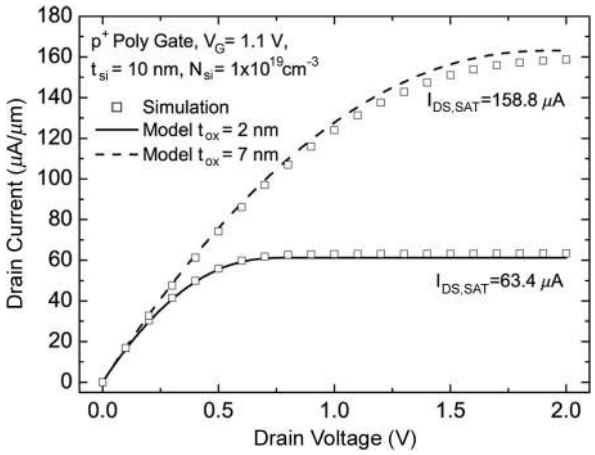

Fig. 12. Drain current versus drain voltage of a DG-JLFET for different oxide thicknesses. The transistors are biased at a gate voltage equal to 1.1 V ($\sim V_{\rm FB}$).

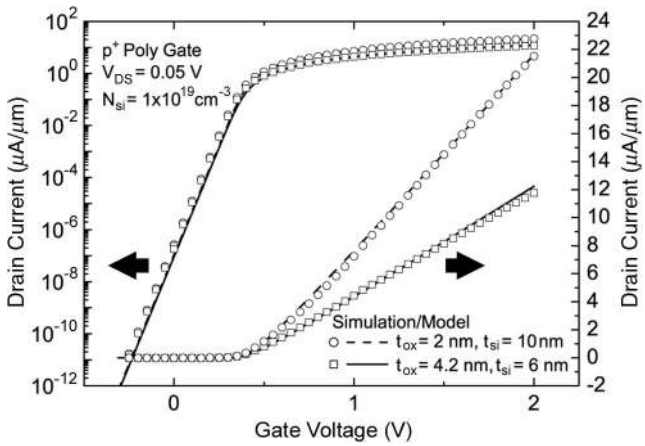

Fig. 13. Drain current versus gate voltage of two DG-JLFETs with equivalent threshold voltages and different channel and oxide thicknesses.

charge Q_S. Therefore, in the saturation region, the drain current is given by

$$I_{\rm DS} \approx \mu \frac{\varepsilon_{\rm ox}}{\beta t_{\rm ox}} \frac{W}{L} \left[(V_G - V_{\rm TH})^2 - \frac{v_T \beta t_{\rm ox}}{\varepsilon_{\rm ox}} \times \sqrt{qN_{\rm si}\pi v_T 2\varepsilon_{\rm si}} e^{(V_G - V_{\rm TH} - V_{\rm DS})/v_T} \right]. \quad (13)$$

Equation (13) has the same form as the saturation current expression for conventional inversion mode DGFETs [6], which also includes a term that exponentially decreases with $V_{\rm DS}$. This term is not included in the piecewise model for DG-JLFETs [5], where the current is made to be constant in saturation. Neglecting the exponentially decreasing term in (13), the saturation current at a gate voltage equal to $V_{\rm FB}$ is approximately given as

$$I_{\rm DS} \approx \mu \frac{\beta t_{\rm ox}}{2\varepsilon_{\rm ox}} \frac{W}{L} (qN_{\rm si} t_{\rm si})^2. \quad (14)$$

Equation (14) shows that the drain current also depends on the gate dielectric thickness when the gate voltage is equal to $V_{\rm FB}$ in the saturation region. This trend in the saturation region is clearly different from the linear region, as expressed by (12). Fig. 12 shows the drain current versus the drain voltage for the devices in Fig. 7, with the applied gate voltage equal to 1.1 V ($\sim V_{\rm FB}$). In the linear region, both drain currents are approximately equal, as expected based on Fig. 7; however, as the devices approach the saturation region, the drain current values are no longer similar. The ratio between the saturation currents for the devices shown in Fig. 12 can be obtained from the ratio of their $\beta t_{\rm ox}$ values. The proposed model gives a ratio equal to 2.76, which is similar to the value extracted from the simulation, i.e., 2.48.

In the subthreshold region, the second terms on the right-hand side of (8) and in (10) are dominant. Therefore, the subthreshold current is approximately given by

$$I_{\rm DS} \approx \mu \frac{W}{L} v_T \sqrt{qN_{\rm si}\pi v_T 2\varepsilon_{\rm si}} e^{(V_G - V_{\rm TH})/v_T} (1 - e^{-V_{\rm DS}/v_T}). \quad (15)$$

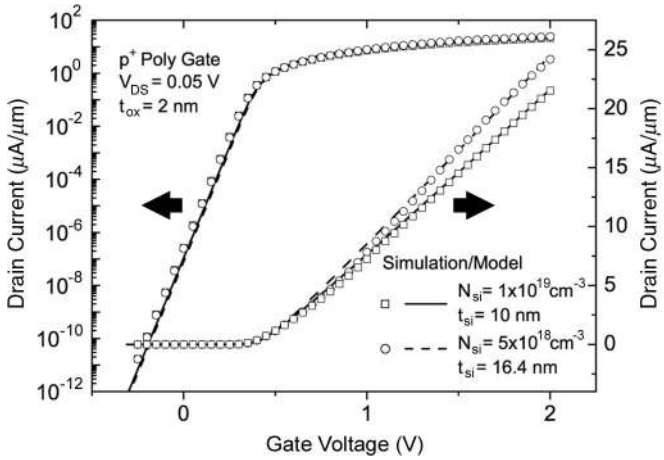

Fig. 14. Drain current versus gate voltage of two DG-JLFETs with equivalent threshold voltages and different channel doping concentrations and channel thicknesses.

This expression is identical to the subthreshold current of the piecewise model proposed for DG-JLFETs [5]. In a manner different from the subthreshold current in conventional inversion-mode DGFETs [6], (15) is not proportional to the channel thickness. Therefore, for devices with the same width, length, doping concentration, and threshold voltage, the subthreshold current in DG-JLFETs would be the same and independent of their dielectric and channel thickness values. For example, a device with $t_{\rm si} = 10$ nm and $t_{\rm ox} = 4$ nm would have the same threshold voltage as a device with $t_{\rm si} = 6$ nm and $t_{\rm ox} = 4.2$ nm, which is expected from (4). These devices would have the same subthreshold current, as described in (15). This behavior is shown in Fig. 13. Although the devices' subthreshold behaviors are equivalent, their linear behaviors are different. In the case of a smaller dielectric thickness, the device exhibits higher on-state current, as shown by (11). Fig. 14 shows the drain current versus the gate voltage of two devices with equivalent threshold voltages but with different channel doping characteristics. The device with less doping has a slightly lower subthreshold current; however, its linear current is clearly increased due to the increment in mobility [15].

VI. Conclusion

In conclusion, a 1-D continuous charge model has been developed for a symmetric long-channel DG-JLFET with Pao–Sah electrostatic assumptions and by extending the parabolic potential approximation in the subthreshold and the linear regions, considering the dopant and mobile carrier charges. The Pao–Sah integral is analytically carried out by utilizing the continuous charge model, obtaining a continuous drain current model that captures the phenomenon of the bulk conduction mechanism in all regions of device operation, i.e., the subthreshold, linear, and saturation regions. It has been shown that the continuous model is in complete agreement with the numerical simulations. In addition, the model predicts the main differences with respect to conventional inversion-mode DGFETs: a reduction of the gate capacitance and subthreshold current proportional dependence only on the channel doping. To complete the proposed model, additional physical effects, e.g., quantum mechanical effects, short-channel effects, field-dependence mobility, and parasitic resistance effects, should be added as future work.

References

[1] J.-P. Colinge, C.-W. Lee, A. Afzalian, N. Dehdashti Akhavan, R. Yan, I. Ferain, P. Razavi, B. O'Neill, A. Blake, M. White, A.-M. Kelleher, B. McCarthy, and R. Murphy, "Nanowire transistors without junctions," *Nat. Nanotechnol.*, vol. 5, no. 3, pp. 225–229, Mar. 2010.

[2] A. Kranti, R. Yan, C.-W. Lee, I. Ferain, R. Yu, N. D. Akhavan, P. Razavi, and J.-P. Colinge, "Junctionless nanowire transistor (JNT): Properties and design guidelines," in *Proc. ESSDERC*, Sep. 14–16, 2010, pp. 357–360.

[3] S. Gundapaneni, S. Ganguly, and A. Kottantharayil, "Bulk planar junctionless transistor (BPJLT): An attractive device alternative for scaling," *IEEE Electron Device Lett.*, vol. 32, no. 3, pp. 261–263, Mar. 2011.

[4] Y. Taur and T. H. Ning, *Modern VLSI Devices,* 2nd ed. Cambridge, U.K.: Cambridge Univ. Press, 2009, p. 530.

[5] J. P. Duarte, S.-J. Choi, D.-I. Moon, and Y.-K. Choi, "Simple analytical bulk current model for long-channel double-gate junctionless transistors," *IEEE Electron Device Lett.*, vol. 32, no. 6, pp. 704–706, Jun. 2011.

[6] Y. Taur, X. Liang, W. Wang, and H. Lu, "A continuous, analytic drain-current model for DG MOSFETs," *IEEE Electron Device Lett.*, vol. 25, no. 2, pp. 107–109, Feb. 2004.

[7] J.-M. Sallese, N. Chevillon, C. Lallement, B. Iniguez, and F. Pregaldiny, "Charge-based modeling of junctionless double-gate field-effect transistors," *IEEE Trans. Electron Devices*, vol. 58, no. 8, pp. 2628–2637, Aug. 2011.

[8] H. C. Pao and C. T. Sah, "Effects of diffusion current on characteristics of metal–oxide (insulator)–semiconductor transistors," *Solid State Electron.*, vol. 9, no. 6, pp. 927–937, Jun. 1966.

[9] P. Francis, A. Terao, D. Flandre, and F. Van de Wiele, "Modeling of ultra-thin double-gate nMOS/SOI transistors," *IEEE Trans. Electron Devices*, vol. 41, no. 5, pp. 715–720, May 1994.

[10] O. Moldovan, A. Cerdeira, D. Jimenez, J.-P. Raskin, V. Kilchytska, D. Flandre, N. Collaert, and B. Iniguez, "Compact model for highly-doped double-gate SOI MOSFETs targeting baseband analog applications," *Solid State Electron.*, vol. 51, no. 5, pp. 655–661, May 2007.

[11] K. K. Young, "Analysis of conduction in fully depleted SOI MOSFETs," *IEEE Trans. Electron Devices*, vol. 36, no. 3, pp. 504–506, Mar. 1989.

[12] K. Suzuki, T. Tanaka, Y. Tosaka, H. Horie, and Y. Arimoto, "Scaling theory for double-gate SOI MOSFETs," *IEEE Trans. Electron Devices*, vol. 40, no. 12, pp. 2326–2329, Dec. 1993.

[13] G. Baccarani and S. Reggiani, "A compact double-gate MOSFET model comprising quantum-mechanical and nonstatic effects," *IEEE Trans. Electron Devices*, vol. 46, no. 8, pp. 1656–1666, Aug. 1999.

[14] *Atlas User's Manual: Device Simulation Software*, Silvaco Int., Santa Clara, CA, 2008.

[15] C. Lombardi, S. Manzini, A. Saporito, and M. Vanzi, "A physically based mobility model for numerical simulation of nonplanar devices," *IEEE Trans. Comput.-Aided Design Integr. Circuits Syst.*, vol. 7, no. 11, pp. 1164–1171, Nov. 1988.

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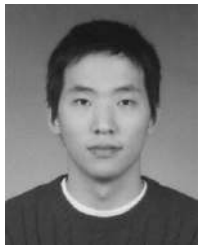

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