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A Fully-Digital, 0.3V, 270 nW Capacitive Sensor Interface Without External References

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***Abstract*— This paper presents a fully-digital capacitive sensor interface. By directly transforming the sensor value instead of using an intermediate step in the voltage domain, the architecture can cope with very low signal swings. An implementation for barometric pressure sensing with a supply voltage of 0.3 V demonstrates the benefits. With a power consumption of only 270 nW and an acquisition time of 1 ms, an ENOB of 6.1 is obtained, resulting in a FOM of 2.1 pJ/conv for the entire interface. This is at least an order of magnitude better than current state-of-the-art implementations.**

I. Introduction

Sensors are gaining popularity in different fields of applications like automotive, Wireless Sensor Networks (WSN), medical care, consumer electronics, etc. Sensor signals need to be pre-processed prior to feeding them to a higher system level with the use of sensor interfaces. In the past, these interface circuits consisted of discrete components and they processed the output signals of a sensor that was external to the chip. Now, the evolution to smart sensors, where the sensor is integrated on the chip results in smaller systems, lower cost and lower power consumption. Moreover, the semiconductor industry is driven towards smaller technologies in order to further reduce the cost and power consumption of the devices. This is crucial when either aiming for cheaper high volume sensor systems or low-power devices for WSN.

Technology scaling is especially beneficial for digital circuits. The reduced parasitic capacitance improves both power and speed performance significantly and a large area reduction can be acquired. Analog circuits, however, are less scalable and suffer more when going to nanometer CMOS technologies. Besides the issues of matching and noise, the threshold voltage (VT) is reduced less significant compared to the power supply. This results in a reduced signal range for analog signals in the voltage domain [1]. Hence, when targetting ultra-low voltage implementations as well as thorough area scaling, digital oriented solutions are needed.This paper presents the design of a fully-digital ultra-low-power, low-voltage capacitive sensor interface, without the need of external time/voltage references, based on a PLL-based conversion mechanism.

The paper is organized as follows. Section II describes the system level overview of the proposed interface followed by the design implementation in section III. Next, in section IV, measurement results are presented and compared to state-of-the-art designs. Finally, some conclusions are drawn in section V.

II. System level overview

Traditionally, a sensor interface consists of a sensor, which converts the physical quantity a(t) into an electrical analog signal b(t). An analog processing chain creates a more usable, larger input signal c(t), and a conversion block digitizes the wanted signal into a digital output d(t) (see Fig.1A). These architectures however suffer from problems such as reduced signal swing and noise, as described in the previous section. When the signal is transformed to frequency information, however, it suffers less from these issues. Furthermore, time conversion mechanisms are gaining popularity since they also take advantage of the improved timing resolution of the higher device speeds in smaller technologies [2].

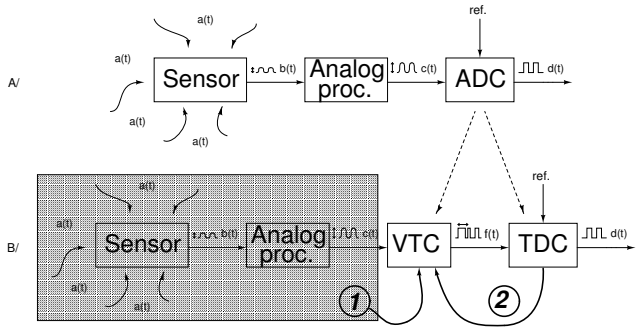

Fig. 1. Basic overview of a sensor interface system. On top (A) a conventional interface is demonstrated which processes the sensor signal in the analog voltage domain before quantizing the information. At the bottom (B) a schematic of an interface, based on time-information conversion mechanism is shown. The two main design approaches of this work are illustrated: avoid processing in the voltage domain (1) and use feedback (2).

Time-based conversion mechanisms replace the traditional Analog-to-Digital Converter (ADC) by two building blocks (see Fig.1B). The Voltage-to-Time Converter (VTC) transforms the analog signal c(t) into time or frequency information f(t) while the Time-to-Digital Converter digitizes this information with the help of a reference frequency. In order to achieve the wanted resolution, an accurate reference clock signal is needed.

A. Design approach

The design approach of the work described in this paper consists of 2 principles which are indicated with (1) and (2) in Fig. 1B:

1) Omit the conversion of the sensor signal into an analog voltage and directly convert it to frequency information. This makes the sensor information less sensitive to noise and it can be processed in a highly digital way.
2) Use feedback to relax the constraints of the different building blocks.

As a feedback mechanism, the proposed architecture will use the PLL-based conversion mechanisms demonstrated in [3]. It has the advantage of combining the nice properties of conventional Sigma-Delta ADCs (oversampling and noise-shaping) without the need of an analog loop filter nor an external reference. This PLL-based schematic is adapted by directly integrating the sensor in the oscillator and hence creating a sensor dependent frequency signal. Capacitive sensors are very useful for this approach as they can be used as part of a variable delay element. Furthermore, these sensors are suited for autonomous sensor applications since they dissipate no power and offer a high sensitivity [4].

B. Working principle

A schematic overview of the PLL-based interface described in [3] is given in Fig. 2A) and consists of the building blocks mentioned in Fig. 1. The voltage-to-time conversion is done by a sensor-steered oscillator OSC_{sens} which creates a sensor dependant frequency f_{sens}. However, this frequency is not measured by an accurate reference signal like normally done in open-loop architectures. The phase of OSC_{sens} is compared to the phase of a second, digitally steered oscillator OSC_{dig}. The steering signal b_{out}, needed to lock OSC_{dig} to OSC_{sens} is a representation of the phase difference between both oscillators. This PLL is a bang-bang PLL having a binary phase detector which only measures whether OSC_{sens} leads or lags the frequency f_{dig} of the digitally steered oscillator [5]. OSC_{dig} is hence only steered by 2 values and thus generates 2 different frequency values. The main benefit of this type of PLL is that the phase detector can easily be implemented by a simple D flip-flop, very suitable for low supply voltages.

We can define the following variables:

$$f_{sens} = f_q + \delta f \tag{1}$$

$$f_{dig} = f_q + \varepsilon f_{bb} \tag{2}$$

$$\varepsilon = sign[\theta_e] \tag{3}$$

where f_q is the quiescent frequency of both oscillators and δf the variation of f_{sens}. Every time the phase difference is measured by the phase detector, the binary error ε is determined as described in equation (3). This error signal is fed back to OSC_{dig} which results in a frequencyshift of $\varepsilon\beta K_{VCO}$.

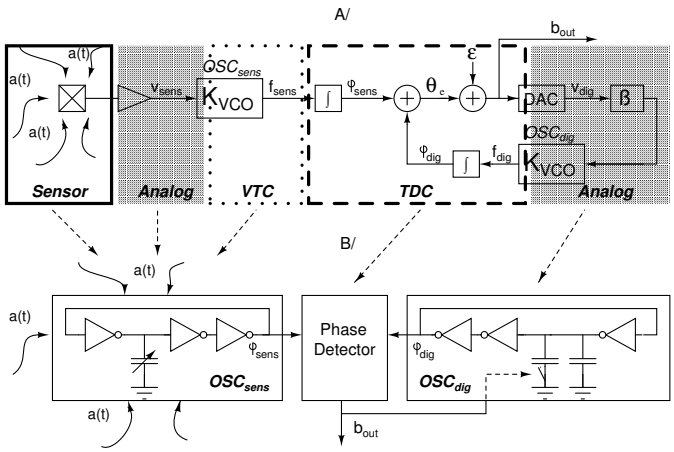

Fig. 2. On top (A), a schematic overview of the PLL system is given as it is described in [3]. The different zones, mentioned in Fig. 1B are highlighted. The bottom schematic (B) displays the proposed, adapted configuration of the PLL-based converter where the sensor is directly integrated in the oscillator and analog processing is avoided.

When the PLL is locked, the average frequency shift over a certain time interval equals the frequency shift δf of OSC_{sens}. Otherwise stated: the average frequency generated by OSC_{dig} equals f_{sens}. This is only true when the duty cycle of the phase detector corresponds to:

$$\delta f = Dc\beta K_{VCO} + (1 - Dc)(-\beta K_{VCO}) \tag{4}$$

Therefore, the value of the duty cycle is respresented by:

$$Dc = (\frac{1}{2} + \frac{\delta f}{2\beta K_{VCO}}) \tag{5}$$

As a result, the duty cycle (corresponding to b_{out}) at the output of the phase detector is proportional to the frequency variation δf of OSC_{sens}. Since δf is also proportional to the wanted sensor value, b_{out} is an (oversampled) digital value of the wanted signal.

In [3], the sensor value is first transformed into a voltage signal which steers a Voltage Controlled Oscillator (VCO). As mentioned, this work will integrate a capacitive sensor in an oscillator creating a Capacitance Controlled Oscillator (CCO). This is described in the next section for a specific test case.

III. Design implementation

A test chip working at a 0.3V supply voltage is designed both to demonstrate the working principle of the proposed architecture and to emphasize the highly digital nature of the proposed work. This chip targets barometric pressure sensing for ultra-low-power applications such as WSN [6] or bladder monitoring [7]. Since these devices are battery powered or use energy scavenging, sub-microwatt power consumption is a hard constraint while accuracy is less important. The test chip has been implemented in an UMC 0.13μm CMOS technology. As a sensor, the barometric pressure sensor E1.3 of Microfab

is used. This sensor has an offset value C_q of 5.7 pF and a variable capacitance δC of 300 fF. An acquisition time of 1 ms is desirable to reduce the duty cycle and to further extend the lifetime of these devices.

An overview of the full system is given by Fig. 2B. It consists of two CCOs and a phase detector which measures whether OSC_{sens} leads or lags OSC_{dig}. The output of this phase detector is the 1 bit oversampled digital output of the sensor signal. It is used to steer the frequency of OSC_{dig} to lock the PLL. While, for bang-bang PLLs, this phase detector is a simple D flip-flop, the design of the CCO is much more stringent.

A. CCO

In order to achieve good performance at ultra-low voltages, the sensor, the analog part and the VTC as well as the DAC and the digitally steered oscillator are replaced by 2 CCOs (see Fig. 3). These CCOs are multistage relaxation oscillator consisting of one variable delay element and a number of dummy delay elements. The delay of the variable delay element is determined by the current I_{load} and the load capacitance C_{load}.

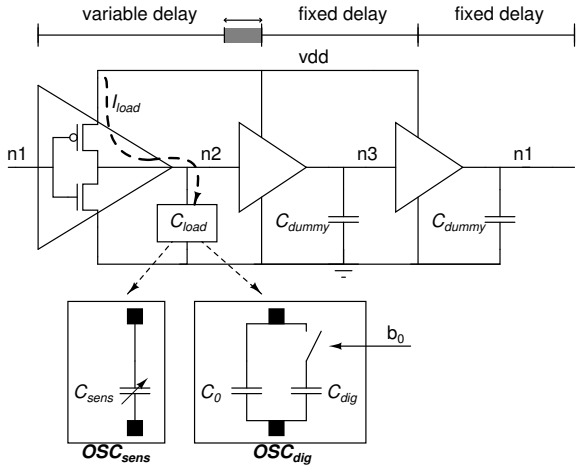

Fig. 3. schematic overview of the CCO which integrates the sensor/DAC in the oscillator.

The oscillating frequency of the multistage relaxation oscillator depends on the time it takes a transition to propagate around the loop [8]. For a standard ringoscillator and assuming an equal rise and fall time for the different stages respectively, this results in:

$$f_0 \approx \frac{I_{load}}{V_{swing} \times (C_{load} + 2C_{dummy})} \quad (6)$$

This shows that the frequency is proportional to the load capacitance C_{load}. In Fig. 3, a distinction is made between the load of OSC_{sens} and OSC_{dig}. The former consists of the capacitive sensor C_{sens} while the latter consists of a constant element C_0 and a switchable element C_{dig}, which is slightly larger than the variable range δC of the sensor.

For this design, a ring oscillator is chosen since it is the most digital oriented block and can run with lower supply voltages compared to differential relaxation oscillators. Furthermore, it doesn't consume static power which results in better overall power performance. While C_{load} is large, C_{dummy} is kept small in order to reduce the power consumption and to increase the sensitivity. On the other hand, the linearity of asymmetric oscillators is worse and they suffer more from phase noise. The linearity error for this design, however, is smaller than 1 % which is less than the required resolution.

B. Matching

Besides the difference in load, matching between the two oscillators is very important. Yet, C_{sens} is an external component which needs to be bonded while $C_0 + C_{dig}$ is an integrated component. To enhance matching, the routing of both pads will be exactly symmetrical and dummy-bondpads will be added for the digital load. They are bonded as well. To perform final calibration, trimming capacitors are added on chip. In order to ensure good behavior of the interface over the full capacitive sensor swing, the switchable element C_{dig} is designed to be bigger than the variable capacitive range of C_{sens}. For this implementation, where the sensor variation is 300 fF, C_{dig} can be programmed to a value between 300 fF and 600 fF.

IV. Measurement Results

Measurements have been done using a sealed container and a reference pressure sensor. The quiescent frequency for this implementation is 825kHz at 300 mV. For an acquisition time of 1 ms, this results in an OSR of 825. While the total current consumption is 901 nA for the entire interface, the Effective Number Of Bits (ENOB) is 6.1. The results are displayed in Fig. 5. The nonlinearity of the pressure to the output is caused by the nonlinear pressure vs. capacitance characteristic of the sensor [9].

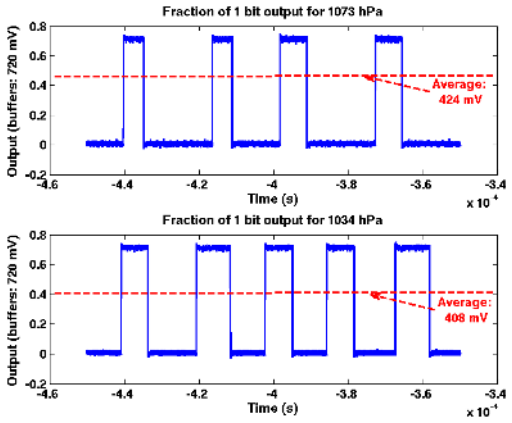

Fig. 4. Experimental (partial) waveform measured on the test chip for two pressure values: 1073 hPa and 1034 hPa.

A part of the output signal is shown in Fig. 4 for two measurements. The top waveform displays a small part of the digital output for a pressure value of 1073 hPa while the bottom waveform is the output which corresponds to 1034 hPa.

TABLE I

PERFORMANCE COMPARISON OF THIS WORK AND OTHER PRESENTED DESIGNS

Ref.	Tech. [μm]	Area	C_0	V-Supply	Resolution [ENOB]	I	Conversion Frequency	FOM
ESSCIRC 2008 [10]	0.32	0.538 mm^2	500 fF	3.3V	no conversion	28 μA	-	-
TCAS 2007 [11]	0.5	9.28 mm^2	10.3 pF	3V	8 bits	2.3 μA	10 Hz	1.37 nJ/conv
ASSCC 2007 [12]	0.18	0.0342 mm^2	3 pF	1.4V	6.8 bits	360 μA	262 kHz	17.3 pJ/conv
[This Work]	0.13	0.0725 mm^2	5.7 pF	0.3V	6.1 bits	901 nA	1 kHz	2.1 pJ/conv

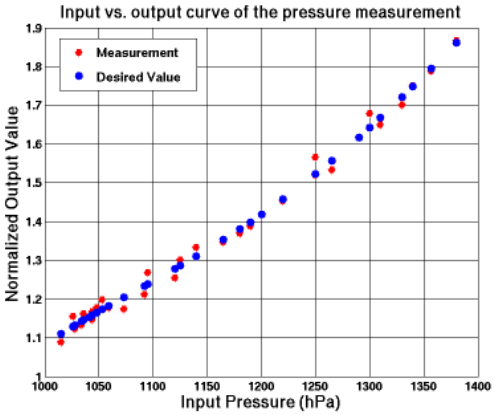

Fig. 5. Measurement results for the pressure measurement from 1018 hPa to 1380 hPa. The Measurement curve describes the measured values where an ENOB of 6.1 is obtained. The other curve corresponds to the desired curve. The nonlinearity is due to the nonlinear characteristic of the sensor.

The performance of the interface is compared to the state-of-the-art with the Figure Of Merit (FOM) described in [11]:

$$FOM = \frac{P}{2^{ENOB} \times 2 \times Bandwidth} \tag{7}$$

Table I gives an overview of the specifications of this design and a comparison with 3 different state-of-the-art capacitive interfaces. Since the power consumption of the proposed work is very low, a very good FOM is acquired despite the moderate resolution. Therefore, it is demonstrated that, in spite of the non-idealities of ultra-low-voltage processing, a competitive interface is realized. The implementation of the chip is shown in Fig. 6 and the active area is only 0.0725 mm^2.

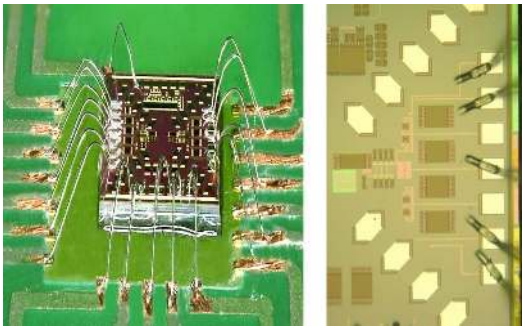

Fig. 6. Die photograph of the capacitive sensor interface. On the left, a picture of the bonded die can be observed. On the right, 2D chip photo is displayed where the active area is 0.0725 mm^2

V. CONCLUSION

This paper describes a fully-digital 0.3V capacitive sensor interface. It's functionality has been proven with a power consumption of 270 nW and a FOM of 2.1 pJ/conv. for the entire interface, which exceeds current state-of-the-art. Furthermore, no external reference is needed. An ENOB of 6.1 is achieved. By improving the matching and phase noise of the oscillators, higher resolutions can be obtained at the cost of more power consumption.

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