A Fully Integrated 24-GHz Eight-Element Phased-Array Receiver in Silicon

Xiang Guan, *Student Member, IEEE*, Hossein Hashemi, *Member, IEEE*, and Ali Hajimiri, *Member, IEEE*

***Abstract*—This paper reports the first fully integrated 24-GHz eight-element phased-array receiver in a SiGe BiCMOS technology. The receiver utilizes a heterodyne topology and the signal combining is performed at an IF of 4.8 GHz. The phase-shifting with 4 bits of resolution is realized at the LO port of the first down-conversion mixer. A ring *LC* voltage-controlled oscillator (VCO) generates 16 different phases of the LO. An integrated 19.2-GHz frequency synthesizer locks the VCO frequency to a 75-MHz external reference. Each signal path achieves a gain of 43 dB, a noise figure of 7.4 dB, and an IIP3 of −11 dBm. The eight-path array achieves an array gain of 61 dB and a peak-to-null ratio of 20 dB and improves the signal-to-noise ratio at the output by 9 dB.**

***Index Terms*—BiCMOS integrated circuits, low-noise amplifiers, phase shifting, phased arrays, receivers, wireless communications.**

I. Introduction

OMNIDIRECTIONAL communication has been used extensively in various applications due to its insensitivity to orientation and location. Unfortunately, such systems suffer from several shortcomings. The transmitter radiates electromagnetic power in all directions, a small fraction of which reaches the intended receiver. Thus, for a given receiver sensitivity, a substantially higher power needs to be radiated by an omnidirectional transmitter. Not only is a major fraction of this power wasted, but also it is often reflected off of various objects, resulting in multipath fading and additional interference for other users.

On the other hand, in a directional communication system, power is only transmitted in the desirable direction(s) and is received from the intended source(s). This is commonly achieved by using directional antennas (e.g., a parabolic dish) that provide antenna gain for certain directions and attenuation in others. Due to the passive nature of the antenna and the conservation of energy, the antenna gain and its directionality go together; a higher gain corresponds to a narrower beam width. Directional antennas are used when the relative location and orientation of neither the transmitter nor the receiver change quickly or frequently and are known in advance. For example, this is the case in fixed-point microwave links and satellite receivers. The additional antenna gain at the transmitter and/or receiver can substantially improve the signal-to-noise-plus-interference ratio (SNIR) and thereby increase the effective channel capacity. However, a single directional antenna is not well suited for portable applications, where its orientation needs to be changed quickly and constantly via mechanical means.

Fortunately, multiple-antenna phased arrays can be used to imitate a directional antenna whose bearing can be controlled electronically with no need for mechanical movement [1]–[6]. This electronic steering makes it possible to take advantage of the antenna gain and directionality while eliminating the need for continuous mechanical reorientation of the antenna. Additionally, multiple-antenna systems alleviate the requirements for individual active devices used in the array and make the system more robust to individual component failure.

Various forms of multiple antenna systems provide a plethora of solutions for communications and radar, such as multiple-input-multiple-out (MIMO) diversity transceivers and synthetic aperture radars (SARs). Phased arrays constitute a special class of multiple antenna systems that enable beam and null forming in various directions. However, these systems have been implemented using a large number of microwave modules, adding to their cost and complexity [5], [6].

Higher frequencies offer more bandwidth while reducing the required antenna size and spacing. The industrial, scientific, and medical (ISM) band at 24 GHz is a good candidate for broadband communication using multiple-antenna systems with a small size. Additionally, for indoor environments, the delay spread is smaller compared to lower frequency bands such as 2.4 and 5 GHz, allowing higher data rates [7]. A 2002 FCC ruling has opened the 22–29-GHz band for automotive radar systems, such as autonomous cruise control (ACC) [8].

In the last paragraph of his seminal paper published in 1965 [9], Gordon Moore prophesied: "Even in the microwave area, structures included in the definition of integrated electronics will become increasingly important... The successful realization of such items as phased-array antennas, for example, using a multiplicity of integrated microwave power sources, could completely revolutionize radar." Integration of a complete phased array system in silicon results in substantial improvements in cost, size, and reliability. At the same time, it provides numerous opportunities to perform on-chip signal processing and conditioning, without having to go off-chip, leading to additional savings in cost and power.

In this paper, we introduce the first fully integrated silicon-based eight-element phased-array receiver operating at 24 GHz that realizes Moore's prophecy in silicon almost 40 years later. In Section II, we review the phased-array principles of operation and its performance advantages. Section III covers the architecture of the phased-array receiver. The circuit details of various

Manuscript received April 19, 2004; revised July 15, 2004.

X. Guan and A. Hajimiri are with the Moore Laboratory, California Institute of Technology, Pasadena, CA 91125 USA (e-mail: xiangg@caltech.edu).

H. Hashemi is with the Department of Electrical Engineering—Electrophysics, University of Southern California, Los Angeles, CA 90089 USA.

Digital Object Identifier 10.1109/JSSC.2004.836339

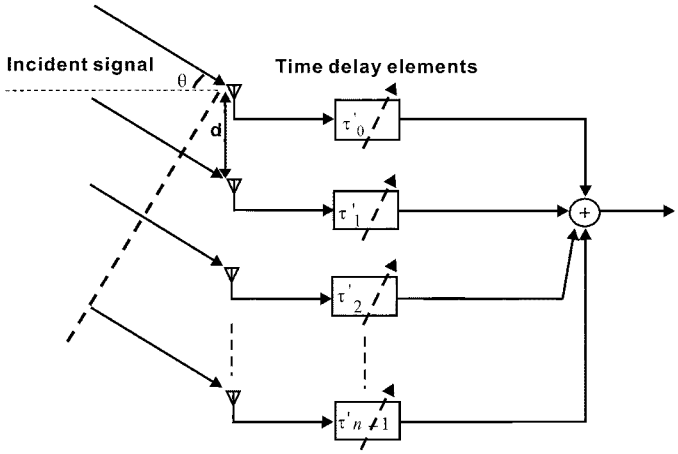

Fig. 1. A generic phased-array architecture.

blocks of the phased array are discussed in Section IV. Section V shows the measurement results.

II. Review of Phased-Array Principle

A phased-array receiver consists of several signal paths, each connected to a separate antenna. Generally, radiated signal arrives at spatially separated antenna elements at different times. An ideal phased-array compensates for the time-delay difference between the elements and combines the signals coherently to enhance the reception from the desired direction(s), while rejecting emissions from other directions. The antenna elements of the array can be arranged in different spatial configurations [4]. We will use a one-dimensional (1-D) n-element linear array as an example to illustrate the principle as shown in Fig. 1. We will discuss only the receiver case in this paper, but similar concepts are applicable to the transmitter due to reciprocity.

A. Delay Versus Phase Compensation

For a plane wave, the signal arrives at each antenna element with a progressive time delay τ at each antenna. This delay difference between two adjacent elements is related to their distance d and the signal angle of incidence with respect to the normal θ by

$$c\tau = d\sin\theta \tag{1}$$

where c is the speed of light. In general, the signal arriving at the first antenna element is given by

$$S_0(t) = A(t)\cos[\omega_c t + \varphi(t)] \tag{2}$$

where $A(t)$ and $\varphi(t)$ are the amplitude and phase of the signal and ω_c is the carrier frequency. The signal received by the kth element can be expressed as

$$\begin{aligned} S_k(t) &= S_0(t - k\tau) \\ &= A(t - k\tau)\cos[\omega_c t - k\omega_c\tau + \varphi(t - k\tau)]. \end{aligned} \tag{3}$$

The equal spacing of the antenna elements is reflected in (3) as a progressive phase difference $\omega_c\tau$ and a progressive time delay τ in $A(t)$ and $\varphi(t)$. Adjustable time-delay elements τ_k' can compensate the signal delay and phase difference simultaneously, as shown in Fig. 1. The combined signal $S_{\rm sum}(t)$ can be expressed as

$$\begin{aligned} S_{\rm sum}(t) &= \sum_{k=0}^{n-1} S_k(t - \tau_k') \\ &= \sum_{k=0}^{n-1} A(t - k\tau - \tau_k') \\ &\quad \times \cos\left[\omega_c t - \omega_c\tau_k' - k\omega_c\tau + \varphi(t - k\tau - \tau_k')\right]. \end{aligned} \tag{4}$$

For $\tau_k' = -k\tau$, the total output power signal is given by

$$S_{\rm sum}(t) = nA(t)\cos[\omega_c t + \varphi(t)]. \tag{5}$$

The most straightforward way to obtain this time delay is by using broadband adjustable delay elements in the RF path. However, adjustable time delays at RF are challenging to integrate due to many nonideal effects, such as loss, noise, and nonlinearity. While an ideal delay can compensate the arrival time differences at all frequencies, in narrow-band applications it can be approximated via other means. For a narrow-band signal, $A(t)$ and $\varphi(t)$ change slowly relative to the carrier frequency, i.e., when τ is much less than the symbol period, we have

$$A(t) \approx A(t - k\tau) \tag{6}$$

$$\varphi(t) \approx \varphi(t - k\tau). \tag{7}$$

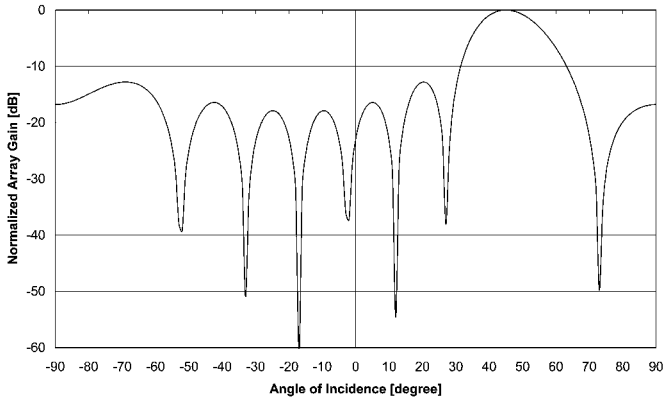

Fig. 2. Receive pattern of an eight-element array with omnidirectional antenna elements and $d = \lambda/2$.

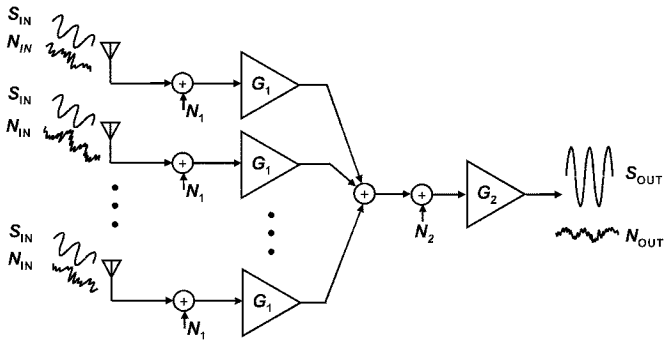

Fig. 3. Phased array improves SNR at the output due to coherent signal combining and uncorrelated nature of the noise.

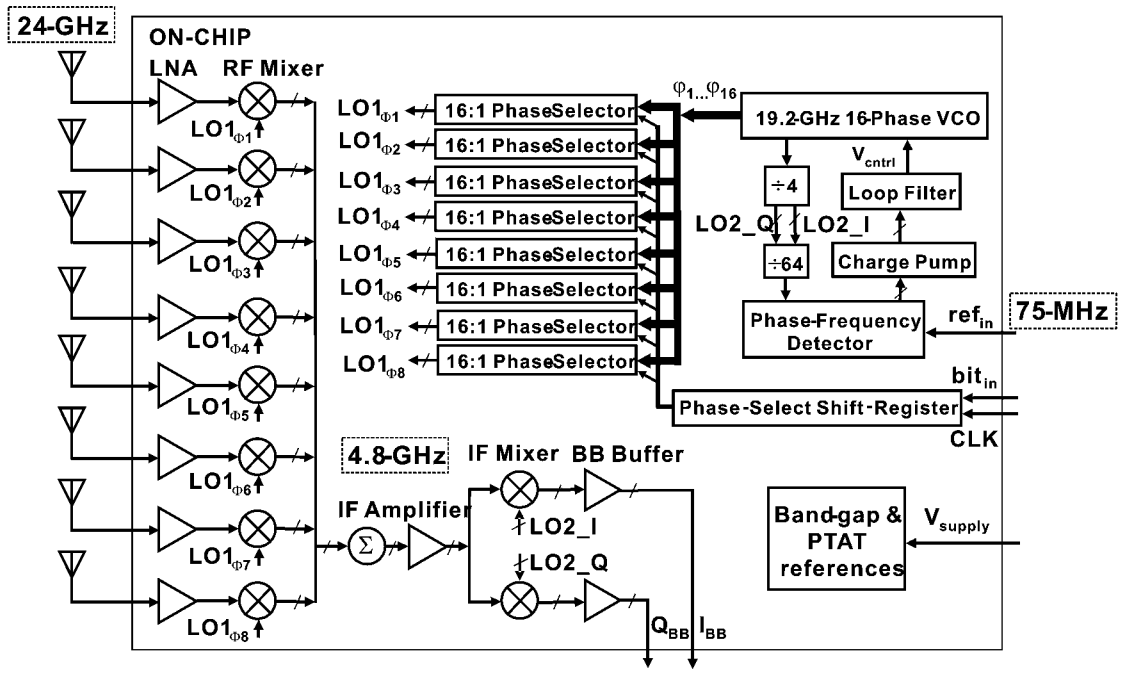

Fig. 4. The 24-GHz eight-element phased-array receiver architecture.

Therefore, we only need to compensate for the progressive phase difference $\omega_c\tau$ in (3). The time-delay element can be replaced by a phase shifter which provides a phase shift of θ_k to the kth element. To add the signal coherently, θ_n should be given by

$$\theta_k = k\omega_c\tau. \tag{8}$$

Unlike the wideband case, phase compensation for narrow-band signals can be made at various locations in the receiving chain, i.e., RF, LO, IF, analog baseband, or digital domain.

An additional advantage of a phased array is its ability to significantly attenuate the incident interference power from other directions. To illustrate this property, the receive pattern of an eight-element array is plotted in Fig. 2 for a 45° signal angle of incidence. The plot is for a narrow-band signal and an antenna spacing of $d = \lambda/2$ where λ is the wavelength. It can be seen that the signals incident from other angles are significantly suppressed. Additionally, in phased-array systems, the signal power in each path can also be weighted to adjust the null positions or to obtain a lower side-lobe level [3], [4].

B. Sensitivity Improvement

In a receiver, for a given modulation scheme, a maximum acceptable bit error rate (BER) translates to a minimum signal-to-noise ratio (SNR) at the baseband output of the receiver (input of the demodulator). For a given receiver sensitivity, the output SNR sets an upper limit on the noise figure of the receiver. The noise figure (NF) is defined as the ratio of the total output noise power to the output noise power caused only by the source [10]. In the case of a single-path receiver, we have

$$10\log(\mathrm{SNR_{out}}) = 10\log(\mathrm{SNR_{in}}) - \mathrm{NF} \tag{9}$$

which *cannot* be directly applied to multiport systems, such as phased arrays. Consider the n-path phased-array system, shown in Fig. 3. Since the input signals are added coherently, then

$$S_{\mathrm{out}} = n^2 G_1 G_2 S_{\mathrm{in}}. \tag{10}$$

The antenna's noise contribution is primarily determined by the temperature of the object(s) at which it is pointed. When antenna noise sources are uncorrelated, such as in indoor environment, the output total noise power is given by

$$N_{\mathrm{out}} = n(N_{\mathrm{in}} + N_1)G_1G_2 + N_2G_2. \tag{11}$$

Thus, compared to the output SNR of a single-path receiver, the output SNR of the array is improved by a factor between n and n^2, depending on the noise and gain contribution of different stages. The array noise factor can be expressed as

$$F = \frac{n(N_{\mathrm{in}} + N_1)G_1G_2 + N_2G_2}{nN_{\mathrm{in}}G_1G_2} \tag{12}$$

$$= n\frac{\mathrm{SNR_{in}}}{\mathrm{SNR_{out}}} \tag{13}$$

which shows that the SNR at the phased-array output can be even smaller than SNR at the input if $n > F$. For a given NF, an n-array receiver improves the sensitivity by $10\log(n)$ in decibels compared to a single-path receiver. For instance, an eight-element phased array can improves receiver sensitivity by 9 dB.

III. System Architecture

Fig. 4 shows the block diagram of the 24-GHz, eight-element phased-array receiver [11]. The receiver uses two-step down conversion with an IF of 4.8 GHz, allowing both LO frequencies to be generated using a single synthesizer loop and a divide-by-four. LO phase shifting is adopted in this study because the receiver is less sensitive to the amplitude variations

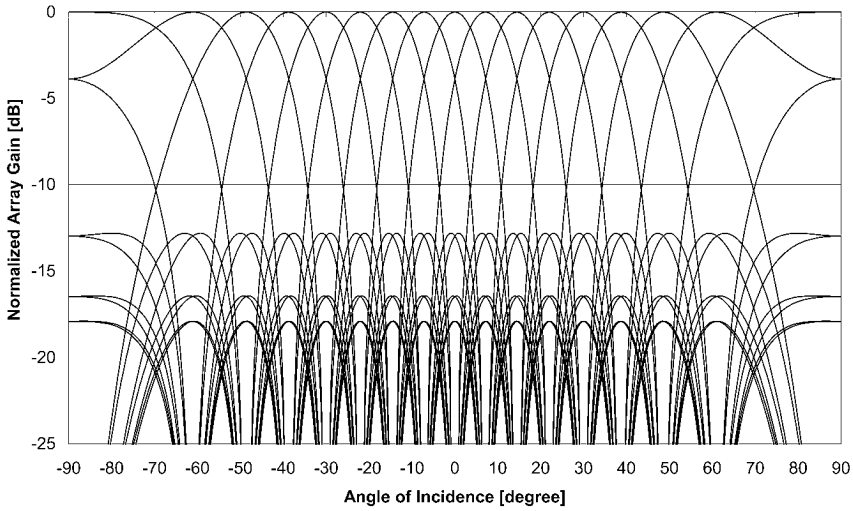

Fig. 5. Array patterns of 16 different LO phase setttings.

at the LO ports of the mixers. A single oscillator core generates 16 discrete phases providing 4 bits (22.5°) of raw phase resolution. The simulated 16 corresponding array patterns are shown in Fig. 5, for omnidirectional antenna elements with a spacing of $\lambda/2$. Fig. 5 illustrates that the system is capable of steering the beam from $-90°$ to $+90°$ and steering step size of 7.2° at the normal direction. A set of eight phase selectors, i.e., analog phase multiplexer, apply the appropriate phase of the LO to the corresponding RF mixer for each element independently. The operating state of the chip, including phase-selection information (beam-steering angle), is serially loaded into an on-chip shift-register using a standard serial interface. The image at 14.4 GHz is attenuated by the front-end's narrow-band transfer function, i.e., antenna and low-noise amplifier (LNA).

Each of the eight RF front-ends consists of two inductively degenerated common-emitter LNA stages in series followed by a double-balanced Gilbert-type mixer. The input of the first LNA is matched to 50 Ω and the subsequent blocks of the front-end are power matched for maximum power transfer. The outputs of all eight mixers are combined in current domain and terminated to a tuned load at the IF. The combined signal is further amplified by an IF amplifier and downconverted to baseband by a pair of double-balanced Gilbert-type mixers, driven by I and Q signals generated by the divide-by-4 block. Two baseband differential buffers drive the I and Q outputs. On-chip PTAT and bandgap references generate the bias currents and voltages, respectively.

IV. Circuits Implementation

A. Low-Noise Amplifier

The LNA is the most critical block in the receive chain in terms of sensitivity. It needs to provide sufficient gain to suppress the noise of the subsequent mixer with a low noise factor by itself and a well-defined real input impedance, which is usually 50 Ω. The LNA used in phased-array systems requires a particularly low-power design since multiple identical LNAs are operating concurrently in the system.

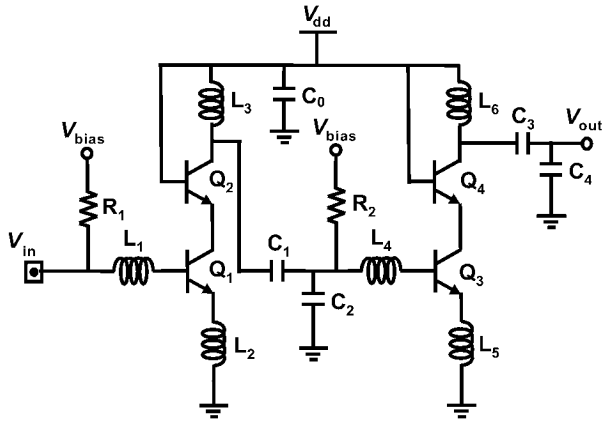

Fig. 6. Two-stage 24-GHz LNA.

The dramatic increase in the speed of bipolar and CMOS transistors in the last decade and novel design techniques have extended the operation range of silicon-based integrated LNA from low gigahertz to much higher frequency bands [12]–[15]. The choice of topologies depends on the ratio of the operation frequency ω_o to the transistor cut-off frequency ω_t [13]. The inductively degenerated common-emitter LNA can provide a high gain and low noise simultaneously for a small ω_o/ω_t. When ω_o becomes comparable to ω_t, the common-gate (CG) LNA exhibits competitive performance, particularly with a feedthrough resistor [13]. The process used in this work provides SiGe HBT with a cut-off frequency of 120 GHz, corresponding to a small ω_o/ω_t of 0.2 only. Therefore, inductively degenerated common-emitter topology is adopted as shown in Fig. 6.

The input transistor size and dc current are chosen to obtain power and noise matching simultaneously by using the steps described in [16]. First, the current density associated with the minimum NF is found by simulation. Then the input transistor is scaled until the optimum input impedance for low noise has a 50-Ω real part. The optimization results in a dc current of 4 mA and an emitter degeneration inductance of 0.2 nH. The cascode transistor Q_2 is used to improve reverse isolation.

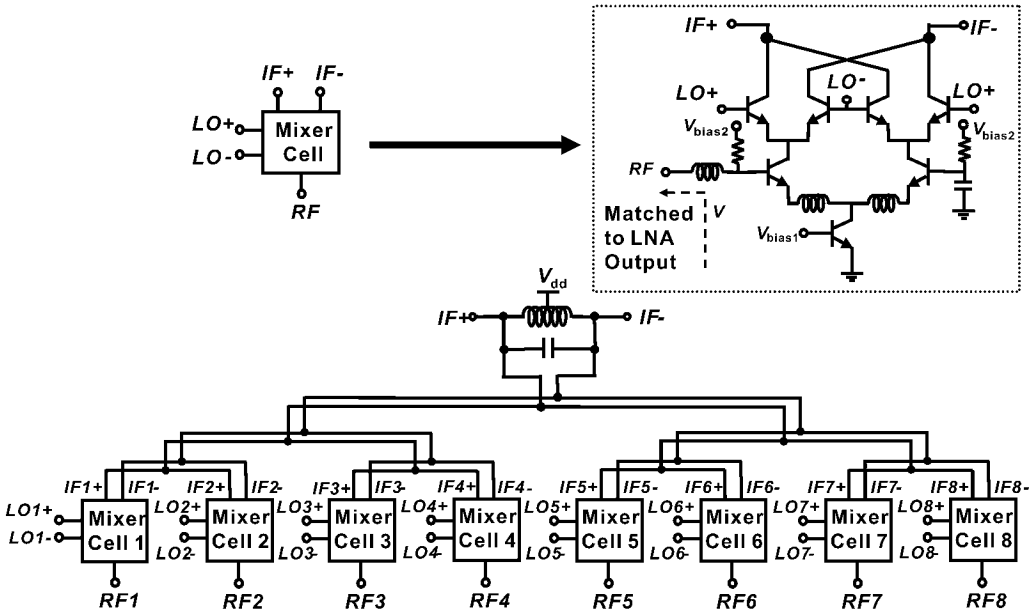

Fig. 7. RF mixers and IF combining network.

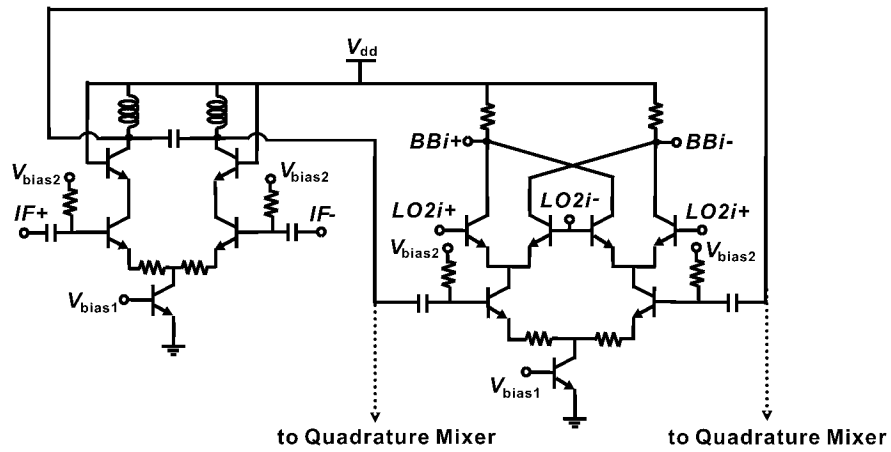

Fig. 8. IF amplifier and mixer.

At 24 GHz, the available gain of a single stage is limited by the small load inductance due to the large collector capacitance of Q_2 and the load capacitance. Simulation results show that the power gain achievable by one stage is not sufficient to suppress the noise of the subsequent stages, so an identical second stage is added.

At 24 GHz, the interactions between various blocks can make them very sensitive to variations in other adjacent blocks. To minimize this sensitivity, we have impedance-matched the input and output of individual building blocks to 50 Ω. This way the performance of the adjacent blocks will not be affected while they can be designed and optimized independently.

A capacitive divider formed by C_1 and C_2 transforms the output impedance of the first stage to 50 Ω, which is also the optimum impedance for the second stage in terms of power and noise. C_1 and C_2 are chosen to be 100 and 180 fF, respectively, and L_4 has an inductance of 0.2 nH, occupying 50 μm × 50 μm silicon area. The matching network loss at 24 GHz is simulated to be lower than 0.25 dB.

At 24 GHz, the bond-wire inductance has a considerable effect on the input reflection coefficient of the LNA. The LNA is designed to be well matched to 50 Ω (S_{11} less than −10 dB) on chip and tolerant to bond-wire inductance up to 0.3 nH. The V_{dd} and ground lines of the LNA are bypassed on chip with a MIM capacitor C_0 resonating at 24 GHz.

All of the inductors used in this LNA are between 0.2–0.5 nH. To save silicon area, spiral inductors are used, although slab inductors can provide higher quality factors. All of the spirals and interconnections are modeled by electromagnetic simulations using IE3D [17].

B. Mixer and IF Combining Network

Gilbert-type double-balanced multipliers are used to down-convert the single-ended 24-GHz RF signal to a differential signal at 4.8 GHz IF, as shown in Fig. 7. The input of the mixer is impedance matched to the LNA output through an impedance-transforming network. Inductive emitter degeneration is used to improve mixer linearity. A dc bias current of

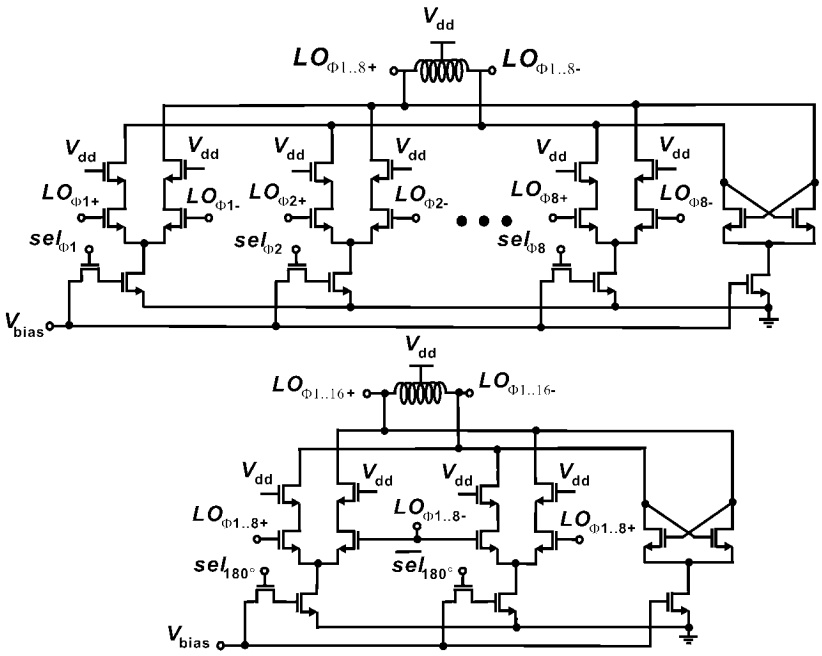

Fig. 9. Schematics of phase selector.

1.25 mA is chosen for each mixing cell which is a reasonable tradeoff between power dissipation, linearity, and noise figure. Each mixing cell has a conversion transconductance of 6.5 mA/V. The downconverted IF signal is subsequently combined in the current domain through a symmetric binary tree and terminated to a tuned load at 4.8 GHz.

C. IF Amplifier and Mixers

The IF amplifier is the first block after signal combining. It can be seen from (12) that the noise contribution of such blocks in overall noise figure is not only suppressed by the single-path gain of the front-end, but also by an array gain of n. At this point, the interference arriving at the input of the IF amplifier is already attenuated by the spatial selectivity of the array pattern. Therefore, both noise and linearity requirements of the IF amplifier and subsequent blocks are relaxed as a direct advantage of the phased array. Fig. 8 shows the schematics of the IF amplifier and I and Q mixers. The IF amplifier and mixer consume 1.6 and 2.3 mA of dc current, respectively.

D. LO Path Circuitry

The 16-phase 19-GHz VCO is designed as a ring of eight differential CMOS amplifiers with tuned loads [18]. The center frequency of the VCO is locked by a third-order frequency synthesizer to a 75-MHz external reference. The 16 phases generated at a VCO core are distributed to local phase selectors of each of the eight paths through a symmetric binary tree structure [19], so that each path has independent access to all 16 phases of the LO. The LO phase selection for each path is done in two steps, as shown in Fig. 9. Initially, an array of eight differential pairs with switchable current sources and a shared tuned load selects one of the eight LO phase pairs. A dummy array with complementary switching signals maintains a constant load on the VCO buffers and prevents variations in phase while switching. Next, the polarity (the sign bit) of the LO is selected by a similar 2-to-1 phase selector providing all 16 LO phases. The second phase-selection stage also provides additional gain to compensate for the loss of the distribution network. Each 16:1 phase selector consumes 12 mA. The design of the multiple phase generation, distribution network, frequency synthesizer circuits, and their effects on array performance are discussed in great detail in [20].

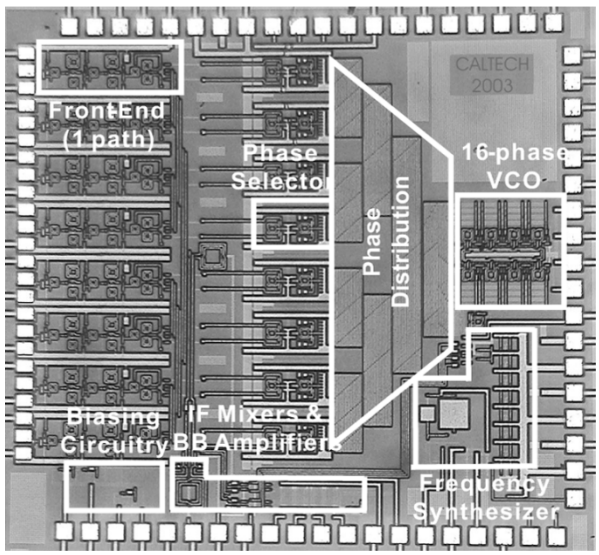

Fig. 10. Die microphotograph.

V. Experimental Results

The phased-array receiver is implemented in IBM 7HP SiGe BiCMOS technology with a bipolar f_T of 120 GHz and 0.18-μm CMOS transistors [21]. It offers five metal layers with a 4-μm-thick top analog metal used for on-chip spiral inductors as well as transmission lines routing the high-frequency signals. The die microphotograph of the phased-array receiver is shown in Fig. 10. The size of the chip is 3.3×3.5 mm^2.

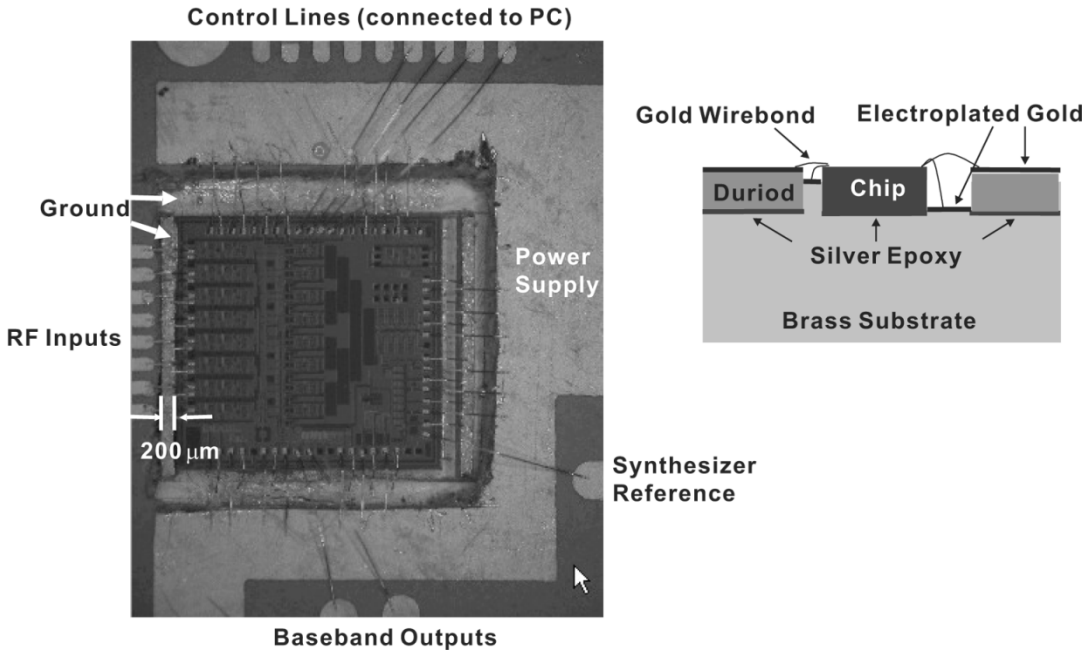

Fig. 11. Test package.

The die and test board are mounted on a brass platform using silver epoxy, as shown in Fig. 11. The thickness of the employed Duroid board is chosen to be 0.25 mm, which is approximately the same height as the chip. This minimizes signal bond-wire length and curvature. A 3.5-mm-long brass step with width and height of 200 μm is built along the RF side of the chip. The ground pads for the RF circuitry are wire-bonded to the top surface of this step to minimize the ground bond-wire length. The inputs of every path are symmetrically wire-bonded to 50-Ω transmission lines on board.

The free-running VCO achieves a phase noise of -103 dBc/Hz at 1-MHz offset. The frequency synthesizer is locked from 18.7 to 20.8 GHz with a settling time of less than 50 μs. Fig. 12 shows the locked spectrum of the frequency synthesizer.

The input reflection coefficients S_{11} at 24-GHz RF ports are characterized both on chip and at the SMA connectors of the RF inputs on board. The receiver demonstrates good input matching properties at the frequency range of interest in both cases, as shown in Fig. 13.

Fig. 14(a) depicts the gain of a single path as a function of the input frequency, showing a 43-dB peak gain at 23 GHz and 35-dB on-chip image rejection. The image signals will be further attenuated by narrow-band antennas. A 3-dB gain variation is observed among all paths. The receiver noise figure as a function of input frequency is shown in Fig. 14(b). A double-sideband noise figure of 7.4 dB is measured over the signal bandwidth of 250 MHz. Fig. 14(c) and (d) shows the measured nonlinearity of a single path. The input-referred 1-dB compression point is observed at -27 dBm, and the input-referred intercept point of the third-order distortion is -11.5 dBm.

Fig. 15 shows the on-chip isolation between different paths. The signal is fed to the fifth path only. The phase selector of each path is turned on alternatively to measure the output power caused by coupling. When all phase selectors are off, the system has a -27-dB signal leakage (normalized to single-path gain).

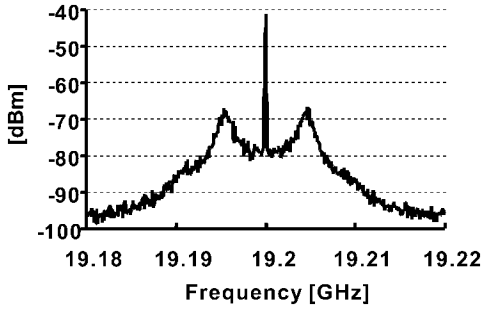

Fig. 12. Locked spectrum of the frequency synthesizer.

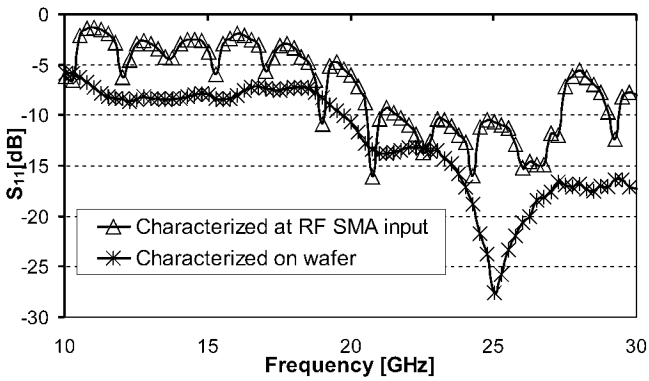

Fig. 13. Input reflection coefficients.

The coupling is lower than -20 dB in all paths. The strongest coupling is seen between adjacent paths, e.g., the fourth and fifth paths, as expected. However, when the phase selector at the fourth path is turned off and the one at the sixth path is turned on, a significantly lower output power is observed, which may be due to the coexisting coupling and leakage canceling each other. The coupling between nonadjacent paths is close to or lower than the leakage level.

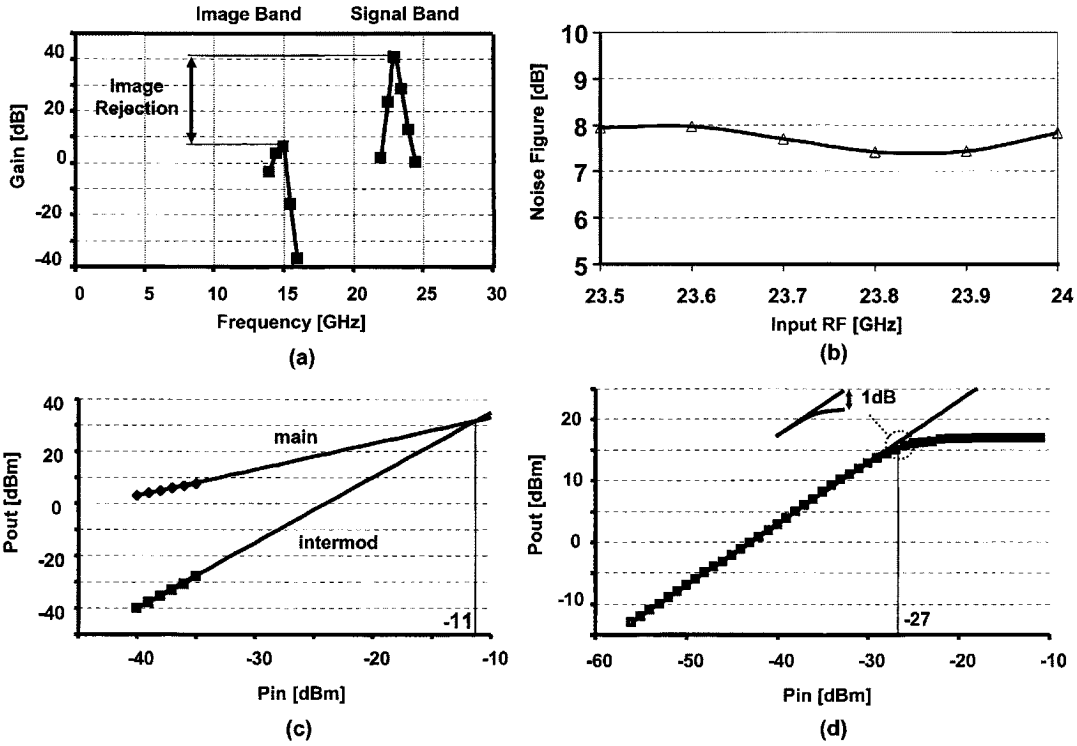

Fig. 14. Signal path performance. (a) Gain versus frequency. (b) Noise figure. (c) Two-tone test. (d) The 1-dB compression point.

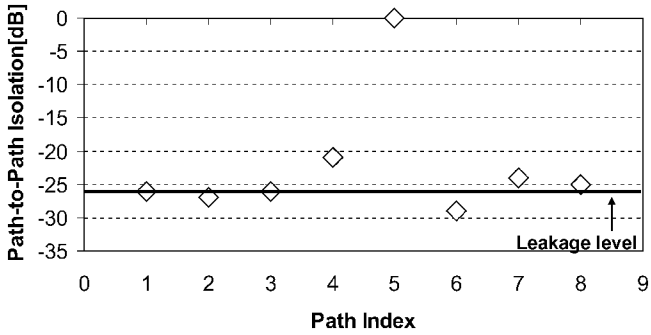

Fig. 15. On-chip path-to-path isolation.

The array performance is assessed using the setup shown in Fig. 16. An artificial wave front is generated by feeding the RF inputs to each receiver path via power splitters and adjustable phase shifters. This way, the array performance is measured independently of the antenna properties. Figs. 17 and 18 show the measured array patterns at different LO phase settings for two- and four-path operations, respectively. Figs. 17 and 18 clearly demonstrate the spatial selectivity of the phased-array receiver and its steering of the beam over the entire 180° range by LO phase programming. The measured performance is summarized in Table I.

TABLE I
PERFORMANCE SUMMARY

Signal Path Performance (per path)	
Peak Gain	43dB
Noise-Figure	7.4dB
Input-Referred 1dB Compression Point	-27dBm
Input-Referred 3rd-Order Intercept Point	-11.5dBm (2 tones 5MHz apart)
On-chip Image Rejection	35dB
S11	< -10dB
LO Path Performance	
Synthesizer locking range	2GHz
Synthesizer bandwidth	7MHz
Synthesizer settling time	< 50μs
VCO phase noise	-103dBc/Hz @ 1MHz offset
Complete Receiver Performance (8 paths)	
Total Array Gain	61dB
SNR Improvement	9dB
Phase-shifting Resolution	11.25°
Beam-forming Peak-to-Null Ratio	20dB (measured for 4 paths)
Power Dissipation @ 2.5V	364mA 287mA (w/o biasing and baseband buffers)
Technology	SiGe, 120GHz HBT 0.18μm CMOS
Die Area	3.5mm x 3.3mm

VI. CONCLUSION

A silicon-based fully integrated 24-GHz eight-element phased-array receiver is demonstrated for the first time. The phased array realizes phase shifting with 22.5° resolution at the LO port of the first down-conversion mixer. Each signal path achieves a gain of 43 dB, a noise figure of 7.4 dB, and an IIP3 of −11 dBm. The eight-element array improves SNR at the baseband output by 9 dB, demonstrating an array gain of 61 dB and a peak-to-null ratio of 20 dB.

ACKNOWLEDGMENT

The authors would like to acknowledge IBM Corporation for chip fabrication. They would also like to thank R. Aparicio, A. Natarajan, A. Komijani, D. Lu, M. Morgan, and Prof. D. Rutledge for valuable technical discussions, N. Wadefalk and A. Shen for their assistance preparing the printed

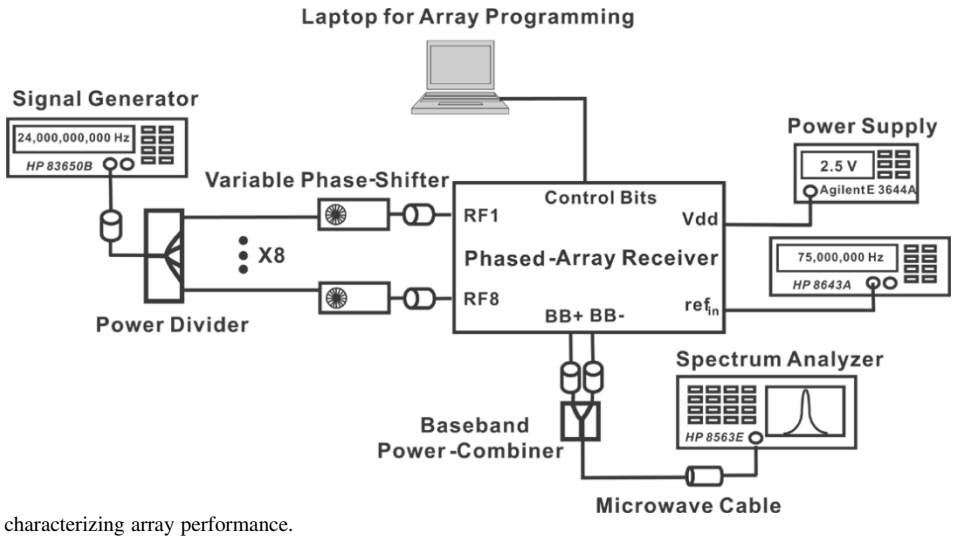

Fig. 16. Test setup for characterizing array performance.

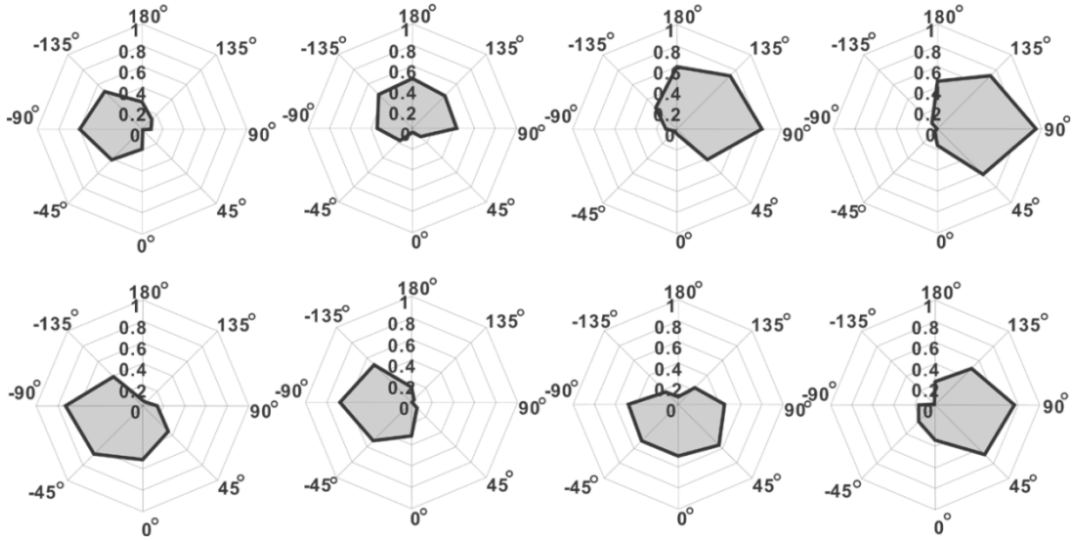

Fig. 17. Normalized two-path array gain as a function of input phase difference at eight different LO settings.

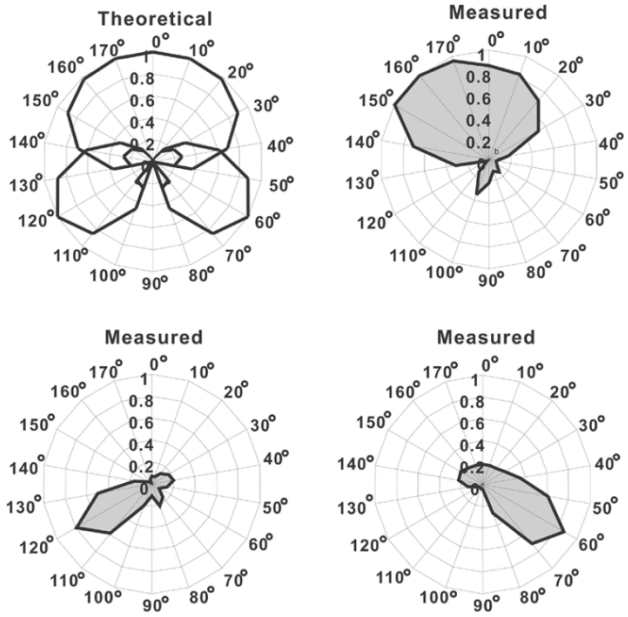

Fig. 18. Normalized four-path array gain as a function of incident angle at three different LO settings compared to theoretical results.

circuit board and microwave package, and R. Chunara for providing the original version of the software for programming the phased-array receiver.

REFERENCES

[1] V. Aulock and W. H., "Properties of phased arrays," *Proc. IRE*, vol. 48, pp. 1715–1728, Oct. 1960.
[2] *Significant Phased Array Papers*, R. C. Hansen, Ed., Artech House, Norwood, MA, 1973.
[3] R. S. Elliott, *Antenna Theory and Design*. Englewood Cliffs, NJ: Prentice-Hall, 1981.
[4] *The RF and Microwave Handbook, Session 6.9*, M. Golio, Ed., CRC Press, Boca Raton, FL, 2000.
[5] D. Parker and D. C. Zimmermann, "Phased arrays—Part I: Theory and architectures," *IEEE Trans. Microwave Theory Tech*, vol. 50, pp. 678–687, Mar. 2002.
[6] ——, *Phased-Arrays—Part II: Implementations, Applications, and Future Trends*, vol. 50, no. 3, pp. 688–698, Mar. 2002.
[7] D. Lu *et al.*, "Investigation of indoor radio channel from 2.4 GHz to 24 GHz," in *IEEE AP-S Int. Symp. Digs*, June 2003, pp. 134–137.
[8] Federal Communications Commission, FCC 02-04, 15.515.15.521.
[9] G. E. Moore, "Cramming more components onto integrated circuits," *Electron.*, vol. 38, no. 8, pp. 114–117, Apr. 1965.
[10] "IRE standards on electron tubes: Definition of terms," *Proc. IRE*, vol. 45, pp. 983–1010, July 1957.

[11] H. Hashemi, X. Guan, and A. Hajimiri, "A fully integrated 24 GHz 8-path phased-array receiver in silicon," in *ISSCC Dig. Tech. Papers*, vol. 47, Feb. 2004, pp. 390–391.
[12] G. Schuppener, T. Harada, and Y. Li, "A 23-GHz low-noise amplifer in SiGe heterojunction bipolar technology," in *IEEE Radio Frequency Integrated Circuits Symp. Dig. Papers*, May 2001, pp. 177–180.
[13] X. Guan and A. Hajimiri, "A 24-GHz CMOS front-end," *IEEE J. Solid-State Circuits*, vol. 39, pp. 368–373, Feb. 2003.
[14] F. Ellinger, "26–42 GHz SOI CMOS low noise amplifer," *IEEE J. Solid-State Circuits*, vol. 39, pp. 522–528, Mar. 2004.
[15] S. Reynolds, B. Floyd, U. Pfeiffer, and T. Zwick, "60 GHz tranceiver circuits in SiGe bipolar technology," in *ISSCC Dig. Tech. Papers*, vol. 47, Feb. 2004, pp. 442–443.
[16] S. P. Voinigescu, "A scalable high frequency noise model for bipolar transistors with application to optimal transistor sizing for low-noise amplifier design," in *IEEE Proc. Bipolar Circuits and Technology Meeting*, Sep. 1996, pp. 61–64.
[17] *IE3D Electromagnetic Simulation User Manual, Release 8*, 2001.
[18] J. Savoj and B. Razavi, "A 10-Gb/s CMOS clock and data recovery circuit with a half-rate binary phase-frequency detector," *IEEE J. Solid-State Circuits*, vol. 38, pp. 13–21, Jan. 2003.
[19] X. Guan, H. Hashemi, A. Komijani, and A. Hajimiri, "Multiple phase generation and distribution for a fully-integrated 24-GHz phased-array receiver in silicon," in *IEEE Radio Frequency Integrated Circuits Symp. Dig. Papers*, June 2004.
[20] H. Hashemi, X. Guan, A. Komijani, and A. Hajimiri, "A 24-GHz SiGe phased-array receiver: LO phase shifting approach," *IEEE Trans. Microwave Theory Tech.*, Jan. 2005.
[21] A. Joseph *et al.*, "A 0.18 μm BiCMOS technology featuring 120/100 GHz (ft/fmax) HBT and ASIC-compatible CMOS using copper interconnect," in *Proc. BCTM*, 2001, pp. 143–146.

Xiang Guan (S'98) received the B.S. degree in electrical engineering from Tsinghua University, Beijing, China, in 1996 and the M.Eng. degree in electrical engineering from the National University of Singapore in 2000. He is currently working toward the Ph.D. degree at the California Institute of Technology, Pasadena.

From 1996 to 1997, he was a Research Assistant with the Integrated Circuits Group, Instituto Superior Tecnico, Lisbon, Portugal, involved in the development of a data-acquisition chip for electrocardiogram remote monitoring devices. During the summer of 2003, he was a Co-op Researcher with the IBM Thomas J. Watson Research Center, Yorktown Heights, NY.

Mr. Guan was the recipient of the Analog Devices Outstanding Student Designer Award in 2002.

Hossein Hashemi (M'99) received the B.S. and M.S. degrees in electronics engineering from Sharif University of Technology, Tehran, Iran, in 1997 and 1999, respectively, and the M.S. and Ph.D. degrees in electrical engineering from the California Institute of Technology, Pasadena, in 2001 and 2003, respectively.

He joined the Department of Electrical Engineering—Electrophysics, University of Southern California, Los Angeles, in 2003 as an Assistant Professor, where the core of his research constitutes the study of integrated communication circuits and systems.

Dr. Hashemi was the recipient of the Outstanding Accomplishment Award from the von Brimer foundation in 2000, the Outstanding Student Designer Award from Analog Devices in 2001, and an Intel Fellowship in 2002. He is an Associate Editor of the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS, PART II.

Ali Hajimiri (S'95–M'99) received the B.S. degree in electronics engineering from the Sharif University of Technology, Tehran, Iran, and the M.S. and Ph.D. degrees in electrical engineering from Stanford University, Stanford, CA, in 1996 and 1998, respectively.

He was a Design Engineer with Philips Semiconductors, where he worked on a BiCMOS chipset for GSM and cellular units from 1993 to 1994. In 1995, he was with Sun Microsystems, where he worked on the UltraSPARC microprocessor's cache RAM design methodology. During the summer of 1997, he was with Lucent Technologies, Laboratories, Murray Hill, NJ, where he investigated low-phase-noise integrated oscillators. In 1998, he joined the Faculty of the California Institute of Technology, Pasadena, where he is an Associate Professor of Electrical Engineering and the director of Microelectronics and Noise Laboratories. His research interests are high-speed and RF integrated circuits. He is a coauthor of *The Design of Low Noise Oscillators* (Boston, MA: Kluwer, 1999) and holds several U.S. and European patents. He is a cofounder of Axiom Microdevices Inc.

Dr. Hajimiri is on the top 100 innovators (TR100) list. He was the Gold medal winner of the National Physics Competition and the Bronze Medal winner of the 21st International Physics Olympiad, Groningen, Netherlands. He was a corecipient of the International Solid-State Circuits Conference (ISSCC) 1998 Jack Kilby Outstanding Paper Award and a three times winner of the IBM faculty partnership award as well as National Science Foundation CAREER award. He is an Associate Editor of the IEEE JOURNAL OF SOLID-STATE CIRCUITS (JSSC) and a member of the Technical Program Committee of the International Solid-State Circuits Conference (ISSCC). He has also served as an Associate Editor of the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS (TCAS) PART II, a member of the Technical Program Committees of the International Conference on Computer Aided Design (ICCAD), Guest Editor of the IEEE TRANSACTIONS ON MICROWAVE THEORY AND TECHNIQUES, and a member of the Guest Editorial Board of the *Transactions of Institute of Electronics, Information and Communication Engineers of Japan* (IEICE).