A Fully Integrated 24-GHz Phased-Array Transmitter in CMOS

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***Abstract*—This paper presents the first fully integrated 24-GHz phased-array transmitter designed using 0.18-μm CMOS transistors. The four-element array includes four on-chip CMOS power amplifiers, with outputs matched to 50 Ω, that are each capable of generating up to 14.5 dBm of output power at 24 GHz. The heterodyne transmitter has a two-step quadrature up-conversion architecture with local oscillator (LO) frequencies of 4.8 and 19.2 GHz, which are generated by an on-chip frequency synthesizer. Four-bit LO path phase shifting is implemented in each element at 19.2 GHz, and the transmitter achieves a peak-to-null ratio of 23 dB with raw beam-steering resolution of 7° for radiation normal to the array. The transmitter can support data rates of 500 Mb/s on each channel (with BPSK modulation) and occupies 6.8 mm $\times$ 2.1 mm of die area.**

***Index Terms*—CMOS, integrated circuits, multiphase oscillator, phased arrays, power amplifiers, radar, transmitter, wireless communications.**

I. Introduction

HIGH-FREQUENCY phased-array systems have been ubiquitous in the fields of radar and radio astronomy [1]–[3]. However, these systems rely on specialized discrete components and careful assembly of modules that increase cost and complexity of manufacturing. Integration on silicon makes it possible to realize complex phased-array systems, with on-chip mixed-signal and digital signal processing, at lower cost and with higher reliability. Furthermore, digital tuning and calibration in integrated systems can be used to improve the performance of critical analog/RF parts [4], [5]. Importantly, the very low incremental cost of signal processing elements, i.e., transistors, and the benefits of integration such as short and robust interconnects and good component matching enable the realization of novel phased-array architectures that are designed specifically for existing and emerging applications [6], [7]. For instance, phased-array-based transmitters and receivers, operating at high frequencies where large bandwidths are available, are well suited for high data rate directional point-to-point wireless communication networks and for short-range radar applications such as collision avoidance and assisted parking in automobiles.

The physical size of such integrated phased-array systems is restricted by the size of the antennas and the spacing between them. In a system employing resonance-based antennas, the antenna size and spacing decrease with an increase in frequency. Thus, the large bandwidths and smaller physical system size render high frequencies attractive for integrated phased-array implementation.

A particularly interesting frequency for integrated phased-array system implementation is 24 GHz. The Industrial, Scientific, and Medical (ISM) band at 24 GHz has been opened up for wireless point-to-point communications by the Federal Communications Commission (FCC) [8]. In addition, 7 GHz of spectrum from 22 to 29 GHz has been allocated for ultra-wideband vehicular radar applications, making the 24-GHz band appealing from both wireless communication and car radar perspectives.

CMOS process technologies are the most attractive among silicon-based technologies for integrated systems due to the benefits of scaling and the possibility of integrating the digital backbone with the RF front-end. However, the low active gain of MOS transistors and the lossy passives at high frequencies have prevented any significant movement toward integrating entire high-frequency phased-array systems on CMOS technologies. The fully integrated four-element 24-GHz phased-array transmitter, with on-chip power amplifiers, reported in this paper is not only the first fully integrated phased-array transmitter but also the first system to demonstrate such levels of integration at 24 GHz using 0.18-μm CMOS transistors. The transmitter reported in this paper and the eight-element phased-array SiGe receiver presented in [6] demonstrate the feasibility of 24-GHz phased-array systems in silicon-based processes.

In the following sections, the system level and circuit level aspects in the design of the transmitter will be discussed in depth. Section II provides a brief introduction to the properties and advantages of phased-array transmitters while Section III discusses the tradeoffs of high-frequency phased-array wireless communication. Different phased-array architectures, particularly the local oscillator (LO) phase-shifting architecture adopted in this paper, are examined in Section IV. The architecture of the transmitter and the design of key circuit building blocks are described in Section V, and the measurement results are presented in Section VI.

II. Phased-Array Principles

In a multiple-element transmitter, a beam is formed in a desired direction by varying the relative delay in each element to compensate for the difference in propagation delays for signals from different elements. Electronic variation of the delay enables beam steering without actual mechanical reorientation of the antennas. Fig. 1 shows a simplified n-element phased-array transmitter. When the input signal $s(t)$ is distributed to elements

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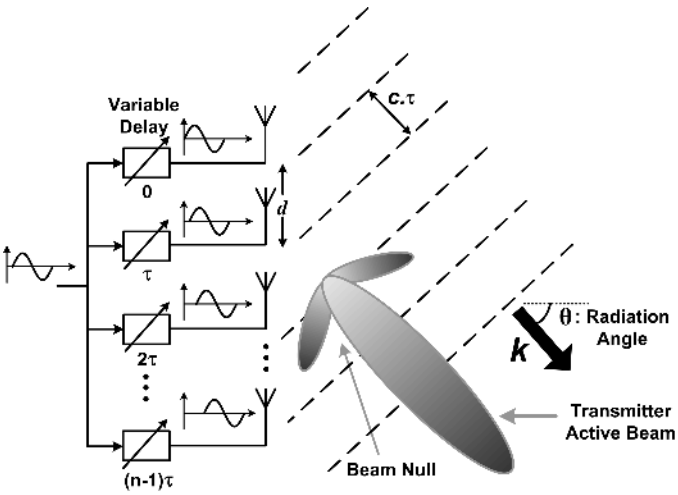


Fig. 1. n-element phased-array transmitter.

that delay the signal by multiples of τ, the combined signal in a direction θ is given by

$$S(t) = \sum_{k=0}^{n-1} s\left(t - k\tau - (n-1-k)\frac{d\sin\theta}{c}\right). \qquad (1)$$

Therefore, the signals from all elements add up coherently in the direction $\theta = \sin^{-1}(c\tau/d)$, where d is the spacing between antennas and c is the velocity of light. This coherent addition increases the power radiated in the desired direction while incoherent addition of the signal in other directions ensures lower interference power at receivers that are not targeted. It can be seen from (1) that in an n-element transmitter, if each element radiates P watts omnidirectionally, the effective isotropic radiated power (EIRP)[1] in the main beam direction is n^2P watts. For example, if each transmitter in a four-element array radiates 14 dBm, the EIRP in the beam direction is increased by 12 dB $(20\log_{10}4)$ to 26 dBm. This increase in signal power at the receiver is particularly useful at high frequencies, where the efficiency and output power of silicon-based power amplifiers are low, path loss is high, and the receiver sensitivity is low. From a system perspective, implementing a phased array at the receiver side as well improves receiver sensitivity, thereby increasing channel capacity. The directivity of the phased-array transmitter–receiver system permits higher frequency reuse due to better interference suppression and rejection, leading to increased network capacity.

III. High-Frequency Wireless Communication

The large bandwidths and smaller physical system size motivate a move to high frequencies for wireless communications. In this section, the tradeoffs of high-frequency wireless networks are discussed, with an emphasis on phased-array systems.

The beamforming and electronic beam-steering properties of phased arrays provide a solution to the demand for directional

[1]The EIRP in a particular direction is the power that an isotropic transmitter would have to radiate to cause the same field strength in that direction.

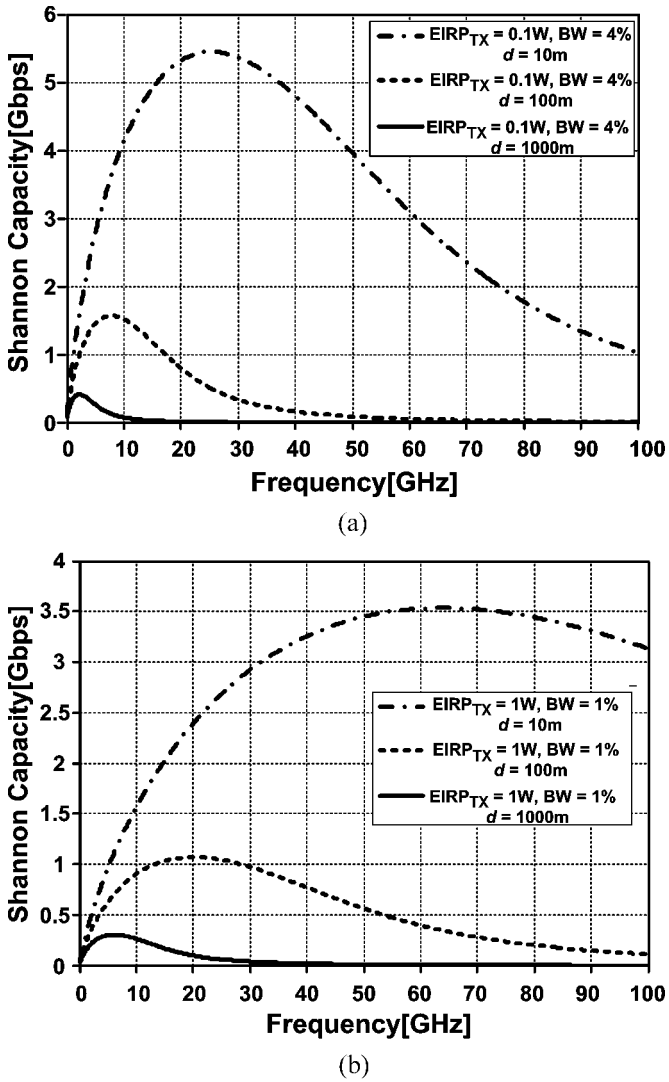


Fig. 2. Comparison of channel capacities for different system parameters demonstrates the tradeoffs of moving to high frequencies. (a) Channel capacity for EIRP $= 0.1$ W, BW $= 4\%$. (b) Channel capacity for EIRP $= 1$ W, BW $= 1\%$.

wireless links at high frequencies.[2] Resonance-based planar antennas such as dipoles or patch antennas are well suited for an integrated phased-array-based system with electronic beam steering. A typical patch antenna array at 24 GHz, for instance, has an antenna gain of 10 dB [9].[3] According to the antenna theorem, the aperture area of an antenna, for a given gain, decreases with an increase in frequency, reducing the power collected at the receiver at high frequencies [10]. The collected power cannot be increased by increasing the aperture area, as that increases antenna gain, making the antenna more directional and hence limiting the angles at which phased-array operation is possible. Thus, in a resonance-antenna-based system,

[2]The spatial specifications in the 24- to 24.25-GHz band call for a main lobe beamwidth not exceeding 3.5° in the azimuthal and the elevation planes [8].

[3]A four-element array, implemented with antennas that have 10-dB gain, will have an effective antenna gain of 22 dB. Therefore, in the four-element array, to achieve the maximum permitted EIRP of 29.7 dBm in the 24- to 24.25-GHz band [8], each transmitter has to generate 7.7 dBm. In the 22- to 29-GHz band, the low EIRP requirements (~ -2.5 dBm) make large bandwidth the primary focus of design.

the advantage of large bandwidths at high frequencies is offset to some extent by the lower received power and the higher receiver noise figure at high frequencies.

For a transmit EIRP of $P_{\rm TX}$, the signal power at the receiver $P_{\rm RX}$ is given by Friis' equation [11]

$$P_{\rm RX} = P_{\rm TX}\left(\frac{\lambda}{4\pi}\right)^2 \frac{G_{\rm TX}G_{\rm RX}}{d^l} \tag{2}$$

where $G_{\rm TX}$ and $G_{\rm RX}$ are the receiver and transmitter antenna gain, λ is the wavelength, d is the distance between transmitter and receiver, and l is the exponent that can be higher than the nominal value of 2 to account for excess path loss. In order to explore the tradeoffs of moving to high frequencies, the channel capacity C (in bit per second) given by Shannon's theorem [12]

$$C = {\rm BW}\log_2(1+{\rm SNR}) \tag{3}$$

is calculated for different carrier frequencies f_c while keeping the fractional bandwidth constant, accounting for larger bandwidths at higher frequencies. The noise figure of the receiver is assumed to increase linearly with frequency [13]. A noise figure of 3 dB is assumed at 6 GHz, resulting in a noise figure of 7 dB at 24 GHz.[4] The individual antennas are assumed to be isotropic and no excess path loss is considered (i.e., $l = 2$). Fig. 2(a) and (b) plots the channel capacity against carrier frequencies under the assumptions made above for two sets of EIRP and fractional bandwidth values. The fact that the curves are not monotonic and exhibit a peak demonstrates the tradeoff between larger bandwidths, lower collected power, and higher noise figure at high frequencies. The peak in the channel capacity curve moves to lower frequencies for higher transmitter–receiver separations and moves to higher frequencies with higher transmit EIRP or lower noise figure, both of which can be improved by implementing multiple-antenna systems such as phased arrays. Fig. 3 plots the channel capacity for different transmitter–receiver separations, assuming a bandwidth of 250 MHz, EIRP of 30 dBm, and receiver noise figure of 7 dB at 24 GHz. In a four-element phased-array receiver, the signal-to-noise ratio (SNR) at the output may be improved by up to 6 dB [6]. When this improvement in SNR is included in (2) and (3), it can be seen that high-speed (greater than 1 Gb/s) phased-array data links are possible up to a distance of 200 m at 24 GHz.

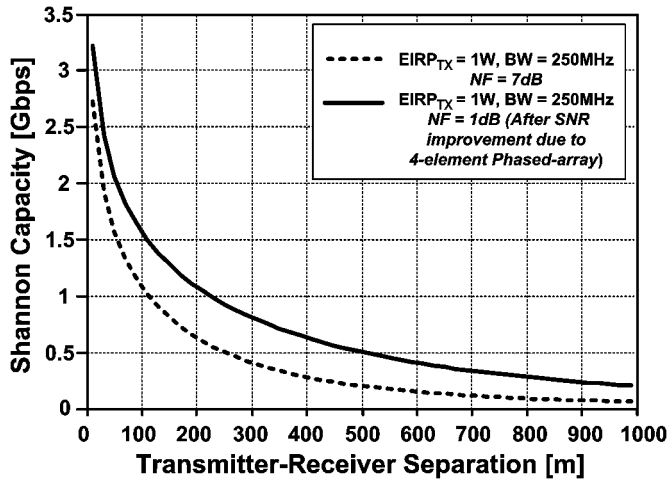


Fig. 3. Channel capacity for different transmitter–receiver separations at 24 GHz.

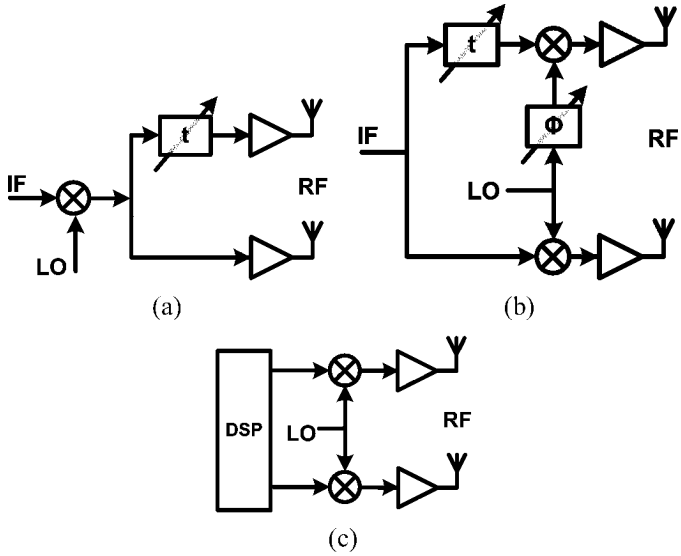


Fig. 4. Broadband array architectures. (a) Delay in RF path. (b) Delay in IF path and LO phase shift. (c) Digital delay at baseband.

IV. Phased-Array Architectures

A. Delay and Phase-Shifting Architectures

Ideally, to achieve broadband phased-array operation, a true-time delay is required in each element. In the architecture in Fig. 4(a), the required time delay is implemented in the RF path in each element. However, implementing a broadband low-loss true-time delay element at RF, which is capable of large variation, occupies a practical area, and scales well with an increase in number of elements, poses several problems. The true-time delay in the RF path can be replaced equivalently by a delay in the IF path and a phase shift in the LO path/IF path as shown in Fig. 4(b), or by implementing the delay in the digital domain as shown in Fig. 4(c). While an analog delay element at IF has the same problems as a delay at RF, practical considerations of mixed-signal circuits and digital signal processor (DSP) performance limit the digital array architecture [14].

If the bandwidth of interest is sufficiently narrow, the time delay (a linear phase shift in the frequency domain) can be approximated by a constant phase shift at the center frequency. The phase-shift architecture can be implemented as an approximation of the delay-based architecture in Fig. 4(a), which leads to a phase shift in the RF signal path [Fig. 5(a)], or as an approximation of the architecture in Fig. 4(b), which leads to a phase shift in the LO path or IF signal path [Fig. 5(b) and (c)].

Low-loss phase shifters in the RF path have attracted research interest [15], [16]. If the phase-shifter loss is not uniform for all phase shifts, variable gain amplifiers are required in each element to equalize the phase-shifter losses to avoid array pattern degradation.

Phase shifters in the LO path circumvent this problem as the circuits in the LO path such as the voltage-controlled oscillator

[4]Noise figure $F = 1 + (f/6e9)$.

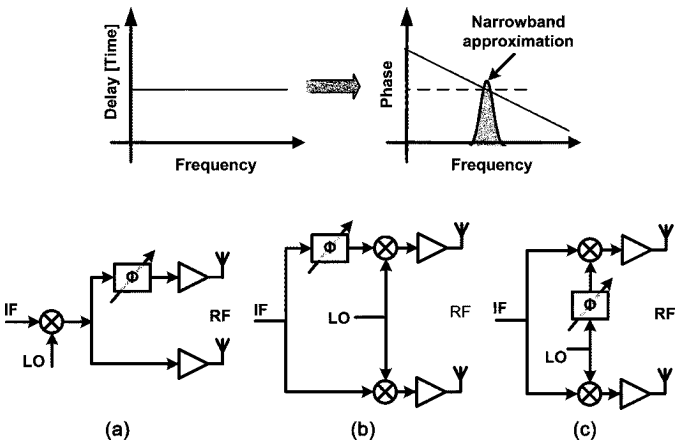


Fig. 5. Narrowband phased-array architectures. (a) RF phase shift. (b) IF phase shift. (c) LO phase shift.

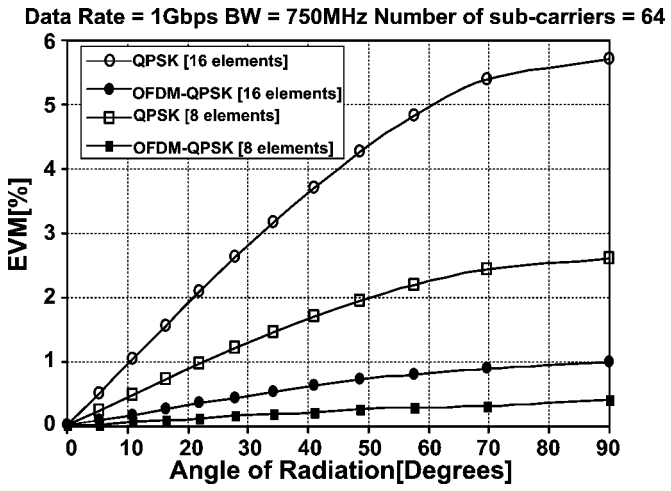


Fig. 6. EVM improvement provided by normalized OFDM-QPSK modulation over QPSK modulation for 8-element and 16-element transmitter.

(VCO) and the LO path amplifiers operate in saturation by design since the performance of the mixers in the up-conversion path is improved with larger LO voltage swings. Furthermore, with large LO signal swings at the LO ports of the mixers, the sensitivity of mixer gain to the LO signal amplitude is low. As a result, with phase shifters in the LO path, the variation in signal amplitude for different values of phase shift is minimal. Therefore, the LO path phase-shifting architecture has been chosen for the phased-array transmitter.

B. Effects of Narrowband Approximation

The narrowband LO phase-shift architecture [shown in Fig. 5(c)] leads to some signal distortion due to dispersion. The input signal that is distributed to each element in a phased-array transmitter can be represented as $s(t) = v(t)\cos[\omega_{\rm RF}t + \phi(t)]$, where $v(t)$ and $\phi(t)$ represent the baseband signal modulating the carrier. When phase shifts are implemented in each element to achieve a radiation angle of θ, for which the propagation delay between successive elements differs by τ, the combined signal power is

$$S(t) = \sum_{k=0}^{n-1} v(t - k\tau)\cos\left[\omega_{\rm RF}t + \phi(t - k\tau)\right]. \qquad (4)$$

Thus, none of the phase-shifting architectures ensure that the baseband modulating signals add up coherently resulting in a signal distortion that is manifested as a higher error vector magnitude (EVM). EVM increases with an increase in the number of elements and/or the bandwidth of the baseband signal, and can be a source of error on both the transmitter and receiver side leading to higher bit error rates [17]. As will be explained below, a method to mitigate the deterministic errors caused by the phase-shift approximation is to use a normalized orthogonal frequency division multiplexing (OFDM) modulation scheme for the baseband input that is distributed to all the elements in the transmitter.

For a QPSK signal at data rate R bits per second, the time period of each symbol $T_s = 1/2R$. Therefore, the complex digital baseband signal is $s_d(nT_s) = b_n$ where b_n is complex. In OFDM, the total bandwidth of the system is divided into N_c channels, with the N_c subcarriers orthogonal. The baseband digital data are divided into N_c parallel streams, each of which is used to modulate a subcarrier [18]. Thus, each OFDM symbol consists of N_c QPSK symbols, and for each frame (of duration N_cT_s), $s_d(nT_s) = \sum_{k=0}^{N_c-1} b_k e^{j2\pi(kn/N_c)}$

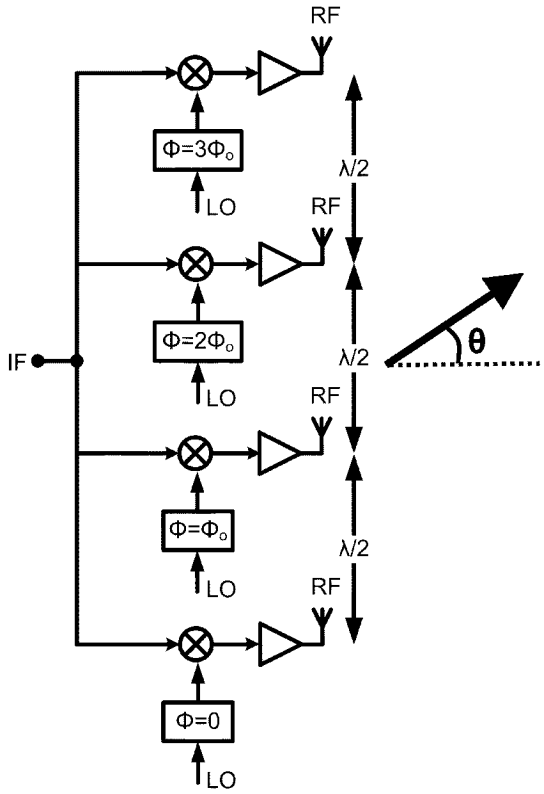
Since each of the channels in the OFDM scheme is narrowband, the error due to the time delay being replaced by a constant phase shift can be largely corrected by multiplying the input modulating each subcarrier by a complex normalizing factor α_k such that

$$s_d(nT_s) = \sum_{k=0}^{N_c-1} \alpha_k b_k e^{j2\pi\frac{kn}{N_c}}. \qquad (5)$$

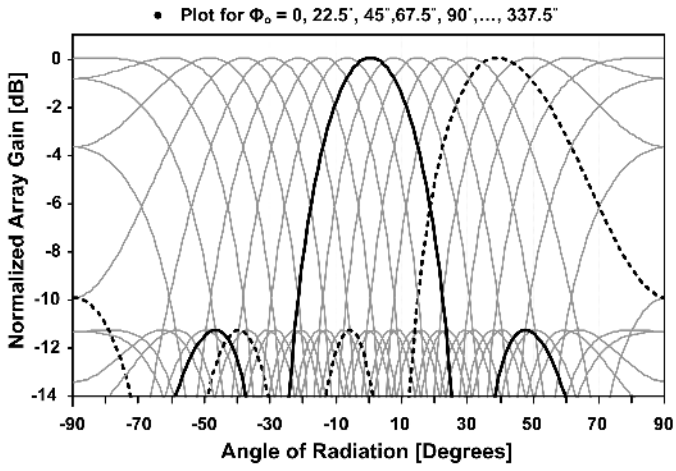
The memoryless predistortion coefficients α_k depend upon the direction of radiation that is known *a priori* in the transmitter. The same normalization scheme can also be implemented in a phased-array receiver to account for similar signal distortion due to dispersion. Fig. 6 compares the EVM for a raw QPSK modulation scheme and for a 64-subcarrier OFDM-QPSK modulation scheme with complex normalization in a 24-GHz phased-array transmitter with 8 and 16 elements. The signal has a data rate of 1 Gb/s and a bandwidth of 750 MHz. The maximum EVM, corresponding to a worst-case radiation angle of 90°, improves from 5.8% to 1% in the 16 element case, demonstrating the efficacy of the normalized OFDM scheme. Thus, careful choice of modulation schemes and simple equalization methods can render the implementation of actual analog or digital delay in each element unnecessary. Increasing the number of subcarriers decreases the EVM further and can compensate for increased distortion due to higher signal bandwidth and/or higher number of elements in the array.

C. Array Pattern Performance

The transmitter described in this paper is based on a phase-shifting architecture that was introduced in [14] in the context of a receiver. Fig. 7(a) shows a simplified four-element phased-array transmitter with LO path phase shifting. Relative phase



(a)



(b)

Fig. 7. Array gain for four-element LO path phase-shifting transmitter. (a) Four-element LO phase-shift phased-array transmitter. (b) Array gain for four-element phased-array transmitter.

shifts of ϕ, 2ϕ, and 3ϕ are implemented in the elements. The angle of radiation θ is given by

$$\theta = \sin^{-1}\left(\frac{\phi c}{\omega_{\mathrm{RF}} d}\right) \tag{6}$$

where c is the velocity of light and d is the spacing between the antennas. For $d = \lambda_{\mathrm{RF}}/2$

$$\theta = \sin^{-1}\left(\frac{\phi}{\pi}\right). \tag{7}$$

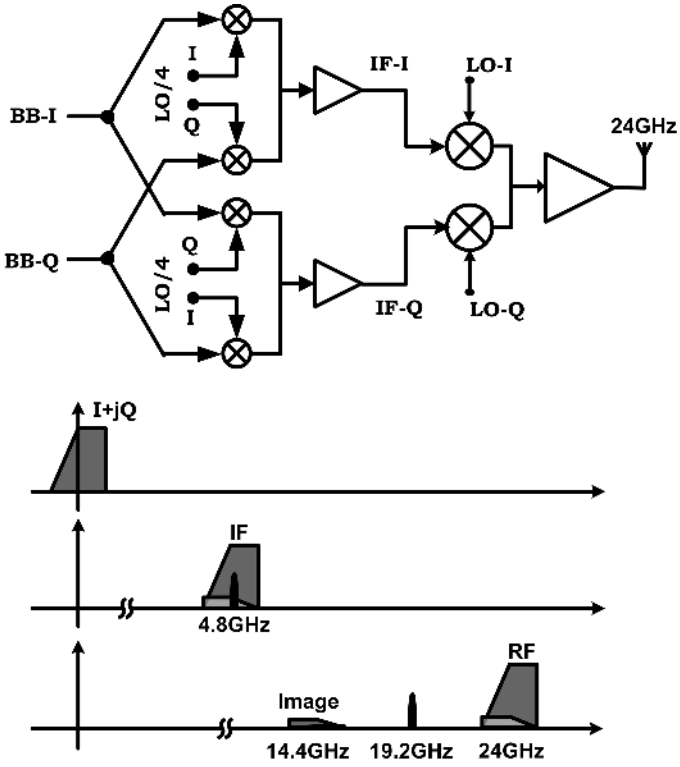


Fig. 8. Equivalent architecture of a single transmitter element and frequency plan.

Fig. 7(b) plots the array gain versus angle of radiation for 16 uniformly spaced values of ϕ with a step size of 22.5°. As can be seen from the figure, the phase-shift resolution is sufficient to radiate at all angles at close to peak array gain. The 3-dB beamwidth for radiation that is normal to the axis of the array is 26° and the beam-steering resolution is 7°. The beamwidth and the beam-steering resolution increase as the angle of radiation becomes more oblique. The array pattern is degraded by mismatches in the signal amplitude and LO phase shift across different elements. For example, in the case of a two-element transmitter, an amplitude mismatch of 3 dB translates to a peak-to-null ratio of 15.3 dB. The error in the beam direction, due to a given absolute error in LO phase shifting, depends upon the actual beam direction and can be derived from (7).

V. Transmitter Architecture

In this section, the architecture of the phased-array transmitter is discussed in depth. This is followed by a detailed description of the circuits in the signal path and the LO path.

The four-element fully integrated transmitter has on-chip power amplifiers [19] as well as an integrated frequency synthesizer. Due to concerns related to frequency pulling, direct up-conversion was considered to be unsuitable. A two-step up-conversion architecture was chosen for the transmitter with LO frequencies of 4.8 and 19.2 GHz (Fig. 8). The two LO frequencies are generated by a single synthesizer loop using a divide-by-four.

Quadrature up-conversion was implemented in both stages [20]. The image attenuation of the first up-conversion step depends upon the matching and quadrature accuracy of the

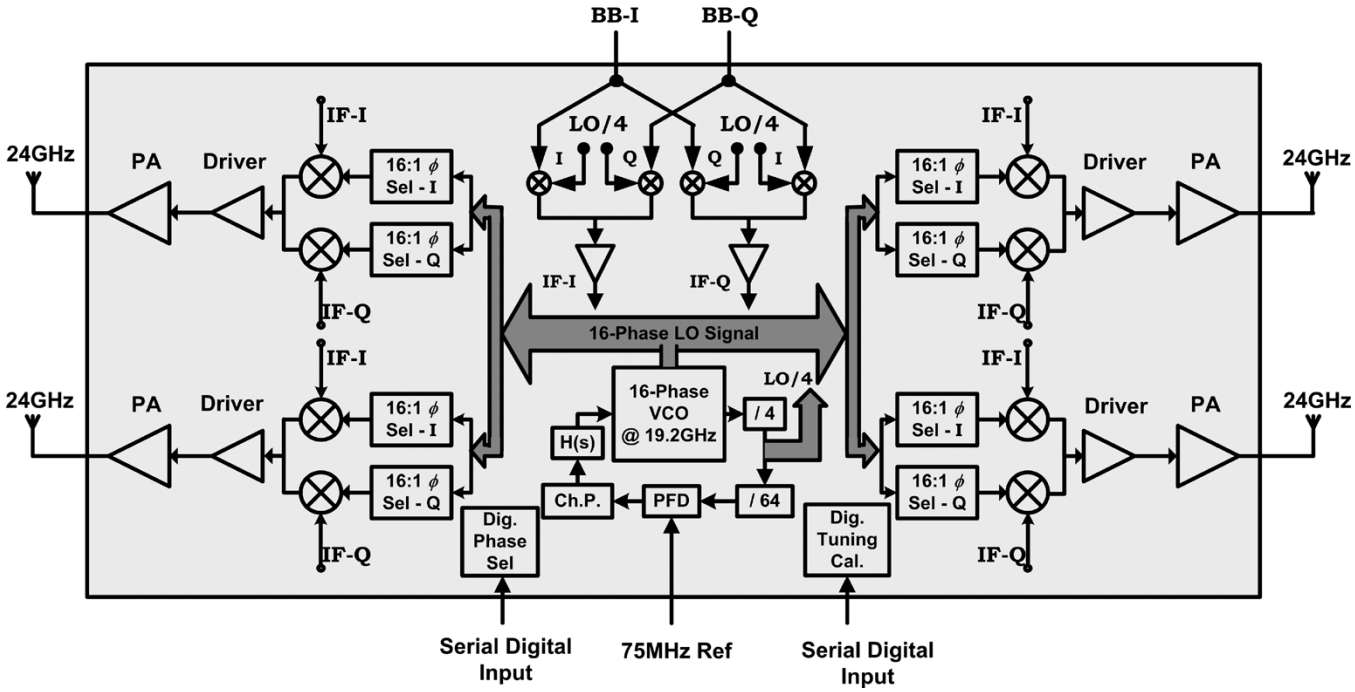


Fig. 9. Architecture and floor plan of 24-GHz four-element phased-array transmitter.

first up-conversion step. The image signal of the second up-conversion step falls at 14.4 GHz and is therefore attenuated not only by the quadrature architecture but also by the tuned stages at RF.

Fig. 9 shows the architecture and floor plan of the four-element transmitter [21]. In the signal path, the baseband I and Q signals are up-converted to 4.8 GHz by a pair of quadrature up-conversion mixers. The 4.8-GHz I and Q signals are buffered and provided to the 4.8- to 24-GHz up-conversion mixers in each element. The output of the mixers is amplified and differential to single-ended conversion is performed to drive the on-chip single-ended CMOS power amplifiers that are matched at the output to 50 Ω.

In the LO path, the output of the 16-phase 19.2-GHz VCO is provided to the phase selectors in each element. These phase selectors select the right phase of the LO in each element for the desired beam direction. The phase-selection circuitry is controlled by shift registers that can be programmed using a digital serial interface, enabling electronic beam steering. The VCO is part of an on-chip frequency synthesizer that generates the 19.2-GHz LO signals from a 75-MHz reference. A divide-by-four in the synthesizer loop generates the 4.8-GHz LO I and Q signals for the first up-conversion step.

A. Circuits in Signal Path

1) IF and RF Up-Conversion Mixers: The baseband-to-4.8-GHz quadrature mixers common to all elements are Gilbert-type up-conversion mixers. The first up-conversion mixer consumes 3.8 mA of dc current while the buffers following the mixer consume 4.3 mA. The output of these buffers is distributed to the quadrature up-conversion mixers in each element using a symmetric H-tree structure to ensure good array performance.

Fig. 10(a) shows the schematic of 4.8- to 24-GHz up-conversion mixers in each element. These mixers are essentially Gilbert-type up-conversion mixers with some of the dc current provided by the p-channel field-effect transistors (PFETs) [22], [23]. The current in the IF transconductance part of the mixer (M_1 and M_2) needs to be high to improve mixer linearity and gain. However, the V_{GS} drop in the switching devices (M_3, M_4, M_5, and M_6) increases significantly with higher dc current and hence the amplitude of the LO needed to switch these transistors increases. Therefore, to increase the conversion gain at a given LO swing and to reduce the sensitivity of the conversion gain to the LO amplitude, part of the dc current ($\sim$55%) is provided by the PFETs (M_7 and M_8), which reduce the dc current and, consequently, the V_{GS} drop across the switching devices. Fig. 10(b) plots the simulated conversion gain of the quadrature mixers against LO amplitude for the same dc current in the IF transconductance part, with and without the PFETs. It can be seen that, with the PFET current sources, the simulated quadrature conversion gain increases from 6 to 9.7 dB for a 200-mV peak-to-peak LO swing and is less sensitive to LO amplitude. The quadrature mixers draw a total current of 10 mA from a 2.5-V supply.

2) Tunable Passive Loads at 24 GHz: The cascade of tuned stages in the RF path in each element exacerbates any off-tuning in the passive loads. To avoid the problem of gain loss due to off-tuning, switchable capacitors, controlled by programmable shift registers, were implemented at the output of some of the high-frequency stages [Fig. 11(a)]. In the predriver stage, for example, these capacitors allow the center frequency to be tuned from 23.7 to 26.3 GHz, which is sufficient to account for process variations and errors in simulation of passives [Fig. 11(b)].

3) Balun: All the circuits up to and including the 24-GHz PA driver are differential while the PA was designed to be single ended. To avoid power and efficiency loss at the output of the

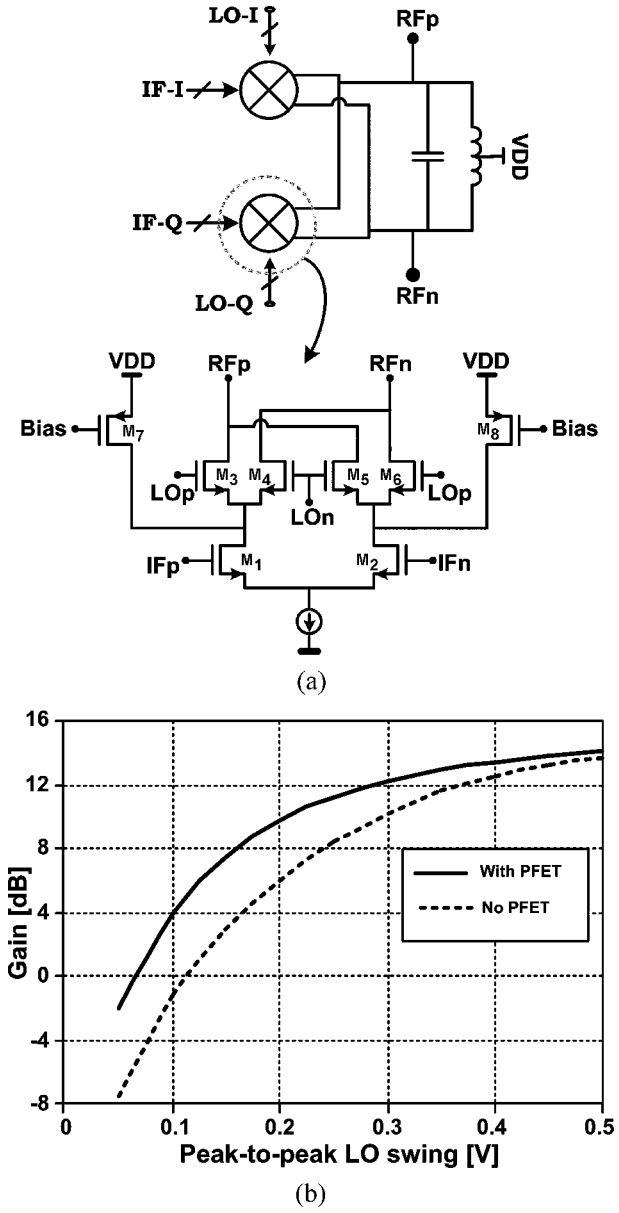


Fig. 10. RF up-conversion mixers (4.8–24 GHz). (a) Gilbert-type mixer with PFETs for current boosting. (b) Variation of gain with LO amplitude with and without current boosting.

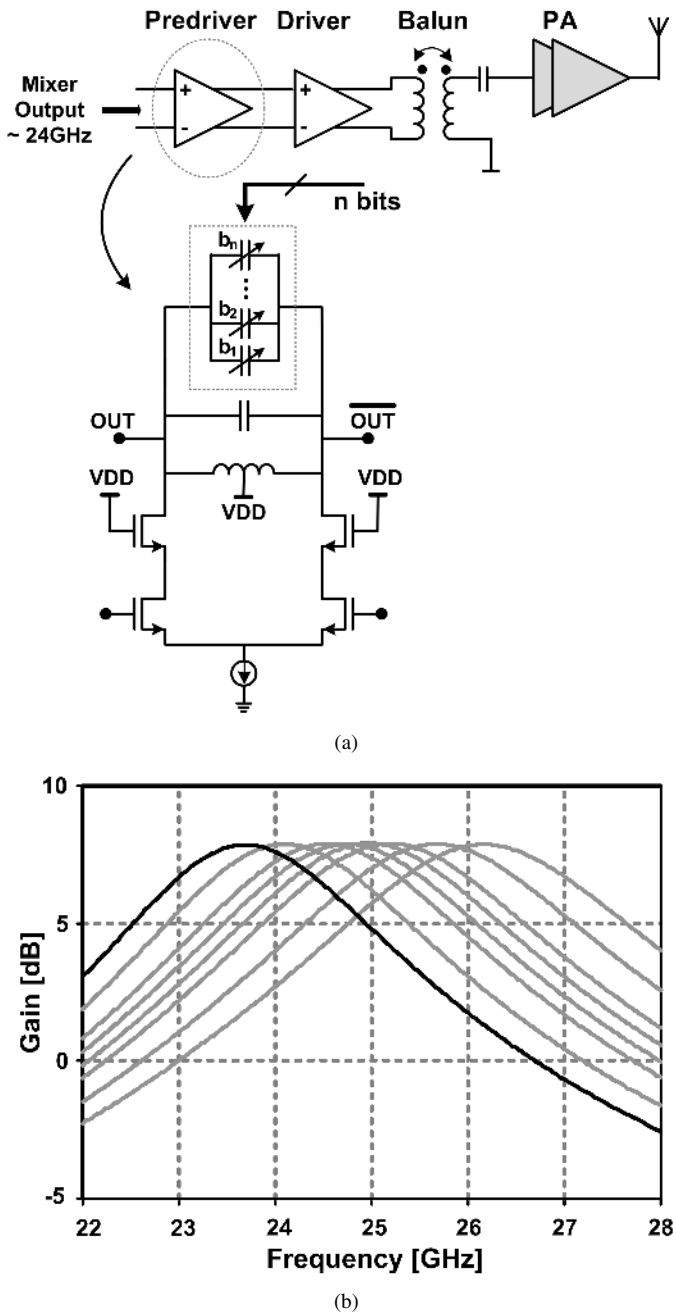


Fig. 11. Digital tuning calibration in high-frequency stages. (a) Predriver stage with switchable capacitors in load. (b) Simulated change in center frequency with digital tuning control.

PA, a balanced–unbalanced converter (balun) was placed before the PA. This eliminates the need for an off-chip balun or a differential antenna. As shown in Fig. 12, the balun was realized with a single-turn transformer to minimize substrate loss through capacitive coupling. Electromagnetic simulations show an insertion loss of 1.5 dB for the balun when input and output parasitic inductances are tuned out with parallel capacitors [24].

4) Power Amplifier (PA): The transmitter contains four on-chip power amplifiers matched at the output to 50 Ω. The amplifier, shown in Fig. 13(a), is similar to the stand-alone amplifier reported in [25]. While the input of the stand-alone amplifier is matched to 50 Ω, the parasitic inductance of the balun is used to tune out the input capacitance in the first stage of the amplifier integrated in the transmitter. The PA has two gain stages with each gain stage consisting of a cascode transistor pair to ensure stability and increase breakdown voltage. The PA is designed to operate in class AB mode. As the transistor $f_{\max}$ is 65 GHz, the harmonic content at the drain of the transistor for the 24-GHz input signal is low. Harmonic-matching-based classes such as class E and class F therefore did not increase efficiency significantly in simulation and were not used. The output and interstage matching networks in the PA are realized with the substrate-shielded coplanar waveguide structure shown in Fig. 13(b) to reduce power losses and area [26]. In this structure, the presence of the ground shield beneath the coplanar signal line increases the capacitance per unit length, C_u. However, as the return current cannot flow through the patterned ground shield, the inductance per unit length, L_u, remains the same. The simultaneously high C_u and L_u result

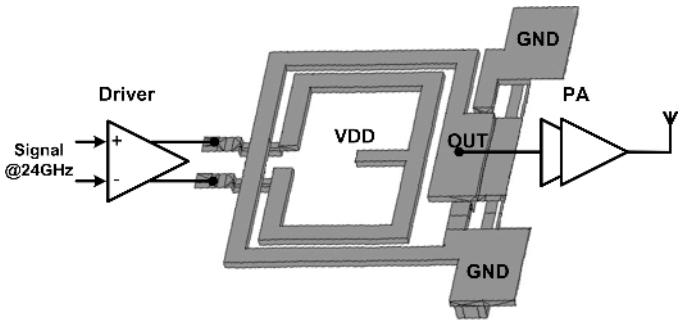


Fig. 12. Balun for differential to single-ended conversion at PA input.

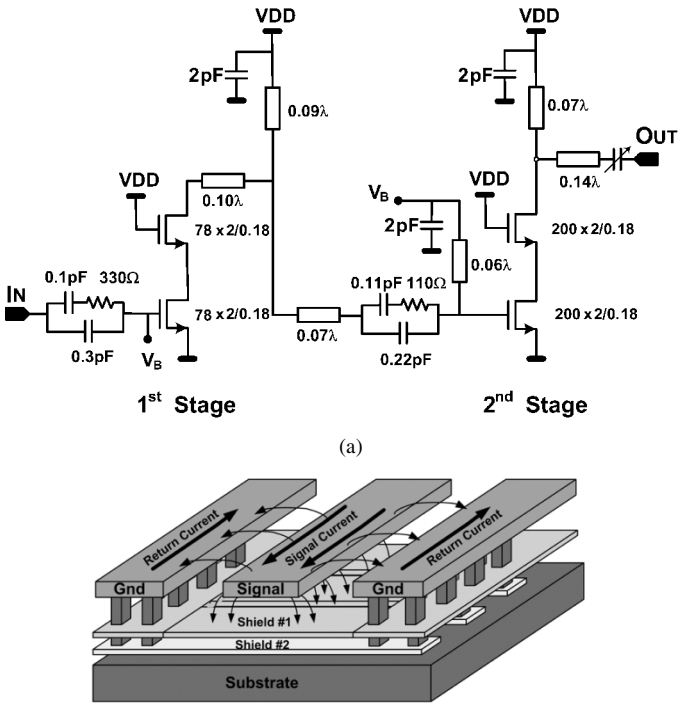


Fig. 13. On-chip power amplifier. (a) Two-stage on-chip power amplifier. (b) Substrate-shielded coplanar waveguide structure.

in lower wave velocity, leading to more than a factor of two reduction in wavelength at 24 GHz when compared to a standard coplanar waveguide structure in silicon dioxide. Additionally, as the structure is well shielded, the isolation between the power amplifier and other circuits in the transmitter is improved. The low loss per unit length (1 dB/mm), improved isolation, and short wavelengths make this structure particularly suitable for integrating multiple power amplifiers on the same die.

Amplifier stability is improved by the RC network at the input of each stage, which guarantees low frequency stability. Further details on the design of the power amplifier and the waveguide structure can be found in [19] and [25].

B. LO Path Circuits

The multiple-phase VCO, shown in Fig. 14, is at the heart of the LO phase-shifting architecture adopted in this paper. The 19.2-GHz CMOS VCO consists of eight differential amplifiers connected together in a ring structure and is similar to the design in [14]. As the ring is closed by flipping the inputs of the last

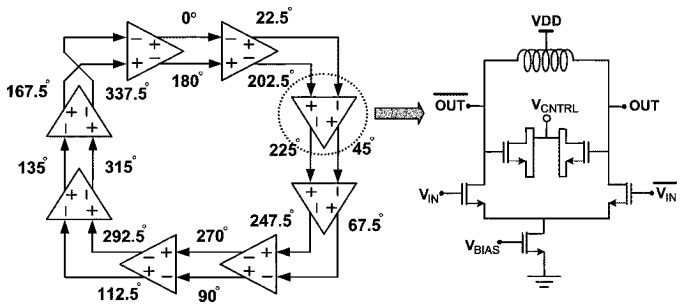


Fig. 14. 19.2-GHz 16-phase CMOS VCO.

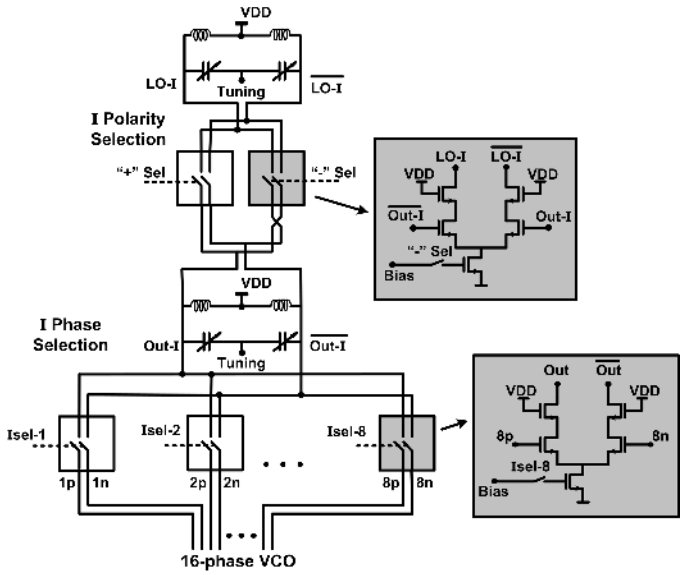


Fig. 15. Two-stage phase selector.

amplifier, the VCO is capable of generating 16 equally spaced phases of the LO with a step size of 22.5° [27]. As previously discussed, this step size is sufficient for a four-element phased-array system.

The outputs of the VCO have to be provided to the phase selectors in each element in a symmetric fashion as any asymmetry in this distribution leads to an error in the phase shift causing degradation of the array pattern. Therefore, a symmetric H-tree structure, using the top two thick metal layers, is used to distribute the multiple VCO outputs.

The phase selectors for the I and Q LO phases in each element work in two stages, with the first stage selecting the right differential pair and the second stage determining the polarity. The eight differential outputs of the VCO are provided to two sets of eight differential pairs that comprise the first stages of the I and Q phase selectors. The differential outputs are also provided to a dummy set of differential pairs to ensure that the VCO buffers see a constant load. Fig. 15 shows the phase-selection circuitry that determines the phase for the I signal to the mixer LO ports. An identical circuit selects the phase for the Q signal independently. As shown in Fig. 15, the tail current of each differential pair in the first stage is controlled by a shift register. By turning on the right differential pair in the first stage, the VCO differential pair outputs corresponding to desired phase for the I signal can be selected. The second stage of the phase selectors

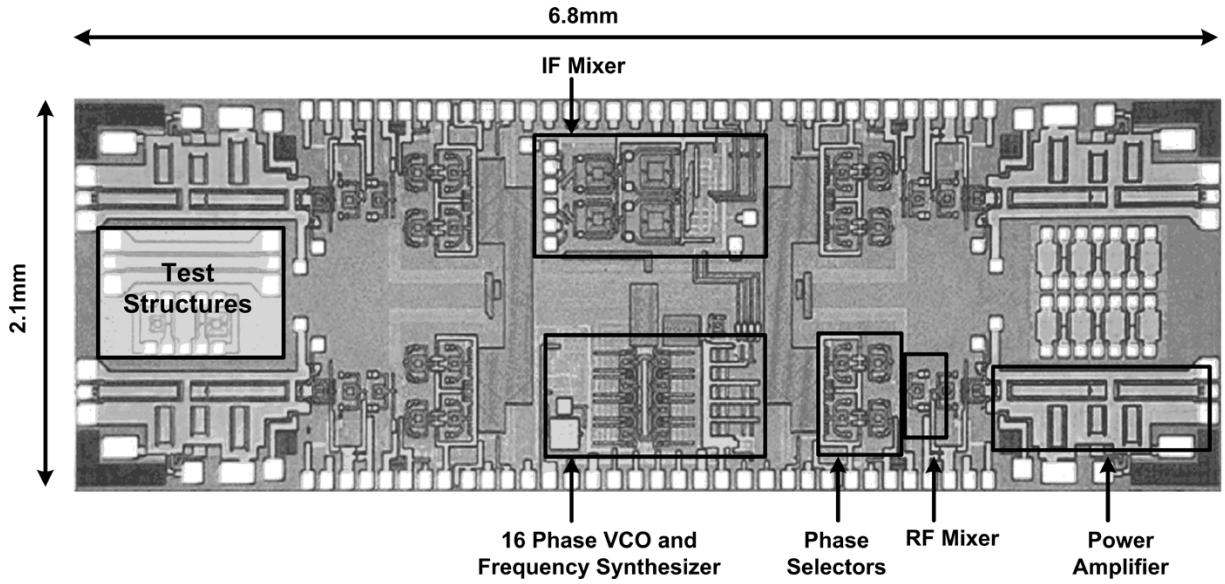


Fig. 16. Die micrograph of 24-GHz four-element phased-array transmitter.

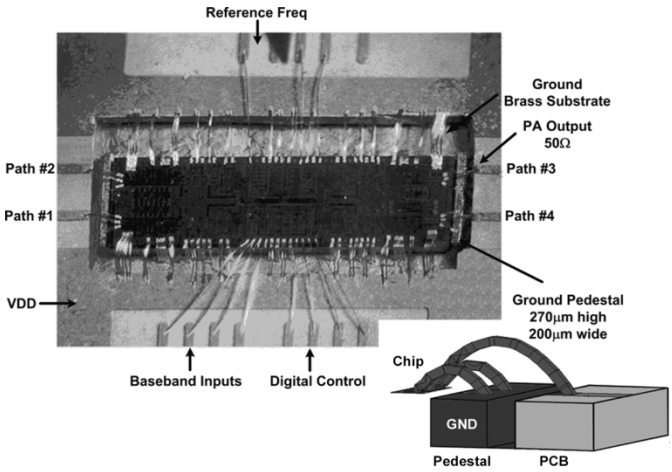


Fig. 17. Measurement setup to characterize transmitter performance.

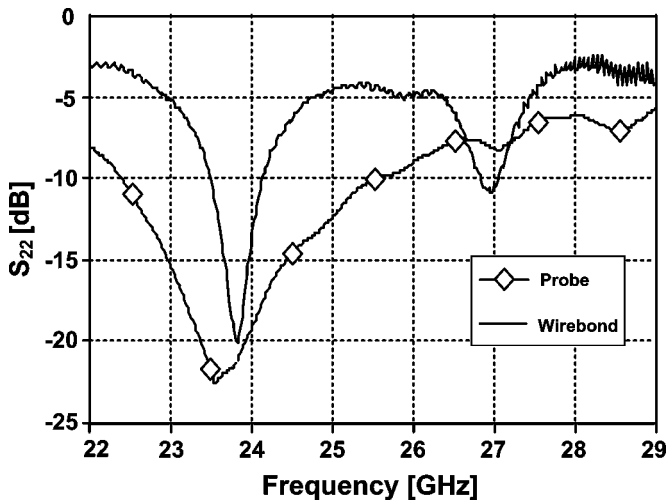


Fig. 18. Output matching with probe-based testing and with wirebonds to PCB.

consists of a set of two differential pairs with tail current sources that are also controlled by the shift registers (Fig. 15). The inputs to these differential pairs are anti-phase with respect to each other. Thus, the output can either be in-phase or anti-phase with respect to the input. In the dummy set, the tail current sources of the differential pairs is controlled by bits complementary to the LO I and Q phase-selection bits to ensure constant loading of the VCO buffers. The eight differential pairs (six dummy, one I, and one Q) that are turned on for any given phase shift draw a total of 16 mA and the differential pairs in the second stage draw 3.1 mA each. While independent I and Q LO phase selection provides flexibility to account for phase distribution and device mismatches, in practice the LO distribution and matching was sufficient to render independent selection superfluous.

Interpolation of the raw 16 phases of the VCO is possible by selecting more than one differential pair in the first stage of the phase selectors. (The two-stage phase selection procedure limits the phase shifts that can be generated by using this interpolation method.) For example, when the differential pairs corresponding to 0° phase and 22.5° phase are enabled, the output has a phase of 11.25°.

VI. Experimental Results

The phased-array transmitter has four elements and is implemented using 0.18-μm CMOS transistors in a BiCMOS process [28]. The f_T of the NMOS transistors in the process is 65 GHz. The process offers five metal layers with the thickness of the top two metal layers being 4 μm and 1.25 μm, respectively. Fig. 16 shows a die photograph of the transmitter which occupies 6.8 mm $\times$ 2.1 mm of die area.

A high-frequency printed circuit board (PCB) measurement setup has been designed to characterize complete system performance. Some of the packaging parasitics such as wirebond inductance have been taken into account during circuit design. Fig. 17 shows a close-up of the measurement setup for the transmitter chip. The PCB is a high-frequency laminate that is compatible with planar antenna design and is supported by a brass substrate that acts as the ground. Two ground pedestals are milled on the brass substrate and the chip is mounted on the substrate, between the pedestals, using silver epoxy. By wirebonding the PA ground pads onto the pedestals, the length

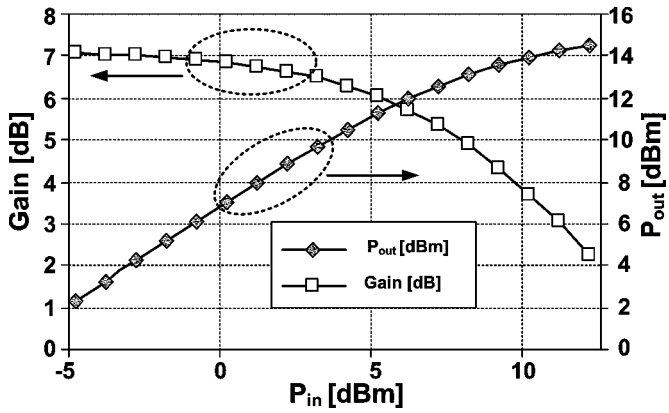


Fig. 19. Performance of on-chip 24-GHz CMOS power amplifier.

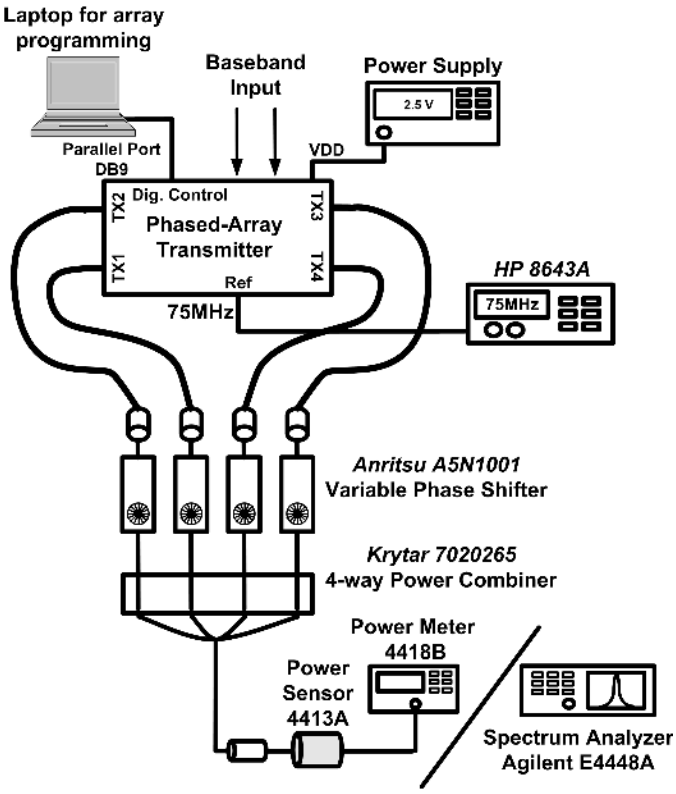


Fig. 20. Array measurement setup.

and therefore the inductance of these wirebonds are reduced. The height of the PCB (10-mil dielectric thickness) is chosen to be close to the height of the chip $(\sim 350\ \mu\text{m})$ to reduce the length of the wirebonds to traces on the PCB. Fig. 18 shows the output matching of a single element of the transmitter when measured by probing and by wirebonding the output to the PCB. Though the match with wirebonds is more narrowband, the output matching is better than 10 dB from 23.4 to 24.1 GHz. A broader frequency range for matching can be achieved by using flip-chip-based packaging techniques.

Fig. 19 summarizes the performance of the on-chip power amplifiers, which are capable of generating up to 14.5 dBm of output power at 24 GHz with an output-referred 1-dB compression point of 11 dBm. The coupling between multiple power amplifiers on the same die is a concern in an integrated phased-array system. The physical distance (∼1 mm) between

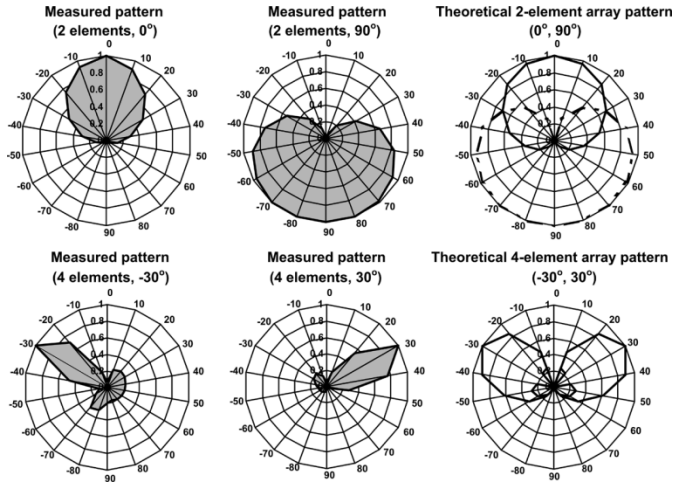


Fig. 21. Comparison of theoretical and measured array pattern with two elements and with four elements active.

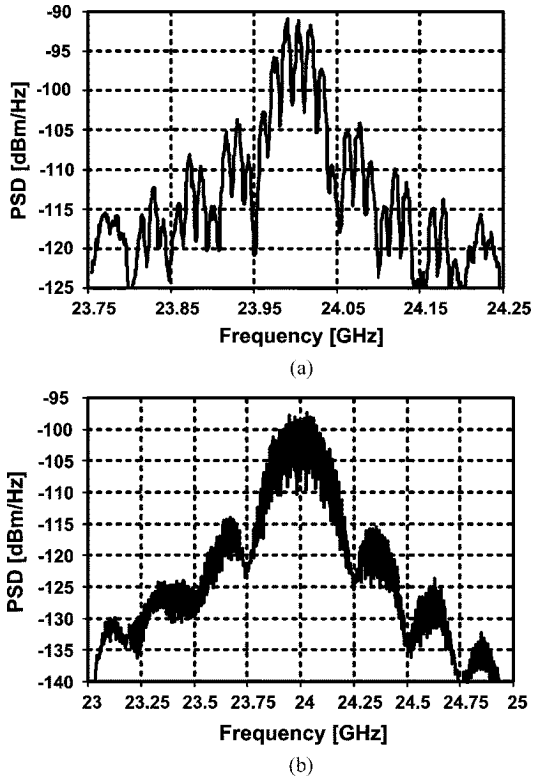


Fig. 22. Output spectrum of transmitter for 100- and 500-Mb/s QPSK input. (a) Output spectrum for 100-Mb/s QPSK input. (b) Output spectrum for 500-Mb/s QPSK input.

the power amplifiers and the use of a shielded transmission line in matching networks improve the isolation in this work. In order to measure the isolation between elements, three of the elements were deactivated by switching off all the LO phases in the phase selectors in those elements. The isolation was determined by comparing the power at the output of the active element with the output power of the three inactive elements. The worst case isolation (i.e., between two adjacent elements) is measured to be 28 dB.

The image rejection of the first up-conversion stage, which depends upon the quadrature matching of the mixers and the first

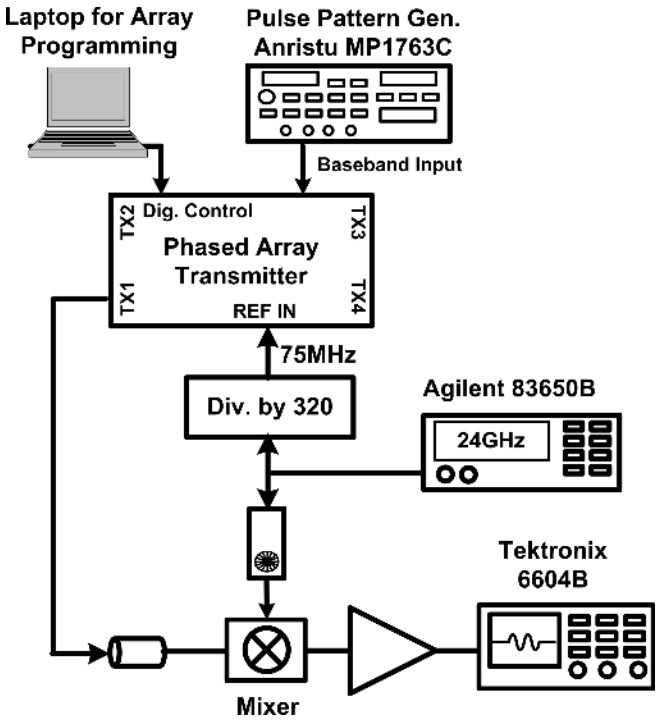


Fig. 23. Setup for direct down-conversion of 24-GHz transmitter output.

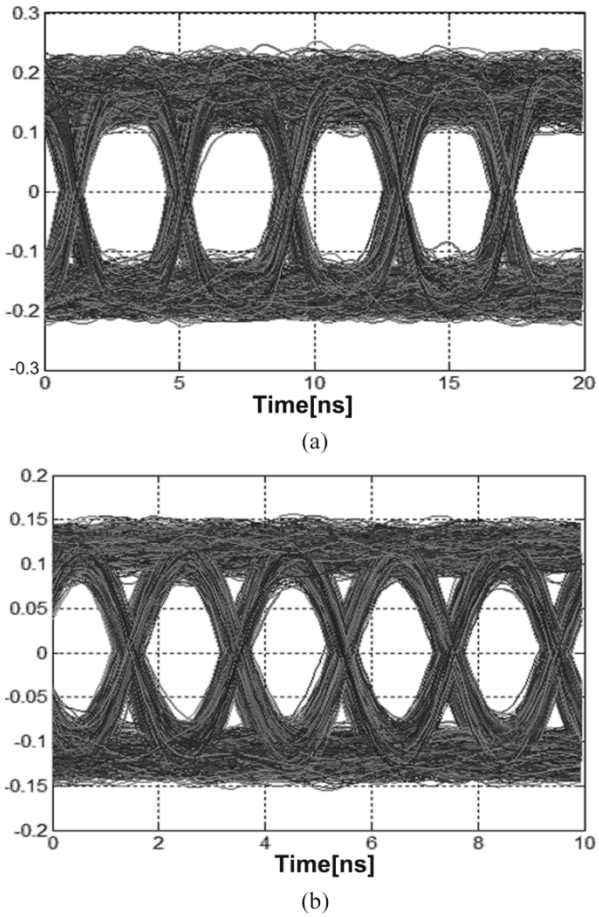


Fig. 24. Eye diagram of the down-converted transmitter output for 250- and 500-Mb/s BPSK input. (a) Single-channel 250 Mb/s (only to I channel): EVM $= 9.7\%$. (b) Single-channel 500 Mb/s (only to I channel): EVM $= 9.8\%$.

TABLE I
TRANSMITTER PERFORMANCE SUMMARY

On-Chip CMOS Power Amplifier Performance	
Maximum Saturated Output Power	+14dBm
Current Consumption @ 2.5V	68mA
Output Match @ 24GHz	-20dB
Equivalent 4-element EIRP	+26dBm
Output Referred 1dB compression point	11dBm
Peak PAE	6.5%
Output 3rd-order Intercept Point (OIP3)	14dBm
Phased Array Performance	
Peak-to-Null Ratio for 4-element Array	> 23dB
Beam Steering Resolution (for normal radiation)	< 10°
3dB Array Beam-Width @ 30° Radiation Angle	17°
Isolation between Paths (including wire bonds)	> 28dB
Image Signal Attenuation	
First upconversion	> 24dB
Second upconversion (image @ 14.4GHz)	> 43dB
Transmit 3dB Bandwidth	> 400MHz
Current Consumption @ 2.5V	
Signal Path (per element)	26mA
Phase Selector (per element)	34mA
16-Phase Frequency Synthesizer	180mA
Total (including IF stage and VCO buffers)	788mA
Device Technology	0.18μm CMOS
Die Area	6.8mm x 2.1mm

LO, is 24 dB. The image signal of the second up-conversion step, which falls at 14.4 GHz, is found to be attenuated by 43 dB due to the additional attenuation provided by the tuned stages at RF.

To measure the performance of the transmitter alone, without antenna nonidealities such as coupling, the different propagation delays for each element for each direction of radiation have to be replicated. This is done by connecting the output of each element to variable phase shifters (Fig. 20). By varying the relative phase shift in the external phase shifters, the propagation delays for each beam direction can be emulated. The output of the phase shifters is combined and measured using a spectrum analyzer or a power meter. Fig. 21 shows the measured performance of the transmitter with two elements active and with all four elements active. When compared to theory, these results demonstrate the proper functioning of the phased-array transmitter. The worst-case peak-to-null ratio with all four elements active is 23 dB.

While the PA has a bandwidth of 3.1 GHz, the bandwidth of the entire transmitter is constrained by the bandwidth of the IF stages and also by the cascade of tuned stages at IF and RF. Fig. 22, which shows the measured spectrum of the transmitter when a 100- and 500-Mb/s QPSK signal is provided at baseband, indicates that the transmitter is capable of supporting high data rates. To measure the performance of the transmitter for high data rate input, an external direct down-conversion receiver was assembled, consisting of a passive mixer followed

by an amplifier (Fig. 23). For this measurement, the LO signal that is used for down-conversion needs to be locked to the carrier signal of the transmitter. Therefore, the 24-GHz LO signal to the external mixer is divided by 320 to generate the 75-MHz reference for the on-chip frequency synthesizer. The baseband input was provided to one channel using a pseudorandom bit pattern generator and no pulse shaping was done at the input to minimize intersymbol interference (ISI). Fig. 24 plots the eye diagram for the down-converted baseband filtered output for the 250- and 500-Mb/s BPSK signal. The measured EVM did not increase significantly with an increase in data rate, indicating that it is dominated by the noise in the external down-conversion setup.

The entire system with four on-chip power amplifiers draws 788 mA from a 2.5-V supply. The measured performance of the chip is summarized in Table I.

VII. Conclusion

In this paper, the first fully integrated phased-array transmitter has been demonstrated using 0.18-μm CMOS transistors, proving the feasibility of high-frequency integrated phased-array systems on silicon-based processes. The tradeoffs of high-frequency wireless communication are discussed. The limitations of phase-shifting architectures are explored and methods to overcome them are suggested. The 4-bit local oscillator (LO) path phase-shifting approach adopted in the transmitter has better than 10° beam-steering resolution for radiation normal to the array. Each on-chip PA is capable of generating up to 14.5 dBm of output power, translating to an effective isotropic radiated power (EIRP) of 26.5 dBm. The transmitter is capable of supporting data rates in excess of 500 Mb/s and is well suited for 24-GHz wireless links.

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