A Fully Integrated DAC for CMOS Position-Based Charge Qubits with Single-Electron Detector Loopback Testing

Ali Esmailiyan, Hongying Wang, *Member, IEEE*, Mike Asker, Eugene Koskin *Member, IEEE*, Dirk Leipold, *Member, IEEE*, Imran Bashir, *Senior Member, IEEE*, Kai Xu, *Member, IEEE*, Anna Koziol, Elena Blokhina, *Senior Member, IEEE*, and R. Bogdan Staszewski, *Fellow, IEEE*

***Abstract*—This letter presents a fully integrated interface circuitry with a position-based charge qubit structure implemented in 22-nm FDSOI CMOS. The quantum structure is controlled by a tiny capacitive DAC (CDAC) that occupies 3.5×45 μm^2 and consumes 0.27 mW running at a 2-GHz system clock. The state of the quantum structure is measured by a single-electron detector that consumes 1 mW (including its output driver) with an area of 40×25 μm^2. The low power and miniaturized layout of these circuits pave the way for integration in a large quantum core with thousands of qubits, which is a necessity for practical quantum computers. The CDAC output noise of 12 μV-rms is estimated through mathematical analysis while the $\leq$ 0.225 mV-rms input referred noise of the detector is verified by measurements at 3.4 K. The functionality of the system and performance of the CDAC are verified in a loopback mode with the detector sensing the CDAC-induced electron tunneling from the floating diffusion node into the quantum structure.**

***Index Terms*—Capacitive DAC (CDAC), position-based qubits, quantum computer, quantum dot (QD), single-electron detector.**

I. Introduction

To achieve the goal of surpassing traditional computers and to provide solutions to complex real-world problems, quantum computers have to employ at least hundreds of thousands of qubits [1]. Qubits are sensitive to environmental noise and even at ultra-low temperature around 10 mK, the error rate is more than 0.1% per computational step [2], hence hundreds of error correcting qubits must be employed per each effective qubit. This demands the massive scalability in the number of qubits [3]–[5], but it poses main bottlenecks in the growing number of I/O signals for off-chip control electronics, as well as I/O congestion and system complexity [1], [6], [7]. To address this scaling problem, CMOS technology has been recently investigated for constructing spin [8] and position-based charge [9] qubits, which will naturally allow them to be monolithically integrated with their control, stimulus, and readout circuitry.

Our proposed quantum processor unit (QPU) uses *on-chip* interface circuitry to *electrostatically* set the quantum states of position-based charge qubits in accordance with a given quantum algorithm [9]–[12]. These proposed quantum states are controlled by adjusting potential barriers between quantum dots (QDs) to establish, via tunneling and entanglement, the intended functions of quantum gates. This demands high-speed voltage pulses with fine amplitude and width resolution, complexity of which grows with the QD array (QDA) structure size. In contrast with the spin-based qubit interfaces that require wide bandwidth circuitry operating at microwaves [4], the charge-based qubits can be electrostatically interfaced with baseband pulses [10], [12]. Furthermore, although the charge qubits are known to suffer from the relatively short decoherence time (50 ns to 1 μs), the ultra-high transition frequency f_T in advanced CMOS can help to fit over a thousand quantum gate operations within the useful decoherence duration [9].

In this letter, we focus on the most critical block of such a qubit interface circuit—capacitive DAC (CDAC), which must provide precisely controlled voltage levels and pulses of ultra-low noise at ultra-low power consumption. Since the CDAC directly connects with the *nanoscopic* and fragile quantum structure, it is not straightforward to characterize it. As a solution, we exploit the nearby single-electron detector in a test loopback configuration. A concurrent letter [12] covers some theoretical aspects of the implemented QDA structure and primarily focuses on injecting single electrons into the QDs. This CDAC is one of the key blocks used for that purpose. A previous version of the QPU chip was published last year in [10] and focuses on the overall digital circuitry including a pattern generator that produces the high-speed programmable digital pulses used by this CDAC.

II. Qubit Interface Circuitry

A. Imposer/Injector Topology

Fig. 1 presents an overview of the CMOS position-based charge qubit structure containing an array of QDs [9], [11], [12], with schematics of nearby interfacing circuitry: reset, control, single-electron injector, and detector. It is part of a quantum processor implemented in 22-nm FDSOI CMOS and operating at cryogenic temperature of 3.4 K, whose earlier version was presented in [10]. A 20-μm device exclusion region is maintained between the quantum structure and the interface circuits in order to minimize dopant induced de-coherence of the quantum state. Only the reset switch and the first source follower of the detector path are placed in close proximity of the last QD (realized as a floating depleted well), since their loading capacitance impacts the readout charge-to-voltage (Q-to-V) conversion gain.

From the perspective of controlling the quantum states, the versatile nature of the CDAC necessitates the circuit design specifications to cover all operations pertaining to the quantum core: precharge, reset, as well as a single-electron injection, extraction, and transfer. Another compounding issue is that even the simplest quantum structure requires many controlling signals; all routed to an extremely confined space [10]. Moreover, the stringent timing and skew requirement on the control signals calls for a modular and tiled floor plan. Power

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Ali Esmailiyan, Elena Blokhina, and R. Bogdan Staszewski are with Equal1 Labs Ltd., NovaUCD, Dublin D04, Ireland, and also with the School of Electrical and Electronic Engineering, University College Dublin, Dublin D04, Ireland (e-mail: ali.esmailiyan@equal1.com).

Hongying Wang, Eugene Koskin, and Kai Xu are with the School of Electrical and Electronic Engineering, University College Dublin, Dublin D04, Ireland (e-mail: kai.xu@ucd.ie).

Mike Asker, Dirk Leipold, and Imran Bashir are with Equal1 Labs Inc., Fremont, CA 94536 USA, and also with Equal1 Labs Ltd., NovaUCD, Dublin D04, Ireland.

Anna Koziol was with the School of Electrical and Electronic Engineering, University College Dublin, Dublin D04, Ireland. She is now with the Department of Measurement and Electronics, AGH University of Science and Technology, 30-059 Krakow, Poland.

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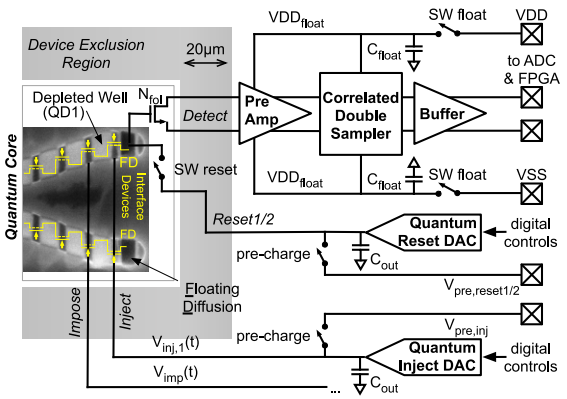

Fig. 1. Transmission electron microscopy (TEM) picture of electrostatic-qubit quantum core with schematic of interfacing circuitry.

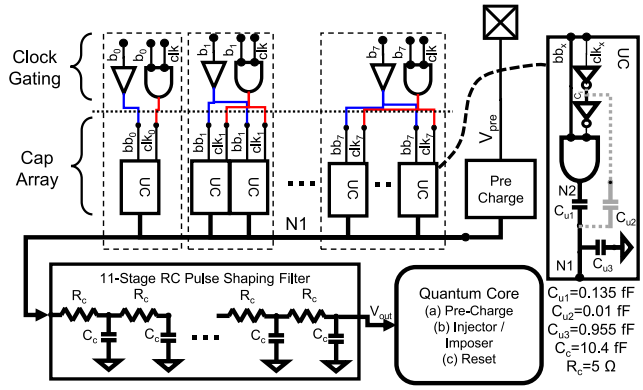

Fig. 2. Top-level schematic of CDAC.

consumption and kT/C noise are the other key factors dictating the design of the CDAC capacitor array.

The proposed 8-bit binary-controlled CDAC architecture with 255 identical weight units in Fig. 2 addresses the aforementioned challenges. The key building blocks within the CDAC are the circuitry for clock gating, capacitor array, precharge (pedestal setting), and pulse shaping filter. The capacitors in the binary-controlled array are split into unit cells (UCs), one of which is shown on the right side of Fig. 2. The unit cell comprises of logic gates driving the capacitive divider (C_{u1} and $\sum C_{u3}$). A noteworthy feature inside this block is a parasitically coupled negative clock edge, through C_{u2}, to compensate for switch charge injection and clock feed-through at the CDAC output. This mechanism limits the over- and under-shooting on node N1, which is critical for the proper QD operation. The negative clock edge injects a small compensating charge into N1 while the AND gate input ramps 5 ps later in the opposite direction and therefore the error voltage is reduced.

The clock gating reduces the dynamic power consumption by propagating the 2-GHz clock only to the enabled bits in the 8-bit CDAC. The precharge circuit sets a dc voltage on N1 before the CDAC is activated in order to establish the pedestal of the QD energy barrier levels. The 11-stage *RC* pulse-shaping filter reduces fast transients at V_{out}. R_c is realized with low metal layer Metal1 (M1) trace of 50-nm width, which still meets the DRC rules. At the time of design, it was not known that polysilicon resistors (without salicide) would work at 4K [8], [13]. All capacitors are designed with intermediate metal layers with a density of 5.08 fF per μm^2.

The CDAC output voltage that is dynamically added to the pedestal V_{pre} is

$$V_{\text{out}}(D) = \frac{D \cdot C_{u1}}{C_{\text{out}} + 255C_{u1}} V_{\text{DD}} \tag{1}$$

TABLE I
SUMMARY OF KEY SPECIFICATIONS FOR THE CDAC

	Speed	Voltage Range	LSB	Overshoot	Jitter
	GHz	mV	mV	mV	ps-peak
CDAC goal	2	70	0.3	0.3	5

$C_{\text{out}} = 11C_c + 255C_{u3}$ is defined as the total *static* capacitance between the CDAC's output and ground, including the 11-stage filter that becomes effective after its settling within a few time constants. C_{out} does not include the 255 units of the *dynamically* switched capacitor C_{u1}. Given the extracted values in Fig. 2 bottom right, the full-scale range of the CDAC from the precharge level (pedestal) is $V_{\text{out}}(D = 255) \approx 70\,\text{mV}$. The step size is thus $V_{\text{out, LSB}} \approx 273\,\mu\text{V}$. The bias for the precharge switch V_{pre} is supplied from an off-chip reference. Reducing the leakage at the control gates within the precharge switch is ensured by using long-channel MOS transistors.

It is essential that the kT/C noise power is not significant in order to avoid any influence on the Coulomb blockade effects in the QD structure. The equivalent total noise at the output of CDAC (i.e., N1) can be calculated by adding noise contributed by each switch-cap circuit of Fig. 2. The output noise due to the ith switching bit of D can be calculated as

$$\bar{v}^2_{\text{noise}}(b_i) = \left(\frac{2^i \cdot C_{u1}}{2^i \cdot C_{u1} + C'_{\text{out}}}\right)^2 \cdot \frac{kT}{\frac{C'_{\text{out}} \times 2^i \cdot C_{u1}}{C'_{\text{out}} + 2^i \cdot C_{u1}}} \tag{2}$$

where $C'_{\text{out}} \approx C_{\text{out}} + 255C_{u1}$ now includes both the static and dynamic capacitors at the CDAC output. Equation (2) calculates the noise based on the voltage division of the two series capacitors: C_{u1} in the ith unit cell and the total shunt capacitance seen at the DAC output. By the assumption that the noise contribution of all the switch-caps in the CDAC are uncorrelated, the total worst-case noise can be obtained by the summation of (2), which is calculated separately for all the b_{i} switch-caps in Fig. 2

$$\bar{v}^2_{\text{noise}} = \bar{v}^2_{\text{noise}}(\text{precharge}) + \sum_{i=0}^{7} \bar{v}^2_{\text{noise}}(b_i). \tag{3}$$

By substituting (3) with its equivalent values and with some simplifications, it can be concluded that the total output noise of CDAC is dominated by the precharge switch

$$\bar{v}^2_{\text{noise}} \approx \frac{kT}{C'_{\text{out}}}\left(1 + \frac{128 \cdot C_{u1}}{C'_{\text{out}}}\right). \tag{4}$$

With the unit capacitor $C_{\text{u1}} = 0.135\,\text{fF}$, $C'_{\text{out}} = 392\,\text{fF}$, the CDAC noise can be calculated at $T = 4\,\text{K}$ to be 12 μV-rms or 4.3% of LSB.

Table I summarizes the key specifications for the CDAC in the proposed system. The values are derived from physical equations and COMSOL multiphysics modeling of the QDA structures [9], [11]. To overcome the kT/q thermal energy of an electron, the LSB voltage step (i.e., resolution) at the tunnel junction between QDs should be finer than 300 μV at 4 K. However, the voltage applied at the imposer gates should be $\sim 10\times$ larger due to the capacitive division between C_{ox} (gate oxide capacitance) and C_t (tunnel junction capacitance). As a result, the required CDAC resolution shall be finer than 300 μV $\times 10 = 3$ mV. Further, in order to cover various mismatch errors and model inaccuracy at 4 K, an extra margin of $10\times$ was added, hence the DAC resolution was ultimately set at 300 μV. The decoherence time in our QDA system is estimated to be greater than 50 ns. The CDAC should be sufficiently fast such that it can shuttle the electron between multiple QDs within the decoherence time. Hence, the targeted sampling period for the CDAC is set to 0.5 ns, although it will decrease in the future for larger QDA structures. Timing error of the DAC output can change the equivalent injected energy into the QD and can result in a variation of energy level of the electron (i.e.,

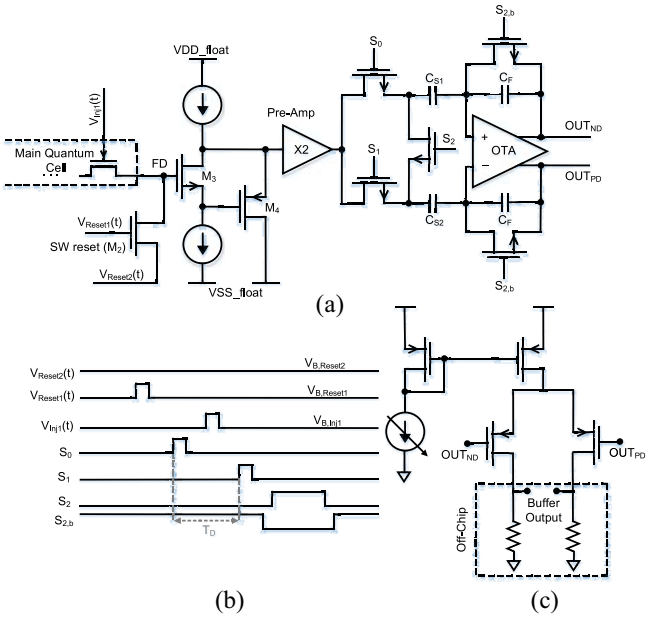

Fig. 3. Single-electron detecting readout path: (a) front-end circuitry, (b) CDS controlling signal waveforms, and (c) output buffer topology.

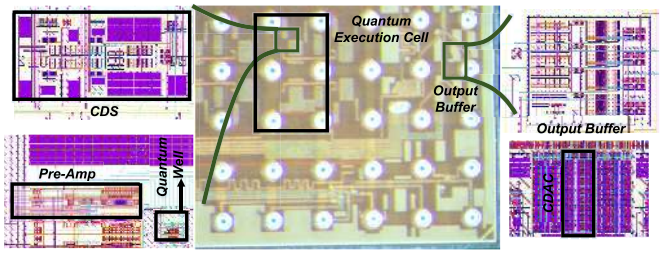

Fig. 4. Die micrograph with layout of major blocks (the ball pad spacing is 0.25 mm).

quantum state). The equivalent area under the DAC output pulses is proportional to that injected energy. If the voltage noise and ripples of the DAC output pulses can be ignored, then the equivalent error in the injected electron's energy would be limited to the timing errors of the pulses. By considering the 0.5-ns pulse duration of the DAC output signals, the timing error should be at least 10^2 times smaller, resulting in the maximum allowed DAC's timing error of 5 ps.

B. Readout path

Fig. 3(a) details the readout circuitry for detecting the state of the quantum structure. It functions as a single-electron detector to observe a gain or loss of an individual electron within a window determined by S_0 and S_1 pulses from the floating diffusion (FD) interface node between the quantum and classic circuits. It consists of a double source follower $M_{3,4}$, a preamplifier (pre-amp) and a switched-capacitor correlated double sampler (CDS). The minimum-size M_3 was selected to maximize the Q-to-V gain. However, such a choice brings up significant flicker noise from the device, but it is effectively rejected by the CDS scheme that samples the signal twice with S_0 and S_1 pulses within a short time interval, just before and after the electron is expected to be injected into or received from the floating depleted quantum well (labeled as "FD" in Fig.1).

III. Measurement Results

Fig. 4 shows a section of the fully integrated quantum core with the control electronics in 22-nm FDSOI, emphasizing the areas of

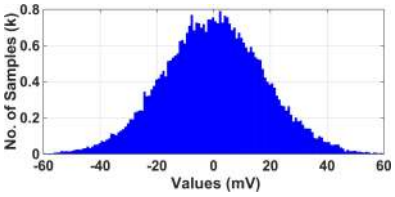

Fig. 5. Measured deviation signal at the output buffer.

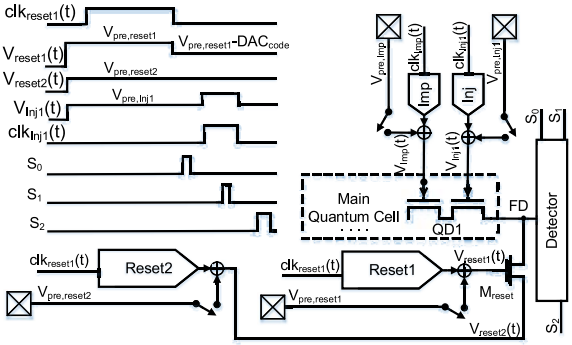

Fig. 6. Signal sequence to characterize CDAC by draining an electron from node FD.

the quantum core, the device exclusion area, low-noise preamplifier, CDS, and output buffer. The CDAC occupies $3.5\times45\ \mu m^2$ and consumes 0.27 mW in dynamic power running at a 2 GHz system clock. The single-electron detector occupies $40\times25\ \mu m^2$ and consumes 1 mW (including its output driver). This presents a potential for high-scale integration at 4 K where over 1 W of heat extraction is available.

The single-electron detector is characterized first. Fig. 5 shows the detector's output voltage at 3.4 K over 10 000 trials while the FD is kept undisturbed. The standard deviation of the detector output noise is 18 mV-rms. With the simulated detector gain of 80 (V/V), the input-referred noise is 0.225 mV_{rms}.

Characterizing the pulsing DAC designed to drive the "fragile" single-electron injection structure is a very difficult task. Fig. 6 illustrates the proposed "loop-back" measurement method[1] using the nearby single-electron detector with CDS that senses a difference in the FD potential developed between S_0 and S_1 pulses. The reset device first momentarily sets the FD potential. During the sequence, an electron is injected via tunneling from FD node into the first QD (QD1) resulting in a loss of charge and therefore a positive *quantum* change in voltage at that node, which is measured by the detector before (S_0) and after (S_1), the injection event in order to get a *net* charge loss. However, this operation is contingent upon the reset switch transistor M_{reset} staying under subthreshold regime. If not, then V_{reset2} will pull the FD node and any information associated with the electron injection will be lost. Consequently, when the gate and source of M_{reset} are swept over a suitable range, there will be a set of $V_{\text{pre,reset1}}$ and $V_{\text{pre,reset2}}$ voltages when the M_{reset} transistor just *barely* turns on, i.e., when $V_{gs} = V_{\text{pre,reset1}} - V_{\text{pre,reset2}}$ is right at the strict neighborhood of the threshold voltage, V_{th}. This will ensure the subsequent electron injection from node FD into the QD structure. If $V_{GS} > V_{th}$, then node FD will be ac grounded during the quantum experiment and detection. If $V_{GS} < V_{th}$, then node FD will simply not get reset. Lowering V_{gs} after the reset by means of the CDAC will help M_{reset} to stay below V_{th} during the electron injection and detection phases. The window between these two regions

[1]This is similar in concept to loop-back modes in radio transceivers for testing and calibrating entire chains.

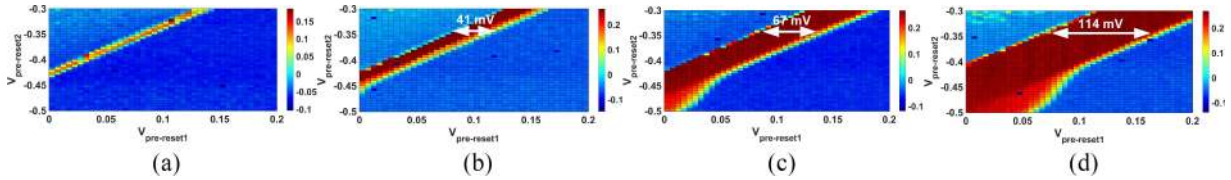

Fig. 7. Measured heatmaps of the output detector voltage when $V_{\text{pre, reset1}}(t)$ and $V_{\text{pre, reset2}}(t)$ are swept for CDAC code examples of (a) 0, (b) 75, (c) 150, and (d) 255.

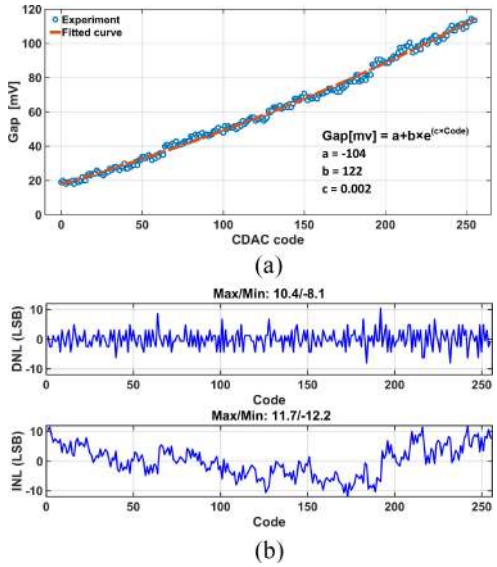

Fig. 8. Measurement results of the voltage gap for (a) different CDAC code and (b) DNL/INL results.

is proportional to the voltage swing at the CDAC output, which is ideally proportional to the DAC code, as per (1).

Fig. 7 plots the measurement results of the applied pulses in Fig. 6 with the heat color indicating the detector path output voltage. Very high $V_{\text{pre,reset1}}$ (x-axis) and very low $V_{\text{pre,reset2}}$ (y-axis) during the measurement result in constant voltage at FD and, as a result, the output voltage variation of the detector will be close to zero (lower blue area in Fig. 7). If $V_{\text{pre,reset1,2}}$ are set appropriately, as stated above, the detected voltage change (red area in Fig. 7) will correspond to an electron loss due to the tunneling from FD to QD1. The red gap area in Fig. 7 is changing from 20 to 114 mV, which is equal to the output voltage step change of $V_{\text{reset1}}(t)$ caused by the CDAC.

Fig. 8(a) plots the voltage gap shown in Fig. 7, which corresponds to (1), versus the CDAC code, D. The DNL and INL nonlinearities of the CDAC transfer function in Fig. 8(a) are plotted in subfigure (b). The INL nonlinearity is due to the small unit capacitor size and increased mismatch at 4 K, but here it is not critical, as the size and consumed power, as well as voltage stability, repeatability, and low noise, are of utmost importance. Despite the DNL of 10, the system works as intended in the manual/experimental mode of operation, which merely requires precise pulse transitions between *two semi-static* voltage levels. It would need to be improved in future versions to avail of algorithmic searches for the optimal reset, injector, and imposer voltages.

IV. Conclusion

We have introduced and experimentally verified a fully integrated interface between a quantum processor core operating at 3.4 K with its nonquantum (i.e., classical) circuitry that sets and reads the quantum states. The quantum processor is built with position-based charge qubits employing an array of QDs. The interfacing circuitry comprises a single-electron injector and detector, connected to an FD node, which is the point-of-contact between the quantum and non-quantum domains. The injector moves an electron from the FD node to the QD structure, while the detector senses the event. The interface circuitry further comprises a reset transistor for momentarily setting a potential on the FD node, as well as imposers for manipulating the energy potentials of the QDA. The underlying circuit for the injector, imposer, and reset device is a CDAC, which must minimize its noise, transients, power consumption, and area. The CDAC is tested and characterized in a loopback configuration with the single-electron detector, which also verifies the functionality of the detector, reset device, and the quantum tunneling into the QD structure.

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