A Fully-integrated Split-electrode SSHC Rectifier for Piezoelectric Energy Harvesting

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***Abstract*—In order to efficiently extract power from piezoelectric vibration energy harvesters, various active rectifiers have been proposed in the past decade, which include Synchronized Switch Harvesting on Inductor (SSHI), Synchronous Electric Charge Extraction (SECE), etc. Although reported active rectifiers show good performance improvements compared to full-bridge rectifiers (FBR), large off-chip inductors are typically required and the system volume is inevitably increased as a result, counter to the requirement for system miniaturization. In this paper, a fully-integrated split-electrode SSHC (synchronized switch harvesting on capacitors) rectifier is proposed, which achieves significant performance enhancement without employing any off-chip components. The proposed circuit is designed and fabricated in a $0.18\,\mu\text{m}$ CMOS process and it is co-integrated with a custom MEMS (microelectromechanical systems) piezoelectric transducer with its electrode layer equally split into four regions. The measured results show that the proposed rectifier can provide up to 8.2× and 5.2× boost, using on-chip and off-chip diodes respectively, in harvested power compared to a FBR under low excitation levels and the peak rectified output power achieves $186\,\mu\text{W}$.**

***Index Terms*—Energy harvesting, piezoelectric transducer, synchronized switch harvesting on inductor (SSHI), synchronized switch harvesting on capacitors (SSHC), fully-integrated system, switched capacitors, power conditioning, rectifiers.**

I. Introduction

Along with the development of the Internet of Everything (IoE), miniaturized piezoelectric vibration-based energy harvesters have drawn significant interest as a means of harvesting ambient kinetic energy to power wireless sensor nodes in wireless sensor networks (WSN) [1]–[3]. Since the environmental vibration is periodic and highly unpredictable, the energy generated by a piezoelectric transducer (PT) cannot be directly used and an interface circuit is needed to rectify the generated power and provide a stable DC supply to the loads. Full-bridge rectifiers (FBR) are widely employed in most commercially available power management units (PMU) due to their simplicity and stability; however, the low power-extraction efficiency of FBRs limits the usable output power for loads, especially under low ambient excitation levels [4], [5]. In order to increase rectified power, a variety of active interface circuits have been proposed in the past decades, which include SSHI (synchronized switch harvesting on inductor), SECE (synchronous electric charge extraction), etc [6]–[16]. Although these reported rectifiers show good performance enhancement compared to FBRs under low excitation levels, they typically require large inductors to achieve good performance and the inductance values can be up to 10's mH. These inductors significantly increase the system volume, especially for MEMS-CMOS co-integrated systems, counter to the requirement for system miniaturization.

Recently, an inductorless interface circuit was proposed by Chen et al. [17] that uses a technique called flipping-capacitor rectifier (FCR), which employs a number of switched capacitors (SC) to synchronously flip the voltage across the PT. The work achieves a fully integrated implementation with high performance enhancement thanks to the small inherent capacitance of the PT ($C_P = 80\,\text{pF}$). The term "high performance" used here and later in this paper means the extracted power ratio between using an active rectifier and using a passive FBR is high, and this ratio is usually in range of $1 - 10$ for reported interface circuits. However, this small PT with high resonant frequency ($110\,\text{kHz}$) used in [17] is typically used in ultrasonic wireless power transfer (WPT) systems and may not be suitable for kinetic vibration energy harvesting since the real-world kinetic vibration typically has a much lower frequency range between 10's Hz and 1's kHz. PTs targeting this frequency range usually have much higher inherent capacitance C_P (between 1's nF and 100's nF), and as a result, the required total capacitance value for the FCR technique will be too large to be implemented on-chip. Besides the FCR technique, a SSHC (synchronized switch harvesting on capacitors) rectifier has been proposed in [18]. Similar to SSHI rectifiers, the SSHC rectifier employs capacitors instead of inductors to perform synchronous voltage flip. The number of employed capacitors can be configured to any positive integer according to the trade-off on performance and system volume: more capacitors result in higher performance.

Fig. 1 shows the circuit diagrams of a full-bridge rectifier, a SSHI rectifier and a SSHC rectifier. While the PT is vibrating, it can be modeled as a current source I_P in parallel with a capacitor C_P. This equivalent circuit model of a PT has been proven to be inaccurate for PTs with strong electromechanical coupling [19]. However, the PT used in this paper is fabricated

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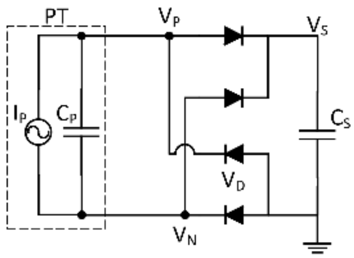
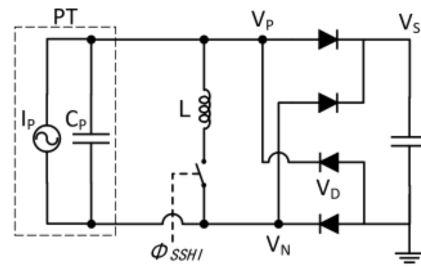
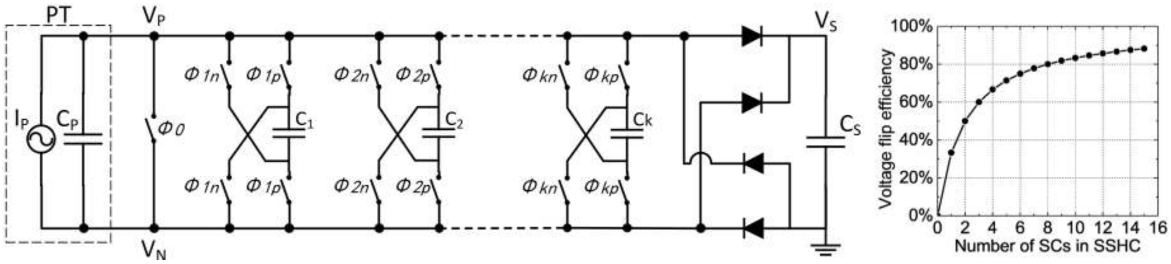


(a) Full-bridge rectifier.



(b) SSHI rectifier.



(c) SSHC rectifier with k switched capacitors (SC) and the theoretical voltage flip efficiencies.

Fig. 1: Circuit diagrams of (a) a full-bridge rectifier, (b) a SSHI rectifier and (c) a SSHC rectifier with k switched capacitors.

in a commercial MEMS process with AlN (Aluminum Nitride) as the piezoelectric material. Due to the low piezoelectric coefficient and coupling factor of AlN (around $1-2$ orders of magnitude lower than PZT), the electromechanical coupling is weak for AlN and the generated voltage across the PT has very little effect on the mechanical vibrations. In this case, the specified equivalent circuit model comprising a current source and a capacitor is sufficiently accurate. The voltage flip efficiency plot in Fig. 1c shows that more SCs in a SSHC rectifier can increase the voltage flip efficiency, hence, the power extraction performance. The relation between voltage flip efficiency and output power will be derived later in Section II-B. Previous work clarifying this relation can also be found in [6], [16], [20], [21]. According to different applications and performance requirements, the SSHC rectifier can be configured by employing a suitable number of SCs. Despite the performance and configurable architecture of the SSHC rectifier, the switched capacitors (SC) are sometimes difficult to be implemented on-chip, since the SCs need to have equal capacitance as C_P to achieve optimal performance [18]. The term “optimal performance” used here and later in this paper means the voltage flip efficiency is maximum while varying the capacitance values of the SCs. This peak is achieved while C_P is the same as all the SCs and the flip efficiency plot in Fig. 1c actually shows the optimal flip efficiency when $C_P = C_{SC}$. Although on-chip implementations can be easily achieved while using small PTs, such as the PT with $C_P = 80\,\mathrm{pF}$ used in [17], it is almost impossible to implement the SCs on-chip for large PTs in kinetic vibration energy harvesting systems since such PTs typically have C_P values between 1’s nF and 100’s nF.

In this paper, a fully integrated split-electrode SSHC (SE-SSHC) rectifier is proposed to perform synchronous voltage flip. With the proposed architecture, required SCs to achieve the optimal performance is significantly reduced so that they can be easily implemented on-chip even for PTs with large C_P capacitance. Since this design does not require any off-chip component (except for power capacitors), the system volume is significantly reduced while achieving high performance. The rest of this paper is organized as follows. Section II presents the proposed SE-SSHC rectifier and provides power analysis in comparison with a FBR. Detailed circuit implementations are shown in Section III. Measured results and comparisons with state-of-the-art rectifiers are provided in Section IV and a conclusion is provided in the last section.

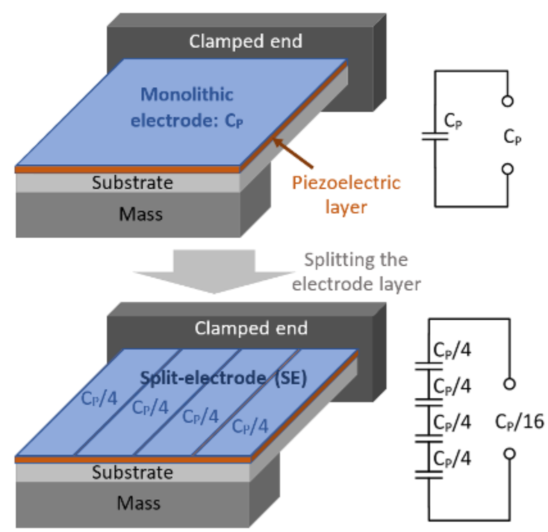


Fig. 2: Splitting the monolithic electrode electrode of a PT into 4 regions.

II. Proposed SE-SSHC system

As previously discussed, the SSHC rectifier shown in Fig. 1c requires all the switched capacitors (SC) have the equal

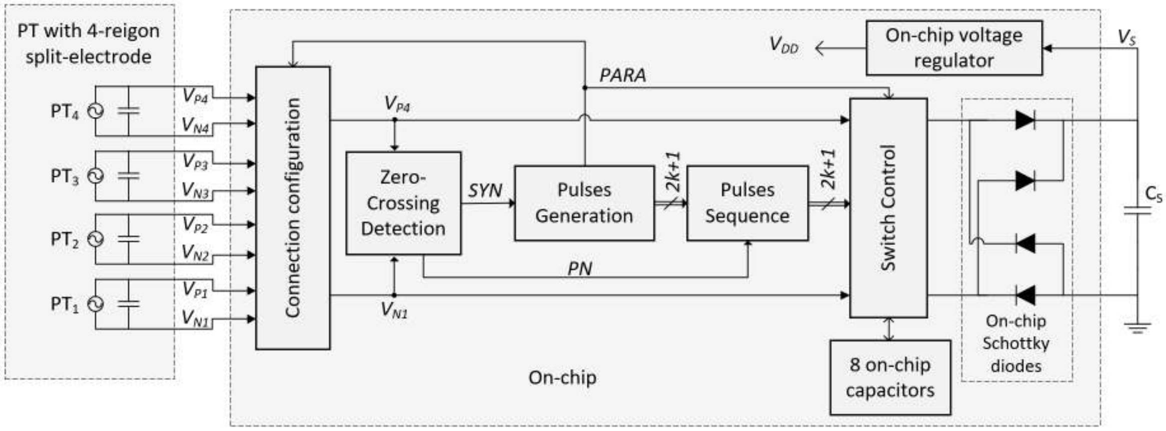


Fig. 3: System architecture of the proposed SE-SSHC rectifier.

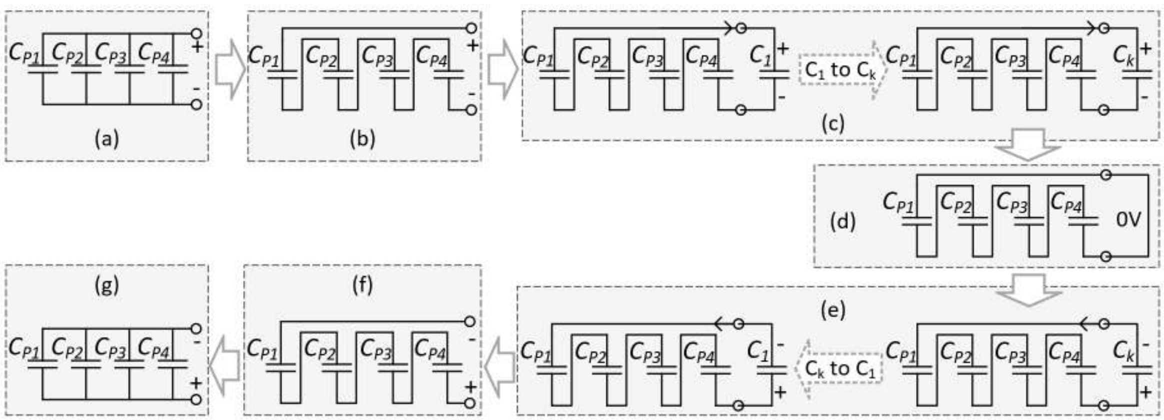


Fig. 4: Schematic description of the connection configuration cycle during voltage flip.

capacitance as that of the PT to achieve the optimal performance, such as $C_1 = C_2 = \cdots = C_k = C_P$. This requirement makes on-chip implementation of SCs very impractical when PTs with large C_P values are employed. In order to address a fully integrated implementation, the optimal SC values need to be significantly decreased. In the proposed SE-SSHC system, a split-electrode PT is employed with its electrode layer split into several regions, assuming n regions ($n = 4$ in this work). During the voltage flip time instants, the four regions are temporarily connected in series so that the effective capacitance of the PT is decreased by $4^2 = 16$ times, as shown in Fig. 2. As a result, the required SCs in the SSHC rectifier are also decreased by 16 times such that they can be implemented on-chip. In this work, the PT is designed and fabricated in a commercial MEMS process. In order to achieve this design, the n regions need to be completely separated for all the layers in the MEMS process, including the top electrode layer, piezoelectric layer and doped-Silicon substrate layer. These n regions are strongly coupled with a common proof mass at the free end of the cantilever. With this design, the n regions are mechanically coupled and electrically insulated. As a result, the signals generated from all the regions are identical in amplitude, frequency and phase; hence, they can be perfectly connected in parallel or in series [22]. This section presents the proposed SE-SSHC rectifier at the system level. The performance compared with a FBR is then theoretically analyzed.

A. System architecture

Fig. 3 shows the system architecture of the proposed SE-SSHC rectifier co-integrated with a PT with its electrode split into 4 regions. The regions of the PT are connected into the SE-SSHC system through the “connection configuration” block, which configures the connection of the four regions according to the signal $PARA$. At each zero-crossing moment of the current source generated from the PT, the “zero-crossing detection” block generates a rising edge in the signal SYN by monitoring voltages at nodes V_{P4} and V_{N1}. A signal PN is also generated indicating the polarization of the voltage across the PT, noted as V_{PT}, which equals to $V_{P4} - V_{N1}$. Following the rising edge of SYN, $2k+1$ pulses are sequentially generated, where k is the number of SCs enabled for a SSHC rectifier. In the meantime, the signal $PARA$ is pulled down to force a series connection of the 4 electrode regions and to disconnect the system from the full-bridge rectifier (FBR) during the voltage flip instants. The following “pulse sequence” block sequences the $2k+1$ pulses according to the signal PN to flip V_{PT} from positive to negative, or vice-versa. The sequenced $2k+1$ pulses drive the “switch control” block together with the on-chip SCs to perform voltage flip.

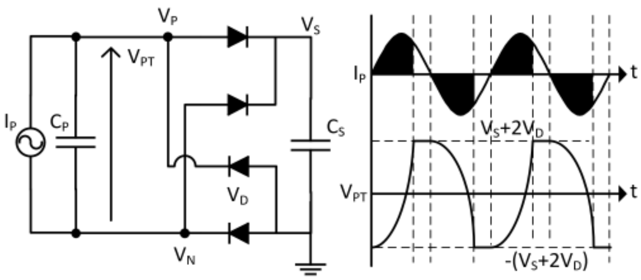


Fig. 5: Full-bridge rectifier and the associated waveforms.

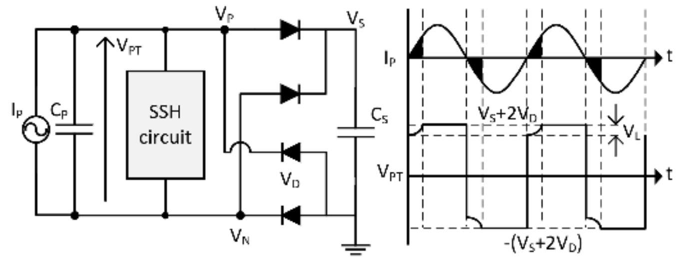


Fig. 6: SSH rectifier and the associated waveforms.

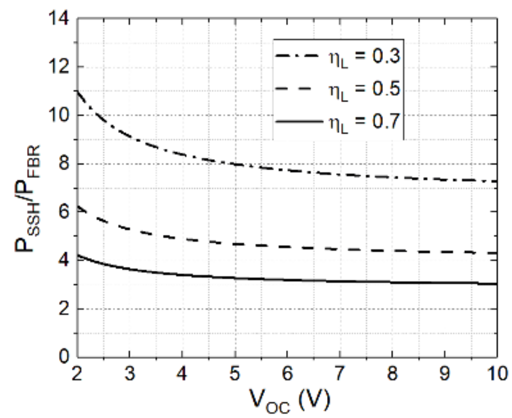


Fig. 7: Theoretical performance improvement of a SSH rectifier compared with a FBR (P_{SSH}/P_{FBR}) with on-chip diodes ($V_D = 0.25\,\mathrm{V}$) in a range of V_{OC}.

After the voltage flip is complete, $PARA$ goes back to high to configure the 4 regions back to a parallel connection until the next zero-crossing moment. An on-chip voltage regulator is employed to generate a $1.5\,\mathrm{V}$ DC supply for the system.

Fig. 4 shows one connection configuration cycle while V_{PT} is being flipped from positive to negative. State (a) is the moment to commence the voltage flip, which is also the zero-crossing moment of I_P. Before voltage flip commences, the four regions of the PT is configured to be connected in series, as shown in (b). The states (c), (d) and (e) show how the voltage is flipped with $2k+1$ sequential pulses, where k is the number of SCs enabled in a SSHC rectifier. The first k pulses connect the PT to all the k SCs sequentially from C_1 to C_k. The middle pulse shorts the PT to clear the remaining charge in the PT. The last k pulses connect the k SCs to the PT sequentially, but in a reversed order (from C_k to C_1) and in an opposite polarization compared to the first k pulses. After all these $2k+1$ pulses, the voltage across the PT is flipped, as shown in (f). The four regions of the PT is then configured back to a parallel connection shown in (g). When the voltage across the PT needs to be flipped from negative to positive, the configuration cycle is reversed to be from state (g) to state (a).

B. Performance analysis

In order to evaluate the performance enhancement of the proposed circuit, it is useful to analyze the rectified power of a passive full-bridge rectifier (FBR). Fig. 5 shows the circuit diagram of a FBR and the associated waveforms. When the PT is vibrating, it can be modeled as a current source, I_P, in parallel with a capacitor, C_P. The current source can be expressed as $I_P = I_0 \sin(\omega t)$, where $\omega = 2\pi f_P$ and f_P is the excitation frequency. In a half period of I_P, the total generated charge by the PT can be expressed as:

$$Q_{tot} = \int_0^{\frac{T}{2}} I_0 \sin \omega t \mathrm{d}t = \frac{2I_0}{\omega} \tag{1}$$

While the PT is in an open-circuit, the open-circuit zero-to-peak amplitude can be shown as:

$$V_{OC} = \frac{1}{2}\frac{Q_{tot}}{C_P} = \frac{I_0}{\omega C_P} \tag{2}$$

When the PT is connected to a FBR, the FBR sets a voltage threshold for V_{PT} to overcome and V_{PT} needs to attain either $V_S + 2V_D$ or $-(V_S + 2V_D)$ before generated charge can be transferred into the power capacitor C_S, where V_S is the voltage across the capacitor C_S and V_D is the forward voltage drop of the diodes. For each half period, V_{PT} needs to be flipped from $\pm(V_S{+}2V_D)$ to $\mp(V_S{+}2V_D)$ and the charge used to flip V_{PT} between these two voltage levels is not extracted. Hence, the remaining charge transferred into C_S can be written as:

$$\begin{aligned} Q_{FBR} &= Q_{tot} - 2(V_S + 2V_D)C_P \\ &= 2C_P(V_{OC} - V_S - 2V_D) \end{aligned} \tag{3}$$

Assuming the voltage increase in C_S in a half I_P period is very small compared to V_S value, the extracted power stored in C_S can be expressed as:

$$P_{FBR} = \frac{V_S Q_{FBR}}{T/2} = 4 f_P C_P V_S (V_{OC} - V_S - 2V_D) \tag{4}$$

The peak value of P_{FBR} can be found by setting the derivative of (4) to 0 and the optimal value of V_S to achieve the peak power is:

$$V_{S,opt} = \frac{V_{OC}}{2} - V_D \tag{5}$$

While V_S achieves its optimal value shown in (5), the peak extracted power by a FBR can be expressed as:

$$P_{FBR,max} = 4 f_P C_P (\frac{V_{OC}}{2} - V_D)^2 \tag{6}$$

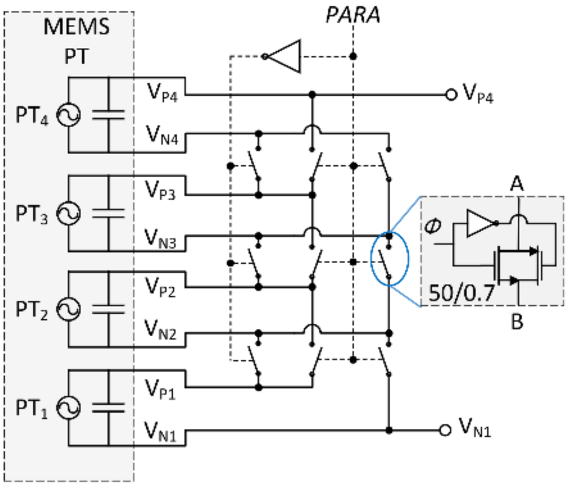


Fig. 8: Circuit diagram of the connection configuration block.

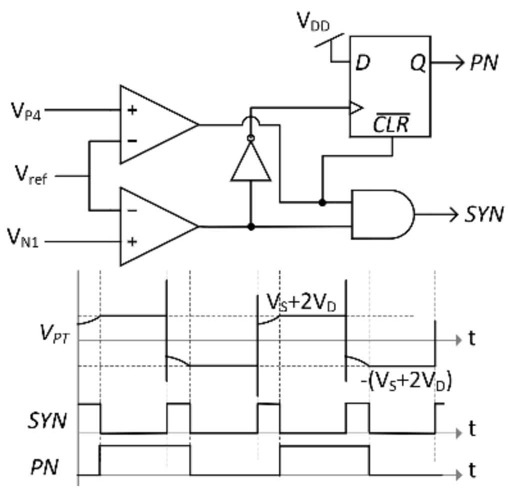


Fig. 9: Circuit diagram of the zero-crossing detection block.

The power expressed in (6) is the peak power while $V_S = V_{S,opt}$. While off-chip Schottky diodes are employed, the effective voltage drop V_D at the current level of I_P can be very low and V_D can be ignored in this case. However, on-chip Schottky diodes usually have higher V_D values and the voltage drop cannot be ignored for fully integrated systems.

The extracted power of a SSH (synchronized switch harvesting) rectifier will also be analyzed to show the improvement compared with the FBR. Fig. 6 shows the circuit diagram of a SSH rectifier and the associated waveforms. A SSH rectifier aims to synchronously flip the voltage V_{PT} every half period of I_P to minimize the charge wastage due to flipping V_{PT} with the generated charge by the PT. However, there is some voltage loss after voltage flip and it is shown as V_L in the waveform of V_{PT}. The loss ratio after voltage flip can be written as:

$$\eta_L = \frac{V_L}{V_S + 2V_D} \tag{7}$$

Some amount of charge generated by the PT is used to compensate the loss V_L; hence, the remaining charge transferred into C_S can be written as:

$$Q_{SSH} = Q_{tot} - V_L C_P = C_P(2V_{OC} - V_L) \tag{8}$$

Therefore, the extracted power stored in C_S can be expressed as:

$$P_{SSH} = \frac{V_S Q_{SSH}}{T/2} = 2f_P C_P V_S (2V_{OC} - V_L) \tag{9}$$

The above equation attains its maximum power while V_S satisfies:

$$V_{S,opt} = \frac{V_{OC}}{\eta_L} - V_D \tag{10}$$

The maximum output power of a SSH rectifier can then be written as:

$$P_{SSH,max} = 2\eta_L f_P C_P (\frac{V_{OC}}{\eta_L} - V_D)^2 \tag{11}$$

Comparing the peak power values for a FBR in (6) and a SSH rectifier in (11), the performance enhancement of a SSH rectifier can be expressed as:

$$\frac{P_{SSH,max}}{P_{FBR,max}} = \frac{2}{\eta_L}(\frac{V_{OC} - \eta_L V_D}{V_{OC} - 2V_D})^2 \tag{12}$$

The equation (12) is plotted in Fig. 7 with $V_D = 0.25$ V (on-chip diodes). The three lines represent values for three voltage flip loss ratios of $\eta_L = 0.3$, $\eta_L = 0.5$ and $\eta_L = 0.7$, which are approximately equal to measured values while enabling 8, 3 and 1 SCs, respectively, in the proposed SE-SSHC rectifier in Section IV. It can be seen that P_{SSH}/P_{FBR} is higher when loss ratio is lower (or flip efficiency is higher). If discrete Schottky diodes are employed, the voltage drop V_D can be ignored and the above becomes $2/\eta_L$. It can be seen that the performance enhancement of a SSH rectifier depends on the voltage flip efficiency (or loss ratio η_L) and the loss ratio can be decreased by employing larger inductors in SSHI rectifiers or employing more SCs in SSHC rectifiers.

III. Circuit Implementations

From the system architecture shown in Fig. 3, it can be seen that there are five main blocks in the proposed SE-SSHC interface circuit, which are the "connection configuration", "zero-crossing detection", "pulses generation", "pulses sequence" and "switch control" (including 8 on-chip configurable SCs) blocks. The detailed transistor-level circuit diagrams and operations for all the blocks are presented in the following sections.

A. Connection configuration

Fig. 8 shows the circuit diagram of the connection configuration block, which connects the four regions of the PT into the SE-SSHC rectification system. Since the four regions need to be connected in series during voltage flip moments, this block configures the connection of the PT according to the signal $PARA$. While $PARA$ is high, the four regions are electrically connected in parallel, otherwise, in series. During the series connection, the four regions should be connected

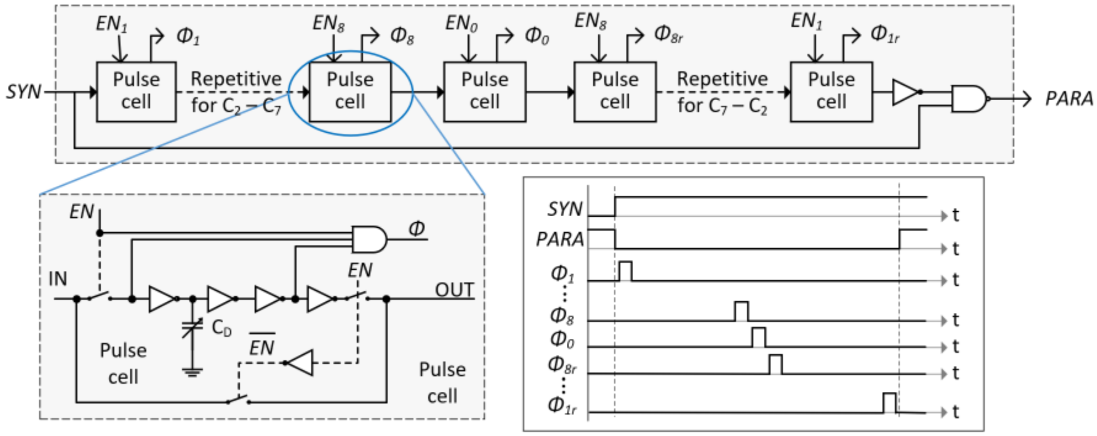


Fig. 10: Circuit diagram of the pulse generation block and associated waveforms.

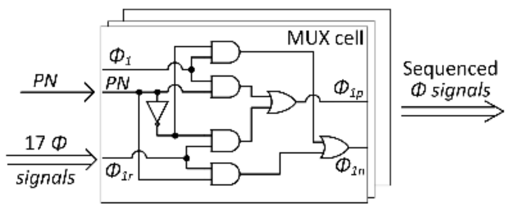


Fig. 11: Circuit diagram of the pulse sequencing block.

with consideration of voltage polarity of each region so that the series-connected model results in a summed-up voltage. Regardless of which connection configuration is chosen, nodes V_{P4} and V_{N1} are always connected to the system.

B. Zero-crossing detection

The circuit diagram and associated waveforms of the zero-crossing detection block is shown in Fig. 9. The voltage flip occurs while the current source generated from the PT is close to zero, which is also the moment when V_{PT} achieves its peak value, where $V_{PT} = V_{P4} - V_{N1}$. In order to find this moment, two continuous-time comparators are employed to compare V_{P4} and V_{N1} with a reference voltage V_{ref}. While V_{PT} achieves its peak and starts to rise or decrease, one of V_{P4} and V_{N1} is close to $-V_D$ and the other one is close to $V_S + V_D$. The reference voltage V_{ref} is set slightly higher than the negative value of the voltage drop of a diode ($-V_D$) so that one of the two comparators can be triggered when either V_{P4} or V_{N1} leaves $-V_D$ and starts to increase towards $V_S + V_D$. At this moment, a rising edge is generated in the signal SYN and it keeps high until the voltage V_{PT} is completed flipped. In this block, the signal PN is also generated to indicate the polarization of V_{PT} at the moment of the rising edge of SYN. This signal is used in following blocks to sequence up to 17 pulses according to the voltage flip direction, from $\pm(V_S + 2V_D)$ to $\mp(V_S + 2V_D)$.

C. Pulse generation and sequencing

Fig. 10 shows the circuit diagram and waveforms of the pulse generation block. In this implementation, the number of employed on-chip SCs in the SSHC rectifier is chosen at $k = 8$; hence, up to 17 $(2k+1)$ pulses should be generated to perform voltage flip. In this block, 17 pulse cells are employed to generate up to 17 non-overlapping sequential pulses. At each rising edge of the input signal SYN, the 17 pulse cells are sequentially driven to generate one individual pulse in each cell. The 8 on-chip SCs can be selectively enabled by eight input signals $EN_1 - EN_8$ and the pulse ϕ_0 is enabled by EN_0. While all of the 9 EN signals are low, the entire system simply works as a full-bridge rectifier (FBR) since all of the switches in the SSHC rectifier keep OFF. While only EN_0 is enabled, the system works as a switch-only rectifier, which has been presented in [6]. The input EN_0 is forced to high if any of $EN_1 - EN_8$ are high because the phase ϕ_0 is indispensable in a SSHC rectifier to clear the residual charge in C_P in the middle phase of the voltage flip process. Besides the up to 17 pulses, the signal $PARA$ keeps low during the entire voltage flip process to configure the four regions of the PT to a series connection. The circuit diagram of a pulse cell is also presented in the figure and it shows that one individual pulse is generated by ANDing the delayed and inverted version of the input signal. All of the 17 pulse cells are identical and the input of each cell is the output of the previous cell, except that the input of the first cell is SYN. The delay in one cell is performed using two weak inverters charging an on-chip capacitor, which can be adjusted to tune the pulsewidth of the generated pulse signal. The three switches in the pulse cell aim to enable and bypass the selected cells according to the EN signals.

Before the 17 pulses are used to drive the switches to perform voltage flip, they need to be sequenced according to the voltage flip directions, which is the signal PN. When PN is high, the voltage across the PT is positive and it needs to be flipped towards negative; hence, the sequence of the 17 pulses should be $\phi_{1p} \rightarrow \phi_{2p} \rightarrow \phi_{3p} \rightarrow \phi_{4p} \rightarrow \phi_{5p} \rightarrow \phi_{6p} \rightarrow \phi_{7p} \rightarrow \phi_{8p} \rightarrow \phi_0 \rightarrow \phi_{8n} \rightarrow \phi_{7n} \rightarrow \phi_{6n} \rightarrow \phi_{5n} \rightarrow \phi_{4n} \rightarrow \phi_{3n} \rightarrow \phi_{2n} \rightarrow \phi_{1n}$. The first 8 pulses aim to sequentially transfer charge from the PT to the 8 SCs, C_1 to C_8. The middle pulse ϕ_0 clears the residual charge in the PT and the following 8 pulses sequentially connect the 8 SCs in an opposite sense to

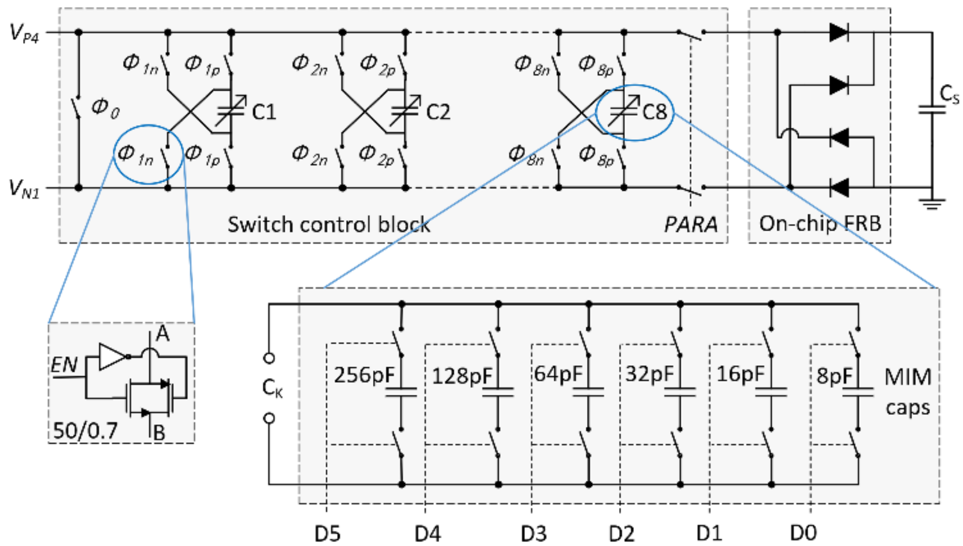


Fig. 12: Circuit diagram of the switch control block and on-chip switched capacitors.

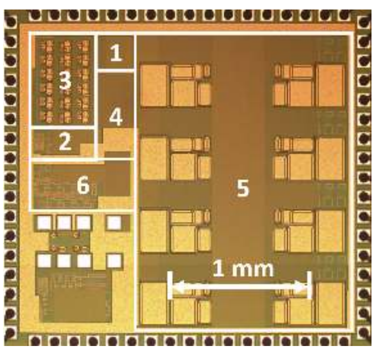


Fig. 13: Micrograph of the test chip fabricated in a $0.18\,\mu$m CMOS foundry process. The active area of the proposed SE-SSHC rectifier is around $3.9\,\mathrm{mm}^2$. 1, zero-crossing; 2, connection configuration; 3, pulses generation; 4, pulses sequence; 5, switch control; 6, on-chip FBR and voltage regulator.

flip the voltage V_{PT} towards negative. When PN is low, the voltage V_{PT} needs to flipped from negative to positive and the order of the 17 pulses should be completely reversed. Fig. 11 shows the circuit diagram of the pulse sequencing block, which consists of 9 identical MUX (multiplexer) cells. 8 MUX cells are for 16 pulses driving SCs from C_1 to C_8 and a redundant MUX cell is added for the pulse ϕ_0 to ensure that all pulses have the same delay to avoid overlapping.

D. Switch control and on-chip capacitor arrays

Fig. 12 shows the circuit diagram of the switch control block, which consists of 35 analog CMOS switches in total, including 1 switch for ϕ_0, 32 switches for the 8 SCs and 2 additional switches to disconnect the system from the FBR during voltage flip instant. The eight SCs, $C_1 - C_8$, are implemented on-chip with 8 dual-MIM capacitor arrays and their capacitance can be adjusted externally according to the capacitance of the PT, C_P. Since the electrode of the PT is split into 4 regions in this implementation, the resulting

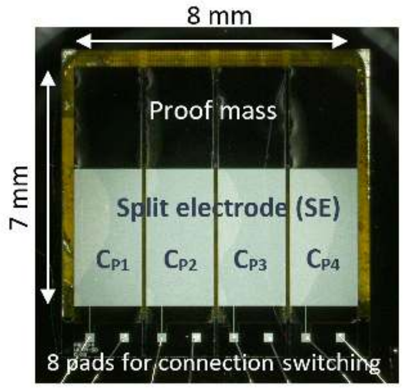
TABLE I: Power consumption breakdown.

Loss mechanism	Power loss	Percentage
Connection config	390 nW	15.1%
Zero-cross detection	221 nW	8.5%
Pulse generation	85 nW	3.3%
Pulse sequencing	0.4 nW	0.02%
Switch control	1470 nW	56.8%
Voltage regulator	423 nW	16.3%
Simulated total	2.59 µW	100%
Measured total	∼ 0.9 µW	(static)
Measured total	∼ 2.9 µW	(dynamic)

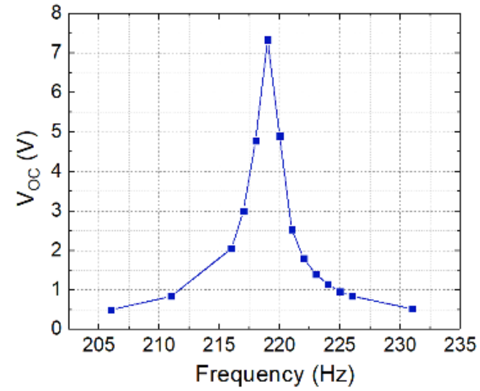
SC value should equal to $C_P/16$ for optimal voltage flip performance. In this work, the capacitor array for one SC can be set up to around $500\,\mathrm{pF}$; hence, the system can support PTs with C_P capacitance as high as $8\,\mathrm{nF}$, which include most MEMS (microelectromechanical systems) PTs and even some macroscopic PTs. Since the smallest capacitance of the SCs can be set to $8\,\mathrm{pF}$, which corresponds to $C_P = 64\,\mathrm{pF}$, the proposed system can also support most piezoelectric ultrasonic power receivers with C_P between 10's $-$ 100's pF. The density of the dual-MIM capacitor in this implementation is $4.1\,\mathrm{fF}/\mu\mathrm{m}^2$. Main parasitic factors in this block include the parasitic capacitance added into the capacitor array and the parasitic resistance of the switches. The former introduces additional capacitance in the capacitor array resulting in a value of capacitance greater than the expected value for an optimal voltage flip efficiency. The latter increases the time constant for charging and discharging the SCs. However, due to the small capacitance of SCs, thanks to the split-electrode design, and the low operating frequency (100's Hz), the switch resistance has little effect on the performance.

IV. Measurement results

The proposed SE-SSHC interface circuit was designed and fabricated in a $0.18\,\mu$m HV CMOS process. The die photo of

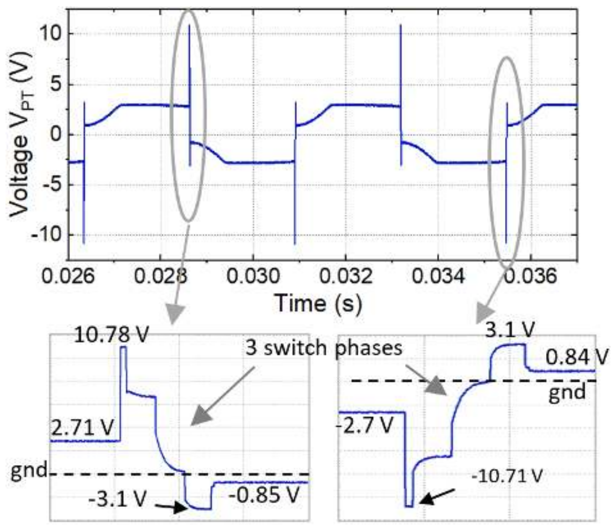


(a) PT fabricated in MEMS process by MEMSCAP.

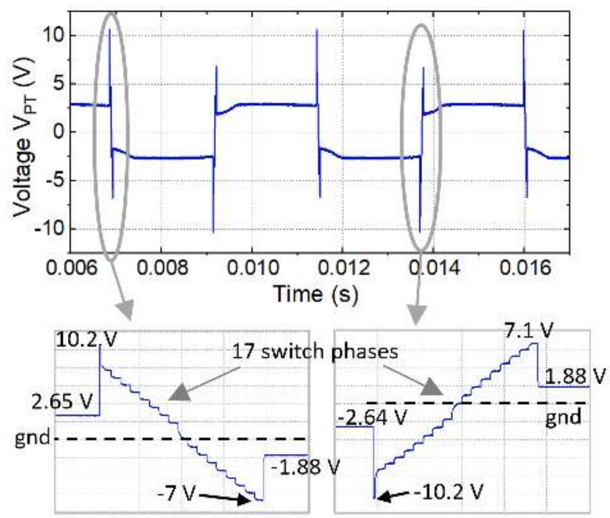


(b) Open-circuit voltage amplitude (V_{OC}) in frequency at acceleration level of $1.0\,\mathrm{g}$.

Fig. 14: Micrograph of the micro-fabricated piezoelectric transducer (PT) with its electrode split into four regions and its frequency response.



(a) 1 SC enabled.



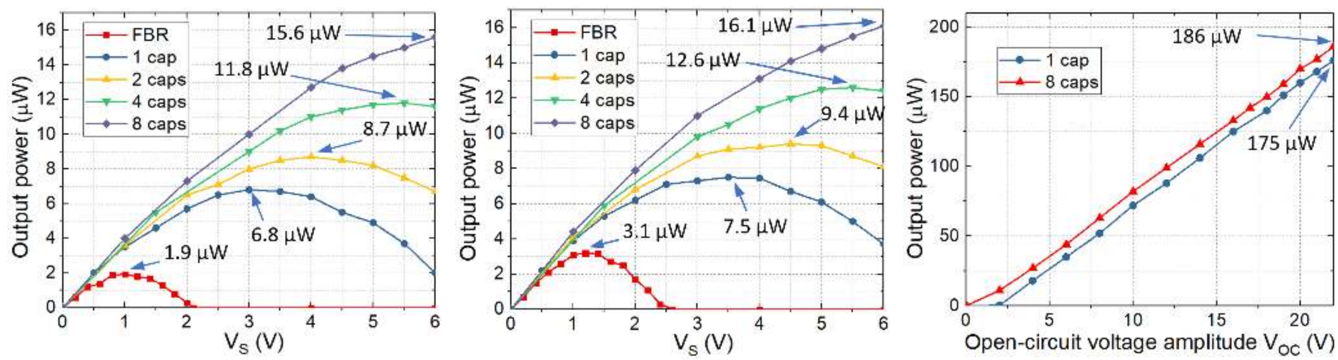
(b) 8 SCs enabled.

Fig. 15: Measured waveform of voltage V_{PT}.

the test chip is shown in Fig. 13. To meet the high-voltage requirement, an extra mask has been used in the $0.18\,\mu$m CMOS process to add high-voltage thick-oxide transistors.

In order to evaluate the proposed system, a MEMS PT with its electrode split into 4 regions was fabricated and the micrograph is shown in Fig. 14a. The PT was fabricated in a commercial MEMS foundry, MEMSCAP, using AlN as the piezoelectric material. Fig. 14b shows the open-circuit voltage amplitude (V_{OC}) by sweeping the excitation frequency around its natural frequency at a base acceleration level of $1.0\,\mathrm{g}$. The total capacitance with the 4 regions connected in parallel is measured to be $C_P = 1.94\,\mathrm{nF}$. The capacitance is reduced to $155\,\mathrm{pF}$ while the 4 regions are connected in series and this value is in the operational range of the on-chip SC arrays. Hence, the on-chip SC arrays should be configured to form an equivalent capacitor of around $155\,\mathrm{pF}$. To achieve this, the switches D4, D1 and D0 in Fig. 12 are ON while the other switches are kept OFF. This results in an equivalent capacitor of around $152\,\mathrm{pF}$. During the measurements with the proposed SE-SSHC rectifier, a shaker (LDS V406) was excited at the natural frequency of the MEMS PT at $219\,\mathrm{Hz}$ and driven by a sine wave from a function generator (Agilent 33250A) amplified by a power amplifier (LDS PA100E).

Fig. 15 shows the measured waveforms of the voltage across the PT, V_{PT}, while the number of enabled on-chip SCs are set to 1 and 8. It can be seen that there are spikes for voltage flip instants due to the increased V_{PT} voltage (increased by 4 times) due to the series connection of the four electrode regions. In Fig. 15a, only one SC in the proposed rectifier is enabled. The zoom-in voltage flip instants for V_{PT} flipped from positive to negative and from negative to positive are also shown in the two sub-figures. Before the voltage flip commences, the four regions are configured to a series connection and it can be observed that the voltage V_{PT} is increased by 4 times. Then the voltage flip commences and V_{PT} is flipped in three phases. Since there is only one SC enabled, three switch pulses are generated to perform the voltage flip. After the voltage is flipped, the four electrode



(a) (b) (c)

Fig. 16: Measured output power of a FBR and the proposed SE-SSHC rectifier with up to 8 on-chip SCs enabled. (a) Output power with on-chip diodes of $V_D \approx 0.25\,\text{V}$ while $V_{OC} = 2.5\,\text{V}$. (b) Output power with off-chip diodes of $V_D \approx 0.05\,\text{V}$ while $V_{OC} = 2.5\,\text{V}$. (c) Output power in a wide range of excitation levels (up to $V_{OC} = 22\,\text{V}$, equivalent to 3.4 g) with $V_S = 5\,\text{V}$.

TABLE II: Performance comparison with state-of-the-art interface circuits. [(a)]with on-chip diodes. [(b)]with off-chip diodes.

Reference	Technique	PT	Piezoelectric capacitance	Frequency	V_{OC}	Inductor	$\frac{P_{IC}}{P_{FBR}}$
JSSC2010 [6]	Bias-flip (SSHI)	Mide V22B	18 nF	225 Hz	2.4	820 µH	4
JSSC2012 [23]	PSCE	Mide V22B	19.5 nF	173 Hz	9 V	10 mH	2.1
JSSC2014 [24]	Energy-investing	Mide V22B	15 nF	143 Hz	2.6 V	330 µH	3.6
JSSC2014 [14]	SSHI	Custom MEMS	8.5 nF	155 Hz	8.2 V	470 µH	2.5
TPEL2016 [9]	SECE	Q220-A4303YB	52 nF	60 Hz	2.35 V	560 µH	3
ISSCC2016 [25]	SSHI	MIDE V21B	26 nF	134 Hz	2.45 V	3.3 mH	6.8
JSSC2017 [17]	FCR	Piezo P5A4E	0.08 nF	110 kHz	–	On-chip caps	4.8
This work	SE-SSHC	Custom MEMS	1.94 nF	219 Hz	2.5 V	On-chip caps	3.6 – 8.2[(a)] 2.4 – 5.2[(b)]

regions is configured back to a parallel connection. The results shows that the voltage flip efficiency is around 31%. The waveform while all the 8 SCs are enabled is shown in Fig. 15b and in this case, 17 pulses are needed to flip the voltage. The voltage flip efficiency in this case is measured to be around 71%.

Fig. 16 shows the measured output power transferred into the capacitor C_S connected at the output of the FBR. In Fig. 16a, the excitation level is fixed at a level such that the open-circuit zero-to-peak voltage is $V_{OC} = 2.5\,\text{V}$. The output voltage V_S is varied from $0\,\text{V}$ to $6\,\text{V}$ to show the maximum power points for all the cases. The voltage drop of the on-chip Schottky diodes forming the FBR is measured at around $V_D \approx 0.25\,\text{V}$. The output power values of a FBR and the proposed SE-SSHC rectifier with 1, 2, 4 and 8 SCs enabled are measured and plotted. When using the on-chip FBR, it can be seen that the peak output power extracted by a passive FBR is $1.9\,\mu\text{W}$. After the SE-SSHC rectifier is turned ON with one SC enabled, the peak power is increased to $6.8\,\mu\text{W}$ with $3.58\times$ performance enhancement. This is because the voltage V_{PT} is synchronously flipped and the flip efficiency is measured to be around 31%. While all the 8 on-chip SCs are enabled, the peak power achieves $15.6\,\mu\text{W}$ and the performance is enhanced by $8.2\times$ compared with the FBR. A FBR built of four off-chip Schottky diodes is also used during measurement, as shown in Fig. 16b, and the diode voltage drop in this case is measured at around $V_D \approx 0.05\,\text{V}$. Due to the lower voltage drop, the extracted power by a passive FBR is significantly increased. Although the power from the proposed SE-SSHC rectifier is increased as well, the performance improvement compared to the FBR is decreased due to the lower V_D. The peak power values marked in Fig. 16a and Fig. 16b correspond to specific V_S values. In order to achieve power at these optimal points, maximum power point tracking (MPPT) technique is required to dynamically adjust V_S according to input excitation levels [11], [26]. Fig. 16c shows the measured output power while the excitation level is varied from 0 g to 3.4 g, which is equivalent to V_{OC} voltage varying from 0 V to 22 V. The reason of not keeping increasing the excitation level is because this is the highest level that the MEMS PT can tolerate before fracture occurs. The measurement shows the highest possible power that the MEMS PT can provide and this value is measured to be $186\,\mu\mathrm{W}$ with the proposed SE-SSHC rectifier while 8 on-chip SCs are enabled.

Table II shows the performance comparisons between the proposed SE-SSHC rectifier and reported interface circuits for piezoelectric vibration energy harvesting. Among all the previously reported rectifiers, most of them require large inductors to perform voltage flip, which significantly increases the system size. Although [17] proposed a flipping-capacitor rectifier (FCR) achieving voltage flip with on-chip capacitors, this particular rectifier aims to work with PTs with extremely small C_P capacitance. The proposed SE-SSHC rectifier achieves high performance enhancement without using any inductors. In addition, thanks to the split-electrode (SE) design, the proposed rectifier can serve PTs with much larger C_P capacitance using small on-chip SC values to perform voltage flip.

V. Conclusion

This paper presents a SE-SSHC rectifier for piezoelectric energy harvesting which performs synchronous voltage flip using on-chip SCs. Compared with the conventional SSHC rectifier, the proposed circuit employs a PT with its electrode split into several regions and these regions are temporarily connected in series during voltage flip instants. With this topology, the effective capacitance of the PT is significantly decreased; hence, the required SCs for a SSHC rectifier are also significantly decreased such that they can be implemented on-chip. Compared with state-of-the-art rectifiers using inductors, the proposed circuit is fully integrated, which dramatically decreases the system volume, especially preferable for miniaturized energy harvesting systems. Compared with the recently reported FCR circuit, the proposed system can work with a wide variety of PTs with inherent capacitance values ranging from 10's pF to 1's nF.

References

[1] S. Du and A. A. Seshia, "A fully integrated split-electrode synchronized-switch-harvesting-on-capacitors (se-sshc) rectifier for piezoelectric energy harvesting with between 358enhancement," in *2018 IEEE International Solid - State Circuits Conference - (ISSCC)*, Conference Proceedings, pp. 152–154.

[2] G. Zhou, L. Huang, W. Li, and Z. Zhu, "Harvesting ambient environmental energy for wireless sensor networks: A survey," *Journal of Sensors*, vol. 2014, p. 20, 2014. [Online]. Available: http://dx.doi.org/10.1155/2014/815467

[3] P. D. Mitcheson, E. M. Yeatman, G. K. Rao, A. S. Holmes, and T. C. Green, "Energy harvesting from human and machine motion for wireless electronic devices," *Proceedings of the IEEE*, vol. 96, no. 9, pp. 1457–1486, 2008.

[4] A. Khaligh, Z. Peng, and Z. Cong, "Kinetic energy harvesting using piezoelectric and electromagnetic technologies - state of the art," *IEEE Transactions on Industrial Electronics*, vol. 57, no. 3, pp. 850–860, 2010.

[5] G. D. Szarka, B. H. Stark, and S. G. Burrow, "Review of power conditioning for kinetic energy harvesting systems," *Power Electronics, IEEE Transactions on*, vol. 27, no. 2, pp. 803–815, 2012.

[6] Y. K. Ramadass and A. P. Chandrakasan, "An efficient piezoelectric energy harvesting interface circuit using a bias-flip rectifier and shared inductor," *IEEE Journal of Solid-State Circuits*, vol. 45, no. 1, pp. 189–204, 2010.

[7] S. Du, Y. Jia, C. D. Do, and A. A. Seshia, "An efficient sshi interface with increased input range for piezoelectric energy harvesting under variable conditions," *IEEE Journal of Solid-State Circuits*, vol. 51, no. 11, pp. 2729–2742, 2016.

[8] P. Gasnier, J. Willemin, S. Boisseau, G. Despesse, C. Condemine, G. Gouvernet, and J. J. Chaillout, "An autonomous piezoelectric energy harvesting ic based on a synchronous multi-shot technique," *IEEE Journal of Solid-State Circuits*, vol. 49, no. 7, pp. 1561–1570, 2014.

[9] M. Dini, A. Romani, M. Filippi, and M. Tartagni, "A nanopower synchronous charge extractor ic for low-voltage piezoelectric energy harvesting with residual charge inversion," *IEEE Transactions on Power Electronics*, vol. 31, no. 2, pp. 1263–1274, 2016.

[10] H. Shen, H. Ji, J. Qiu, Y. Bian, and D. Liu, "Adaptive synchronized switch harvesting: A new piezoelectric energy harvesting scheme for wideband vibrations," *Sensors and Actuators A: Physical*, vol. 226, pp. 21–36, 2015.

[11] M. Shim, J. Kim, J. Jeong, S. Park, and C. Kim, "Self-powered 30uw to 10 mw piezoelectric energy harvesting system with 9.09 ms/v maximum power point tracking time," *IEEE Journal of Solid-State Circuits*, vol. 50, no. 10, pp. 2367–2379, 2015.

[12] G. Shi, Y. Xia, Y. Ye, L. Qian, and Q. Li, "An efficient self-powered synchronous electric charge extraction interface circuit for piezoelectric energy harvesting systems," *Journal of Intelligent Material Systems and Structures*, p. 1045389X15624796, 2016.

[13] S. Du, Y. Jia, and A. A. Seshia, "An efficient inductorless dynamically configured interface circuit for piezoelectric vibration energy harvesting," *IEEE Transactions on Power Electronics*, vol. 32, no. 5, pp. 3595–3609, 2017.

[14] E. E. Aktakka and K. Najafi, "A micro inertial energy harvesting platform with self-supplied power management circuit for autonomous wireless sensor nodes," *IEEE Journal of Solid-State Circuits*, vol. 49, no. 9, pp. 2017–2029, 2014.

[15] A. Romani, M. Filippi, and M. Tartagni, "Micropower design of a fully autonomous energy harvesting circuit for arrays of piezoelectric transducers," *Power Electronics, IEEE Transactions on*, vol. 29, no. 2, pp. 729–739, 2014.

[16] D. A. Sanchez, J. Leicht, F. Hagedorn, E. Jodka, E. Fazel, and Y. Manoli, "A parallel-sshi rectifier for piezoelectric energy harvesting of periodic and shock excitations," *IEEE Journal of Solid-State Circuits*, vol. 51, no. 12, pp. 2867–2879, 2016.

[17] Z. Chen, M. K. Law, P. I. Mak, W. H. Ki, and R. P. Martins, "Fully integrated inductor-less flipping-capacitor rectifier for piezoelectric energy harvesting," *IEEE Journal of Solid-State Circuits*, vol. 52, no. 12, pp. 3168–3180, 2017.

[18] S. Du and A. A. Seshia, "An inductorless bias-flip rectifier for piezoelectric energy harvesting," *IEEE Journal of Solid-State Circuits*, vol. 52, no. 10, pp. 2746–2757, 2017.

[19] Y. Yang and L. Tang, "Equivalent circuit modeling of piezoelectric energy harvesters," *Journal of Intelligent Material Systems and Structures*, 2009.

[20] S. Du, G. A. J. Amaratunga, and A. A. Seshia, "A cold-startup sshi rectifier for piezoelectric energy harvesters with increased open-circuit voltage," *IEEE Transactions on Power Electronics*, pp. 1–1, 2018.

[21] L. Wu, X. D. Do, S. G. Lee, and D. S. Ha, "A self-powered and optimal sshi circuit integrated with an active rectifier for piezoelectric energy harvesting," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 64, no. 3, pp. 537–549, 2017.

[22] S. Du, Y. Jia, C. Zhao, G. A. J. Amaratunga, and A. A. Seshia, "A passive design scheme to increase the rectified power of piezoelectric energy harvesters," *IEEE Transactions on Industrial Electronics*, vol. 65, no. 9, pp. 7095–7105, 2018.

[23] T. Hehn, F. Hagedorn, D. Maurath, D. Marinkovic, I. Kuehne, A. Frey, and Y. Manoli, "A fully autonomous integrated interface circuit for piezoelectric harvesters," *IEEE Journal of Solid-State Circuits*, vol. 47, no. 9, pp. 2185–2198, 2012.

[24] D. Kwon and G. A. Rincon-Mora, "A single-inductor 0.35 um cmos energy-investing piezoelectric harvester," *IEEE Journal of Solid-State Circuits*, vol. 49, no. 10, pp. 2277–2291, 2014.

[25] D. A. Sanchez, J. Leicht, E. Jodka, E. Fazel, and Y. Manoli, "A 4uw-to-1mw parallel-sshi rectifier for piezoelectric energy harvesting of periodic and shock excitations with inductor sharing, cold start-up and up to 681extraction improvement," in *2016 IEEE International Solid-State Circuits Conference (ISSCC)*, Conference Proceedings, pp. 366–367.

[26] N. Kong and D. S. Ha, "Low-power design of a self-powered piezoelectric energy harvesting system with maximum power point tracking," *Power Electronics, IEEE Transactions on*, vol. 27, no. 5, pp. 2298–2308, 2012.

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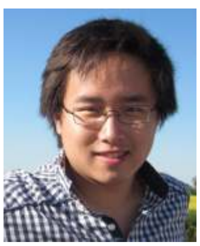

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