A FULLY SYMMETRICAL SENSE AMPLIFIER FOR NON-VOLATILE MEMORIES

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ABSTRACT

This paper presents a fully symmetrical sense amplifier topology for advanced non-volatile memories. The proposed structure ensures zero systematic offset, together with adequate rejection of disturbs coming from capacitive coupling with noisy substrate, power supply, and ground. The presented topology has been designed for phase change memories, however, it is also suitable for use in other non-volatile storage devices such as magnetic RAMs and Flash memories. Experimental results on sensing time, offset, and sensitivity demonstrated the effectiveness of the proposed scheme.

1. INTRODUCTION

In recent years, more and more research efforts are being devoted in the area of semiconductor non-volatile storage technology, due the fact that charge storage devices such as Flash memories are approaching technology limits. In particular, new kinds of memory cells, where the storage element can be modelled as a variable resistor, have been developed. These include magnetic RAMs (MRAMs) and phase change memories (PCMs). In these cases, the information stored in any cell is the difference in resistance between two different programmed states.

In MRAM cells [1], a binary state change is achieved by switching the magnetization of high-sensitive spin material. Pulsed currents of different values allow the transition between parallel and antiparallel spin states, which correspond to different electrical resistivity.

In phase change, or Ovonic Unified Memory (OUM), technology [2], [3], the storage device is made of a thin film of chalcogenide alloy, that changes between amorphous and polycrystalline phase when thermally stimulated. The phase conversion of any storage element is obtained by appropriately heating (through electrical pulses) and then cooling a small, and thermally isolated portion of the material.

In the above memories, reading basically consists in measuring the resistance of the addressed storage device. To this end, a predetermined voltage is forced across the storage element of the selected cell, and the ensuing current flow is sensed. In practice, the cell current is compared to a reference current provided by an identical cell programmed to a suitable resistance value. To obtain the best sense accuracy, the reference cell is located within the memory array and is identically biased. This choice minimizes boundary effects and allows thermal tracking between the reference and the array cells.

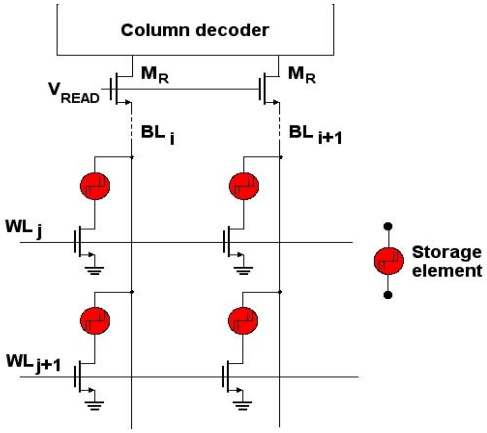

Fig. 1 – Detail of a PCM memory array.

To be more specific, in the following, we will refer to the case of PCM technology, although all concepts are also valid for other kinds of non-volatile storage devices such as MRAMs and Flash memories. Fig. 1 depicts a detail of a PCM memory array including four memory cells together with the associated selection transistors (in this Figure, MOS selection devices are assumed, although substrate bipolar transistors can also be used). In read operations, an adequate voltage V_{READ} is applied to the gate of cascode device M_R (which operates in saturation), thereby forcing the required sense voltage across the addressed storage element.

A key point to reduce reprogramming time is to perform SET (low impedance, logic 1) and RESET (high impedance, logic 0) operations without resorting to program&verify and erase&verify techniques [4, 5]. However, this approach results in larger distributions for SET and RESET states. It is therefore apparent that very accurate sensing circuits are needed. In addition, PCM

technology seems to be very promising also for multilevel storage applications [6], in which high sensing accuracy is a vital requirement as a consequence of the reduced spacing between adjacent programmed states.
In this paper, a sense amplifier designed for PCM technology is presented. A fully symmetrical topology is adopted, so as to avoid any systematic mismatch between the reference and the array input branch, thereby minimizing offset. The sense amplifier has been integrated in a 4 Mb (2048 rows × 2048 columns) PCM test-chip and experimentally evaluated.

2. CIRCUIT DESCRIPTION

Many current-mode sense amplifiers for non-volatile memories have been presented in the literature. Solutions proposed in [7], [8] are inspired by the popular configuration shown in Fig. 2 [9]. In this figure, for simplicity, reference and cell currents are represented with ideal current generators (I_{ref} and I_{cell}, respectively).

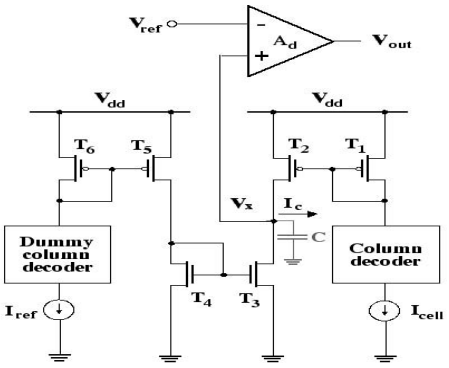

Fig. 2 – Conventional sense amplifier configuration.

The difference between the addressed-cell and the reference current, $I_c = I_{cell} - I_{ref}$, is integrated onto parasitic capacitor C, thus giving rise to a voltage which is compared to a reference voltage V_{ref} by a voltage comparator A_d.
The above structure is affected by a systematic offset due to its asymmetry. In particular, during a read operation, the current I_c fed to the integrating capacitor is equal to

$$I_c = \gamma_1 I_{cell} - -_2 I_{ref} \quad (1)$$

where γ_1 and γ_2 are given by:

$$\gamma_1 = \frac{1 + \lambda_p \Delta V_{DS,sat2}}{1 + \Delta_p \Delta V_{DS,sat1}} \quad (2)$$

$$\Delta_2 = \frac{1 + \Delta_p \Delta V_{DS,sat5}}{1 + \Delta_p \Delta V_{DS,sat6}} \frac{1 + \Delta_n \Delta V_{DS,sat3}}{1 + \Delta_n \Delta V_{DS,sat4}} \quad (3)$$

In the above equations, λ_n and λ_p are the NMOS and the PMOS channel length modulation parameter, respectively, and $\Delta V_{DS,sati} = V_{DSi} - V_{Dsat}$, V_{DSi} and V_{Dsat} being the drain-to-source voltage of transistor T_i and the drain-to-source saturation voltage. Even when I_{cell} and I_{ref} are identical, Δ_1 and Δ_2 are different, thus leading to systematic current offset, which adversely affects sensing accuracy. For instance, with a supply voltage V_{dd} = 3 V, assuming a conventional fabrication technology with threshold voltages equal to 0.8 V and $\Delta_n \approx \Delta_p$ on the order of 0.02 V^{-1}, from (2) and (3), we obtain a current offset of about $0.035 I_{cell}$, which can be critical in several applications (in the above calculation, the drain voltage of devices T_2 and T_3, V_x, was assumed at midrange).
Furthermore, since the impedances at the comparator input terminals are different, disturbs coming from sources such as capacitive coupling with noisy substrate, V_{dd}, or ground may limit sense accuracy.
A final disadvantage of the above topology is the risk of kickback effects [10] on the reference voltage V_{ref} when a large number of sense amplifiers are active simultaneously, as occurs in the case of high read parallelism.
The above drawbacks are overcome by using the sense amplifier topology shown in Fig. 3. All PMOS transistors, as well as all NMOS transistors, have the same aspect ratio, respectively. In this way, all mirror factors are set to unit. Capacitors C_M and C_R represent the parasitic capacitances associated to the input nodes of the voltage comparator A_d, hereinafter referred to as *matside* and *refside*, respectively. Ideally, C_M and C_R integrate the current differences $I_{cell} - I_{ref}$ and $I_{rel} - I_{celf}$, respectively.

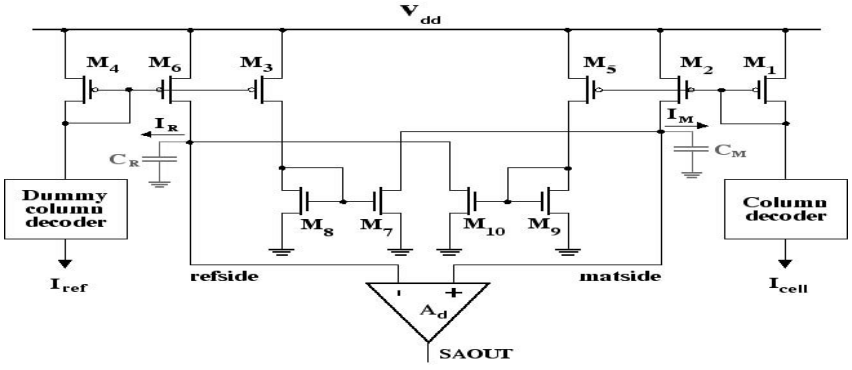

Fig. 3 – Circuit diagram of the proposed sense amplifier.

The ensuing voltages are fed to the negative and the positive input terminal of the comparator, which therefore detects the cell contents. In particular, the comparator output *SAOUT* is driven to 1 when $I_{cell} > I_{ref}$ (SET cell), while it is forced to 0 when $I_{cell} < I_{ref}$ (RESET cell).

To ensure a more symmetrical behaviour, the comparator input nodes are equalized before any sensing operation. Equalization is achieved by means of the circuit in Fig. 4 (signal *EQ* active high). The equalization level is set to V_{READ} so as to avoid the need for generating an additional stable voltage.

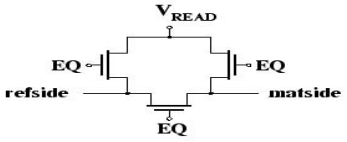

Fig. 4 – Equalization circuit.

To speed-up sensing, when a read operation is requested, bit-lines are precharged (with a conventional circuit, not shown in Fig. 3). When precharge and equalization are over, the sensing operation starts, and the reference and the addressed cell currents give rise to two opposite-polarity voltage ramps, which are fed to the inverting and the non-inverting input, respectively, of the comparator A_d. The latter is implemented by a single-ended differential amplifier (its design was carried out so as to minimize offset contributions).

Even though the proposed sense amplifier requires a larger area than the conventional one (Fig. 2), the array efficiency is negligibly affected. Indeed, in a non-volatile memory chip, the area occupation of the sense amplifiers is very small as compared to that of the memory array, since the sense amplifier count is equal to the sense parallelism. It should also be pointed out that, although the proposed scheme includes two input branches, a differential signal is provided at the comparator input. Hence, in order to obtain the same sensing time, the current consumption is substantially the same with respect to the structure in Fig. 2.

3. SYSTEMATIC-MISMATCH ANALYSIS

When current mirror mismatches are taken into account, the values of the current differences I_M and I_R turn out to be:

$$I_M = \alpha_{M1} I_{cell} - - _{R2} I_{ref} \quad (4)$$

$$I_R = - _{R1} I_{ref} - - _{M2} I_{cell} \quad (5)$$

where α_{M1} and α_{R1} are the current mismatches introduced by current mirrors $M_1 - M_2$ and $M_4 - M_6$, respectively, and α_{M2} and α_{R2} are the current mismatches due to the pair of current mirrors $M_1 - M_5$, $M_9 - M_{10}$ and $M_4 - M_3$, $M_8 - M_7$ also respectively.

The difference between currents I_M and I_R, which acts as the effective current signal that produces the input signal of the comparator, can therefore be expressed as follows:

$$I_M - I_R = K_1 I_{cell} - K_2 I_{ref} \quad (6)$$

where $K_1 = \alpha_{M1} + \alpha_{M2}$ and $K_2 = \alpha_{R1} + \alpha_{R2}$.

If we assume, for simplicity, that no random mismatch is present and consider only systematic mismatch contributions, a straightforward analysis leads to the following expressions of K_1 and K_2:

$$K_1 = \frac{\left(1 + \lambda_p \Delta V_{DS,sat2}\right)\left(1 + \Delta_n \Delta V_{DS,sat9}\right) + \left(1 + \Delta_p \Delta V_{DS,sat5}\right)\left(1 + \Delta_n \Delta V_{DS,sat10}\right)}{\left(1 + \Delta_p \Delta V_{DS,sat1}\right)\left(1 + \Delta_n \Delta V_{DS,sat9}\right)} \quad (7)$$

$$K_2 = \frac{\left(1 + \Delta_p \Delta V_{DS,sat6}\right)\left(1 + \Delta_n \Delta V_{DS,sat8}\right) + \left(1 + \Delta_p \Delta V_{DS,sat3}\right)\left(1 + \Delta_n \Delta V_{DS,sat7}\right)}{\left(1 + \Delta_p \Delta V_{DS,sat4}\right)\left(1 + \Delta_n \Delta V_{DS,sat8}\right)} \quad (8)$$

In the absence of any process mismatch, all PMOS and all NMOS transistors have the same channel length modulation parameter, respectively. In addition, when I_{ref} is equal to I_{cell}, the drain-to-source voltages of corresponding devices are identical and, hence, $K_1 = K_2$. Therefore, no systematic current offset is present, which leads to zero systematic voltage offset at the comparator input. It is worth to underline that the absence of any systematic offset enables the designer to use a reduced channel length for the current mirror devices, which results in higher operating speed.

It should also be pointed out that, thanks to the perfect symmetry of the proposed topology, the inverting and the non-inverting input of the comparator are driven with identical impedance. Any disturb coming from sources such as capacitive coupling with noisy substrate, V_{dd}, or ground, is treated as a common-mode signal and is therefore rejected.

4. EXPERIMENTAL RESULTS

The proposed sense amplifier was integrated in a 4-Mb PCM test-chip, fabricated in single-poly, single-well, double-metal, 0.35-µm (0.18-µm in the memory array), p-substrate CMOS process. Fig. 5 shows a microphotograph of a portion of the integrated test-chip, in which one sense amplifier has been highlighted.

Several measurements were carried out to evaluate sense amplifier speed, offset, and sensitivity performance.

In our test-chip, a nominal supply voltage V_{cc} of 1.8 V is used for the control logic and most of the peripheral circuit, including the comparators A_d in the sense amplifiers. However, from Figures 1 and 3, it is apparent that the current mirror section of the sense amplifier needs a higher supply voltage in order to guarantee adequate voltage room to the common-gate device, the column decoder, and the diode-connected transistor above the bit-line voltage (≈ 0.6 V). An on-chip regulated charge pump provides the power supply V_{dd} to the sense amplifiers as well as to other circuits in the test-chip. As the latter require a supply voltage of 3.6 V, V_{dd} was set to this value. It should be pointed out that speed, offset, and sensitivity performances of the current mirror section are not substantially affected by the value of this supply. V_{READ} was set to 1.24 V, as natural devices (nominal threshold voltage = 0.45 V) were used as common-gate transistors in the scheme in Fig. 1.

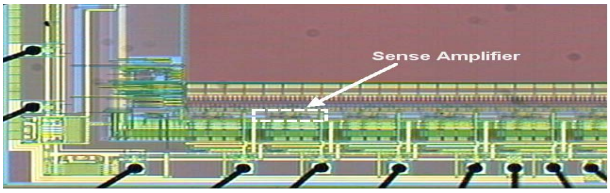

Fig. 5 – Microphotograph of a portion of the integrated test-chip.

Sensing time was evaluated by comparing the current flowing through a cell programmed to the SET state (I_{cell} = 40 µA) and the current (I_{ref} = 30 µA) generated by the reference cell. Fig. 6 shows the experimental transient waveforms. Since $I_{cell} > I_{ref}$, the voltage at node *matside* increases, while the voltage at node *refside* decreases, thereby giving rise to a high logic level at the comparator output *SAOUT*. During the equalisation phase, the voltage comparator circuitry forces *SAOUT* to ground. To prevent any risk of glitches at *SAOUT*, the comparator is enabled about 6 ns after equalization is over by means of a dedicated control signal (not shown in Fig. 3). Sensing time, which corresponds to the delay from the falling edge of *EQ* to the rising edge of *SAOUT*, is within 10 ns, which is on the same order as the sensing time of conventional non-latched sense amplifiers for non-volatile memories. High voltage swing (from ground to V_{dd}) was provided to signal *EQ* so as to speed-up equalization. To this end, conventional voltage elevators [11] were used.

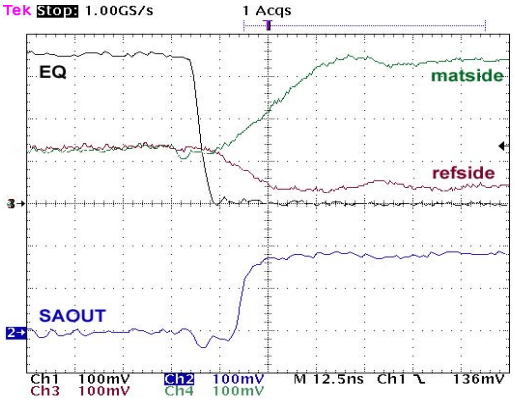

Fig. 6 – Measured voltage waveforms at nodes *matside*, *refside*, *EQ*, and *SAOUT* (active probes, attenuation by a factor of 10).

The test-chip also includes a current generator controlled by an external voltage (program accuracy 0.1 µA), which was used as the current reference for offset and sensitivity measurement. Table 1 summarizes the experimental results of offset and sensitivity on seven samples (I_{cell} = 40 µA).

	Sample						
	1	**2**	**3**	**4**	**5**	**6**	**7**
Offset [µA]	0.2	-0.1	0	0	0.2	0	-0.2
Sensitivity [µA]	0.9	0.7	0.6	0.65	0.7	0.5	0.85

Tab. 1 – Measured offset and sensitivity of seven samples.

The average offset is 0.014 µA, with a standard deviation of 0.135 µA, whereas the average sensitivity value is 0.7 µA, with a worst-case value of 0.9 µA. The offset voltage in samples 1, 2, 5, and 7 is ascribed to random mismatch effects (neglected in the analysis of Section 3) in the current mirrors and in the voltage comparator.

5. CONCLUSIONS

In this paper, a fully symmetrical sense amplifier topology has been presented. This structure prevents any systematic mismatches between the reference and the array input branch. The proposed architecture has been integrated in a PCM 4 Mb test-chip. Experimental results showed that the proposed architecture is able to work with adequate speed (10 ns), very reduced offset, and high sensitivity (better than 1 µA). Although the presented topology has been developed for PCM technology, it is also suitable for use in other non-volatile storage devices such as MRAMs and Flash memories.

6. ACKNOWLEDGMENTS

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7. REFERENCES

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