A General Approach to Synthesis and Analysis of Quasi-Resonant Converters

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Abstract—A method for systematic synthesis of quasi-resonant (QR) topologies by addition of resonant elements to a parent PWM converter network is proposed. It is found that there are six QR classes with two resonant elements, including two novel classes. More complex QR converters can be generated by a recursive application of the synthesis method. Topological definitions of all known and novel QR classes follow directly from the synthesis method and topological properties of PWM parents. The synthesis of QR converters is augmented by a study of possible switch realizations and operating modes. In particular, it is demonstrated that a controllable rectifier can be used to accomplish the constant-frequency control in all QR classes. Links between the QR converters and the underlying PWM networks are extended to general dc and small-signal ac models, in which the model of the PWM parent is explicitly exposed. Results of steady-state analyses of selected QR classes and operating modes include boundaries of operating regions, dc characteristics, a comparison of switching transitions and switch stresses, and a discussion of relevant design trade-offs.

I. INTRODUCTION

RECENTLY, resonant power converters have attracted much attention because of their ability to operate efficiently at higher switching frequencies than more conventional PWM (square-wave) converter topologies. Assuming that the efficiency can be maintained while increasing the operating frequency, proportionally lower values of energy-storage elements yield smaller and lighter power converters. This was the main motivation behind the introduction of converter topologies with resonant switches, also known as zero-current-switching (ZC) and zero-voltage-switching (ZV) quasi-resonant [1]–[3]. Many variations of the quasi-resonant converters were discussed in [4]. A generalization of the resonant switches [5] resulted in the discovery of two more classes named zero-voltage and zero-current quasi-square-wave in [6]. Classes of multi-resonant converters with more complex resonant networks were introduced in [7].

Common to all these converter topologies is that they are derived from PWM converters by adding resonant elements in order to shape the switch voltage and current waveforms. Instead of simultaneous abrupt transitions in the switch voltage and current, the newly introduced converters exhibit smooth, quasi-sinusoidal waveforms. The switch current (or the switch voltage) is zero before and immediately after the switching transi-

tion so that the switching losses associated with the transitions are greatly reduced.

The astonishing variety of the recently introduced converter topologies, for which we adopt a common name—quasi-resonant (QR), poses an apparent problem of how to comprehend, analyze, compare, select and finally design QR converters. Much needed analytical results and modeling methods started to appear in parallel with the introduction of novel converter topologies. In particular, an analysis method that provides unified dc and small-signal ac models for the entire classes of ZC and ZV converters was suggested in [8]. A remarkable aspect of the unifying analysis method is that it relates the properties of quasi-resonant converters to well-known properties of underlying PWM converters.

The main purpose of this paper is to provide a method for systematic synthesis and topological characterization of QR converters and to extend the unifying analysis method to all QR classes. The definition of QR converters in Section II provides a framework for the systematic synthesis described in Section III. The topological characterization that follows from the synthesis method is used together with the unifying analysis method in the derivation of a general dc model in Section IV and a general ac model in Section V. dc analyses of selected QR classes and operating modes are presented in Section VI, and a comparison of QR topologies is undertaken in Section VII. Main results are summarized in Section VIII.

II. QUASI-RESONANT CONVERTERS

As pointed out in the introductory section, various classes of quasi-resonant converters were introduced by modifications of PWM converters. This provides a starting point for our discussion:

Definition 1: If resonant elements (capacitors and inductors) are added to a PWM converter such that its network at dc is not altered, the resulting network is a quasi-resonant converter. By the network at dc, we mean the converter network in which all inductors are shorted and all capacitors are removed, while the sources, loads and switches are retained.

The PWM converter in Definition 1 has a single source V_g, load R, a number of capacitors, a number of inductors and two single-pole, single-throw switches. A more rigorous definition of the PWM network can be found in [9]. It is assumed that steady-state capacitor voltages and inductor currents are dc quantities with a relatively small superimposed ac ripple. We also assume that all elements are ideal and that converters are 100% efficient.

III. SYNTHESIS OF QUASI-RESONANT CONVERTERS

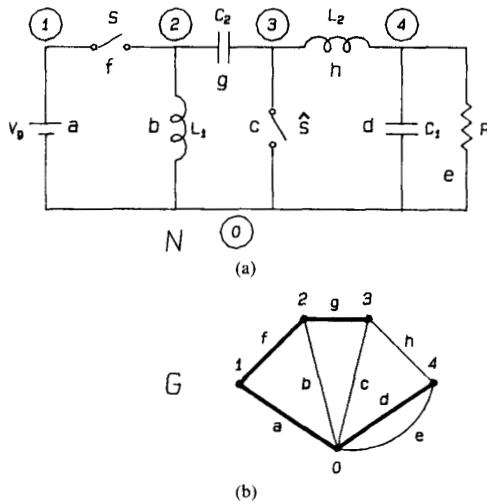Consider, as an example, the inverse Sepic PWM converter in Fig. 1(a). We assume that the converter operates in the con-

Fig. 1. PWM converter (a) and graph G for converter network N (b). Elements of tree $\mathfrak{I}_s$ are highlighted.

Fig. 2. Examples of four possible ways to add extra edge (i) to graph G of Fig. 1(b).

tinuous conduction mode—when the S-switch is on, the $\hat{S}$-switch is off and vice versa. If D is the duty ratio of the S-switch, $M(D) = D/(1 - D)$ is the dc conversion ratio of the converter in Fig. 1(a).

The graph G of the converter network N is shown in Fig. 1(b). One possible tree ($\mathfrak{I}_s$) for the graph G consists of edges that correspond to V_g, C_1, C_2, and S. The tree-elements (branches) (a, d, f, g) are highlighted in Fig. 1(b). The co-tree elements (chords) are the edges (b, c, e, h) that correspond to L_1, $\hat{S}$, R, and L_2, respectively.

Suppose that a graph G^+ is constructed by adding an extra edge (i) to the graph G. Examples of four possible ways to add an edge are shown in Fig. 2. In cases (a) and (b), in which the added edge forms a cut-set or a loop by itself, the resulting graph G^+ is separable and the network N^+ is completely equivalent to the original network N. Cases (c) and (d) represent nontrivial modifications of the original network. In case (c), the edge (i) is added between two nodes of the graph G. Note that the tree $\mathfrak{I}_s$ is also a tree for the graph G^+, while the added edge belongs to the co-tree of G^+. In case (d), a node of the original graph (node 2 in the example of Fig. 2(d)) is split into two nodes (2' and 2"). Edges incident to the node are also split so that some of them (b, f) are incident to the node 2', while the remaining edge (g) is incident to the node 2". Finally, the edge (i) is added between the nodes 2' and 2". In this case, elements of the original tree $\mathfrak{I}_s$ and the added edge form a tree for the resulting graph G^+.

In general, the two distinct positions of the added edge can be summarized as follows. Construct a graph G^+ by adding an edge to a given graph G.

A) If the edge is added between two existing nodes of the graph G, then every tree for the graph G is a tree for the graph G^+ and the added edge is a chord;

B) If a node of G is split into two nodes and the edge is added between them, then every tree for the graph G together with the added edge is a tree for the graph G^+.

If the added element is in the A-position, it must form a loop (the fundamental loop) with branches for any tree of the graph G. For example, in Fig. 2(c), the added edge (i) forms the
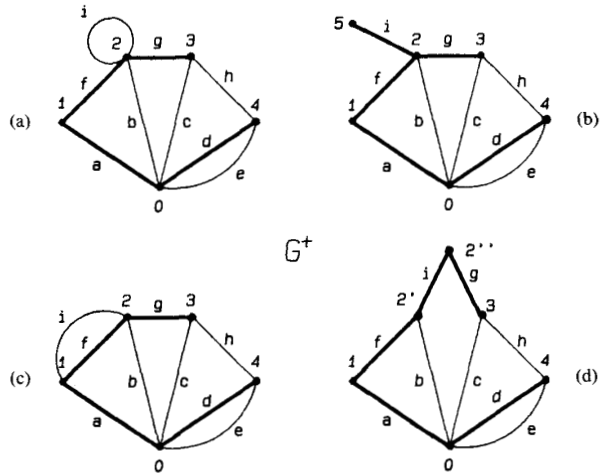
fundamental loop with the branch (f). If the added element is in the B-position, it forms a cut-set (the fundamental cut-set) with chords of the original network. For example, in Fig. 2(d), the added edge (i) forms the fundamental cut-set with chords (c) and (h).

To construct a QR converter, we start with a parent PWM converter network N and examine the A- and the B-positions of added resonant elements. We cannot proceed, however, without being able to identify trees of the PWM network in terms of PWM elements: source V_g, load R, capacitors, inductors and the two switches—S and $\hat{S}$. Property 1 of [9] gives a necessary topological characterization of PWM converters:

Property 1: For a PWM converter represented by its graph G.

• Voltage source V_g, capacitors and the switch S form a tree. This tree is denoted by $\mathfrak{I}_s$;

• Voltage source V_g, capacitors and the switch $\hat{S}$ form a tree. This tree is denoted by $\hat{\mathfrak{I}}_s$.

Now, positions of resonant elements can be examined with respect to the trees $\mathfrak{I}_s$ and $\hat{\mathfrak{I}}_s$.

A. Synthesis of QR Converters with Two Resonant Elements

At least two resonant elements—a resonant capacitor (C_r) and a resonant inductor (L_r)—must be added to a PWM converter network in order to construct a quasi-resonant converter.

Suppose that the resonant capacitor is added in the A-position. The condition that $N^+ = N$ at dc is always fulfilled. Then, since the resonant capacitor is a chord with respect to the trees $\mathfrak{I}_s$ and $\hat{\mathfrak{I}}_s$, it forms the fundamental loop with branches—a combination of capacitors, source V_g, and a switch (S or $\hat{S}$). Therefore, there are three possibilities, which are detailed next.

The resonant capacitor C_r forms a loop with the following:

1) a non-empty set of PWM capacitors;

2) (C/S): the switch S and a possibly empty set of PWM capacitors;

3) ($C/\hat{S}$): the switch $\hat{S}$ and a possibly empty set of PWM capacitors.

Here, the term PWM capacitors denotes the capacitors in the PWM network together with the input voltage source V_g. In case 1, the added capacitor C_r cannot affect the waveforms in

the PWM converter. The remaining two A-positions are the ClS position and the $Cl\hat{S}$ position. The notation indicates that the resonant element is a capacitor (C) and that it is in a loop (l) with a switch (S or $\hat{S}$). From Property 1, it follows that cases 2 and 3 are equivalent. The distinction between the positions ClS and $Cl\hat{S}$ becomes important only after the second resonant element is added.

In the inverse Sepic converter, for example, the resonant element can be added between any two nodes, so that there are 10 possible A-positions. Four of them (nodes 0-1, 0-4, 1-4, 2-3) are excluded because they belong to case 1, while the remaining positions (nodes 0-2, 0-3, 1-2, 1-3, 2-4, 3-4) belong to cases 2 and 3.

Suppose that the resonant capacitor is added in the B-position. Then, the resonant capacitor is a branch and it forms a cut-set with chords for the tree $\mathfrak{I}_s$ or $\hat{\mathfrak{I}}_s$. In contrast to the A-positions, however, the condition that $N^+ = N$ at dc may not be satisfied for every B-position of the resonant capacitor. In fact, this condition can be satisfied only if the resonant capacitor and a non-empty set of PWM capacitors (and no other elements) form a cut-set in G^+. Therefore, eligible B-positions are the following:

The resonant capacitor C_r forms a cut-set with a non-empty set of PWM capacitors and a cut-set with the following:

1) a non-empty set of PWM inductors and (possibly) load R;
2) load R, a switch (S or $\hat{S}$), and a possibly empty set of PWM inductors;
3) (CcS): the switch S and a non-empty set of PWM inductors;
4) ($Cc\hat{S}$): the switch $\hat{S}$ and a non-empty set of PWM inductors.

In case 1, the insertion of C_r does not affect waveforms in the PWM converter because the PWM inductors and the load R carry dc currents only. Case 2 implies that the voltage across the resonant capacitor contributes to the output voltage, which contradicts the basic requirement that the output voltage ripple is small. The remaining two B-positions are CcS and $Cc\hat{S}$, where c stands for cut-set.

In the example of the inverse Sepic converter, there are only two eligible B-positions of the resonant capacitor—in series with one of the two capacitors—C_1 or C_2. The position in series with C_1 is excluded because it belongs to case 1, so that the only valid B-position is in series with the PWM capacitor C_2. In most cases, the position CcS or the position $Cc\hat{S}$ will imply that the resonant capacitor is placed in series with a single capacitor in the PWM network. Then, inserting the resonant capacitor is equivalent to reducing the value of the PWM capacitor.

An analysis analogous to the one completed for possible positions of the resonant capacitor could be carried out for the resonant inductor as well. Instead, we arrive at possible positions of the resonant inductor by duality:

The resonant inductor L_r can be in the following:

1) (LcS, $Lc\hat{S}$): a cut-set with a switch (S or $\hat{S}$) and a possibly empty set of PWM inductors;
2) (LlS, $Ll\hat{S}$): a loop with a non-empty set of PWM inductors, and in a loop with a switch (S or $\hat{S}$) and a non-empty set of PWM capacitors.

Following the adopted notation, the two B-positions are denoted by LcS and $Lc\hat{S}$, while the two A-positions are denoted by LlS and $Ll\hat{S}$.

Four positions of the resonant capacitor and four positions of the resonant inductor can be combined in up to 16 ways. After non-feasible and redundant combinations are eliminated, we ar-

		LcS	$Lc\hat{S}$	LlS	$Ll\hat{S}$
ClS		×	ZV	ZV-QSW	
$Cl\hat{S}$		ZC	×		
CcS		ZC-QSW		×	Q_n-PWM
$Cc\hat{S}$				Q_f-PWM	×

Fig. 3. Complete set of QR classes with two resonant elements.

rive at the complete set of distinct classes of QR converters with two resonant elements. Topological definitions for the three pairs of dual classes follow from Fig. 3.

Zero-current (ZC) [1], zero-voltage (ZV) [3], zero-current quasi-square-wave (ZC-QSW) and zero-voltage quasi-square-wave (ZV-QSW) [5] are known QR classes. Proper topological definitions were given only for the ZC and ZV classes in [8]. Here, in addition to topological definitions and systematic classification of all known QR classes, two new QR classes named on-resonant and off-resonant quasi-PWM (Q_n-PWM and Q_f-PWM) are uncovered and pointed out in Fig. 3.

The circuit examples shown in Fig. 4, are derived from the inverse Sepic PWM converter. They illustrate loops and cut-sets in the topological definitions of QR converters with two resonant elements. The two Q-PWM converters have exactly the same topology as the parent PWM converter. This is a result of the fact that the PWM capacitor in series with the resonant capacitor and the PWM inductor in parallel with the resonant inductor are simply absorbed. It is interesting to note that a Q-PWM converter can also be viewed as a PWM converter operating simultaneously in the discontinuous inductor current mode (DICM) and a discontinuous capacitor voltage mode (DCVM) [13]. In the same manner, QSW converters can be considered as PWM converters operating in DICM or in DCVM to which a single resonant element is added. In the sense of this interpretation, only ZV and ZC converters would represent true quasi-resonant converters with two resonant elements.

B. Topological Variations

For a given QR class, positions of L_r and C_r within a PWM converter are not unique. However, switch voltage and current waveforms, as well as dc characteristics, are the same for all topological variations. The number of topological variations is largest in the ZC and ZV classes because the requirement that $N^+ = N$ at dc imposes no restrictions on positions of the resonant elements. The number of variations is smallest in the two Q-PWM classes. For example, the two inverse Sepic Q-PWM converters in Fig. 4(e)-(f) are unique. Resonant elements can also be distributed through various positions encompassed by the topological definitions without affecting conversion properties and switch waveforms.

C. Degenerate QR Classes with Two Resonant Elements

In the preceding discussion, positions of the two resonant elements were examined with respect to the trees of the PWM par-
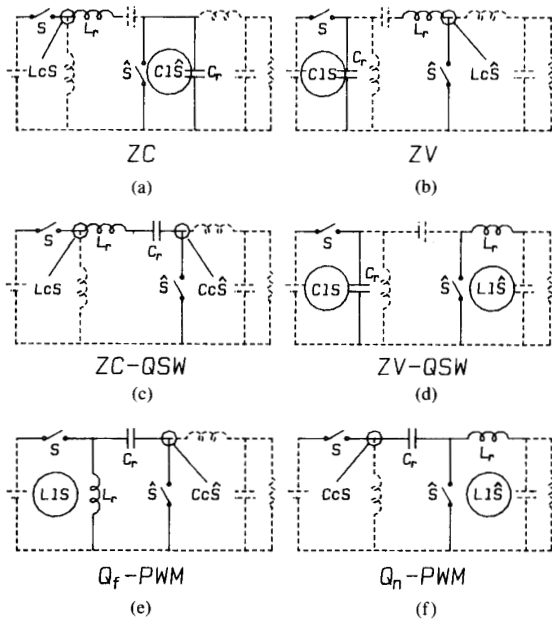
ZC
(a)

ZV
(b)

ZC-QSW
(c)

ZV-QSW
(d)

Q_f-PWM
(e)

Q_n-PWM
(f)

Fig. 4. Examples of QR converters derived from inverse Sepic converter.

(a)

(b)

Fig. 5. Examples of ClL (a) and LcC (b) QR converters.

ent network. However, in the process of adding the resonant elements, the parent network for the second resonant element is changed—the original tree or the original co-tree is augmented by the first resonant element.

Suppose that the resonant inductor is first added in the B-position (LcS or $Lc\hat{S}$). Then, in addition to ClS and $Cl\hat{S}$, there exists another A-position for the resonant capacitor.

(ClL): C_r is in a loop with the resonant inductor L_r and a possibly empty set of PWM capacitors. An example of the inverse Sepic converter with resonant elements added in the ClL position is shown in Fig. 5(a).

Similarly, if the resonant capacitor is first added in the A-position (ClS or $Cl\hat{S}$), one more B-position for the resonant inductor is possible, in addition to LcS and $Lc\hat{S}$.

(LcC): L_r is in a cut-set with the resonant capacitor C_r and a possibly empty set of PWM inductors.

An example of the inverse Sepic LcC-converters is shown in Fig. 5(b). Apparently, the dual positions ClL and LcC define yet another pair of QR networks. It can be shown that no operating modes with zero-voltage/zero-current transitions are feasible in these two degenerate QR classes unless both S and $\hat{S}$ are active (controllable) switches. Then, the ClL-class is of the zero-voltage type while the LcC-class is of the zero-current type.

D. Synthesis of More Complex QR Converters

Classes of QR converters with more than two resonant elements can be constructed recursively, by adding a single resonant element to a previously defined QR network. Again, for the additional resonant element, the A-position and the B-position can be examined with respect to the known trees $\mathfrak{I}_s^+$ and $\hat{\mathfrak{I}}_s^+$ of the parent QR converter.

Take, as an example, the ZV class and add a new resonant capacitor C_{r1}. The tree $\mathfrak{I}_s^+$ (or $\hat{\mathfrak{I}}_s^+$) for the parent ZV network contains the S-switch (or the $\hat{S}$-switch), PWM capacitors and
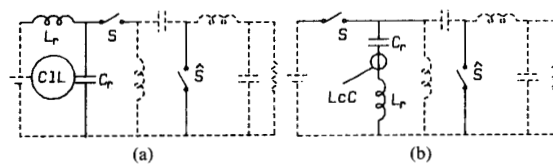
the resonant inductor L_r, while the corresponding co-tree contains the $\hat{S}$-switch (or the S-switch), PWM inductors, load R, and the resonant capacitor C_r. Therefore, possible A-positions of the resonant capacitor C_{r1} are ClS and ClL, while possible B-positions are CcS and $Cc\hat{S}$.

In general, simplicity of the converter network is beneficial from the standpoints of efficiency, size, weight and cost trade-offs. Also, analysis and consequently design of more complex QR converters are inevitably more involved. Thus, introduction and utilization of more complex resonant networks must be well motivated and justified.

Among QR converters defined from the ZV parent class, it is easy to recognize that the ClS position of the additional resonant capacitor C_{r1} defines the class of zero-voltage multi-resonant converters [7]. The more complex resonant network in the ZV-MR converters is justified by the fact that all major circuit parasitics can be absorbed by the resonant elements.

E. Switch Realizations

Operating modes and properties of QR converters can be substantially different for different realizations of the switches, as evident from the examples of the half-wave and the full-wave modes of ZC and ZV converters [8]. Possible realizations of the two switches in a quasi-resonant converter are summarized in Fig. 6.

In addition to the conventional realization (one controllable switch, one rectifier diode), both switches can be controllable. The technique of synchronous rectification in which controllable switches are used as rectifiers is proposed for PWM converters primarily as a means of reducing the rectifier conduction losses. In classes of QR converters, however, a controllable rectifier also yields a number of novel operating modes and, most importantly, the possibility of constant-frequency control [12].

A total of five distinct combinations can be inferred from the diagram of possible switch realizations:

CD: current-bidirectional + diode;
VD: voltage-bidirectional + diode;
CC: current-bidirectional + current-bidirectional;
VV: voltage-bidirectional + voltage-bidirectional;
CV: current-bidirectional + voltage-bidirectional.

F. Operating States and Operating Modes

For every possible position of the switches, a switched-mode converter reduces a linear, time-variant network or, as we shall say from now on, the converter is in one of its operating states. Then, an operating mode can be defined as a periodic sequence of operating states. It is convenient to denote the operating states of a converter by the position (on = 1, off = 0) of the two switches—S and $\hat{S}$. For example, the continuous conduction mode of PWM converters can be represented by a periodic se-
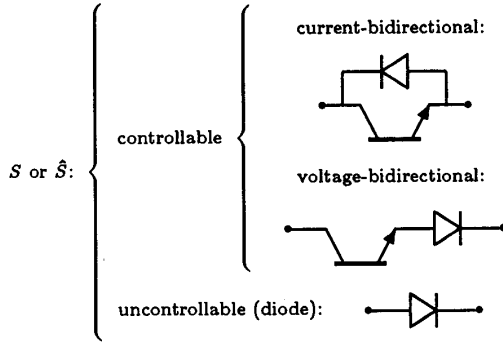
Fig. 6. Realizations of two switches in quasi-resonant converters.

Fig. 7. DC model of PWM parent (a) and DC model of quasi-resonant converter (b).

quence of two operating states:

$$\cdots \rightarrow \boxed{1\text{-}0} \rightarrow \boxed{0\text{-}1} \rightarrow \cdots . \tag{1}$$

In the (1-0)-state, the S-switch is on, and the $\hat{S}$-switch is off. At the transition from the (1-0)-state to the (0-1) state, both switches change their positions. In addition to the states (1-0) and (0-1), two more states are possible: the state when both switches are on, and the state when both switches are off. For a given QR topology and a given switch realization, the periodic sequence of operating states is not unique and many operating modes exist. Thus, in contrast to PWM converters where most of the operating characteristics can be deduced from the topology alone, a study of possible operating modes is necessary .in order to fully characterize various QR topologies. Among numerous possible operating modes, of most practical interest are those with all lossless (zero-voltage or zero-current) switching transitions.

IV. A GENERAL DC MODEL

A unifying analysis method that links properties of a QR converter to properties of its PWM parent was devised in [8], where it was applied to the ZC and ZV classes. The purpose of this section is to show how the same analysis method is applicable whenever the network of a PWM-derived converter is the same as the network of the PWM parent at dc, and to derive a general dc model for QR converters.

The dc model of the PWM parent converter is shown in Fig. 7(a). The dc conversion ratio $\mathfrak{M}$ is

$$\mathfrak{M} \equiv \frac{V_{out}}{V_g} = M(D), \tag{2}$$

where D is the duty ratio of the S-switch and $M(D)$ is the well-known conversion-ratio function. For example, $M(D) = D$ for the buck converter, $1/(1 - D)$ for the boost converter, $D/(1 - D)$ for the buck-boost, Ćuk, Sepic converters, etc. In general, the dc model of the PWM parent follows from the state-space averaging method [10].

In [8] it was shown that the two switches, S and $\hat{S}$, form a loop with a non-empty set of PWM capacitors and a cut-set with a non-empty set of PWM inductors in every PWM converter. One may also note that both conclusions follow immediately from Property 1. Thus, the environment for the two switches in a PWM converter is shown in Fig. 8. The sum of all voltages in the loop with the switches is denoted by v_{off}, while the sum of all currents in the cut-set with the switches is denoted by i_{on}.

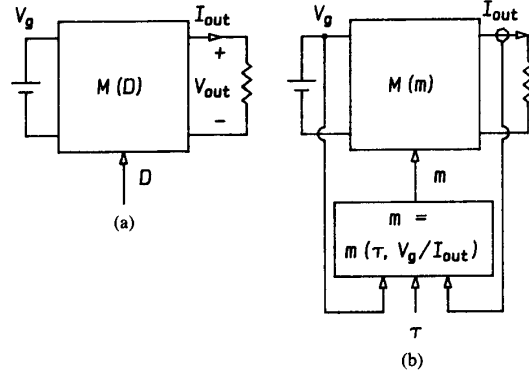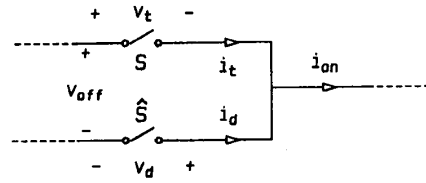Fig. 8. Environment for switches in PWM converter.

For example, in the inverse Sepic converter of Fig. 1(a), S, $\hat{S}$, V_g, and C_2 form a loop, while S, $\hat{S}$, and L_1, and L_2 form a cut-set, so that

$$v_{off} = V_g + V_{C2}, \quad i_{on} = I_{L1} + I_{L2}. \tag{3}$$

Reference orientations for voltages and currents are chosen so that averages of v_{off} and i_{on} are always positive quantities. Under the small-ripple assumption, v_{off} and i_{on} are essentially dc quantities.

Suppose that the PWM parent is used to derive a quasi-resonant converter. Since the dc networks are the same, for the average (dc) values of voltages and currents in Fig. 8, one can write

$$\bar{v}_t + \bar{v}_d = \bar{v}_{off} \equiv V_{off}, \tag{4}$$

and

$$\bar{i}_t + \bar{i}_d = \bar{i}_{on} \equiv I_{on}. \tag{5}$$

Here, v_{off} and i_{on} need not be dc quantities. In fact, it can be shown that the resonant capacitor in the $C c S$ position or in the $C c \hat{S}$ position contributes to v_{off}, while the resonant inductor in the $L l S$ position or in the $L l \hat{S}$ position contributes to i_{on}. Therefore, in a QR converter, v_{off} or i_{on} or both waveforms can exhibit substantial variations over a single switching cycle.

The assumption that there are no losses in the converter yield

$$\bar{v}_t \bar{i}_t = \bar{v}_d \bar{i}_d. \tag{6}$$

Define the equivalent duty ratio m by

$$m \equiv \frac{\bar{v}_d}{V_{off}} = \frac{\bar{i}_t}{I_{on}}. \tag{7}$$

From (4)-(6), it is easy to verify that the two expressions for m are equivalent. In a PWM converter the equivalent duty ratio m reduces to the duty ratio D of the s-switch.

The dc conversion ratio $\mathfrak{M}$ of the quasi-resonant converter becomes

$$\mathfrak{M} = M(m), \tag{8}$$

where $M(\cdot)$ is the function inherited from the parent PWM converter. This result is not immediately useful because the equivalent duty ratio m is not known. In general, m is a function of some control variable (τ) for a given operating mode and the ratio $V_{\text{off}}/I_{\text{on}}$,

$$m = m\left(\tau, \frac{V_{\text{off}}}{I_{\text{on}}}\right). \tag{9}$$

However, since

$$\frac{V_{\text{off}}}{I_{\text{on}}} = \frac{V_g}{I_{\text{out}}} = \frac{R}{\mathfrak{M}}, \tag{10}$$

for every PWM parent [9], the equivalent duty ratio can be expressed as a function of the converter external quantities:

$$m = m\left(\tau, \frac{V_g}{I_{\text{out}}}\right). \tag{11}$$

Depending on the switch realization and the operating mode, the control variable τ can be any function of controllable time intervals. With the exception of the two Q-PWM classes, in QR classes with the conventional switch realizations (CD or VD), the only controllable interval is the switching period, so that the control variable τ is the switching frequency.

A general dc model of the quasi-resonant converter is shown in Fig. 7(b). In the dc model of the PWM parent, the duty ratio D is simply replaced by the equivalent duty ratio m. Thus, once m is determined for a given class and a given operating mode, the dc conversion ratio $\mathfrak{M}$ follows from (8) for any particular PWM parent and topological variation.

Normalization is usually introduced in analyses of resonant converters so that obtained results are not referred to particular values of resonant elements. Define the resonant frequency f_r and the characteristic impedance R_o by

$$f_r \equiv \frac{w_r}{2\pi} \equiv \frac{1}{2\pi\sqrt{L_r C_r}}, \quad R_o \equiv \sqrt{\frac{L_r}{C_r}}. \tag{12}$$

Switching frequency f_s is normalized to the resonant frequency f_r, and time is normalized to $1/w_r$:

$$f \equiv \frac{f_s}{f_r}, \quad \theta \equiv w_r t. \tag{13}$$

Voltages are normalized to V_{off}, while currents are normalized to V_{off}/R_o. In particular, δ denotes the average of the current i_{on} normalized to V_{off}/R_o or, equivalently, the output current normalized to V_g/R_o:

$$\delta \equiv \frac{I_{\text{on}} R_o}{V_{\text{off}}} = \frac{I_{\text{out}} R_o}{V_g}. \tag{14}$$

Thus, the equivalent duty ratio can be found as a function of control and load variables, $m = m(\tau, \delta)$.

V. A GENERAL AC MODEL

For PWM converters, the method of state-space averaging (SSA) yields the well-known small-signal averaged model shown as a box in Fig. 9(a). Using the dc model of Fig. 7(b)
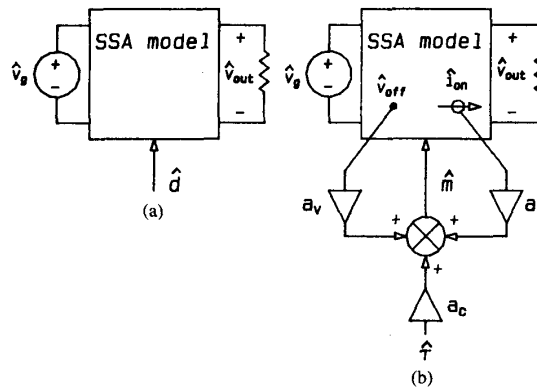

Fig. 9. State-space averaged (SSA) model of PWM parent (a) and averaged model of quasi-resonant converter (b).

as a starting point, the usual averaging and linearization steps yield an averaged small-signal model of quasi-resonant converters shown in Fig. 9(b). The state-space averaged model of the power stage, obtained as if the converter operated in the PWM continuous conduction mode, is embedded in the ac model. The steady-state duty ratio D, which appears as a parameter of the SSA model for PWM converters, is replaced by the steady-state equivalent duty ratio m. Two feedback loops are added around the SSA model—a voltage feedback from $\hat{v}_{\text{off}}$ to $\hat{m}$, with gain a_v, and a current feedback from $\hat{i}_{\text{on}}$ to $\hat{m}$, with gain a_i. The coefficients a_c, a_i, and a_v in

$$\hat{m} = a_c \hat{\tau} + a_i \hat{i}_{\text{on}} + a_v \hat{v}_{\text{off}}, \tag{15}$$

are computed as partial derivatives,

$$a_c \equiv \frac{\partial m}{\partial \tau}, \tag{16}$$

$$a_i \equiv \frac{\partial m}{\partial i_{\text{on}}} = \frac{\partial m}{\partial \delta} \frac{R_o}{V_{\text{off}}}, \tag{17}$$

$$a_v \equiv \frac{\partial m}{\partial v_{\text{off}}} = -a_i \frac{I_{\text{out}}}{V_g}, \tag{18}$$

evaluated at the steady-state operating point. For many QR classes and operating modes the steady state characteristics $m = m(\tau, \delta)$ cannot be obtained in a closed form. Thus, the partial derivatives in (16) and (17) have to be determined numerically. Nevertheless, since the coefficients are the same for all parent PWM topologies, they can be computed once and used from look-up tables or normalized plots. The model equivalent to the model of Fig. 9(b) was experimentally verified for the ZV and ZC classes in [8]. Computation of the feedback coefficients and experimental verification of the model for other QR classes and other operating modes remains to be done.

VI. DC ANALYSIS OF SELECTED QR CLASSES AND OPERATING MODES

In this section we consider only selected classes of QR converters: ZV, ZV-QSW, Q_n-PWM and ZV-MR, switch realizations CD and CC, and operating modes in which all switching transitions are at zero voltage or at zero current. The selection is focused on cases that are more promising with respect to the reduction of switching losses; zero-voltage switching is more favorable than zero-current switching; also, zero-voltage

QR Class	State Equations		
ZV	$\frac{dv_t}{d\theta} = \delta - i_t - i_d$ $\frac{di_d}{d\theta} = v_t + v_d - 1$.		
ZV-QSW	$\frac{dv_d}{d\theta} = i_t + i_d - i_{on}$ $\frac{di_{on}}{d\theta} = v_d - m$ $v_t + v_d = 1$	**State**	**Conditions**
		0-0	$i_t = i_d = 0$
		0-1	$i_t = v_d = 0$
Qn-PWM	$\frac{dv_{off}}{d\theta} = m\delta - i_t$ $\frac{di_{on}}{d\theta} = v_d - m$ $v_{off} = v_t + v_d$ $i_{on} = i_t + i_d$	1-0	$v_t = i_d = 0$
		1-1	$v_t = v_d = 0$
ZV-MR	$\frac{dv_t}{d\theta} = i_r - i_t$ $x\frac{dv_d}{d\theta} = i_r + i_d - \delta$ $\frac{di_r}{d\theta} = 1 - v_t - v_d$		

Fig. 10. State equations for four classes of QR converters together with constraints imposed by switches in each operating state.

switching of a voltage-bidirectional switch is not feasible because the diode in series with the transistor prevents the resonant discharge of the transistor junction capacitance.

A. Operating States and State Equations

A steady-state analysis of a QR class starts with a description of up to four possible operating states. The standard simplifying assumptions are that the converter is lossless and that PWM inductors and PWM capacitors can be taken as ideal current and voltage sources, respectively. Thus, the order of the state description is at most equal to the number of added resonant elements. Equations for the four selected classes are shown in Fig. 10, together with the constraints imposed by the positions of the switches in each operating state. The notation for switch voltages and currents is as shown in Fig. 8. For multi-resonant converters, an additional parameter is the ratio of the two resonant capacitors: C_r in the loop with the S-switch and C_{r1} in the loop with the $\hat{S}$-switch,

$$x \equiv \frac{C_{r1}}{C_r}. \tag{19}$$

From Fig. 10, state trajectories with arbitrary initial conditions can be found in a straightforward manner. It is worth noting that the state equations are written without reference to any particular PWM parent or any particular topological variation. This is a direct consequence of the topological definitions and properties derived by the synthesis method.

B. Operating Modes

Most interesting operating modes in which all transitions occur at zero voltage or at zero current are summarized in Fig. 11. Modes are denoted by Roman numbers with subscripts representing the switch realization.

QR Class	Modes	Sequence of Operating States
ZV	I_{CD}	0-0 → 0-1 → 1-1 → 1-0
	II_{CC}	1-1 → 0-1 → 1-1 → 1-0
ZV-QSW	$I_{CD,CC}$	0-0 → 1-0 → 0-0 → 0-1
Qn-PWM	I_{CD}	1-0 → 1-1 → 0-1 → 0-0
ZV-MR	$I_{CD,CC}$	1-1 → 1-0 → 0-0 → 0-1
	$II_{CD,CC}$	1-1 → 1-0 → 0-0 → 1-0
	$III_{CD,CC}$	1-1 → 0-1 → 0-0 → 0-1
	IV_{CC}	1-1 → 0-1 → 1-1 → 1-0

Fig. 11. Operating modes of selected QR classes.

For a given converter topology, state trajectories and the sequence of operating states are sufficient for a qualitative understanding of the circuit operation. Qualitative descriptions of the modes in Fig. 11 can be found elsewhere: mode I_{CD} of ZV converters is well known as the half-wave mode [3]; mode I_{CD} of ZV-QSW converters is described in [6], while ZV-MR converters in CD modes are described in [7]; various CC modes are studied in [12]; finally, mode I_{CD} of Q_n-PWM converters is discussed in [13].

Experimental QR buck converters are shown in Fig. 12. Waveforms recorded in various operating modes are shown in Fig. 13. Transistor control signal p_t and p_d illustrate the control strategies for various modes. ZV, ZV-QSW, and ZV-MR converters in CD modes are controlled by varying the switching frequency, while the off-time of the S-switch's transistor is constant. The Q_n-PWM converter is controlled just as PWM converters—by varying the duty ratio of the S-switch. In CC modes, the control variable is the control duty ratio D_c, defined as the interval between two controllable transitions relative to the switching period. Thus, in the ZV converter operating in mode II_{CC}, $D_c T$ is the interval between the $\hat{S}$-switch turn-on and the S-switch turn-off. In ZV-QSW and ZV-MR converters, $D_c T$ is the interval between the $\hat{S}$-switch turn-off and the S-switch turn-off.

C. Equivalent Duty Ratio

The computation of the equivalent duty ratio as a function of the appropriate control variable and the normalized load δ requires two steps:

1) A steady-state solution for state trajectories is found by equating initial conditions at the beginning of a switching cycle to the conditions at the end of a switching cycle.

2) Once the steady-state solution is found for the switch waveform, the equivalent duty ratio is determined by definition in (7).

Unfortunately, in most cases, it is not possible to find a closed-form solution for $m(\tau, \delta)$. Details of the computation for various operating modes can be found in [11].

D. Operating Regions and DC Characteristics

For a given operating modes, the operating region is a portion of the normalized load-to-output plane (m-versus-δ plane) in which a steady-state solution for state trajectories can be found.
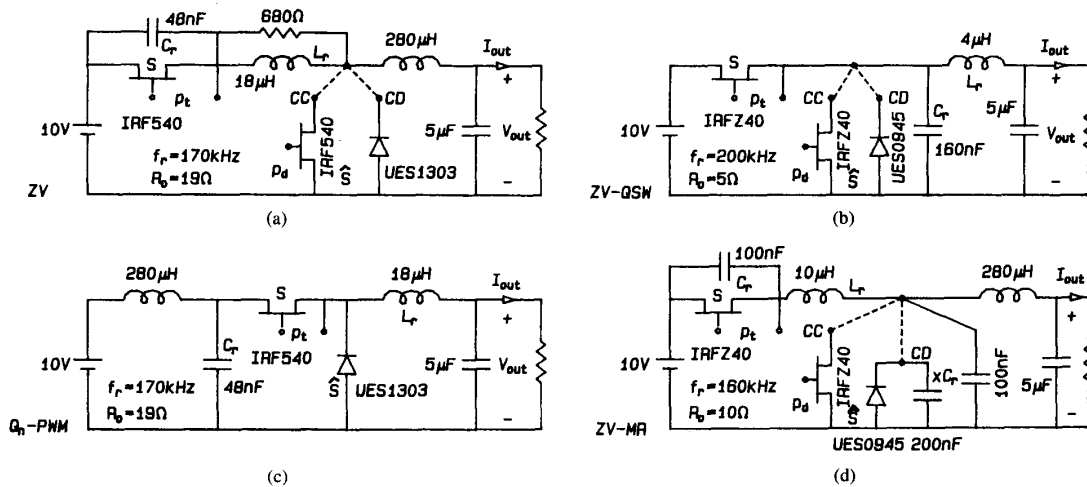
Fig. 12. Experimental QR buck converters.

The operating regions (dotted areas) for the classes and modes under study are shown in Fig. 14. Modes I, II, and III of ZV-MR converters are combined because the control strategy is uniform and because DC characteristics are continuous over the mode boundaries. For all constant-frequency modes, normalized frequency f is a varying parameter.

Zero-voltage switching of conventional ZV converters is lost if the output current is lower than V_g/R_o. This well-known result is shown in Fig. 14(a)—in the load direction, the operating region is bounded from below by the curve $\delta = 1$. Another known result is that the range of attainable conversion ratios is restricted for ZV-QSW converters operating in mode I_{CD} [6]. Indeed, from Fig. 9(c), it follows that the equivalent duty ratios in the range ($0 < m < 0.5$) are not accessible.

Boundaries of the operating regions are of prime design concern. For a given QR converter (given PWM parent, class, operating mode, R_o and f_r), any given set of design specifications (the range of input voltages, the range of output voltages and the range of load currents) can be translated into the normalized load-to-output plane and compared to the corresponding available operating region of Fig. 14. Conversely, plots in Fig. 14 can be used to select parameters R_o, f_r, and consequently values of resonant elements, so that the required range of voltages and load currents fits into the available operating region.

DC characteristics in the normalized load-to-output plane are shown in Fig. 15.

VII. A COMPARISON OF QR CONVERTERS

The existence of numerous QR classes and operating modes poses a problem of how to select and design a converter best suited for a given application. This section is aimed toward better understanding of relative merits of selected QR topologies and related design trade-offs.

A. Switching Transitions and Sensitivity to Circuit Parasitics

The major motivation behind introduction of QR converters is the reduction in switching losses associated with switching transitions and parasitic elements in the converter circuit. A summary of the types of switching transitions is shown in Fig.

16 for the QR classes studied in Section V and for the dual classes. Entries zv and zc denote switching transitions at zero voltages and zero current, respectively. If a switch is turned on at zero voltage, then the same switch is turned off at zero current in the dual converter. Thus, transitions for converters in the Q_n-PWM and Q_f-PWM classes are identical, while the S-switch and the Ŝ-switch have interchanged types of transitions in the ZV and ZC classes. Finally, ZV-QSW/ZC-QSW and likewise ZV-MR/ZC-MR have complementary sets of transitions.

Fig. 16 also summarizes the sensitivity of QR topologies to major circuit parasitic reactances: the S-switch junction capacitance C_t, the Ŝ-switch junction capacitance C_d and the parasitic inductance L_p distributed in the loop with the switches. If the position of the parasitic element is encompassed by the topological definition of a QR class, switching loss mechanisms associated with the element are eliminated. The parasitic element can be absorbed by the resonant element or even used alone as the resonant element.

With respect to the type of switching transitions and sensitivity to the parasitics, ZV-MR topologies are clearly superior to other QR converters. ZV-QSW topologies also exhibit all zero-voltage transitions, but switching losses associated with the parasitic inductance L_p in the loop with the switches are not eliminated. In converters with an isolation transformer, leakage inductance of the transformer appears in the loop with the switches, so that the ZV-QSW class and other classes sensitive to L_p may be suitable for very high-frequency operation only in transformerless applications.

B. Switch Stresses and Design Trade-Offs

In QR converters, switches are exposed to higher stresses than in parent PWM topologies. Thus, if the same power is processed, switching devices with substantially higher voltage and/or current ratings are necessary in the QR topology. This is one of the main disadvantages of QR converters. Higher current stresses also indicate that conduction losses are inevitably higher in QR topologies.

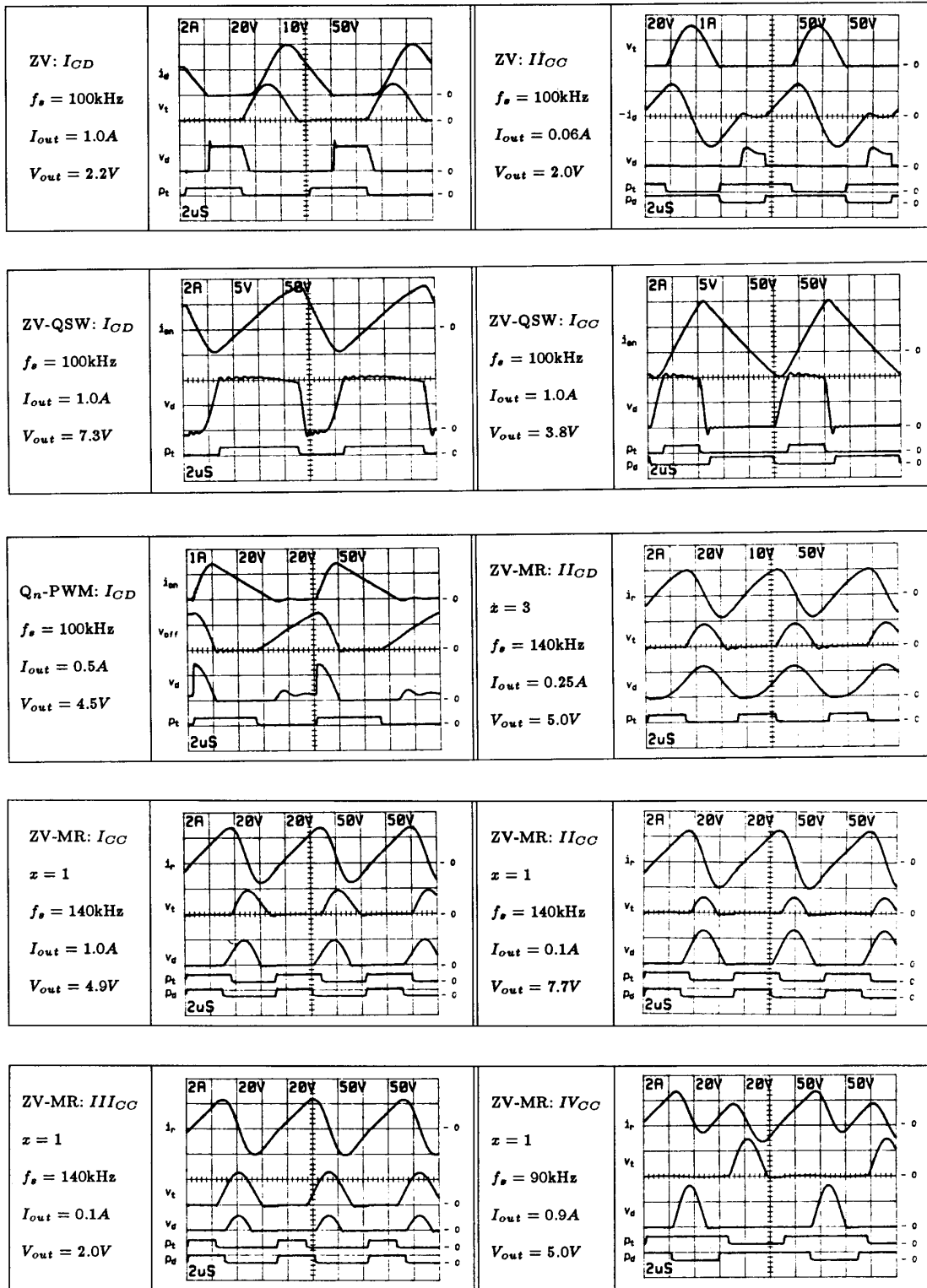Switch stresses are normalized to ideal stresses in the PWM

Fig. 13. Waveforms recorded in experimental QR buck converters. Operating modes and operating conditions are indicated.
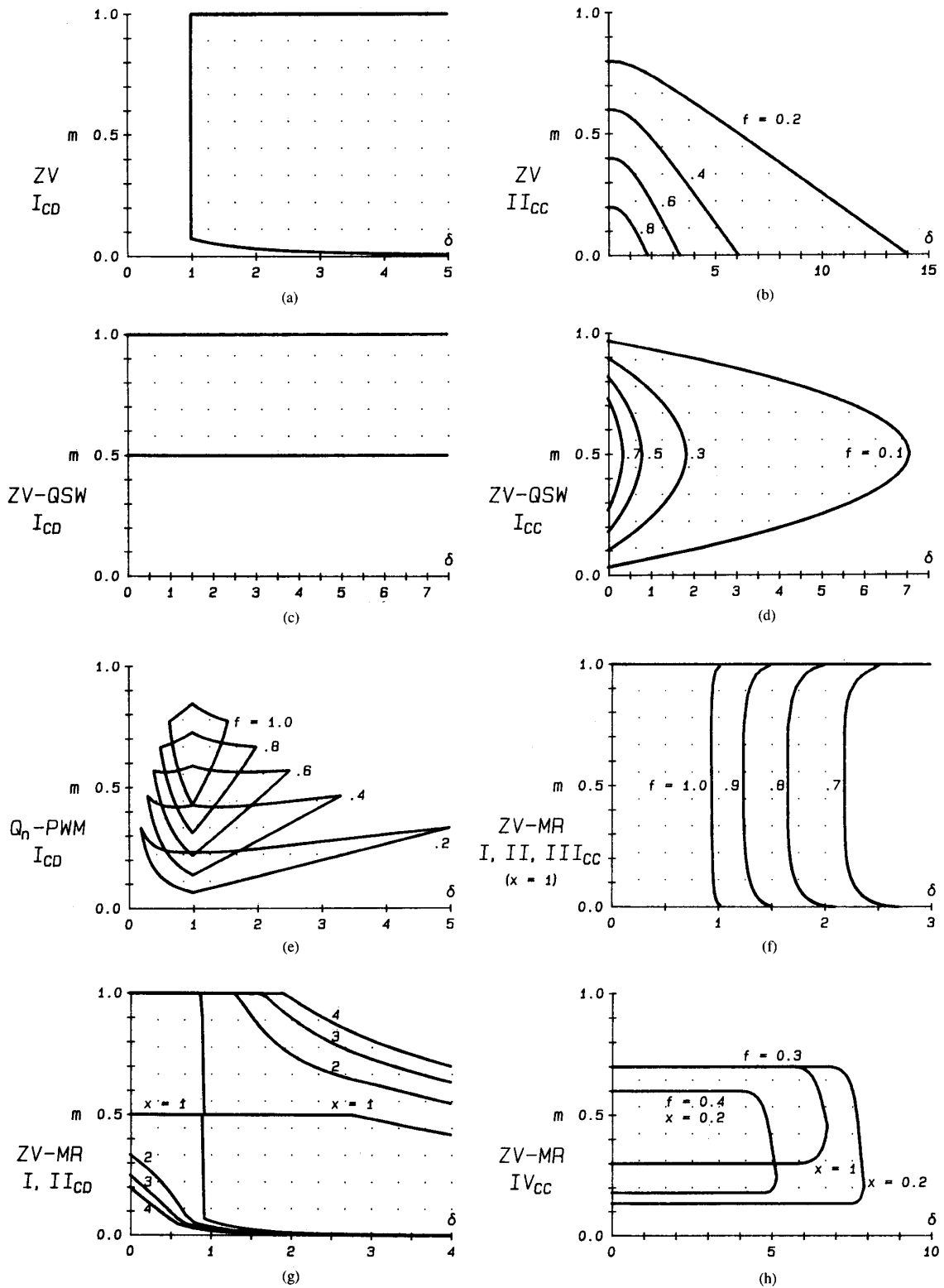
Fig. 14. Operating regions of selected classes and operating modes of QR converters.
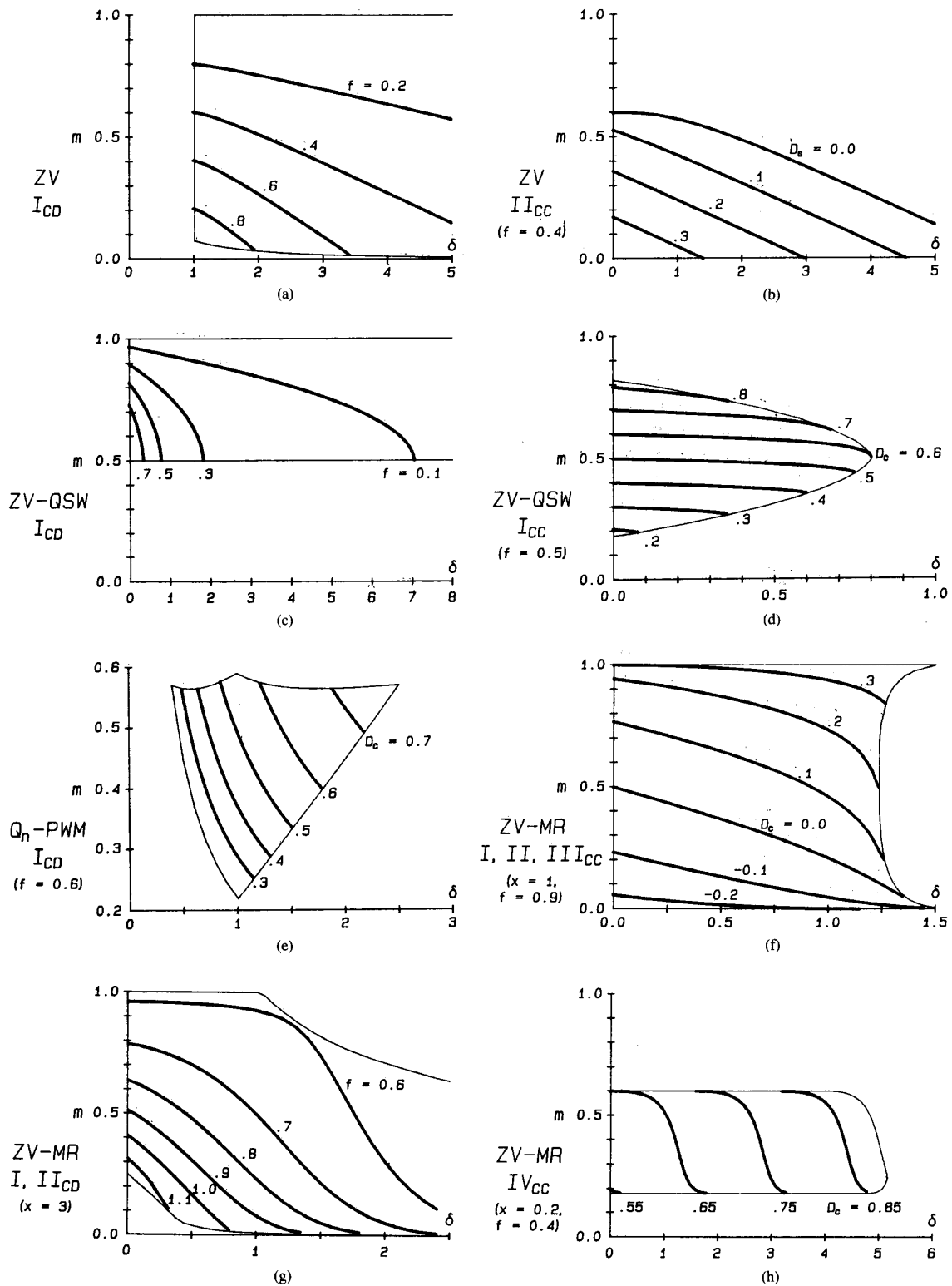
Fig. 15. DC characteristics of selected classes and operating modes of QR converters.

| QR | Switching Transition | | | | Topology | | |
| | S-switch | | $\hat{S}$-switch | | Insensitive to: | | |
Class	$1\rightarrow0$	$0\rightarrow1$	$1\rightarrow0$	$0\rightarrow1$	L_p	C_t	C_d
ZV	zv	zv	zc	zc	√	√	−
ZC	zc	zc	zv	zv	√	−	√
ZV-QSW	zv	zv	zv	zv	−	√	√
ZC-QSW	zc	zc	zc	zc	√	−	−
Q_n-PWM	zc	zv	zv	zc	−	−	−
Q_f-PWM	zc	zv	zv	zc	−	−	−
ZV-MR	zv	zv	zv	zv	√	√	√
ZC-MR	zc	zc	zc	zc	√	−	−

Fig. 16. Comparison of QR converters with respect to type of switching transitions and sensitivity to major parasitic elements.

parent: the voltage stress is normalized to V_{off}, while the current stress is normalized to I_{on} at the maximum output current. Analytical and/or numerical results are summarized in Fig. 17 for the classes and operating modes under study. The comparison results are quite general because they do not refer to any specific converter topology.

In CD models, with the exception of the Q_n-PWM class, frequency f is the control variable. The only parameter that can be selected in the design in the characteristic impedance R_o or, equivalently, the maximum normalized current δ_{max}. In the case of ZV-MR converters, an additional design parameter is the ratio x of the resonant capacitors. On the other hand, in CC modes, the converters are controlled at constant switching frequency, so that the normalized frequency f is an additional design parameter. As shown in Fig. 14, the operating regions in the CC modes are bounded from above in the load direction. In general, selecting a lower value for δ_{max} than the value determined by the boundary of the operating region does not contribute to lower voltage stresses, while current stresses and conduction losses are inevitably higher. Therefore, δ_{max} for CC modes is always assumed to be determined by the boundary of the operating region, while the design trade-offs are discussed with respect to the parameter f.

ZV: Mode I_{CD}

Mode I_{CD} is the well-known half-wave mode of zero-voltage converters. A ZV converter in mode I_{CD} has to be designed for a non-zero minimum output current:

$$\delta_{min} = 1. \tag{20}$$

The transistor voltage stress is proportional to the required load range, as indicated in Fig. 17. Other stresses are relatively low.

ZV: Mode II_{CC}

The operating region is restricted in the m direction. For zero load,

$$m < 1 - f. \tag{21}$$

If the maximum required equivalent duty ratio m^* is specified, the normalized frequency f can be selected anywhere in the range

$$0 < f < 1 - m^*. \tag{22}$$

A lower f contributes to lower current but also to higher voltage stresses. Thus, within the limits indicated in Fig. 17, parameter f can be selected to control the trade-off between the current and the voltage stress. Regardless of the choice for f, the available load range is unlimited because operation at zero load is possible.

ZV-QSW: Mode I_{CD}

The main advantage of ZV-QSW converters is that the voltage stress is equal to 1, i.e., equal to the voltage stress in the PWM parent. A serious limitation for the CD mode is that its operating region is restricted to equivalent duty ratios in the range $0.5 < m < 1$. The operating region is unbounded in the load direction and it includes the zero-load axis, so that δ_{max} is a free design parameter. As shown in Fig. 17, larger δ_{max} contributes to lower current stresses. However, for a given load range, larger δ_{max} also contributes to a wider frequency range. The required frequency range can be estimated from the dc characteristics in Fig. 15(c).

ZV-QSW: Mode I_{CC}

The operating region in the CC mode is symmetrical around $m = 0.5$. In addition to the constant-frequency control, this is another advantage over the conventional switch realization. Three design considerations are relevant for the choice of the normalized frequency f. For lower f: the range of attainable conversion ratios is wider; current stresses are lower; the transition states (the (0-0)-states) are relatively shorter. If the lengths of the transition states become comparable to the switching times of utilized semiconductor devices, benefits of the zero-voltage switching are lost. Thus, the choice of f will be determined by the trade-off between the current stresses and the increased switching losses. As the normalized frequency f gets lower, the distinction between mode I_{CC} and the continuous conduction mode of the PWM parent gradually disappears.

Q_n-PWM: Mode I_{CD}

A major disadvantage of the Q_n-PWM converters is that the operating region (Fig. 14(e)) is restricted to a relatively small portion of the load-to-output plane. Both the range of attainable conversion ratios and the load range are limited. Frequency f can be selected to adjust the available operating region to design specifications. However, one note that the voltage stress is higher for lower f, as indicated in Fig. 17.

A potential advantage of Q_n-PWM converters is that the constant-frequency, variable-duty-ratio control is possible with a single active (not necessarily two-quadrant) switch.

ZV-MR: Modes I, II_{CD}

The operating region shown in Fig. 14(g) includes the zero-load axis, but not for all equivalent duty ratios. At zero load, the theoretical minimum for the equivalent duty ratio,

$$m_{min}(\delta = 0) = \frac{1}{1 + x}, \tag{23}$$

Class	Mode	Peak Voltage Stress S	Peak Voltage Stress $\hat{S}$	Peak Current Stress S	Peak Current Stress $\hat{S}$
ZV	I_{CD}	$\delta_{max}+1$	1	1	2
	II_{CC}	$\to 2 \quad (f \to 1-m^*)$ $\to \infty \quad (f \to 0)$	1	$\to \infty \quad (f \to 1-m^*)$ $\to 2 \quad (f \to 0)$	
ZV-QSW	I_{CD}	1		$1+\sqrt{1+\frac{3x}{4\delta_{max}}}$	
	I_{CC}	1		6.2 $\quad (f = 0.9)$ 4.2 $\quad (f = 0.7)$ 3.2 $\quad (f = 0.5)$ $\to 2.0 \quad (f \to 0)$	
Q_n-PWM	I_{CD}	1.9 $\quad (f = 1.0)$ 2.6 $\quad (f = 0.8)$ 3.6 $\quad (f = 0.6)$ 5.1 $\quad (f = 0.4)$ 8.3 $\quad (f = 0.2)$		≈ 2	
ZV-MR	I,II_{CD} $(x \geq 1)$	$\sqrt{x}+\frac{\delta_{max}}{1+x}\left[\pi - \arctan\sqrt{x^2-1}+\sqrt{x(x-1)}\right]$ $\approx \sqrt{x}+\delta_{max}$ for $x > 2$	2	$1+\frac{\sqrt{x}}{\delta_{max}}$	$\approx 2+\frac{\sqrt{x-1}}{\delta_{max}}$
	I,II,III_{CC} $(x = 1)$	2.3 $\quad (f = 1.0)$ 2.7 $\quad (f = 0.9)$ 3.2 $\quad (f = 0.8)$ 3.8 $\quad (f = 0.7)$ 4.5 $\quad (f = 0.6)$		2.4 $\quad (f = 1.0)$ 2.1 $\quad (f = 0.9)$ 1.9 $\quad (f = 0.8)$ 1.7 $\quad (f = 0.7)$ 1.6 $\quad (f = 0.6)$	
	IV_{CC} $(x = 1)$	$\to 2.0 \quad (f \to 0.5)$ 3.0 $\quad (f = 0.45)$ 4.0 $\quad (f = 0.40)$ 6.7 $\quad (f = 0.30)$ $\to \infty \quad (f \to 0)$		$\to \infty \quad (f \to 0.5)$ 2.2 $\quad (f = 0.45)$ 2.1 $\quad (f = 0.40)$ 2.0 $\quad (f = 0.30)$ $\to 2.0 \quad (f \to 0)$	

Fig. 17. Switch stresses in selected QR classes and operating modes. Stresses are normalized to ideal stresses in PWM parent converter.

is attained for the maximum switching frequency,

$$f_{max} = f(\delta = 0, m = m_{min}) = \sqrt{\frac{1+x}{x}}. \qquad (24)$$

As the load is increased, the lower limit for m decreases toward zero but the upper limit for m starts to decrease from 1 toward zero. As shown in Fig. 14(g), the operating region can be expanded by increasing the ratio x of the resonant capacitors. However, as evident from the analytical results in Fig. 17, voltage and current stresses also increase with x. Therefore, a min-

imum value for x for which the available operating region is sufficiently large should be selected in the design. Then, δ_{max} can be used to achieve a favorable trade-off between voltage and current stresses.

ZV-MR: Modes I, II, III$_{CC}$

In addition to the constant-frequency control, another advantage of ZV-MR converters in CC modes is that the full range of equivalent duty ratios ($0 < m < 1$) is available from no load to full load, provided that

$$f < \min\left(1, \frac{1}{\sqrt{x}}\right). \qquad (25)$$

The results in Fig. 17 are computed for $x = 1$. Stresses are similar to stresses in the CD modes. Parameter f affects the trade-off between voltage and current stresses. In [12], a design of a practical constant-frequency ZV-MR buck converter is discussed in detail.

ZV-MR: Mode IV_{CC}

The operating region is restricted in the m direction:

$$\sqrt{x}f < m < 1 - f, \qquad (26)$$

while the available load range is unlimited (the zero-load axis is included in the operating region). The stresses are higher than in other ZV-MR modes, as shown in Fig. 17 for $x = 1$. A lower x contributes to a lower limit on the equivalent duty ratio, but also to even higher $\hat{S}$-switch voltage stress.

VIII. CONCLUSION

Quasi-resonant (QR) converters are dc-to-dc converters obtained by adding resonant elements to a parent PWM converter. Topological properties of the PWM network are used to examine and classify all possible positions of the added resonant elements. The synthesis method yields two results: first, all possible QR topologies are constructed systematically, without resorting to any intuitively justified circuit manipulations; second, the topological properties necessary for the analysis of QR converters follow directly from the synthesis method.

It is shown that there are six classes of QR converters with two resonant elements, including two novel classes. More complex QR converters are derived by applying the synthesis method recursively, starting from a previously defined QR network.

The systematic synthesis of QR topologies is augmented by a study of possible switch realizations. Just as suggested by the technique of synchronous rectification for PWM converters, a controllable rectifier can be used in order to lower the rectifier conduction losses in QR converters. In view of the fact that operating modes of QR converters can be vastly different only because the active switch is voltage or current bidirectional, it is not surprising that the controllable rectifier also leads to a number of novel operating modes. Most importantly, constant-frequency control becomes possible in all QR classes.

Using the method proposed in [8], dc and small-signal ac analysis of various QR classes and operating modes are unified with respect to all PWM parent converters. A slightly different interpretation of the analysis method yields dc and ac models in which the model of the PWM parent is explicitly exposed. Thus, QR topologies are firmly linked to their PWM parents with respect to topological, dc conversion and dynamic properties.

Steady-state analyses are completed for four selected classes of quasi-resonant converters: zero-voltage, zero-voltage quasi-square-wave, zero-voltage multi-resonant, and a new class—On-resonant quasi-PWM. Operating modes with all lossless (zero-voltage or zero-current) transitions are identified for two switch realizations—a conventional realization with a single current-bidirectional active switch and a single diode, and for a realization with a current-bidirectional controllable rectifier. Results that can be used to compare, select and design QR converters include boundaries of the operating regions, load-to-output dc characteristics, a comparison of switching transitions and sensitivity to major circuit parasitics, a comparison of switch voltage and current stresses, and a discussion of pertinent design trade-offs.

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