A General Translinear Principle for Subthreshold MOS Transistors

Teresa Serrano-Gotarredona, Bernabé Linares-Barranco, and Andreas G. Andreou

***Abstract*—This paper revises the conditions under which the translinear principle can be fully exploited for MOS transistors operating in subthreshold. Due to the exponential nature of subthreshold MOS transistors, the translinear principle applies immediately as long as the source-to-bulk voltages are made equal to zero (or constant). This paper addresses the conditions under which subthreshold MOS transistors still satisfy a translinear principle, but without imposing this constraint on all V_{BS} voltages. It is found that the translinear principle results in a more general formulation than the originally found for BJT's since now multiple translinear loops can be involved. The constraint of an even number of transistors is no longer necessary. Some corollaries are stated as well and, finally, it is shown how to use the theorem for subthreshold MOS transistors operated in the ohmic regime.**

***Index Terms*—CMOS analog integrated circuits, current mode circuits, low-power circuits, nonlinear circuits, subthreshold circuits, translinear circuits, very large scale integration.**

I. Introduction

THE translinear principle, introduced by Gilbert in 1975 [1], is one of the most important circuit theory contributions in the electronics era. In its original formulation, the translinear principle provides a simple and efficient way to analyze and synthesize nonlinear circuits based on bipolar junction transistors (BJT's). Due to their exponential characteristics, the translinear principle can be extended to MOS transistors operating in weak inversion [2], [3] without or with floating-gate devices [4]. For MOS transistors operating above threshold there has also been found a similar way to analyze and synthesize nonlinear circuits [5].

For bipolar transistors one practical problem that may require some attention when applying the translinear principle is the nonzero base current [6]. In contrast, the translinear principle holds for MOS subthreshold transistors in an exact manner if source and bulk are short circuited. However, it has been found that the principle holds as well in an exact manner under different circumstances [2]–[3], although a general subthreshold MOS translinear theorem has not been devised until now. In this paper we provide this general theorem and outline the conditions under which subthreshold MOS transistors, viewed as four terminal devices, satisfy a general translinear principle.

The operation of a subthreshold MOS can be described by the following equation [2], [7]–[9]:

$$I_{DS} = I_o S e^{\kappa(V_{GS}/V_{\rm th})}\, e^{(1-\kappa)(V_{BS}/V_{\rm th})}(1 - e^{-V_{DS}/V_{\rm th}}) \quad (1)$$

where $V_{\rm th} = KT/q$ is the thermal voltage, I_o is a positive constant current, S is the transistor size factor ($S = W/L$, where W is transistor width and L is its length), and κ is a technology-dependent positive parameter. This equation holds true as long as

$$\tfrac{1}{2}\,\phi_{FB} \le V_{GS} \le \phi_{FB} \quad (2)$$

where ϕ_{FB} is the device's flat-band voltage [10]. Voltage V_{BS} can take either positive or negative values as long as the parallel PN diode junction is biased below its forward conduction threshold voltage. Parameter κ is known to have a slight dependency on voltage V_{BS} [2]. However, in this paper we will assume κ to be constant, which is a reasonable assumption if care is taken to make the V_{BS} voltages similar for all transistors.

For operation in saturation, (1) can be simplified to

$$I = \frac{I_{DS}}{S} = I_o e^{\kappa(V_{GS}/V_{\rm th})}\, e^{(1-\kappa)(V_{BS}/V_{\rm th})}, \quad \text{if } V_{DS} \gg V_{\rm th} \quad (3)$$

and can be rewritten as

$$I = I_o i_G^{\kappa} i_B^{(1-\kappa)} \quad (4)$$

where I (a normalized current) is transistor current normalized with respect to transistor size factor $S = W/L$ and i_G, i_B are dimensionless numbers called pseudo-currents and equal to

$$i_G = e^{V_{GS}/V_{\rm th}}$$
$$i_B = e^{V_{BS}/V_{\rm th}} \quad (5)$$

II. Original Translinear Theorem Applied to Subthreshold MOS Transistors

Let us use the symbol in Fig. 1 to represent a weak-inversion MOS in saturation. Let us call the path that goes from the gate terminal G to the source terminal S the G branch (or gate branch), and the path that goes from the bulk terminal B to terminal S the B branch (or bulk branch). We are using a diode-like symbol to represent the exponential relationship between the voltage of the branch and the current flowing out of the device and a capacitive-like termination to each diode symbol to represent the capacitive coupling nature of the gate

Manuscript received October 8, 1997; revised May 11, 1999. This work was supported in part by the ONR under Grant N00014-95-1-0409. This paper was recommended by Associate Editor V. P. Villar.

T. Serrano-Gotarredona and B. Linares-Barranco are with the National Microelectronics Center (CNM), 41012 Sevilla, Spain.

A. G. Andreou is with The Johns Hopkins University, Baltimore, MD 21218 USA.

Publisher Item Identifier S 1057-7122(99)03883-0.

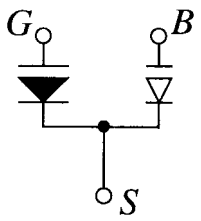


Fig. 1. Translinear symbol representation for subthreshold MOS transistor in saturation.

and bulk terminals. If $V_{BS} = 0$ (or constant) there is an exact exponential relationship between V_{GS} and I_{DS} [see (3)] and the original BJT translinear formulation can be directly and exactly applied (see Fig. 2):

Theorem 1: In a closed loop containing an **equal** number of oppositely connected translinear elements, the product of the normalized currents in the elements connected in the clockwise (CW) direction is equal to the corresponding product for elements connected in the counterclockwise (CCW) direction.

Proof: In a loop, the sum of branch voltages adds to zero. Since voltages of CW-oriented junctions have opposite sign than those of CCW-oriented junctions, the following holds:

$$0 = \sum_{j\in\{\mathrm{CW}\}} V_{GS_j} - \sum_{l\in\{\mathrm{CCW}\}} V_{GS_l}. \tag{6}$$

Since $V_{BS} = 0$ for all subthreshold MOS transistors, using (3) in (6) yields

$$\begin{aligned} 0 &= \frac{V_{\mathrm{th}}}{\kappa} \sum_{j\in\{\mathrm{CW}\}} \ln\left(\frac{I_j}{I_o}\right) - \frac{V_{\mathrm{th}}}{\kappa} \sum_{l\in\{\mathrm{CCW}\}} \ln\left(\frac{I_l}{I_o}\right) \\ &= \frac{V_{\mathrm{th}}}{\kappa} \ln\left(\frac{\displaystyle\prod_{j\in\{\mathrm{CW}\}} I_j}{\displaystyle\prod_{l\in\{\mathrm{CCW}\}} I_l} \frac{\displaystyle\prod_{l\in\{\mathrm{CCW}\}} I_o}{\displaystyle\prod_{j\in\{\mathrm{CW}\}} I_o}\right) \\ \Rightarrow 1 &= \frac{\displaystyle\prod_{j\in\{\mathrm{CW}\}} I_j}{\displaystyle\prod_{l\in\{\mathrm{CCW}\}} I_l} \frac{\displaystyle\prod_{l\in\{\mathrm{CCW}\}} I_o}{\displaystyle\prod_{j\in\{\mathrm{CW}\}} I_o}. \end{aligned} \tag{7}$$

Since tthe number of CW-oriented devices is equal to the CCW-oriented ones, the I_o coefficients in (7) cancel out, thus resulting in

$$\prod_{j\in\{\mathrm{CW}\}} I_j = \prod_{l\in\{\mathrm{CCW}\}} I_l. \tag{8}$$

□

Fig. 2 illustrates this Theorem. In Fig. 2(a) a loop with six G-branches is represented. The B-branches are not shown because their terminals are short circuited together and, consequently, have no effect on the circuit behavior. Fig. 2(b) shows the same circuit, but using the MOS transistor symbol to represent the devices.

III. Generalized Translinear Theorem for Subthreshold MOS Transistors

In this section, we will consider the conditions under which translinear principles can be applied to circuits with subthreshold MOS transistors, but without imposing the constraint of making $V_{BS} = 0$. We will introduce first some preliminary theorems and definitions and then state and prove the generalized translinear theorem for subthreshold MOS devices. Afterwards, a few examples will illustrate the theorem.

The first concepts to be introduced are G loop and B loop. A G loop (or gate loop) is a closed loop of G branches, and a B loop (or bulk loop) is a closed loop of B branches. For these loops we can state translinear theorems for their pseudocurrents.

Theorem 2: In a G loop containing an **arbitrary** number of G branches, the product of pseudocurrents i_G of branches connected in the CW direction is equal to the corresponding product for branches connected in the CCW direction.

Proof: the branch voltages of a G loop satisfy

$$0 = \sum_{j\in\{\mathrm{CW}\}} V_{GS_j} - \sum_{l\in\{\mathrm{CCW}\}} V_{GS_l}. \tag{9}$$

Applying the first equation of (5) in (9) yields

$$\begin{aligned} 0 &= \sum_{j\in\{\mathrm{CW}\}} V_{\mathrm{th}} \ln i_{G_j} - \sum_{l\in\{\mathrm{CCW}\}} V_{\mathrm{th}} \ln i_{G_l} \\ &= V_{\mathrm{th}} \ln \frac{\displaystyle\prod_{j\in\{\mathrm{CW}\}} i_{G_j}}{\displaystyle\prod_{l\in\{\mathrm{CCW}\}} i_{G_l}} \\ \Rightarrow \prod_{j\in\{\mathrm{CW}\}} i_{G_j} &= \prod_{l\in\{\mathrm{CCW}\}} i_{G_l}. \end{aligned} \tag{10}$$

□

Note that since pseudocurrents are dimensionless entities, we can have an arbitrary number of branches oriented CW and another arbitrary number of branches oriented CCW [as opposed to the case of (7)]. A completely equivalent theorem holds directly for B loops.

Up to now, things are similar to classical translinear loops, except that an arbitrary number of branches are allowed. However, the presence of two exponential branch voltages in (3) is what makes subthreshold MOS translinear loops more general and complicated than the classical ones. A first consequence of this fact is the following concept of coupled loops.

Definition 1: Two G loops are said to be coupled if at least one MOS device of the first G loop and at least one other different device of the second G loop share their respective B branches in a common B loop.

This is illustrated in Fig. 3. Devices 1-3-5 form a G loop and devices 2-4-6 form another G loop. However, devices 1-2-3-4 form a B loop, thus causing the previous two G loops to be coupled through the B branches of devices 1-2-3-4.

An equivalent definition applies for coupled B loops. Note that two loops may have a common branch without being necessarily coupled loops.

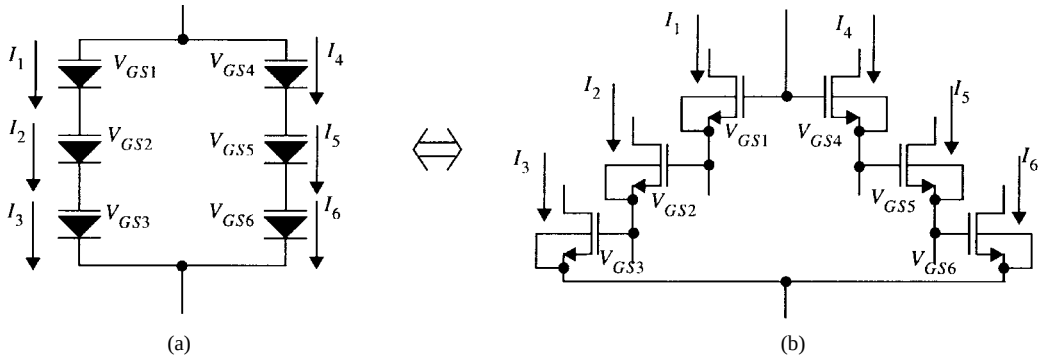


Fig. 2. Subthreshold MOS transistors translinear loop where for all transistors $V_{BS} = 0$. (a) Translinear symbol representation. (b) Circuit schematic representation.

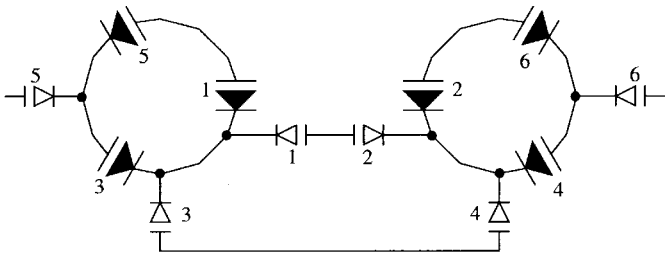


Fig. 3. Example of coupled G loops using translinear symbol representation.

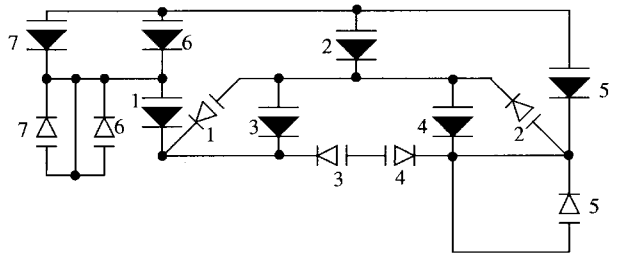


Fig. 4. Illustration of the G-order concept. Devices 1-2-3-6 form a G loop which is coupled to the G loop formed by devices 2-4-5 because devices 1-2-3-4 form a B loop. Devices 1-2-3-4-5-6 form a closed translinear set and so do devices 6 and 7. Device 2 has a G order of $\mathbf{n}_{G2} = 2$ because its G branch belongs to two G loops of the same closed translinear set. All other devices have G order one.

In the example of Fig. 3, we can write for the two G loops

$$\begin{aligned}\frac{I_3 I_5}{I_1} &= I_o\left(\frac{i_{G3}i_{G5}}{i_{G1}}\right)^{\kappa}\left(\frac{i_{B3}i_{B5}}{i_{B1}}\right)^{1-\kappa} \\ &= I_o e^{(V_{BS3}+V_{BS5}-V_{BS1})(1-\kappa/V_{\rm th})} \\ \frac{I_4 I_6}{I_2} &= I_o\left(\frac{i_{G4}i_{G6}}{i_{G2}}\right)^{\kappa}\left(\frac{i_{B4}i_{B6}}{i_{B2}}\right)^{1-\kappa} \\ &= I_o e^{(V_{BS4}+V_{BS6}-V_{BS2})(1-\kappa/V_{\rm th})} \end{aligned} \tag{11}$$

where all pseudocurrents i_G have cancelled out by applying Theorem 2. However, due to B loop 1-2-3-4,

$$V_{BS1} + V_{BS4} = V_{BS2} + V_{BS3} \tag{12}$$

which introduces a coupling between the two equations in (11), and makes G loops 1-3-5 and 2-4-6 to be coupled loops.

When devices form multiple touching loops it is not clear which ones to choose or how many to choose. For example, in Fig. 4 one can choose G loops 1-2-3-6, 6-7, and 2-4-5. But why not consider 1-3-4-5-6, 6-7, and 2-4-5 or 1-3-4-5-7 and 1-2-3-6. One can try all possible options as long as one chooses a set of nonredundant (NR) loops:

Definition 2: A set of loops is said to be NR if the sum of branch voltages of any loop cannot be expressed as a linear combination of the sum of branch voltages of other loops in the set.

For example, in Fig. 4, for G loops 1-2-3-6, 2-4-5, and 1-3-4-5-6 their respective sums of branch voltages are

$$\begin{aligned} V_{GS6} + V_{GS1} &= V_{GS2} + V_{GS3} \\ V_{GS2} + V_{GS4} &= V_{GS5} \\ V_{GS6} + V_{GS1} + V_{GS4} &= V_{GS3} + V_{GS5}. \end{aligned} \tag{13}$$

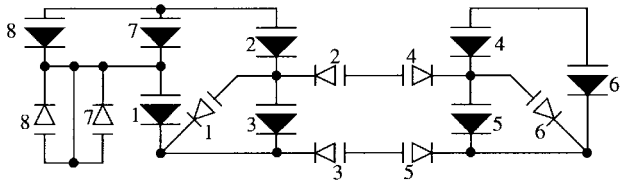


Fig. 5. Example of CTS's. MOS devices 7 and 8 form a CTS and so do MOS devices 1–7.

Any of these three equations can be expressed as a linear combination of the other two. Thus, the three G loops do not form an NR set of G loops. However, any two of these three G loops do form an NR set of G loops.

The fact that subthreshold MOS transistors can form coupled loops, yields naturally to the following concept of the closed translinear set (CTS).

Definition 3: Given a set of MOS devices, and once an NR set of loops has been chosen, a CTS is a set of devices such that all loops they form are only coupled among themselves, but are not coupled to loops where branches of other devices (not belonging to the CTS) are present.

This is illustrated in Fig. 5. Let us select the NR set of G loops 1-2-3-7, 4-5-6, and 7-8 and the NR set of B loops 1-2-3-4-5-6, 7, and 8. G loops 1-2-3-7 and 4-5-6 are coupled because there are B branches of devices of both G loops that are shared in the common B loop 1-2-3-4-5-6. The two G loops, 1-2-3-7 and 4-5-6, and the two B loops, 1-2-3-4-5-6 and 7, are not coupled to other loops (neither are G loop 7-8 nor B loop 8), thus, (for the chosen NR set of loops) devices 1-

2-3-4-5-6-7 form a CTS. On the other hand, neither G loop 7-8 nor B-loops 7 and 8 are coupled to any other loop. Therefore, devices 7-8 form another CTS.

When working with multiple G loops and B loops, with some of them being coupled, it is not very convenient to classify each branch as being CW or CCW oriented, as will become apparent later. Let us instead classify all branches into two orientation groups, the αwise oriented branches and the βwise oriented branches. Two branches are classified into the same group (either the αwise or the βwise) if they appear in the same loop with the same orientation. On the contrary, two branches are classified, each into a different group (one into the αwise, the other into the βwise) if they appear in the same loop with opposite orientation. Note that, now, a CW branch in one loop and a CCW branch in another loop can be classified into the same αwise or βwise group. If a branch is short circuited, it forms a one-branch loop and can be classified as either αwise or βwise.

Another concept that is useful for stating the generalized translinear subthreshold MOS theorem is that of G order and B order of a MOS device in a CTS.

Definition 4: Once an NR set of loops has been chosen, a subthreshold MOS transistor which is part of a CTS is said to have a G order of value $\boldsymbol{n}_G$ if its G branch belongs to $\boldsymbol{n}_G$ G loops of the given CTS.

An equivalent definition of the B order can be stated for B loops. The concept is illustrated in Fig. 4. Let us choose the NR set of G loops 1-2-3-6, 2-4-5, and 6-7 and of B loops 1-2-3-4, 5, 6, and 7. G loops 1-2-3-6 and 2-4-5 are coupled because devices 1-2-3-4 form a B loop. There are no other couplings among the chosen loops. Consequently, devices 1-2-3-4-5-6 form a CTS which consists of G loops 1-2-3-6 and 2-4-5 and B loops 1-2-3-4, 5, and 6. Devices 6 and 7 form one G loop (6-7) and two B loops (6 and 7) which are not coupled to any other loop. Therefore, devices 6 and 7 form another CTS. MOS device 2 has G order $\boldsymbol{n}_{G2} = 2$ because its G branch appears in two G loops of the same CTS. MOS device 6 does not have G order two because, although its G branch belongs to two different G loops, these two loops do not belong to the same CTS. All MOS devices have B order one because their B branches appear only in one B loop.

When a G branch has G order greater than one, it belongs to more than one G loop of the same CTS. In such cases it is possible that the branch be classified as αwise in some G loops and as βwise in other G loops. Under these circumstances, it is convenient to divide its G order into two parts

$$\boldsymbol{n}_G = \boldsymbol{n}_{\alpha,G} + \boldsymbol{n}_{\beta,G} \tag{14}$$

where $\boldsymbol{n}_{\alpha,G}$ (let us call it G-α order) denotes the number of times this G branch is classified as αwise in a CTS and $\boldsymbol{n}_{\beta,G}$ (let us call it G-β order) denotes the times it is classified as βwise in the CTS. Similarly, for B branches, the B order can be separated into the B-α order $(\boldsymbol{n}_{\alpha,B})$ and the B-β order $(\boldsymbol{n}_{\beta,B})$.

Using the concepts and preliminary theorems introduced until now, it is possible to state and prove the generalized translinear theorem for subthreshold MOS transistors[1]:

Theorem 3: Given a set of subthreshold MOS devices and choosing for them a set of NR G loops and B loops, for each CTS the following can be stated.

If it is possible to find an α and βwise classification of their G loops and B loops such that the following pertains.

a) The sum of G-α orders equals the sum of G-β orders

$$\sum_{j\in\{\alpha\text{wise}\}} \boldsymbol{n}_{\alpha,Gj} = \sum_{l\in\{\beta\text{wise}\}} \boldsymbol{n}_{\beta,Gl}. \tag{15}$$

b) Every time a device's G branch is classified as αwise in a G loop, its B branch can be classified as αwise in some B loop, and every time a device's G branch is classified as β wise in a G loop, its B branch can be classified as βwise in some B loop.

Then, the product of normalized currents raised to the power of their G-α order $I^{\boldsymbol{n}_{\alpha,Gj}}$ of all transistors in the CTS whose G branches have been classified αwise equals the product of normalized currents raised to the power of their G-β order $I^{\boldsymbol{n}_{\beta,Gl}}$ of all transistors whose G branches have been classified βwise.

Proof: For each G loop in the CTS, the following holds (as we know from Theorem 2):

$$1 = \frac{\displaystyle\prod_{j\in\{\alpha\text{wise}\}} i_{Gj}}{\displaystyle\prod_{l\in\{\beta\text{wise}\}} i_{Gl}}. \tag{16}$$

Since this is true for every single G loop we can multiply these equations for the chosen set of NR G loops and their product will still be equal to unity

$$\begin{aligned} 1 &= \left.\left(\frac{\displaystyle\prod_{j\in\{\alpha\text{wise}\}} i_{Gj}}{\displaystyle\prod_{l\in\{\beta\text{wise}\}} i_{Gl}}\right)\right|_{G\text{loop}_1} \\ &\quad \times \cdots \times \left.\left(\frac{\displaystyle\prod_{j\in\{\alpha\text{wise}\}} i_{Gj}}{\displaystyle\prod_{l\in\{\beta\text{wise}\}} i_{Gl}}\right)\right|_{G\text{loop}_p} \\ &= \frac{\displaystyle\prod_{j\in\{\alpha\text{wise}\}} (i_{Gj})^{\boldsymbol{n}_{\alpha,Gj}}}{\displaystyle\prod_{l\in\{\beta\text{wise}\}} (i_{Gl})^{\boldsymbol{n}_{\beta,Gl}}}. \end{aligned} \tag{17}$$

Furthermore, we can raise it to the power of κ and it still will be equal to unity

$$1 = \left(\frac{\displaystyle\prod_{j\in\{\alpha\text{wise}\}} (i_{Gj})^{\boldsymbol{n}_{\alpha,Gj}}}{\displaystyle\prod_{l\in\{\beta\text{wise}\}} (i_{Gl})^{\boldsymbol{n}_{\beta,Gl}}}\right)^{\kappa}. \tag{18}$$

[1]The theorem will be stated using G branches as primary branches and making B branches depend on them. However, because of the symmetry between G branches and B branches [due to the symmetry between V_{GS} and V_{BS} voltages as (3)], the theorem can be stated, as well, by interchanging G branches and Bbranches.

Note that, since the devices form a CTS, all branches will be present and no branch of another CTS appears. Consequently, (18) includes all G branches of the CTS and only the branches of this CTS. Equivalently, the same can be stated for all B loops

$$1 = \frac{\prod_{j\in\{\alpha\text{wise}\}} (i_{Bj})^{\boldsymbol{n}_{\alpha,Bj}}}{\prod_{l\in\{\beta\text{wise}\}} (i_{Bl})^{\boldsymbol{n}_{\beta,Bl}}} = \left(\frac{\prod_{j\in\{\alpha\text{wise}\}} (i_{Bj})^{\boldsymbol{n}_{\alpha,Bj}}}{\prod_{l\in\{\beta\text{wise}\}} (i_{Bl})^{\boldsymbol{n}_{\beta,Bl}}} \right)^{1-\kappa} \tag{19}$$

but raising now to the power of $1-\kappa$ for convenience. Note that, due to statement b) in Theorem 3, every time a device has its pseudocurrent i_{Gj} in the numerator of (18), its pseudocurrent i_{Bj} will also appear in the numerator of (19) and both will appear $\boldsymbol{n}_{\alpha,Gj}$ times. And the same holds for pseudocurrents in the denominators of (18) and (19). Therefore, let us define $\boldsymbol{n}_{\alpha,j}$ and $\boldsymbol{n}_{\beta,l}$ such that

$$\begin{aligned} \boldsymbol{n}_{\alpha,Gj} &= \boldsymbol{n}_{\alpha,Bj} = \boldsymbol{n}_{\alpha,j} \\ \boldsymbol{n}_{\beta,Gl} &= \boldsymbol{n}_{\beta,Bl} = \boldsymbol{n}_{\beta,l}. \end{aligned} \tag{20}$$

Also, since the devices form a CTS, (18) includes all devices of the CTS, and so does (19). Consequently, we can multiply (18) and (19) and index the i_G and i_B pseudocurrents of the same device with the same subscript and use this subscript to index the MOS device

$$\begin{aligned} 1 &= \left(\frac{\prod_{j\in\{\alpha\text{wise}\}} (i_{Gj})^{\boldsymbol{n}_{\alpha,Gj}}}{\prod_{l\in\{\beta\text{wise}\}} (i_{Gl})^{\boldsymbol{n}_{\beta,Gl}}} \right)^{\kappa} \cdot \left(\frac{\prod_{j\in\{\alpha\text{wise}\}} (i_{Bj})^{\boldsymbol{n}_{\alpha,Bj}}}{\prod_{l\in\{\beta\text{wise}\}} (i_{Bl})^{\boldsymbol{n}_{\beta,Bl}}} \right)^{1-\kappa} \\ &= \frac{\prod_{j\in\{\alpha\text{wise}\}} (i_{Gj}^{\kappa} i_{Bj}^{1-\kappa})^{\boldsymbol{n}_{\alpha,j}}}{\prod_{l\in\{\beta\text{wise}\}} (i_{Gl}^{\kappa} i_{Bl}^{1-\kappa})^{\boldsymbol{n}_{\beta,l}}} \end{aligned} \tag{21}$$

On the other hand, due to statement a) in the theorem, the following is satisfied:

$$\begin{aligned} 1 &= I_o^{[\Sigma_{j\in\{\alpha\text{wise}\}}\, \boldsymbol{n}_{\alpha,j} - \Sigma_{l\in\{\beta\text{wise}\}}\, \boldsymbol{n}_{\beta,l}]} \\ &= \frac{\prod_{j\in\{\alpha\text{wise}\}} (I_o)^{\boldsymbol{n}_{\alpha,j}}}{\prod_{l\in\{\beta\text{wise}\}} (I_o)^{\boldsymbol{n}_{\beta,l}}}. \end{aligned} \tag{22}$$

By multiplying (21) and (22) and using (4) we obtain

$$\begin{aligned} 1 &= \frac{\prod_{j\in\{\alpha\text{wise}\}} (I_o)^{\boldsymbol{n}_{\alpha,j}}}{\prod_{l\in\{\beta\text{wise}\}} (I_o)^{\boldsymbol{n}_{\beta,l}}} \frac{\prod_{j\in\{\alpha\text{wise}\}} (i_{Gj}^{\kappa} i_{Bj}^{1-\kappa})^{\boldsymbol{n}_{\alpha,j}}}{\prod_{l\in\{\beta\text{wise}\}} (i_{Gl}^{\kappa} i_{Bl}^{1-\kappa})^{\boldsymbol{n}_{\beta,l}}} \\ &= \frac{\prod_{j\in\{\alpha\text{wise}\}} (I_j)^{\boldsymbol{n}_{\alpha,j}}}{\prod_{l\in\{\beta\text{wise}\}} (I_l)^{\boldsymbol{n}_{\beta,l}}} \end{aligned} \tag{23}$$

which concludes the proof of the generalized subthreshold MOS translinear theorem. □

In the remaining of this section this theorem will be illustrated with a few examples. Consider the circuit of Fig. 6, where we can choose the two NR G loops 1-2-3 and 4-5-6 and the two NR B loops 2-6 and 1-3-4-5. The two G loops are coupled through each of the two B loops. Hence, all devices in Fig. 6 form a unique CTS. Table I shows a possible α or βwise classification of the branches. Column G-α denotes MOS devices whose G branch has been classified αwise, column G-β those whose G branch has been classified βwise. Similarly, columns B-α and B-β do the same for B branches. The dashed lines in Table I encircle those devices in a common loop. In Table I, the classification is such that when a device appears under G-α, it also appears under B-α, and if it appears under G-β, it also appears under B-β, therefore, satisfying the requirement of condition b) in Theorem 3. Since each G or B branch has order one (it appears only in one loop), Table I reveals that the sum of G-α orders is equal to the sum of G-β orders (and the sum of B-α orders is equal to the sum of B-β orders). Consequently, condition a) of Theorem 3 is also satisfied. Therefore, applying Theorem 3 results in

$$\frac{I_1 I_2 I_4}{I_3 I_5 I_6} = 1. \tag{24}$$

For illustration purposes, let us now write the current equation for each transistor as follows. If a G branch is connected αwise, we write its equation as in (4), but if its G branch is connected βwise we invert both sides of the equation

$$\begin{aligned} I_1 &= I_0 & i_{G1}^{\kappa} & & i_{B1}^{1-\kappa} \\ I_2 &= I_o & i_{G2}^{\kappa} & & i_{B2}^{1-\kappa} \\ \frac{1}{I_3} &= \frac{1}{I_o} & \frac{1}{i_{G3}^{\kappa}} & & \frac{1}{i_{B3}^{1-\kappa}} \\ I_4 &= I_o & i_{G4}^{\kappa} & & i_{B4}^{1-\kappa} \\ \frac{1}{I_5} &= \frac{1}{I_o} & \frac{1}{i_{G5}^{\kappa}} & & \frac{1}{i_{B5}^{1-\kappa}} \\ \frac{1}{I_6} &= \frac{1}{I_o} & \frac{1}{i_{G6}^{\kappa}} & & \frac{1}{i_{B6}^{1-\kappa}}. \end{aligned} \tag{25}$$

Pseudocurrents i_{G1}, i_{G2}, and i_{G3} are in the same G loop. Consequently, by Theorem 2

$$1 = \frac{i_{G1}^{\kappa} i_{G2}^{\kappa}}{i_{G3}^{\kappa}}. \tag{26}$$

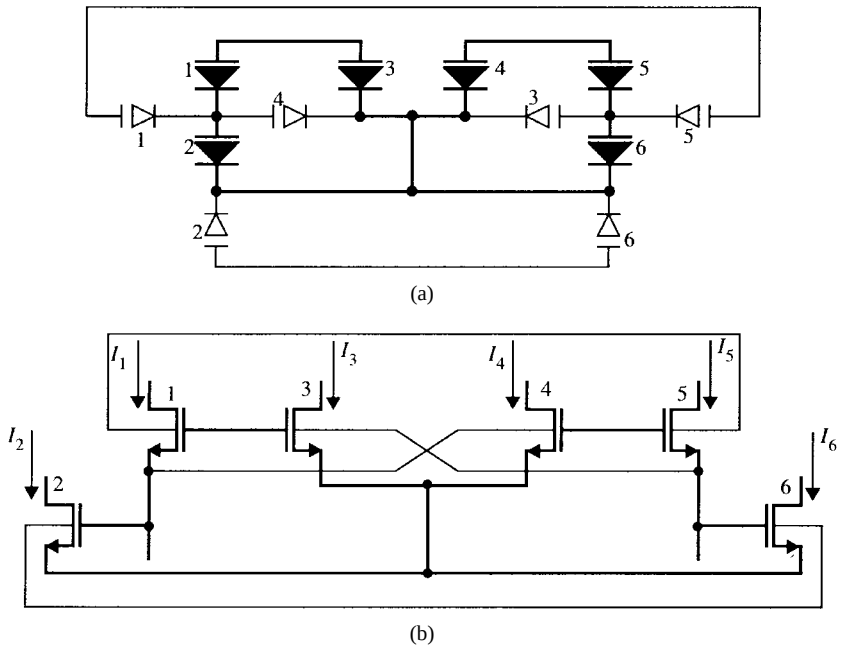


Fig. 6. Example of subthreshold MOS translinear circuit with $V_{BS} \neq 0$. (a) Translinear symbol representation. (b) Circuit schematic representation.

TABLE I

G		B	
α	β	α	β
2 3		2 6	
1 6		1 3	
4 5		4 5	

The same applies for pseudocurrents i_{G4}, i_{G5}, and i_{G6}. Similarly, for pseudocurrents i_B the following is satisfied:

$$1 = \frac{i_{B2}^{1-\kappa}}{i_{B6}^{1-\kappa}}, \quad 1 = \frac{i_{B1}^{1-\kappa} i_{B4}^{1-\kappa}}{i_{B3}^{1-\kappa} i_{B5}^{1-\kappa}}. \tag{27}$$

Consequently, by multiplying all equations in (25), (24) is obtained. Note that the generalized theorem imposes a topological constraint in the way the G loops and B loops are formed. This topological constraint is visualized in Table I, where devices under G-α must also be under B-α and devices under G-β must also be under B-β.

A particular bias arrangement for the circuit in Fig. 6 is shown in Fig. 7, which applies the following constraints to (24) for equally sized transistors:

$$\begin{aligned} I_1 &= I_2 = I_{in1} \\ I_5 &= I_6 = I_{in2} \\ I_3 &= I_{o1} \\ I_4 &= I_{o2} \\ I_{o1} + I_{o2} + I_{in1} + I_{in2} &= 2(I_{in1} + I_{in2}) \end{aligned} \tag{28}$$

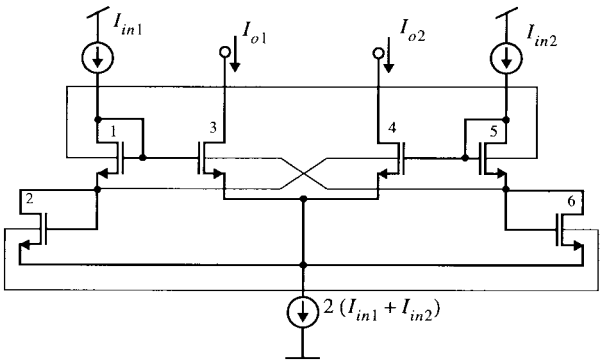


Fig. 7. Particular bias arrangement for the circuit configuration of Fig. 6.

resulting in

$$\begin{aligned} I_{o1} &= \frac{I_{in1} + I_{in2}}{I_{in1}^2 + I_{in2}^2} I_{in1}^2 \\ I_{o2} &= \frac{I_{in1} + I_{in2}}{I_{in1}^2 + I_{in2}^2} I_{in2}^2. \end{aligned} \tag{29}$$

In this example, all branches have α order and β order equal to one because device branches were not present in more than one loop. The example in Fig. 8 illustrates Theorem 3 for the case in which one of the devices has α and β order greater than one. Let us choose the NR set of G loops 1-3-4-5 and 1-2. On the other hand, devices 2-3 form a B loop,[2] while the B branches of devices 1, 4, and 5 form three single-branch B loops. Consequently, B branches of devices 1, 4, and 5 can be classified as αwise or βwise as many times as needed.[3]

[2]This will force $V_{BS2} = -V_{BS3}$ so that one of them must be positive. In such a case, it needs to be insured that the positive V_{BS} voltage is kept below the threshold voltage of the diode PN junction between source and bulk.

[3]Note that the pseudocurrent of such a branch is equal to unity and can be

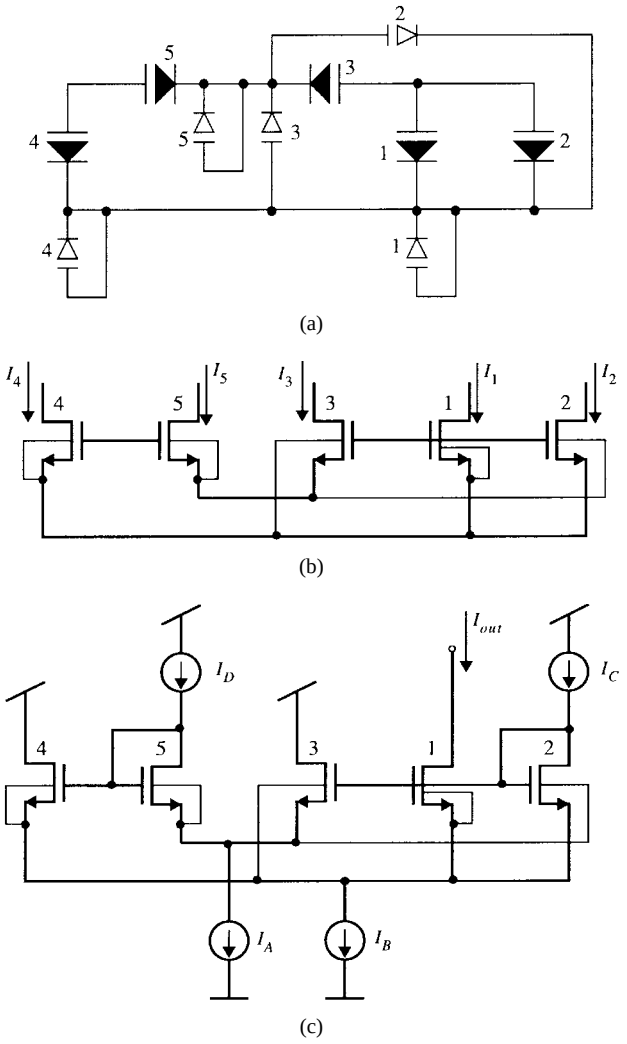


Fig. 8. Example of subthreshold MOS translinear circuit with one device having order-a higher than one. (a) Translinear symbol representation. (b) Circuit schematic representation. (c) Particular bias arrangement.

TABLE II

G		B	
α	β	α	β
3	1	3	1
4	5	2	5
2	1	4	1

Table II shows how G and B branches of the topology in Fig. 8(a) can be classified as αwise and βwise. In B loop 2-3 B branches of devices 2 and 3 are oriented in the same direction, therefore they must appear under the same B column in Table II. Let us put them under B-α. Then, for G loop 1-3-4-5, device 3 should appear under G-α and for G loop 1-2, device 2 should appear under G-α as well. Devices 1, 4, and 5 fill the spaces needed in Table II under column B to fulfill the conditions of Theorem 3. Consequently, the following equality will be satisfied:

$$I_1^2 I_5 = I_2 I_3 I_4. \tag{30}$$

A possible bias arrangement for this circuit is shown in Fig. 8(c) where, for equally sized transistors, the following constraints are applied:

$$\begin{aligned} I_1 &= I_{\text{out}} \\ I_2 &= I_C \\ I_5 &= I_D \\ I_3 + I_5 &= I_A \\ I_1 + I_2 + I_4 &= I_B. \end{aligned} \tag{31}$$

This together with (30) forces I_{out} to solve the following second-order polynomial:

$$\begin{aligned} & I_{\text{out}}^2 + c_1 I_{\text{out}} - c_1 c_2 = 0 \\ & c_1 = \frac{I_C}{I_D}(I_A - I_D) \\ & c_2 = I_B - I_D. \end{aligned} \tag{32}$$

Note that, with the generalized subthreshold MOS translinear theorem, the number of devices does not have to be an even number, as opposed to the traditional translinear theorem. In Fig. 7 there is an even number of transistors, while in Fig. 8 there is an odd number.

IV. Corollaries for the Generalized Subthreshold MOS Translinear Theorem

A set of immediate corollaries follow from the generalized subthreshold MOS translinear theorem:

Corollary 1: It is possible to have an exact translinear subthreshold behavior in a single G loop with all transistor bulks connected to the same terminal if the transistors share their sources pairwise and the G branches form loops of even numbers, half of them connected CW and the other half CCW.

This was anticipated by Vittoz [3] and is illustrated in Fig. 9(a). Devices 1-2-3-4-5-6 form a CTS and so do devices 6-7. For each CTS their G branches and B branches can be classified α and βwise, as is shown, respectively, in Tables III and IV. Applying Theorem 3 results in

$$\begin{aligned} I_1 I_3 I_5 &= I_2 I_4 I_6 \\ I_6 &= I_7. \end{aligned} \tag{33}$$

A particular bias arrangement is shown in Fig. 9(b), which imposes the following constraints for equally sized transistors:

$$\begin{aligned} I_{\text{out}} &= I_7 = I_6 = I_2 \\ I_1 &= I_C \\ I_3 + I_4 &= I_A \\ I_5 + I_6 + I_7 &= I_B \\ I_4 &= I_D \end{aligned} \tag{34}$$

which, together with (33), make current I_{out} solve the following second-order polynomial

$$I_{\text{out}}^2 + 2c_1 I_{\text{out}} - c_1 c_2 = 0$$

arbitrarily added to the numerator or denominator of (23) as many times as desired.

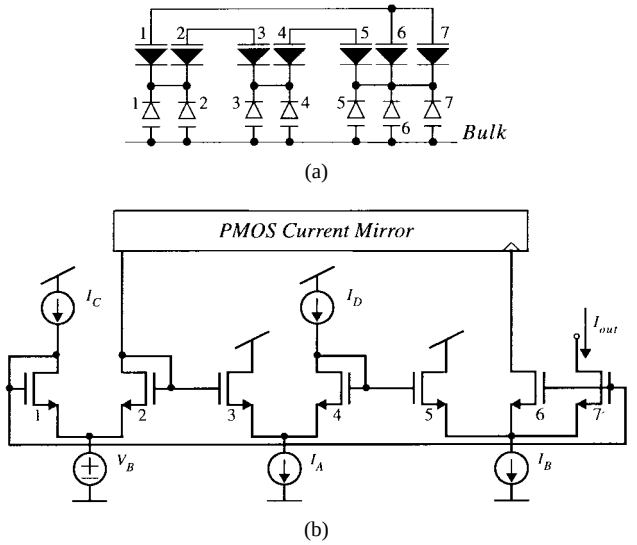


Fig. 9. Arrangement for translinear subthreshold MOS devices with common bulk and sources shared pairwise. (a) Translinear symbol representation. (b) Schematic representation of a particular bias arrangement.

TABLE III

G		B	
α	β	α	β
1	2	1	2
3	4	3	4
5	6	5	6

TABLE IV

G		B	
α	β	α	β
6	7	6	7

$$c_1 = \frac{I_C}{I_D}(I_A - I_D)$$
$$c_2 = I_B. \tag{35}$$

Corollary 2: There is a need to distinguish among G loops and B loops as long as κ and $1-\kappa$ are different. If a technology is available for which $\kappa = 1-\kappa = 0.5$, there would be no need to distinguish between G branches and B branches, and they could be mixed in common loops.

Corollary 3: If different subthreshold MOS devices are available (for example, NMOS and PMOS), such that they have equal κ, they could be mixed to form translinear loops.

Corollary 4: If two different subthreshold devices are available, such that their κ parameters add to one $(\kappa_1 + \kappa_2 = 1)$, then G branches of the first type of device can be mixed with B branches of the second type, and vice versa, to form translinear loops.

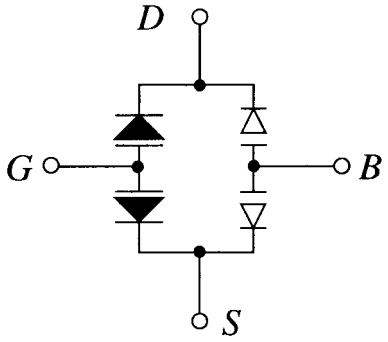


Fig. 10. Translinear symbol representation for subthreshold MOS in ohmic regime.

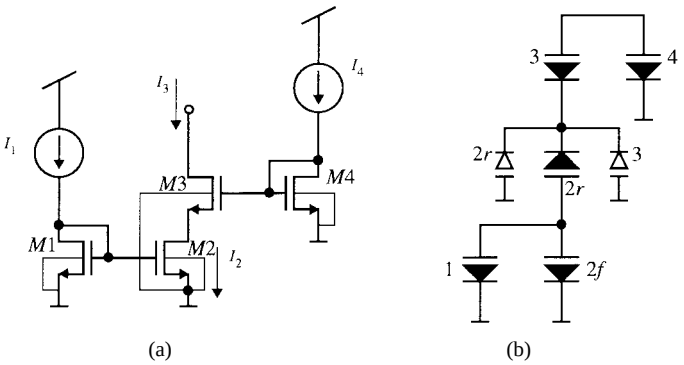


Fig. 11. Subthreshold MOS circuit with one transistor operating in ohmic region. (a) Circuit schematic. (b) Translinear symbol representation.

V. Extension to Ohmic Operation

As suggested in [2], the translinear principle for subthreshold MOS in saturation is directly extendable to the ohmic region by noting that, from (1), one can obtain the following:

$$I = \frac{I_{DS}}{S} = I_f - I_r$$
$$I_f = I_o e^{(\kappa V_{GS}/V_{\rm th})} e^{((1-\kappa)V_{BS}/V_{\rm th})} = I_o i_{Gf}^{\kappa} i_{Bf}^{1-\kappa}$$
$$I_r = I_o e^{(\kappa V_{GD}/V_{\rm th})} e^{((1-\kappa)V_{BD}/V_{\rm th})} = I_o i_{Gr}^{\kappa} i_{Br}^{1-\kappa}. \tag{36}$$

Under these circumstances, the symbol in Fig. 10 can be used to build (or analyze) circuit diagrams. The symbol indicates that the fictitious current I_f flowing out of terminal S is exponentially controlled by V_{GS} and V_{BS}, while fictitious current I_r flowing out of terminal D is exponentially controlled by voltages V_{GD} and V_{BD}, as given by (36). In this case, however, fictitious currents I_f and I_r need to be eliminated by using $I = I_f - I_r$ and another circuit constraint where I is the physical current (normalized to size factor S) that flows from the drain terminal to the source terminal. Now the device has two G branches, which will be called the Gf branch and Gr branch, and two B branches, which will be called the Bf branch and Br branch. The new Gf and Gr branches can be treated like the previous G branches, and the new Bf and Br branches as the previous B branches.

As an example, consider the circuit in Fig. 11(a), which was introduced by Delbrück in 1991 [11]. All transistors operate in saturation except $M2$. Consequently, all transistors can be represented by the symbol in Fig. 1 except for $M2$, which

TABLE V

G		B	
α	β	α	β
2r	3	2r	3
4	2f	4	2f

TABLE VI

G		B	
α	β	α	β
1	2f	1	2f

has to be represented by the symbol in Fig. 10. The resulting translinear symbol representation is shown in Fig. 11(b). In this figure, the B branches of devices 1, 4 and $2f$ are not shown because both their terminals are connected to ground. In Fig. 11(b) we can choose the two NR G loops 1-2f and 4-3-2r-2f, and B loop 3-2r, which form two CTS's (4-3-2r-2f and 1-2f). For each of them, a possible α and βwise classification table can be filled out, as shown in Tables V and VI. Since in the G loop formed by 4-3-2r-2f G branches 3 and 2r are in opposite directions, and so are B branches 3 and 2r in the B loop, Theorem 3 is fulfilled and, hence, the following translinear relations are satisfied:

$$I_1 = I_{f,2}$$
$$I_{f,2} I_3 = I_{r,2} I_4. \tag{37}$$

On the other hand, by (36)

$$I_2 = I_{f,2} - I_{r,2}. \tag{38}$$

Solving (37)–(38) yields

$$I_1 = \frac{I_4 - I_3}{I_4}. \tag{39}$$

Since $I_3 = I_2$ the output of the circuit is

$$I_3 = \frac{I_1 I_4}{I_1 + I_4}. \tag{40}$$

VI. Conclusions

A general translinear principle for analyzing and searching new circuit topologies for subthreshold MOS transistors is provided. This principle takes into account the presence of the bulk terminal and provides the topological conditions under which subthreshold MOS devices satisfy translinear relations in an exact manner, without having to short circuit bulk and source terminals of all transistors. Several corollaries are derived from the generalized subthreshold MOS translinear theorem. Finally, it is also shown how the principle can be extended to subthreshold MOS transistors operating in ohmic region.

References

[1] B. Gilbert, "Translinear circuits: A proposed classification," *Electron. Lett.*, vol. 11, no. 1, pp. 14–16, 1975.

[2] A. G. Andreou and K. A. Boahen, "Translinear circuits in subthreshold MOS," *J. Analog Integr. Circuits Signal Processing*, vol. 9, pp. 141–166, 1996.

[3] E. A. Vittoz, "Analog VLSI implementation of neural networks," in *Handbook of Neural Computation*. Cambridge: Institute of Physics and Oxford Univ. Press.

[4] B. A. Minch, C. Diorio, P. Hasler, and C. Mead, "Translinear circuits using subthreshold floating-gate MOS transistors," *J. Analog Integr. Circuits Signal Processing*, vol. 9, pp. 167–179, 1996.

[5] E. Seevinck and R. J. Wiegerink, "Generalized translinear circuit principle," *IEEE J. Solid-State Circuits*, vol. 26, pp. 1198–1102, Aug. 1991.

[6] D. R. Frey, "Log-domain filtering: An approach to current-mode filtering," *Proc. Inst. Elec. Eng.*, vol. 140, pt. G, pp. 406–416, Dec. 1993.

[7] E. A. Vittoz and J. Fellrath, "CMOS analog integrated circuits based on weak inversion operation," *IEEE J. Solid-State Circuits*, vol. 12, pp. 224–231, Jun. 1977.

[8] E. A. Vittoz, "Micropower techniques," in *VLSI Circuits for Telecommunications*, Y. P. Tsividis and P. Antognetti, Eds. Englewood Cliffs, NJ: Prentice-Hall, 1985.

[9] C. A. Mead, *Analog VLSI and Neural Systems*. Reading, MA: Addison–Wesley, 1989.

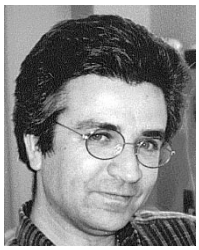
[10] Y. Tsividis, *Operation and Modeling of the MOS Transistor*. New York: McGraw-Hill, 1988.

[11] T. Delbrück, "Bump' circuits for computing similarity and dissimilarity of analog voltages," in *Proc. Int. Joint Conf. Neural Networks*, Seattle WA, 1991, pp. 475–479.

Teresa Serrano-Gotarredona received the B.S. degree in electronic physics and the Ph.D. degree in VLSI neural categorizers from the University of Seville, Sevilla, Spain, in 1992 and 1996, respectively, and the M.S. degree in electrical and computer engineering from the Johns Hopkins University, Baltimore, MD, in 1997, where she was sponsored by a Fulbright Fellowship.

She is now a Research Staff Member at the Analog Design Department, National Microelectronics Cente, Sevilla, Spain. Her research interests include analog circuit design of linear and nonlinear circuits, VLSI neural-based pattern recognition systems, VLSI implementations of neural computing and sensory systems, and VLSI electrical parameter characterization. She is coauthor of the book *Adaptive Resonance Theory Microchips*.

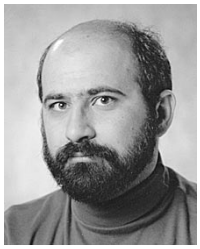
Dr. Serrano-Gotarredona was corecipient of the 1995–1996 IEEE Transactions on Very Large Scale Integration Systems Best Paper Award and the recipient of a Fulbright Fellowship.



Bernabé Linares-Barranco received the B.S. degree in electronic physics, the M.S. degree in microelectronics, and the Ph.D. degree in high-frequency OTA-C oscillator design from the University of Seville, Sevilla, Spain, in 1986, 1987, and 1990, respectively, and the Ph.D. degree in analog neural network design from Texas A&M University, College-Station, TX, in 1991.

Since September 1991 he has been a Senior Researcher with the Analog Design Department, National Microelectronics Center, Sevilla, Spain. From September 1996 to August 1997, he was on sabbatical at the Department of Electrical and Computer Engineering, the Johns Hopkins University, Baltimore, MD. He has been involved with circuit design for telecommunication circuits, VLSI emulators of biological neurons, VLSI neural-based pattern recognition systems, hearing aids, precision circuit design for instrumentation equipment, bio-inspired VLSI vision processing systems, and VLSI electrical parameters characterization. He is coauthor of the book *Adaptive Resonance Theory Microchips*.

Dr. Linares-Barranco was corecipient of the 1995–1996 IEEE Transactions on Very Large Scale Integration Systems Best Paper Award. He organized the 1994 Nips Post-Conference Workshop on neural hardware engineering. Since July 1997, he has been Associate Editor of the IEEE Transactions on circuits and Systems—II and, since January 1998, he has been Associate Editor for the IEEE Transactions on Neural Networks.



Andreas G. Andreou received the M.S.E. and Ph.D. degrees in electrical engineering and computer science from the Johns Hopkins University, Baltimore, MD, in 1983 and 1986, respectively.

From 1987 to 1989 he was a Postdoctoral Fellow and Associate Research Scientist at Johns Hopkins, where he became Assistant Professor in 1989, Associate Professor in 1993, and Professor in 1997. His research interests are in the areas of device physics, integrated circuits, and neural computation. He is coauthor of the book *Adaptive Resonance Theory Microchips*.

Dr. Andreou is a member of Tau Beta Pi.