A generalized CMOS-MEMS platform for micromechanical resonators monolithically

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A generalized CMOS-MEMS platform for micromechanical resonators monolithically integrated with circuits

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Abstract

A generalized foundry-oriented CMOS-MEMS platform well suited for integrated micromechanical resonators alongside IC amplifiers has been developed for commercial multi-user purpose and demonstrated with a fast turnaround time of only 3 months and a variety of design flexibilities for resonator applications. With this platform, different configurations of capacitively-transduced resonators monolithically integrated with their amplifier circuits, spanning frequencies from 500 kHz to 14.5 MHz, have been realized with resonator Q's ranging between 700 and 3500. This platform, specifically featured with various configurations of structural materials, multi-dimensional displacements, different arrangements of mechanical boundary conditions, tiny supports of resonators, large transduction areas, well-defined anchors and performance enhancement scaling with IC fabrication technology, offers a variety of flexible design options targeted for sensor, timing reference, and RF applications. In addition, resonators consisting of metal-oxide composite structures fabricated by this platform offer an effective temperature compensation scheme for the first time in CMOS-MEMS resonators, showing TC_f six times better than that of resonators merely made by CMOS metals.

(Some figures in this article are in colour only in the electronic version)

1. Introduction

The present wireless transceivers composed of conventional off-chip mechanical resonators for frequency generation and frequency selection substantially limit the miniaturization of communication apparatus as well as impede the reduction of cost and system integration for future portable electronics. In order to reduce size, power consumption, and simultaneously enhance device performance, vibrating micromechanical circuits fabricated using IC-compatible MEMS technologies have been developed toward the integration of on-chip RF functionalities [1].

However, prior approaches for merged MEMS/transistor technologies, such as mixed process [2, 3], MEMS-first [4, 5], and MEMS-last [6, 7] strategies, require enormous complexity and compromise of fabrication processes, hence impeding the fast cycling time of modern product development and,

of course, causing huge barriers for industrial design houses. For example, mixed process approaches [2, 3] for CMOS-MEMS integration require multiple passivation and protection steps interleaved between the MEMS and circuit process, resulting in not only a large number of masks but a customized process for each product. Such characteristics cause long development time and significant cost. On the other hand, the MEMS-first process produces microstructure topography which would interfere with the succeeding lithography for advanced circuits, thereby necessitating trenches to accommodate microstructures followed by planarization for later electronics [4] at the expense of process complexity. In addition, lithography and etching of MEMS structures would be very difficult in trenches, especially unsuitable for RF MEMS resonators which usually require much smaller feature size than other MEMS applications. Furthermore, MEMS-first might have contamination issues for conventional

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IC industries [5]. In contrast, MEMS-last approaches [6, 7] suffer restricted thermal budget of post-CMOS processing temperature and limited set of usable structural materials, resulting in a workable but not the best solution for integration.

As a solution to the aforementioned issues, foundry-oriented CMOS-MEMS platforms such as dry-release-based [8–11] (Fedder's group) and wet-release-based [12–17] (Barniol's group) approaches provide ease of use, fast prototyping, and inherently circuit-integrated characteristics for vibrating RF-MEMS applications. Nonetheless, Fedder's group confronted high motional impedance of their fabricated resonators due to the relatively large electrode-to-resonator gap spacing (1–2 μm) from RIE-etched constraint while both Fedder's and Barniol's groups suffered a deficiency in design flexibility on configurations of structural materials, mechanical boundary conditions, vibrating modes, multi-dimensional motions and well-defined anchor geometry without affecting release undercut.

To overcome the above-mentioned deficiency, this paper details a newly developed CMOS-MEMS platform [18] utilizing TSMC 0.35 μm 2-poly-4-metal process with a simple maskless release process, successfully demonstrating ease of use, low cost, fast turnaround time and innate MEMS-circuit integration. Various configurations of capacitively-transduced CMOS-MEMS resonators monolithically integrated with amplifier circuits have been demonstrated using this platform with resonance frequencies spanning from 0.5 to 14.5 MHz and with Q's up to 3500. Thermal stability of resonators fabricated in this platform was experimentally characterized and reported for the first time in any CMOS-MEMS resonators. To alleviate the substantial temperature coefficient of frequency (TC_f) for metal-type CMOS-MEMS resonators, our proposed metal-oxide composite resonators show considerable temperature compensation capability with a linear TC_f of only -59.7 ppm $^\circ$C^{-1}, achieving more than six times improvement of TC_f compared to that of metal-type CMOS-MEMS resonators. In addition, the stress-induced deformation of composite structures is also greatly mitigated. In terms of device performance, the motional impedance R_m, electrical stiffness k_e and power handling capability of the fabricated CMOS-MEMS resonators would then be addressed and characterized in this paper. To further evaluate the potential of this platform for RF-MEMS applications, the major bottleneck of capacitive resonators due to their high motional impedance R_m would be greatly alleviated since the electrode-to-resonator gap spacing d_o, the R_m of which is proportional to the fourth power, can be easily scaled down in this platform with advanced IC technologies, e.g., 0.18 μm or even a smaller feature-sized CMOS process, while other CMOS-MEMS platforms [8–17] show difficulties in moving to advanced technologies due to limitation on fabrication and advanced CMOS configurations. Furthermore, the design and simulation of the CMOS trans-impedance amplifier to enhance the motional current of CMOS-MEMS resonators and convert such current to voltage output would be addressed. Finally, fully integrated CMOS-MEMS resonator circuits occupying a die area of only 340 μm × 110 μm were measured to demonstrate the advantages of monolithic integration.

2. CMOS-MEMS platform and device operation

To demonstrate most of the new features used in this platform, a laterally vibrating free–free beam resonator [19] with a metal-oxide composite structure and with via-supported scheme, as shown in figure 1(*a*), is exemplified here using existing materials of the CMOS 0.35 μm 2-poly-4-metal process with a cross-section view depicted in figure 1(*b*). Such a composite resonator structure is formed utilizing metal (i.e. aluminum and tungsten) and enclosed SiO$_2$ while supported by CMOS vias (VIA) and contacts (CO), as shown in figure 1(*a*), which serve not only as electrical interconnects but also as mechanical supports to effectively preserve vibrating energy within resonator bodies due to the tiny size of these supports. As also shown in figure 1(*a*), an on-chip trans-impedance amplifier is integrated with this free–free beam resonator to resolve (i) feedthroughs from bond pads and (ii) impedance mismatches between resonators and 50 Ω-based testing facilities, therefore allowing us to measure the motional current induced by vibrating motions of resonators without the masking effects from parasitic feedthroughs. In addition, integration of MEMS and circuits eliminating bond pads and wires achieves much smaller form factor for future portable electronics applications.

2.1. Merits of the CMOS-MEMS platform

To maximize the electromechanical coupling coefficient, the minimum lateral electrode-to-resonator gap spacing of 0.5 μm of figure 1(*b*) in this 0.35 μm CMOS foundry process is formed between two smooth sidewalls of the metal/via composite where the transduction areas are greatly improved, allowing smaller motional impedance of these fabricated resonators.

As shown in figure 2, CMOS-MEMS resonators fabricated using the proposed platform specifically possess several unique features including (i) complex structural materials which can be made of the metal/oxide composite (case I and also shown in figure 1(*a*)), metal composite (case II) and metal alone (case III); (ii) various mechanical boundary conditions for resonators such as fixed (not shown here), pinned–pinned (i.e. simple supports) boundary (case II), and free–free boundary (cases I and III) designs; (iii) multi-dimensional displacements of resonators capable of in-plane (cases I and II) and out-of-plane (case III) motions with respect to the substrate surface; (iv) standard CMOS vias (VIA) and contacts (CO) acting as tiny supports of resonators (cases I and II), to effectively isolate the vibrating energy from resonators to their anchors; (v) well-defined anchors without the undercut issue which is often seen in conventional CMOS-MEMS [8–17] or SOI process [20]; (vi) better transducer efficiency attained by utilizing via-connected walls (cases I and II) to form flat sidewall electrodes, all of which offer a variety of flexible options suited for sensor and RF applications.

To reduce the TC_f of conventional MEMS resonators for precise frequency generation, a coated silicon dioxide film with a positive temperature coefficient of Young's modulus ($TC_E \sim +185$ ppm $^\circ$C^{-1}) has been commonly utilized to compensate the negative temperature coefficient of Young's
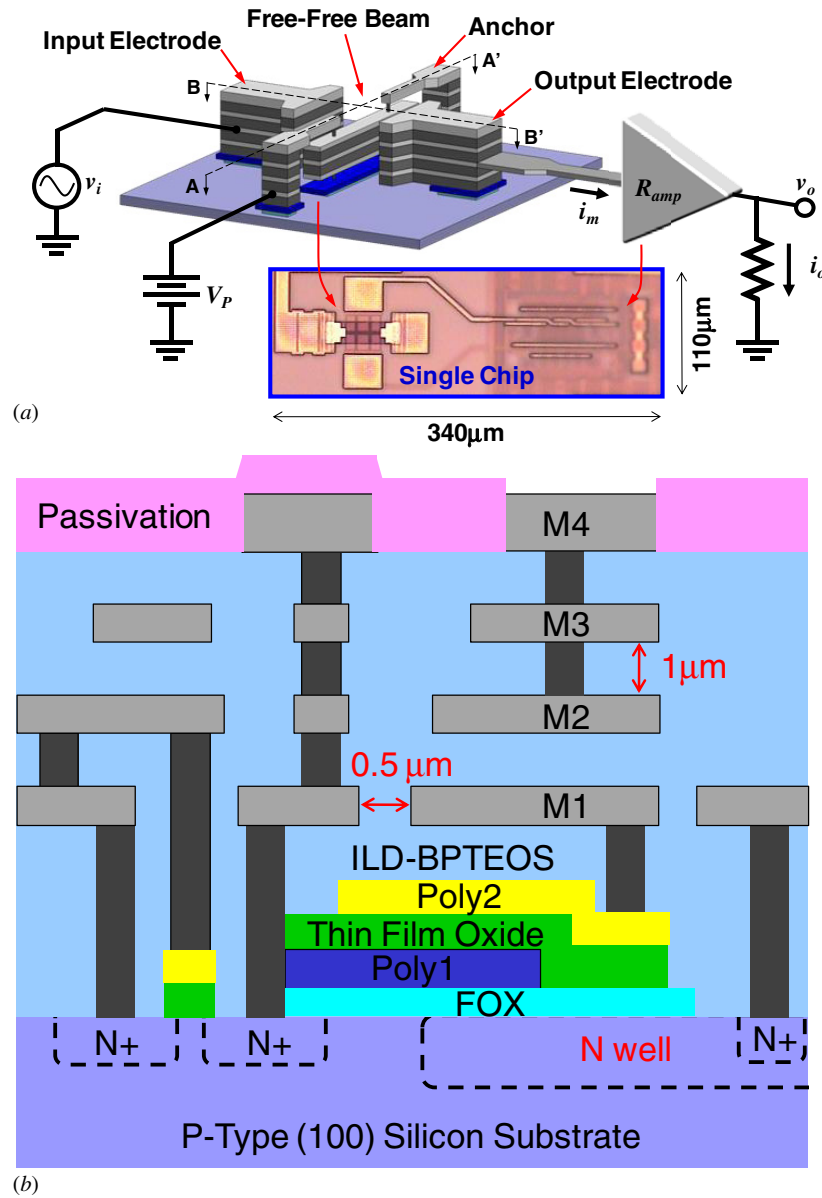
Figure 1. Case I: in-plane Al/W/SiO$_2$ free–free beam. (*a*) Perspective view schematic of a CMOS-MEMS via-supported free–free beam resonator monolithically integrated with an amplifier circuit. (*b*) Cross-section view of a TSMC 0.35 μm 2-poly-4-metal CMOS process utilized to achieve the proposed CMOS-MEMS platform.

modulus (TC_E) of resonators made of silicon [21], AlN [22] and metal [23], thereby resulting in an overall smaller TC_f of these composite resonators. As mentioned above, this platform offering a unique feature of via-connected sidewalls allows a considerable portion of SiO$_2$ enclosed inside resonator structures after the release process, hence achieving significant temperature compensation with the TC_f of -59.7 ppm °C^{-1} for composite resonators in this work, although not as good as resonators made of single-crystal silicon, polysilicon or AlN, but at least comparable to ZnO and LiNbO$_3$. Without the help of enclosed SiO$_2$, mere metal resonators fabricated in this platform behave with much worse TC_f of -358 ppm °C^{-1}. Table 1 presents the comparison of different CMOS-MEMS resonator platforms worldwide in terms of platform capability and resonator characteristics, clearly showing the unique features and advantages of this work

including more design flexibility, lower motional impedance, additional temperature compensation functionality and scaling with advanced CMOS technologies.

2.2. Composite resonator modeling and operation

To excite a CMOS-MEMS composite resonator (shown in figure 3(*a*) for typical two-port testing configuration and in figure 3(*b*) for theoretical modeling), an input ac signal v_i applied onto the input electrode together with a dc-bias voltage V_P applied on the resonator structure would generate an electrostatic force governed by

$$F_d = V_P \frac{\partial C}{\partial y} v_i \tag{1}$$

where $\partial C/\partial y$ is the change in electrode-to-resonator capacitance per unit displacement of the resonator. To obtain
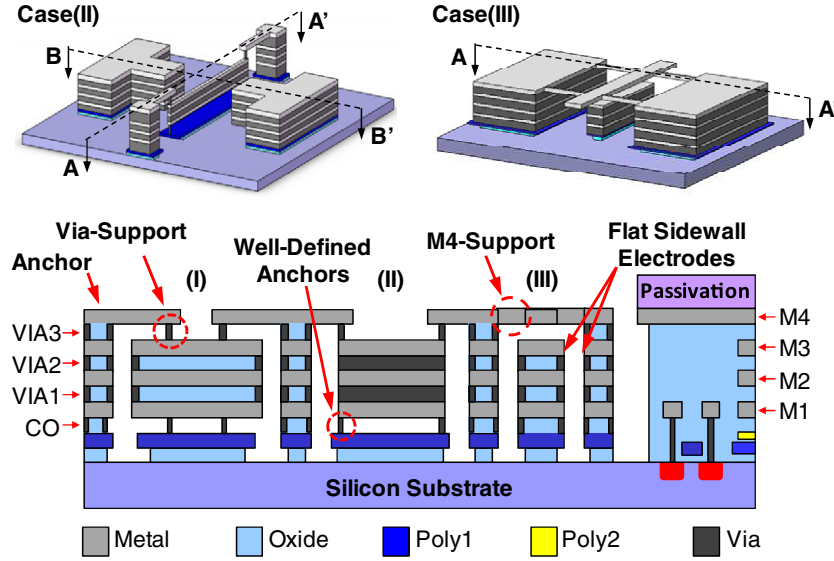
Figure 2. Case II: in-plane Al/W pinned–pinned beam. Case III: out-of-plane Al free–free beam. Cross-section views (A–A′) of various CMOS-MEMS resonators fabricated using the proposed platform. Case I refers to the A–A′ cross-section of figure 1(*a*).
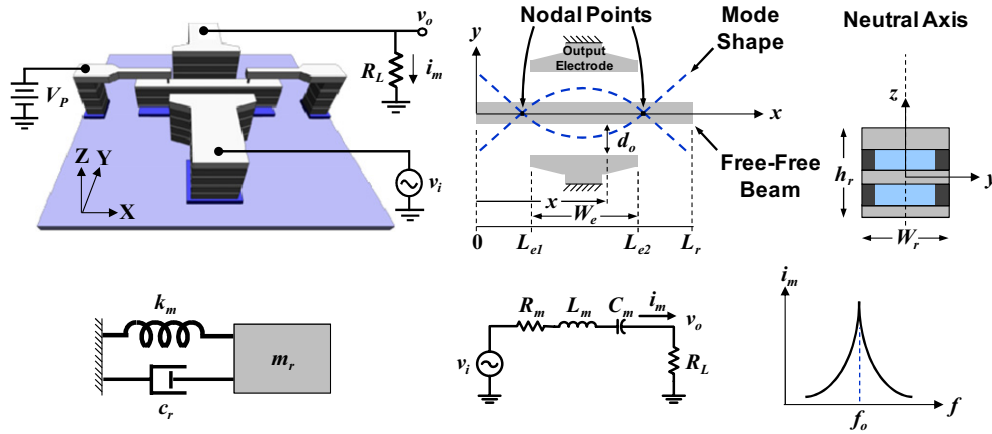

Figure 3. (*a*) Two-port measurement setup, (*b*) resonator cross-section views identifying key parameters for theoretical modeling, (*c*) equivalent lumped mechanical circuit, (*d*) equivalent *RLC* circuit and (*e*) high-Q bandpass biquad behavior for the CMOS-MEMS via-supported free–free beam resonator.

the mechanical resonance frequency of a composite structure, each layer of the composite beam resonator is assumed to have ideal attachment to its adjacent layers. Consequently, the overall mechanical stiffness of the composite beam resonator can be regarded as a shunt combination of stiffness in all layers using the Euler–Bernoulli approach, leading to a nominal mechanical resonance frequency of the composite resonator given by

$$f_{\text{nom}} = \frac{1}{2\pi}\sqrt{\frac{k_m(x)}{m_r(x)}} = \frac{1}{2\pi}(\beta_1 L_r)^2 \sqrt{\frac{\sum(E_i I_i)}{\sum(\rho_i A_i)}}\frac{1}{L_r^2} \quad (2)$$

where $k_m(x)$ and $m_r(x)$ are the mechanical stiffness (without electromechanical coupling) and effective mass, respectively, at location x on the beam resonator, L_r is the length of the beam, β_1 represents the frequency parameter of the fundamental mode of the beam with $(\beta_1 L_r)$ equal to 4.73, i represents the corresponding CMOS structural materials (for example, metal, tungsten and silicon dioxide) and E, ρ, A and I are the Young's modulus, density, cross-section area and moment

of inertia of each structural layer, respectively. Note that via-walls, different from other layered materials, are away from the neutral axis of the composite beam, so the parallel axis theorem should be considered to calculate the effective moment of inertia of via-walls.

Under excitation of the electrostatic force of (1), the resonator would then vibrate as the frequency of v_i matches the effective resonance frequency f_o (including effects of electromechanical coupling) of the beam given by [24]

$$f_o = \frac{1}{2\pi}\sqrt{\frac{k_r(x)}{m_r(x)}} = \frac{1}{2\pi}\sqrt{\frac{k_m(x) - k_e(x)}{m_r(x)}}$$

$$= \frac{1}{2\pi}\sqrt{\frac{k_m(x)}{m_r(x)}}\left[1 - \left\langle\frac{k_e}{k_m}\right\rangle\right]^{1/2} \quad (3)$$

where $k_r(x)$ is the effective stiffness (including electromechanical coupling) at location x on the beam resonator and k_e is the electrical stiffness which can be utilized for frequency tuning

Table 1. Comparison between different CMOS-MEMS platforms using foundry-oriented 0.35 μm processes for resonator applications.

	Capability/characteristic	Fedder group CMU [8–11]	Barniol group UAB [12–17]		This work NTHU		
Platform capability	Foundry	JAZZ 0.35 μm	AMS 0.35 μm		TSMC 0.35 μm		
	Post process	Dry etching (RIE + SF$_6$)	Wet etching		Wet etching		
	Minimum gap spacing, d_o	1.3 μm	40 nm[a], 150 nm[a], 650 nm[b]		0.5 μm[c], 1 μm[d]		
	Motion	In-plane	In-plane/out-of-plane		In-plane/out-of-plane		
	Used material	Al/W/SiO$_2$	Al, Poly		Al/W/SiO$_2$, Al/W, Al		
	Level of structural configuration	Low	Medium		High		
	Tiny support capability	Moderate	Good		Good		
	Transduction area, A_e	Large	Small		Large		
	Gap scaled down with the advanced CMOS process	Difficult	Difficult		Easy		
Measured characteristic	Testing environment	Vacuum	Vacuum	Air	Vacuum		
	dc-bias voltage, V_P (V)	54 20	90 5	10	22 20 90		
	Measured resonance frequency, f_o (Hz)	7.68 M 6.18 M	60 M 22 M	1.04 G	852 K 1.45 M 14.5 M		
	Resonant mode*	F-M SFR	C-C B C-C B	Ring	F-P P-PB F-F B		
	Structural material	Al/W/SiO$_2$	Al PolySi	PolySi	Al Al/W Al/W/SiO$_2$		
	Two-port direct-measured quality factor, Q	1591 996	– 4400	400	3500 810 1590		
	f_o^*Q product	1.2×10^{10} 6.2×10^9	– 9.7×10^{10}	4×10^{11}	3×10^9 1×10^9 2.3×10^{10}		
	Two-port direct-measured motional impedance, R_m (Ω)	N/A	300 M N/A		30.9 k 7.08 M 5.26 M (70 V)		
	Temp. coeff. of freq., TC_f (ppm $^\circ$C^{-1})	N/A	N/A		Al Metal/oxide		
					-358 -59.7		

[a] For PolySi resonators, [b]for metal resonators, [c]for lateral motion, [d]for vertical motion.
*F-M: flexural mode, SFR: square frame resonator (first mode), C-C B: clamped–clamped beam, F-P: flexural plate, P-P B: pinned–pinned beam, F-F beam: free–free beam.

as will be described later in figure 13. The quantity $\langle k_e/k_m \rangle$ is given by [24]

$$\left\langle \frac{k_e}{k_m} \right\rangle = V_P^2 \frac{\varepsilon_o h_r}{d_o^3} \int_{L_{e1}}^{L_{e2}} \frac{\mathrm{d}x}{k_m(x)} \qquad (4)$$

where h_r and d_o are the thickness and electrode-to-resonator gap spacing, respectively, of a given resonator, ε_o is the permittivity in vacuum, $L_{e1} = 0.5(L_r - W_e)$ and $L_{e2} = 0.5(L_r + W_e)$ for a centered electrode and all other geometric variables are given in figure 3(b).

For the purposes of oscillator and filter designs, it is convenient to define an equivalent mass-spring-damper mechanical circuit as depicted in figure 3(c). With reference to figure 3(b), the equivalent mass, spring stiffness, damping factor of figure 3(c) can be expressed as [24]

$$m_r(x) = \frac{\rho_{\mathrm{eff}} W_r h_r \int_0^{L_r} [Y_{\mathrm{mode}}(x)]^2 \, \mathrm{d}x}{[Y_{\mathrm{mode}}(x)]^2}$$

$$\text{where} \quad \rho_{\mathrm{eff}} = \frac{\sum(\rho_i A_i)}{\sum A_i} \qquad (5)$$

$$k_r(x) = (2\pi f_o)^2 m_r(x) \qquad (6)$$

$$c_r(x) = \frac{\sqrt{k_r(x)m_r(x)}}{Q} \qquad (7)$$

where W_r, ρ_{eff} and Q are the width, effective density and quality factor, respectively, of the resonator and where the mode shape function $Y_{\mathrm{mode}}(x)$ is

$$Y_{\mathrm{mode}}(x) = \cosh(\beta_1 x) + \cos(\beta_1 x) - \xi[\sinh(\beta_1 x) + \sin(\beta_1 x)] \qquad (8)$$

where

$$\xi = \frac{\cosh(\beta_1 L_r) - \cos(\beta_1 L_r)}{\sinh(\beta_1 L_r) - \sin(\beta_1 L_r)} \qquad (9)$$

Nodal points can be obtained by setting (8) to zero and solving for x to allow via supports at this location to preserve high Q.

At the resonance frequency, the composite beam vibrates into a corresponding mode shape shown in figure 3(b). This motion creates time-varying capacitance between the beam and output electrode, thereby sourcing out an output motional current i_m governed by

$$i_m = V_P \frac{\partial C}{\partial y} \frac{\partial y}{\partial t} \qquad (10)$$

where $\partial y/\partial t$ represents the velocity of the resonator. With the use of electromechanical analogy, the vibrating mechanical structure can be modeled as an equivalent *RLC* circuit shown in figure 3(d), where the motional inductance, motional capacitance and motional impedance are given by the general expressions as

$$L_m = \frac{m_{\mathrm{re}}}{\eta_e^2}; \qquad C_m = \frac{\eta_e^2}{k_{\mathrm{re}}}; \qquad R_m = \frac{\sqrt{k_{\mathrm{re}}m_{\mathrm{re}}}}{Q\eta_e^2} \qquad (11)$$

where m_{re} (i.e. $m_r(L_r/2)$) and k_{re} (i.e. $k_r(L_r/2)$) are effective mass and spring stiffness at the center location of the beam and where η_e is the electromechanical coupling coefficient which can be written as [24]
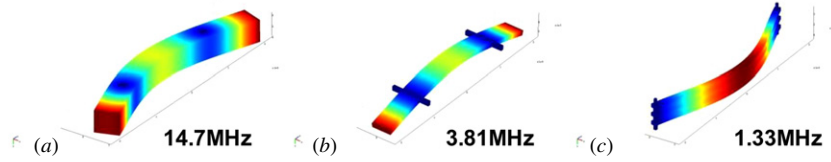
Figure 4. Finite-element simulated mode shapes for the CMOS-MEMS (*a*) in-plane Al/W/SiO$_2$ composite resonator, (*b*) out-of-plane Al resonator, and (*c*) in-plane Al/W composite resonator.
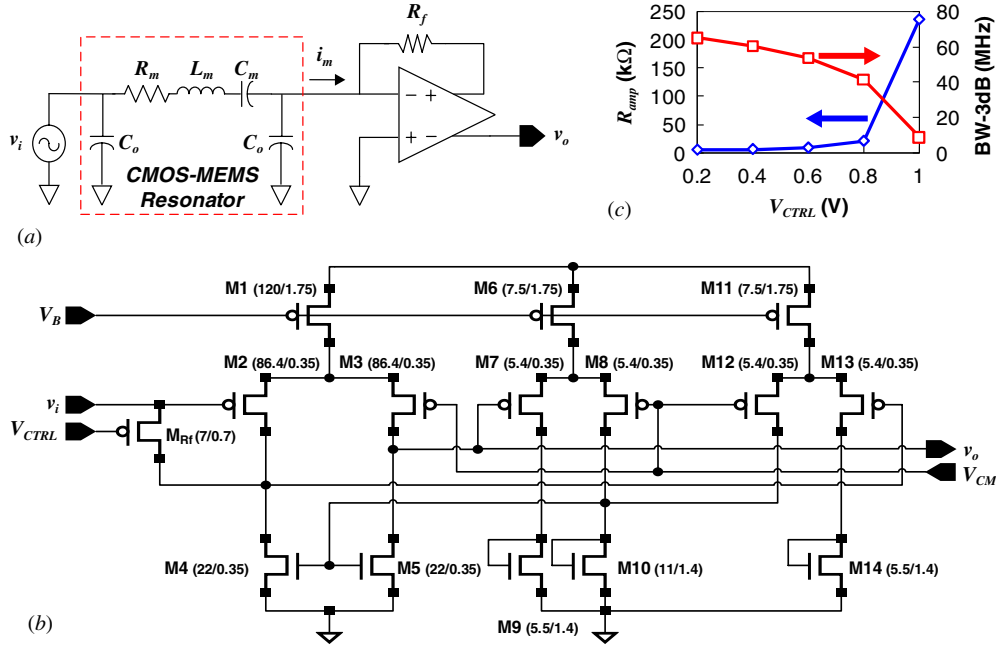

Figure 5. (*a*) Top-level circuit schematic, (*b*) detailed circuit schematic (including transistor dimensions) and (*c*) impedance gain R_{amp} and 3 dB bandwidth versus adjusted voltage V_{CTRL} of the single-stage trans-impedance amplifier used in this work.

$$\eta_e = V_P \frac{\partial C}{\partial y} = V_P \frac{\varepsilon_o h_r (k_{re})^{1/2}}{d_o^2}$$
$$\times \sqrt{\int_{L_{e1}}^{L_{e2}} \left[\int_{L_{e1}}^{L_{e2}} \frac{dx}{k_r(x) Y_{mode}(x)} \right] \cdot Y_{mode}(x) \, dx}. \quad (12)$$

In the light of the low-loss nature of mechanical vibration, the output motional current i_m versus frequency yields a high-Q bandpass biquad frequency spectrum as shown in figure 3(*e*). Figure 4(*a*) shows the finite-element simulated mode shape for an in-plane composite via-supported free–free beam of case I in figure 1(*a*), while figures 4(*b*) and (*c*) present vibrating mode shapes for the out-of-plane free–free beam of case III and the in-plane via-supported pinned–pinned beam of case II in figure 2, respectively.

2.3. CMOS readout circuitry

The key feature of capacitive resonators is the motional impedance R_m which can be derived from (11) and (12) with an expression given by

$$R_m = \frac{d_o^4}{2\pi f_o Q V_P^2 \varepsilon_o^2 h_r^2}$$
$$\times \left[\int_{L_{e1}}^{L_{e2}} \left(\int_{L_{e1}}^{L_{e2}} \frac{dx}{k_r(x) Y_{mode}(x)} \right) \cdot Y_{mode}(x) \, dx \right]^{-1}. \quad (13)$$

From (13), the most dominant factor of a capacitive resonator to achieve low motional impedance is its gap spacing d_o the R_m of which is proportional to the fourth power. In the 0.35 μm CMOS process, the minimum in-plane gap spacing of 0.5 μm as indicated in figure 1(*b*) still yields enormous motional impedance, such as several MΩ, considerably impeding the measurement of the motional current i_m due to impedance mismatch between measured resonators and test equipment usually with 50 Ω input impedance. Hence, a trans-impedance amplifier (TIA) was designed as a readout circuit and used to transfer and amplify the weak motional current of resonators into measurable voltage output.

Figure 5(*a*) presents the top-level circuit schematic of the trans-impedance amplifier (TIA) used in this work to transfer the motional current i_m of vibrating resonators into voltage output v_o with a certain amplification factor R_f. In the detailed circuit schematic of figure 5(*b*), the transistors M_1–M_5 comprise the basic single stage, differential op amp serving as gain stage, while M_6–M_{14} constitute a common-mode feedback (CMFB) circuit that sets its output dc bias point. The bias voltage V_B is applied to the gates of M_1, M_6 and M_{11} with a proper value to ensure that the operation of these tail current sources is in the saturation region. The MOS resistor M_{Rf} working in the triode region provides the resistance R_f and serves as a shunt–shunt feedback element that allows control of the trans-impedance gain via adjustment
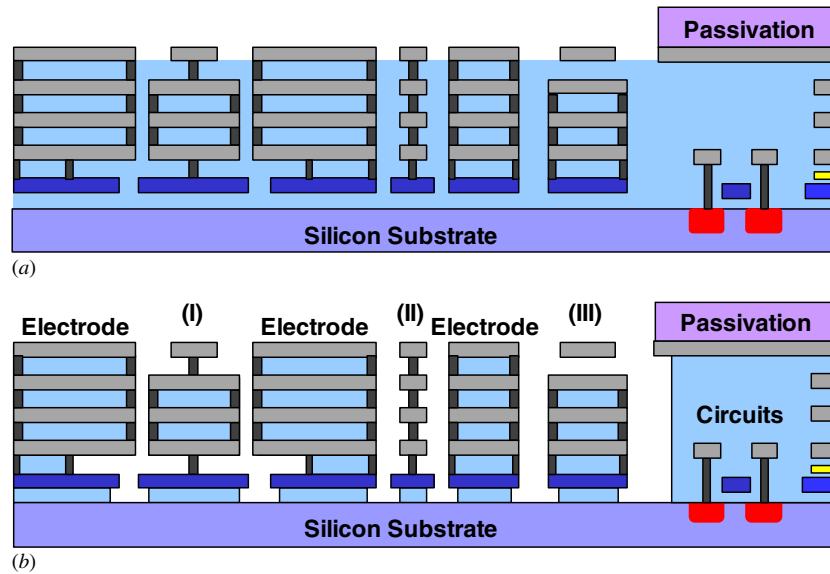
Figure 6. Cross-sections depicting the fabrication process used to achieve CMOS-MEMS resonators in this work. (*a*) After the standard CMOS process, (*b*) after the wet release process. Various types of resonators are realized using this platform, including (I) via-supported free–free beam (B–B′ of case I in figure 1(*a*)), (II) via-supported pinned–pinned beam (B–B′ of case II in figure 2), and (III) metal free–free beam (A–A′ of case III in figure 2).

Table 2. Trans-impedance amplifier design summary.

Specifications	Pre-simulation	Post-simulation
Supply voltage, V_{DD}	3.3 V	
Control voltage, V_{CTRL}	1 V	
Bias voltage, V_B	2.4 V	
Impedance gain, R_{amp}	236.28 kΩ	236.53 kΩ
3 dB bandwidth	17.8 MHz	9.0 MHz
Total current	88.258 μA	88.251 μA
Power consumption	291.25 μW	291.23 μW
Input referred current noise @ 10 MHz	342 fA (Hz)$^{-1/2}$	373 fA (Hz)$^{-1/2}$
Circuit area	200 μm × 110 μm	

of its gate voltage V_{CTRL}. The dimensions of each transistor used in this work are specified in figure 5(*b*). Figure 5(*c*) finally presents the post-simulated (including the parasitic extraction of CAD layout) trans-impedance gain R_{amp} and 3 dB bandwidth versus V_{CTRL}-bias adjustment of the feedback resistor M_{Rf}, showing R_{amp} increase and bandwidth decrease as V_{CTRL} increases. This tunable gain provides additional flexibility to measure CMOS-MEMS resonators with different motional impedance R_m. Table 2 summarizes the presimulation (schematic only) and post-simulation results of figure 5(*b*) under the fixed control voltage V_{CTRL} and bias voltage V_B, indicating that the impedance gain and bandwidth are suitable for readout functions of resonators in this work with proper noise performance and power consumption.

3. Fabrication

To fabricate resonators using the presented platform, chips were manufactured utilizing standard 0.35 μm 2-poly-4-metal CMOS service from TSMC with a cross-section view shown in figure 6(*a*), including two polysilicon layers underneath

four metal (i.e. aluminum) layers. In addition, CMOS circuit areas are masked by the passivation layer mostly comprised of silicon nitride while the MEMS regions (i.e. openings) expose sacrificial oxide to etchant solution. A commercial SiO_2 etchant, silox vapox III (from Transene Company, Inc.) [25], with very high selectivity to metal layers, vias (i.e. tungsten), and contacts (i.e. tungsten) is utilized to release the resonator structures as depicted in figure 6(*b*) without the help of critical point dryers, while the transistor circuits are still protected by the passivation layer. Thanks to the excellent selectivity of the SiO_2 etchant, the via-connected sidewalls (tungsten), which are intact, not only increase the overall transduction areas but also protect the inner SiO_2 from attack by the release etchant, hence providing the metal/oxide composite which greatly benefits the temperature compensation scheme [21] for future timing reference devices since silicon dioxide inherently offers a positive temperature coefficient of Young's modulus (TC_E) which is opposite to that of most of the structural materials.

Figure 6(*b*) also presents a variety of resonators realized in this platform, just to name a few, including (case I) in-plane via-supported free–free beam resonator with Al/W/SiO_2 composite structure, (case II) in-plane via-supported pinned–pinned beam resonator with Al/W composite structure and (case III) out-of-plane free–free beam resonator with aluminum structural material. Figure 7 presents the SEMs of fabricated CMOS-MEMS resonators, showing (a) a chip global view after the release process, (b) an in-plane via-supported free–free beam as depicted in case I of figure 6(*b*), (c) an out-of-plane aluminum free–free beam as depicted in case III of figure 6(*b*), (d) an in-plane via-supported pinned–pinned beam as depicted in case II of figure 6(*b*) and (e) an out-of-plane aluminum flexural-mode plate, indicating that this platform is capable of producing resonators with
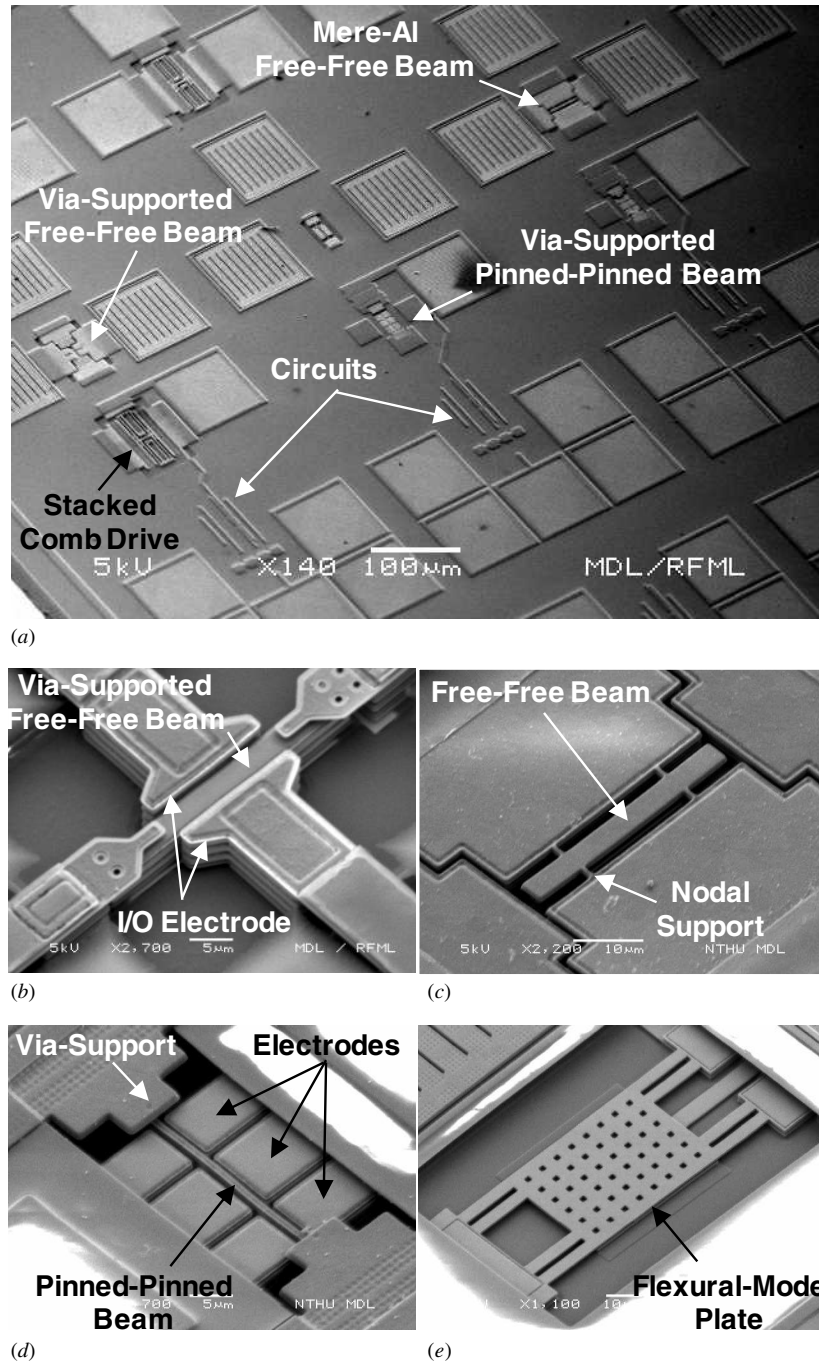
Figure 7. SEM views of fabricated CMOS-MEMS resonators. (*a*) Overall view of a chip. (*b*) In-plane via-supported free–free beam. (*c*) Out-of-plane metal free–free beam. (*d*) In-plane via-supported pinned–pinned beam. (*e*) Out-of-plane flexural-mode plate.

various modes, different mechanical boundary conditions, in-plane and out-of-plane motions and diversified supporting structures. During the wet release process of figure 6(*b*), device-mimic testkeys shown in the SEMs of figure 8 were etched with different time periods to monitor the release process, showing that the sacrificial oxide was gradually removed with the increase of release time, and at the end leaving via/contact supports and composite resonators intact. It is worth mentioning that such tiny supports made of vias or contacts provide excellent mechanical strength to support the resonator body even when a dc-bias voltage of more than

100 V is applied to the resonator structure. Please also note that the anchored plane in figure 8(*d*) is still intact, offering rigid anchor podiums without the undercut issue which is often seen in other fabrication technologies such as the SOI-based release process [20].

The issue of stress gradients on CMOS layers leads to structure bending or curving after release, and therefore often impedes the applications of CMOS-MEMS devices. To investigate the residual stresses of the fabricated CMOS-MEMS resonators, figure 9(*a*) presents the radius of curvature of −2.8 mm for a composite structure of figure 7(*b*), while
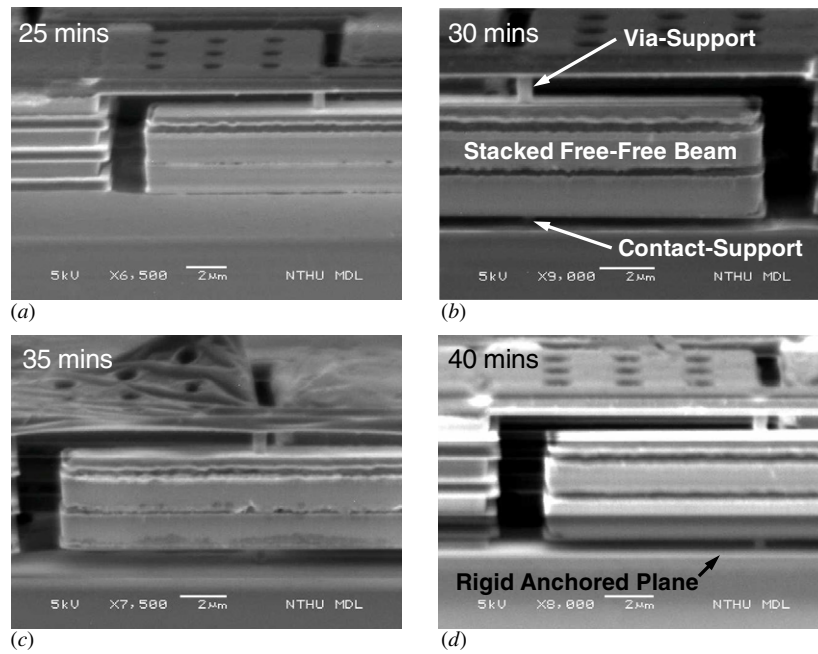
Figure 8. SEM views monitoring the wet release process for CMOS-MEMS resonators with (*a*) 25, (*b*) 30, (*c*) 35 and (*d*) 40 min release time periods.
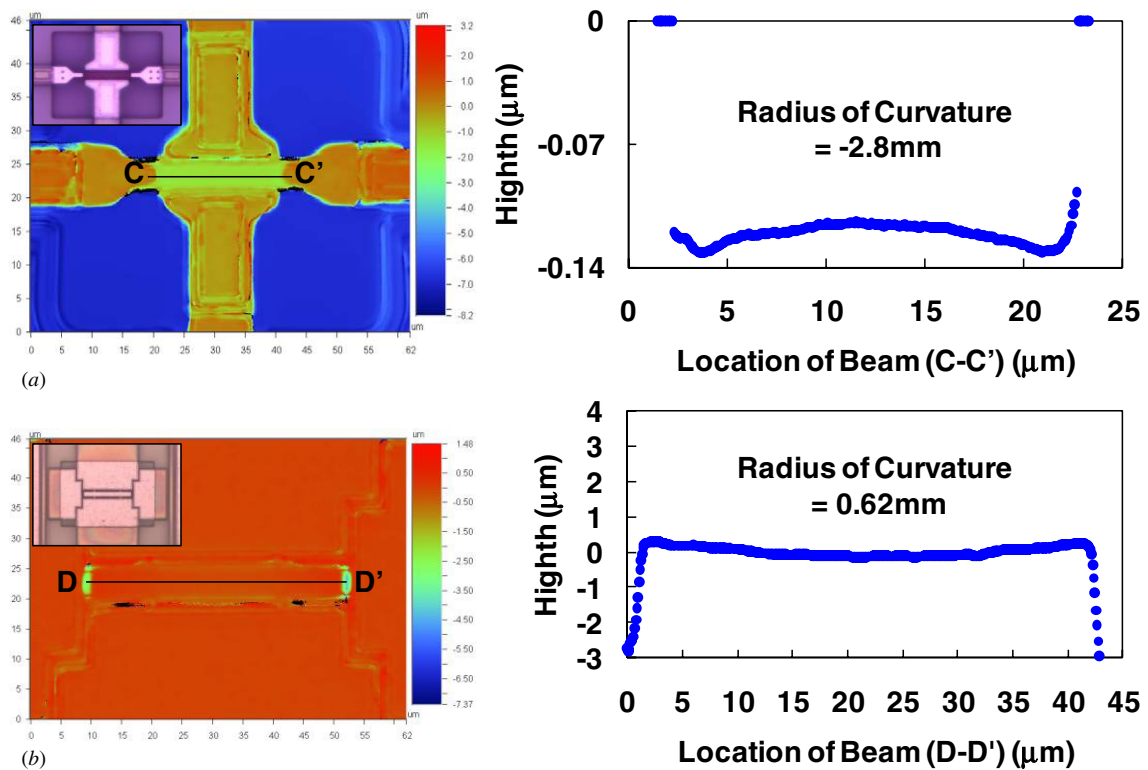

Figure 9. Radii of curvature caused by residual stress from CMOS layers for (*a*) metal-oxide composite structure of figure 7(*b*) and (*b*) metal structure of figure 7(*c*).

figure 9(*b*) shows the radius of curvature of 0.62 mm for the metal structure of figure 7(*c*) by use of the WYKO NT100 optical profiler. Such investigation reveals that the stress issue of CMOS-MEMS devices is greatly relieved once the composite structure is used.

4. Experimental results

The fabricated CMOS-MEMS resonators with their amplifier circuits (cf figure 7(*a*)) were mounted on top of the ceramic substrate by conductive silver paste and then wire-bonded to
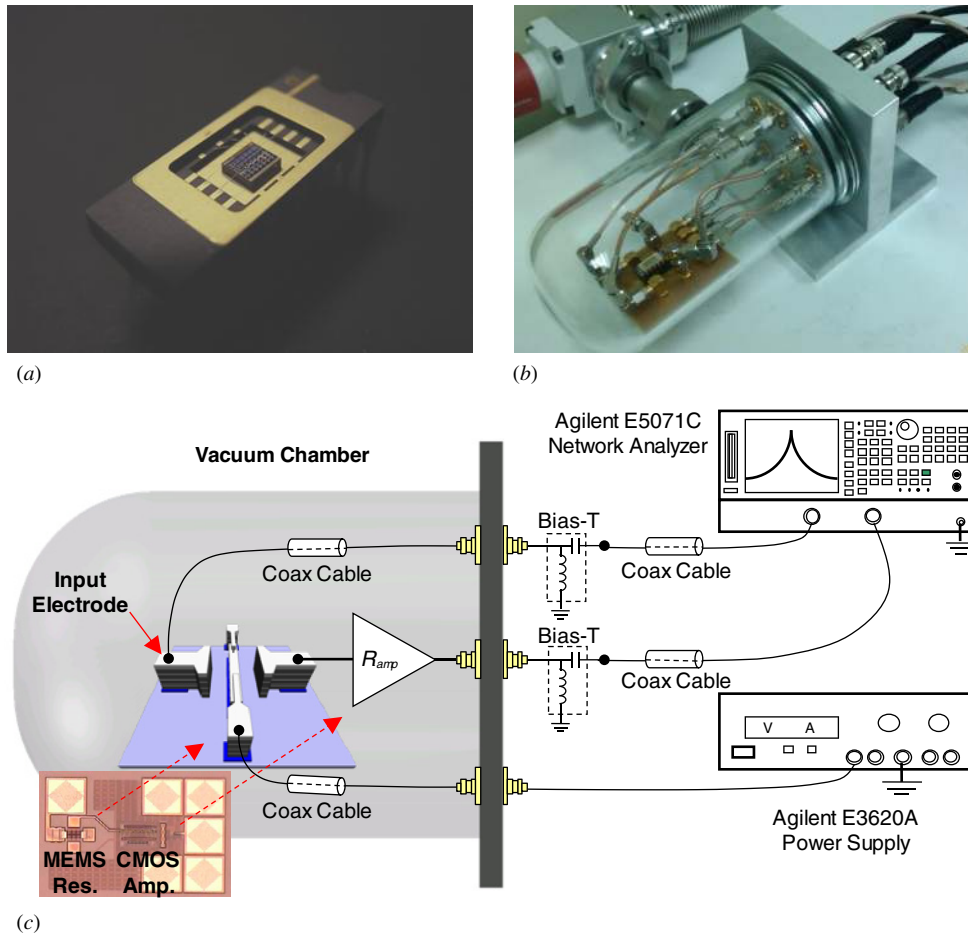
(*a*)   (*b*)

(*c*)

Figure 10. Physical measurement setup for fabricated CMOS-MEMS resonator circuits. (*a*) Tested die sitting on a ceramic housing. (*b*) Printed circuit board inside a vacuum chamber with all required electrical feedthroughs. (*c*) Schematic illustrating the measurement configuration, showing detailed connections of measurement instrumentation.

connect the electrical feedthroughs of the ceramic housing as shown in figure 10(*a*). This ceramic housing was placed on a printed circuit board. In order to reduce the damping effect often causing the *Q* degradation of capacitive resonators, the devices were tested under an environment of controlled pressure down to 20 μTorr using a custom-built chamber with an electrical hook-up shown in figure 10(*b*). Figure 10(*c*) presents the experimental setup for fabricated CMOS-MEMS resonators (including their associated circuits) with a conventional two-port configuration. The RF-out port of an Agilent 5071C network analyzer is directly connected to the input electrode of a CMOS-MEMS resonator inside the vacuum chamber, while the analyzer's RF-in port is connected to the output electrode of the associated CMOS amplifier circuit. A dc bias voltage V_P is applied onto the body of the resonator by Agilent E3620A power supply. The use of the bias-Tees in both the input and output paths prevents damage to the network analyzer once the breakdown of resonators occurs due to high bias voltage (V_P) operation.

Table 3 summarizes the design parameters, theoretical modeling, finite-element simulation and measurement results of CMOS-MEMS resonators used in this work including via-supported free–free beam with Al/W/SiO$_2$ composite structure, via-supported pinned–pinned beam with Al/W

composite structure and out-of-plane Al free–free beam resonators. Without the use of amplifier circuits, figure 11(*a*) presents measured transmission amplitude and phase versus frequency of an in-plane via-supported free–free beam resonator of figure 7(*b*) with metal–oxide composite structure under a bias voltage V_P of 70 V and a pressure of 20 μTorr (i.e. vacuum), showing the motional impedance R_m of 5.26 MΩ. Such a low transmission S$_{21}$ at resonance (i.e. a high impedance R_m) due to a relatively large electrode-to-resonator gap spacing d_o of 0.5 μm prevents the clear measurement of both the quality factor and the ideal 180° phase shift around resonance frequency. However, the measured result of such a standalone CMOS-MEMS resonator provides a valid verification of the R_m of theoretical modeling in (13). Referred to case I in table 3, the calculated R_m of 6.38 MΩ by the use of (13) is in good agreement with measured 5.26 MΩ since the lower value of measured data was mainly from the contribution of parasitic feedthrough current. In contrast, figure 11(*b*) shows the measured frequency characteristic of an out-of-plane flexural-mode plate resonator (cf figure 7(*e*)) with aluminum structural material under a bias of 22.2 V in vacuum, demonstrating *Q* of 3500 and a clear 180° phase transition at 852 kHz with R_m of only 30.9 kΩ due to its large transduction area and relatively
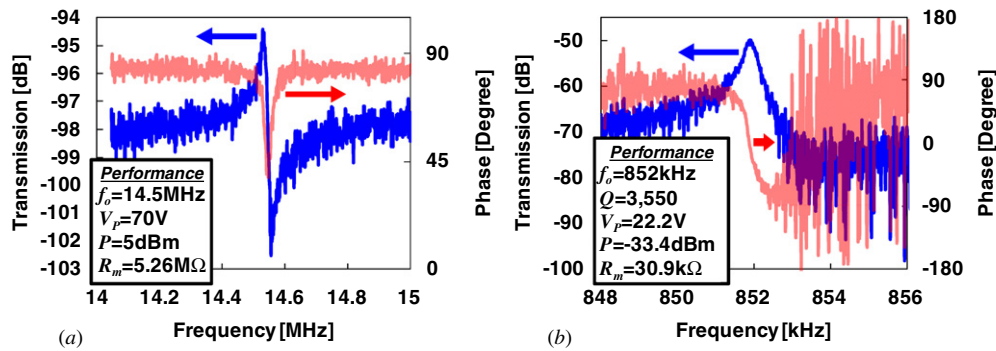
Figure 11. Measured frequency characteristics (in vacuum) including transmission amplitude and phase for standalone: (*a*) Al/W/SiO$_2$ composite via-supported free–free beam resonator of figure 7(*b*) and (*b*) Al flexural-mode plate resonator of figure 7(*e*) without the use of TIA circuits.
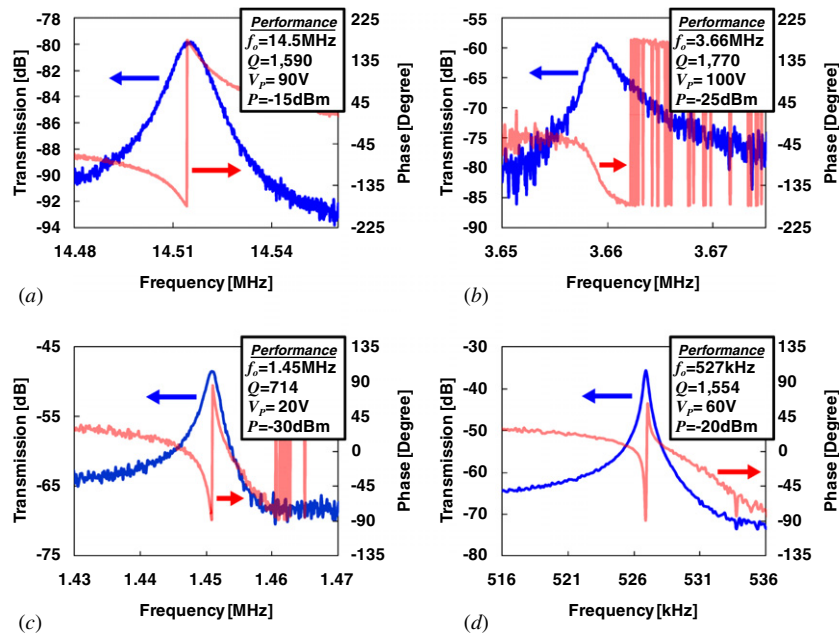

Figure 12. Measured frequency characteristics in vacuum for fabricated CMOS-MEMS resonators integrated with their readout circuits. (*a*) In-plane via-supported free–free beam of figure 7(*b*). (*b*) Out-of-plane free–free beam of figure 7(*c*). (*c*) In-plane via-supported pinned–pinned beam of figures 7(*d*). (*d*) Stacked comb-drive resonator of figure 7(*a*).

low resonance frequency. The R_m of 30.9 kΩ is the lowest motional impedance ever reported in CMOS-MEMS resonators.

Figure 12 presents the measured spectra, including transmission amplitude and phase, for the CMOS-MEMS resonators integrated with their trans-impedance amplifiers, showing the resonance frequencies spanning from 0.5 to 14.5 MHz with Q's in a range of 700–1800. Figure 12(*a*) presents the measured result of an in-plane via-supported free–free beam resonator of figure 7(*b*) with Al/W/SiO$_2$ composite structure under a dc bias of 90 V in vacuum, showing Q of 1590 at 14.5 MHz. Figure 12(*b*) shows the frequency spectrum of the out-of-plane Al free–free beam resonator of figure 7(*c*) centered at 3.66 MHz under a bias of 100 V with Q of 1770. Figure 12(*c*) presents the measured result of an in-plane via-supported pinned–pinned beam resonator of figure 7(*d*) with Al/W composite structure under a bias of only 20 V, showing Q of 714 at 1.45 MHz. The relatively lower Q of this via-supported pinned–pinned beam resonator

compared to others is a result of its mechanical boundary conditions which substantially create an energy transmission path from the resonator body to the anchored substrate, hence leading to much higher vibrational energy loss. Figure 12(*d*) shows the measured frequency response of a stacked comb-drive resonator of figure 7(*a*) under a bias of 60 V in vacuum with the resonance frequency of 527 kHz and with Q of 1554. The measurement results of figure 12 verify the efficacy of this platform which is capable of producing various high-Q CMOS-MEMS resonators integrated with amplifier circuits at different frequencies.

To investigate the electro-softening effect of capacitive resonators as indicated by (3) and (4), frequency tuning capability shown in figure 13(*a*) due to the electrical stiffness k_e was measured for a fabricated 14.5 MHz CMOS-MEMS free–free beam resonator via the adjustment of the dc-bias voltage V_P, indicating that 0.17% tuning range was attained over 60 V of bias variation as shown in figure 13(*b*). Such a bias-dependent frequency tuning might offer a convenient
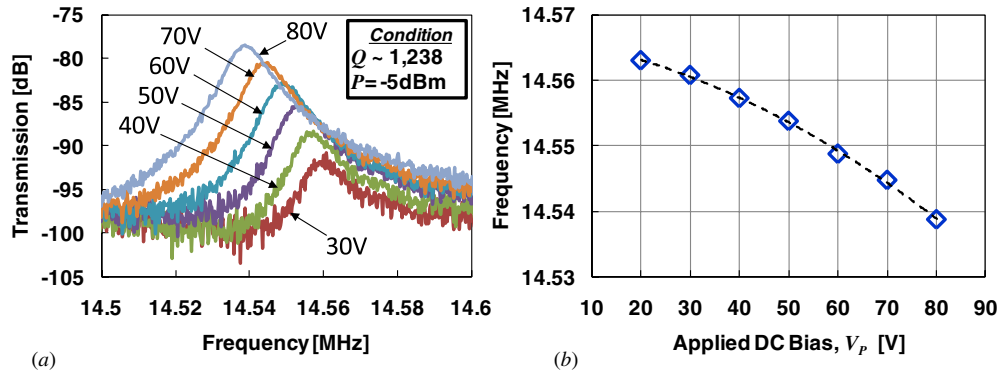
Figure 13. (*a*) Measured frequency characteristics (in vacuum) under different bias voltage V_P for a fabricated via-supported free–free beam resonator (cf figure 7(*b*)) integrated with a TIA readout circuit. (*b*) Resonance frequency versus applied dc bias V_P, showing an electro-softening effect from voltage-tunable electrical stiffness.

Table 3. CMOS-MEMS resonator design and performance summary.

Parameter		(I) Via-supported free–free beam	(II) Via-supported pinned–pinned beam	(III) Mere-metal free–free beam	Unit
	Schematic				
Simulated parameters	μ resonator dimensions, L_r, W_r, h_r	40, 4, 3.945	40, 1, 3.945	40, 4, 0.925	μm
	Electrode width, W_e	19.4	30	20	μm
	Electrode-to-resonator gap, d_o	0.5	0.5	1.0	μm
	dc-bias voltage, V_P	70	25	60	V
	Young's modulus, E_{Al}, E_{SiO2}, E_W	70, 70, 410	70, –, 410	70, –, –	GPa
	Density, ρ_{Al}, ρ_{SiO2}, ρ_W	2700, 2200, 19350	2700, –, 19350	2700, –, –	kg m^{-3}
	Equivalent density, ρ_r	4620	8354	2200	kg m^{-3}
Measured results	Measured resonance frequency, $f_{meas.}$	14.53	1.46	3.64	MHz
	Motional impedance, R_m	5.26	7.08	8.22	MΩ
	Measured quality factor, Q	1590	810 (179)	1770 (911)	–
Calculated and simulated results	Calculated resonance frequency, f_{nom}	15.585	0.88	3.026	MHz
	Simulated resonance frequency, f_{nom}	14.70	1.33	3.807	MHz
	Resonator mass, m_{re}	1.97×10^{-12}	4.92×10^{-13}	2.70×10^{-13}	kg
	Resonator stiffness, k_m	1.89×10^4	15.15	97.79	N m^{-1}
	Calculated resonance frequency, f_o	15.579	0.78	3.00	MHz
	Resonator stiffness, k_{re}	1.89×10^4	11.74	96.30	N m^{-1}
	Motional inductance, L_m	103.61	72.86	287	H
	Motional impedance, R_m	6.38	0.499 (2.26)	1.05 (6.00)	MΩ
	Motional capacitance, C_m	0.001	0.575	0.00978	fF
	Static capacitance, C_o	1.355	2.096	0.708	fF
	Electromechanical transformer turns ratio, η_e	1.38×10^{-7}	8.22×10^{-8}	3.07×10^{-8}	C m^{-1}

*The values in parentheses indicate the calculation based on measured conditions of standalone resonators where no readout circuit was used.

temperature compensation scheme for future timing reference and frequency control applications [26]. To explore the power handling of CMOS-MEMS resonators, figures 14(*a*) and (*b*) present Duffing behavior as the input power increases for a 1.42 MHz via-supported pinned–pinned beam resonator and 532 kHz comb-drive resonator, respectively. Duffing nonlinearity is caused by a third-order effective electrical stiffness [27] between the electrode and resonator that dominates over any third-order mechanical stiffness. As indicated in figure 14(*a*), the maximum input power level

for a CMOS-MEMS beam resonator is around −20 dBm (i.e. 22.4 mV) before it reaches the corresponding bifurcation point. Although the power handling capability of resonators in this work is relatively lower than that of conventional silicon-based resonators [28], a mechanically-coupled array approach [29] can be implemented to greatly improve the power handling of CMOS-MEMS resonators and simultaneously to reduce the motional impedance R_m.

To evaluate the thermal stability of CMOS-MEMS resonators, figures 15(*a*) and (*b*) present plots of fractional
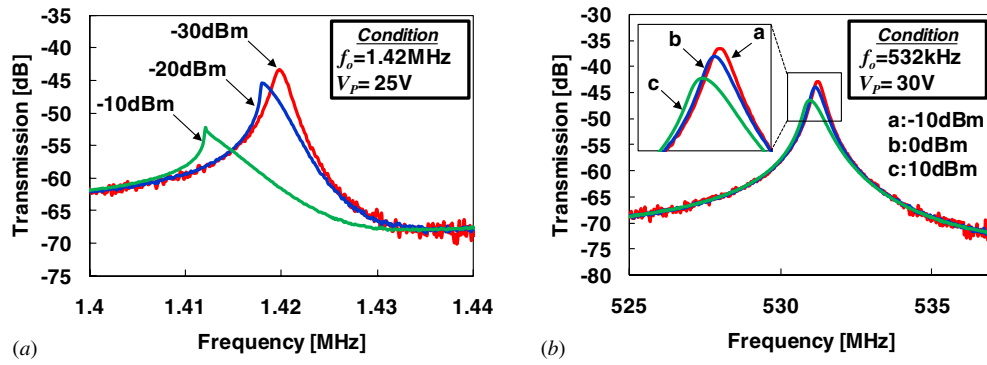
Figure 14. Measured transmission S_{21} versus frequency plots for the fabricated (*a*) Al/W composite via-supported pinned–pinned resonator (cf figure 7(*d*)) and (*b*) stacked comb-drive resonator (cf figure 7(*a*)), showing Duffing nonlinearity as the vibration amplitude increases.
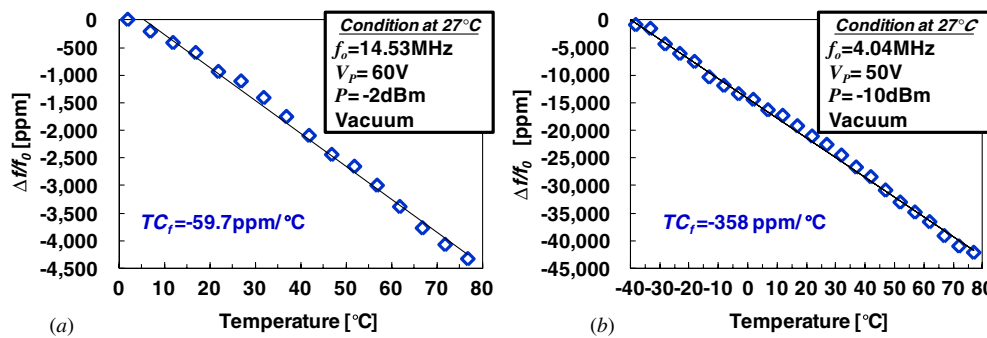

Figure 15. Measured fractional frequency change versus temperature plots for the fabricated (*a*) composite Al/W/SiO$_2$ via-supported free–free beam (cf figure 7(*b*)) and (*b*) Al free–free beam (cf figure 7(*c*)) resonators.
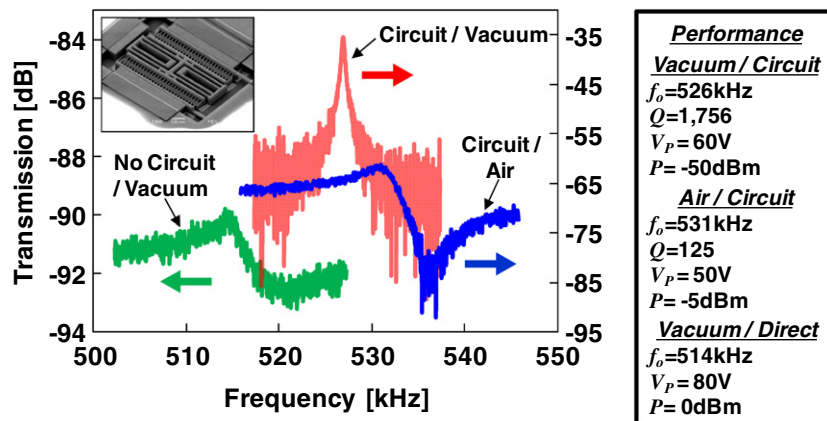

Figure 16. Measured frequency characteristics for stacked comb-drive resonators of figure 7(*a*) under different measuring conditions, including under vacuum without circuit, under air with circuit, and under vacuum with circuit.

frequency change versus temperature measurements for a 14.53 MHz Al/W/SiO$_2$ composite via-supported free–free beam resonator of figure 7(*b*) and a 4.04 MHz mere-Al free–free beam resonator of figure 7(*c*), respectively. The extracted TC_f's of the composite and mere-metal beam resonators are −59.7 and −358 ppm °C^{-1}, respectively, where the thermal stability of the metal–oxide composite structure is six times better than that of its metal counterpart. This is reasonable since SiO$_2$ inside composite resonators as shown in figure 6(*b*) has a positive temperature coefficient of Young's modulus ($TC_E \sim +185$ ppm °C^{-1}) compared with negative TC_E of

most metal materials, leading to stiffness increase of the SiO$_2$ structure as temperature increases and hence alleviating the significant negative TC_f of metal structures. This offers an easy temperature compensation scheme for CMOS-MEMS resonators for future time-keeping and oscillator applications.

Furthermore, figure 16 shows the measured frequency characteristics for stacked comb-drive resonators of figure 7(*a*) under different measured conditions. The transmission characteristic of the resonator integrated with its amplifier tested under vacuum obviously outperforms the measured results of other conditions such as a resonator

Table 4. Reduction of motional impedance using different CMOS technologies [30].

Technology	d_0 (μm)	Structure	h_r (μm)	A_e (μm^2)	R_m (Ω)
0.35 μm, 2P4 M	0.5	M1–M3	3.95	76.63	10.3 M
0.18 μm, 1P6 M	0.28	M1–M5	5.52	107.1	519 k
0.13 μm, 1P7 M	0.21	M1–M6	5.52*	107.1	164 k
90 nm, 1P9 M	0.14	M1–M8	5.52*	107.1	32.4 k

$V_P = 55$ V [31], $W_e = 19.4$ μm.
* Assuming the same thickness of resonators for advanced CMOS technologies.

with its amplifier circuit tested in air and the one tested without circuit but under vacuum, indicating that this work actually takes advantage of vacuum testing and circuit's readout capability to boost Q and improve transmission, therefore demonstrating that integration of MEMS and circuits is crucial for device performance enhancement. The resonance frequency deviation in figure 16 is mainly caused by comb-drive resonators from different dice and under different bias voltage V_P. Pursuant to realizing sufficiently low motional impedance in the near future, table 4 presents the simulated R_m of a given CMOS-MEMS via-supported free–free beam resonator with design parameters of case I in table 3, showing significant R_m reduction with the progress of CMOS technology due to the achievable minimum gap spacing d_o of given resonators. Please note that V_P of 55 V used in the simulations of table 4 was proved to be feasible for the polysilicon free–free beam resonator with d_o of only 100 nm [31] (smaller than 140 nm gap using 90 nm technology), and therefore this value (55 V) is utilized in this work to compare R_m between different technologies. With the continuous advances of the CMOS process, the motional impedance of CMOS-MEMS resonators is expected to be substantially lowered down to a certain level (40 kΩ is possible using 90 nm CMOS as shown in table 4) which is amenable for most RF and sensor applications.

5. Conclusions

This paper presents a general and easy-to-use platform for users to facilitate design and development of high-Q MEMS resonating devices integrated with circuits, thereby capable of achieving single-chip implementation for sensors and communication applications. In addition, fully-integrated CMOS-MEMS resonator circuits, occupying a die area of only 340 μm × 110 μm in this work, offer a very small form factor and low power consumption suited for future portable applications. Furthermore, metal-oxide composite resonator configuration provided by this platform not only alleviates the stress issues often seen in CMOS-MEMS technologies, but, for the first time, greatly improves the TC_f of CMOS-MEMS resonators using SiO$_2$ enclosed to compensate frequency drift due to temperature variation.

Most importantly, the turnaround time for prototyped devices using such a platform is within 3 months, greatly facilitating fabless MEMS design houses. The ease of use and feature of generalization is expected to revolutionize the business model of conventional IDM (integrated device manufacturer) MEMS industry toward a future foundry-oriented process as CMOS progresses.

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