IEEE Access
Multidisciplinary | Rapid Review | Open Access Journal

Received July 22, 2019, accepted August 9, 2019, date of publication August 20, 2019, date of current version September 3, 2019.

Digital Object Identifier 10.1109/ACCESS.2019.2936438

A Generalized One-Bit Control System Using a $\Delta\Sigma$-Quantizer

DHAFER J. ALMAKHLES[1], (Member, IEEE), R. SAKTHIVEL[2], (Senior Member, IEEE), AKSHYA SWAIN[3], (Senior Member, IEEE), UMASHANKAR SUBRAMANIAM[1], (Senior Member, IEEE), AND KHALED ALMUSTAFA[4]

[1]Communications and Networks Department, Prince Sultan University, Riyadh 11586, Saudi Arabia
[2]Department of Applied Mathematics, Bharathiar University, Coimbatore 641046, India
[3]Department of Electrical and Computer Engineering, The University of Auckland, Auckland 1142, New Zealand
[4]Information Systems Department, Prince Sultan University, Riyadh 11586, Saudi Arabia

Corresponding author: Dhafer J. Almakhles (dalmakhles@psu.edu.sa)

This work was supported by the Renewable Energy Laboratory, Prince Sultan University, Saudi Arabia.

ABSTRACT This paper presents the use of a delta-sigma quantizer for generalized one-bit control processing. An equivalent control strategy based on sliding-mode control is employed to derive the necessary condition for the convergence of the proposed one-bit control system in both the continuous-time and discrete-time domains. Under the convergence condition, the binary signals generated by delta-sigma quantizers in the one-bit control system effectively replace their counterpart signals in conventional control systems. This enables a significant reduction in the number of multipliers and overall hardware cost for computing the control laws in one-bit control systems. Our result is applied to design a multiplier-less one-bit generalized proportional and integral controller for the position control of an experimental prototype of a DC motor. An implementation of the one-bit control system is carried out using an FPGA platform to demonstrate the behavior of one-bit generalized proportional and integral controller and compare the results with the standard in terms of implementation efficiency. The results of the simulation and experiment show that the one-bit generalized proportional and integral controller effectively controls the system and achieves the desired specifications. At the same time, the proposed one-bit control system consumes significantly fewer hardware resources than the standard control system.

INDEX TERMS One-bit control processing, delta-sigma quantizer, quantized control systems, equivalent control, sliding mode, generalized proportional and integral.

I. INTRODUCTION

Different techniques of pulse code modulation (PCM) have found wide applications in fields such as communication systems, signal processing, power electronics, and control systems. In particular, the PCM-based delta-sigma quantizer ($\Delta\Sigma$-Q) is eminently suitable for applications where some signals are converted to switch signals represented by a sequence of binary values 0's and +1's such as ON/OFF power electronics systems and actuators [1]–[6] and networked control systems (NCSs) with a binary symmetric channel (i.e., transmitting only one digit 0 or 1 per sample time) [7]–[12]. $\Delta\Sigma$-Qs have been used in different state-space realizations of the *so*-called one-bit processing systems [13]–[16].

For practical considerations, the state-space realizations of transfer functions are often implemented in finite-word-length (FWL) integrated circuits such as field programmable gate arrays (FPGAs), digital signal processors (DSP), microprocessors and microcontrollers. These digital devices offer numerous advantages in terms of cost, performance and maintenance. However, some inherent challenges can arise from the use of such digital platforms due to the discretization effect and quantization error caused by FWL platforms [17]–[19]. Furthermore, inevitable latency is inherently introduced into discrete-time systems due to the nature of these digital systems. Another severe issue lies with the ill-conditioning and sensitivity caused by the high sampling

The associate editor coordinating the review of this article and approving it for publication was Ali Zemouche.

systems using fixed-point arithmetic [15], [20]–[23]. These issues not only degrade the performance but, even worse, may lead to an instability of the entire system.

The above issues motivated researchers to insert ΔΣ-Qs in linear systems with state-space representations such as linear controllers and digital filters. Such systems are referred to as one-bit control or one-bit signal processing systems [15], [21], [24]. The direct processing of one-bit signals, generated by ΔΣ-Qs, has remarkable advantages for digital platforms with limited resources from a computational perspective [3], [15], [16]. The implementation of one-bit control laws alleviates the drawbacks associated with the latency, implementation and maintenance where the hardware and cost of products are constrained. Furthermore, large numbers of wires due to the actuators and sensors interface with controllers through multi-bit digital signals could be significantly reduced by adopting one-bit control techniques [7], [16], [25].

Although the aforementioned works have shown great results in the literature, it is worth noting that much more work is needed in terms of both theoretical and practical advancements. This paper, motivated by [15], presents different uses of ΔΣ-Qs in both continuous-time (CT) and discrete-time (DT) control systems. In particular, a generalized one-bit control system full of trivial parameters[1] is established. According to the definition by Filippov [26], the proposed one-bit control system fits well with differential inclusion due to its discontinuous right-hand side (RHS). Thus, we adopt equivalent-control-based sliding-mode control (ECB-SMC) in our stability analysis of one-bit control systems. We show that the binary signals in a one-bit control system are equivalent to their counterpart signals in the conventional control system. The results of the theoretical analysis are validated through experiments by designing a multiplier-less one-bit generalized proportional and integral (GPI) controller considering an experimental prototype of a DC motor [28], [29]. The implementation of the one-bit control system is carried out using an FPGA platform. The results of the simulation and experiment demonstrate that the one-bit control system effectively controls the system and achieves the desired specifications while consuming fewer hardware resources than the standard control system.

In this paper, the notation I_m denotes the identity matrix with dimensions of $\mathbb{R}^{m\times m}$. The state variables x_i and $\hat{x}_i$ $(i = 1, 2, \ldots, n)$ denote the states of the nominal control system and the state of the one-bit control system, respectively. $1_m = [1 \cdots 1]^T \in \mathbb{Z}^m$ and $0_m = [0 \cdots 0]^T \in \mathbb{Z}^m$ denote vectors of ones and zeros, respectively. We use the standard *Euclidean* norm and the maximum norm of a vector $x \in \mathbb{R}^n$ defined by $\|x\|$ and $\|x\|_\infty$, respectively. Let $\|A\|$ denote the matrix norm of A induced by a vector norm $\|.\|$ in $\mathbb{R}^n$, i.e., $\|A\| = \sup_{\|x\|=1} \|Ax\|$. In our analysis, we use the following well-known mathematical facts: $\boldsymbol{s}^T\ \mathbf{sgn}(\boldsymbol{s})\ \mathcal{D}\ \|\boldsymbol{s}\|_1$, and $\|\boldsymbol{s}\|_\infty \le \|\boldsymbol{s}\| \le \|\boldsymbol{s}\|_1 \le \sqrt{\boldsymbol{m}}\ \|\boldsymbol{s}\|$ for all $\boldsymbol{s} \in \mathbb{R}^m$.

[1] By *trivial parameters*, we mean those that are 0, ±1.

The rest of the paper is organized as follows. The description and stability analysis of the one-bit CT control system embedded with the ΔΣ-Q are given in Section II. Section III discusses the formulated one-bit DT control system embedded with ΔΣ-Q. Guidelines for designing the one-bit DT GPI for position control of a DC motor are briefly discussed in Section IV. The simulations and experimental results for the DC motor control system with the one-bit GPI are presented in Section V, and the concluding remarks are given in Section VI.

II. ONE-BIT CT CONTROL SYSTEM

In this section, a precise formulation and stability analysis for the problem of one-bit CT control system are derived.

A. NOMINAL CT CONTROL SYSTEM DESCRIPTION

Consider the single-input single-output linear time-invariant system given by

$$\dot{\boldsymbol{x}}_t^p = A_p \boldsymbol{x}_t^p + B_p \mathrm{u}_t \tag{1a}$$
$$\mathrm{y}_t^p = C_p \boldsymbol{x}_t^p \tag{1b}$$

where $\boldsymbol{x}_t^p \in \mathbb{R}^{n_p}$ is the state-variable vector, $\mathrm{u}_t \in \mathbb{R}$ denotes the control signal to be designed and $\mathrm{y}_t^p \in \mathbb{R}$ denotes the output of the system. The state-space equations for the controller considered here are given by

$$\dot{\boldsymbol{x}}_t^c = A_c \boldsymbol{x}_t^c + B_{cy} \mathrm{y}_t^p + B_{ce} e_t \tag{2a}$$
$$\mathrm{u}_t = C_c \boldsymbol{x}_t^c + d_{cy} \mathrm{y}_t^p + d_{ce} e_t \tag{2b}$$

where $\boldsymbol{x}_t^c \in \mathbb{R}^{n_c}$ is the state-variable vector of the controller and e_t denotes the output tracking error

$$e_t = r - \mathrm{y}_t^p$$

in which r is a constant reference signal. By combining (1) and (2), the state-space equations for the closed-loop control system become

$$\dot{\boldsymbol{x}}_t = A \boldsymbol{x}_t + B e_t \tag{3a}$$
$$\mathrm{y}_t = C \boldsymbol{x}_t \tag{3b}$$

where

$$\boldsymbol{x}_t = \begin{bmatrix} \boldsymbol{x}_t^p \\ \boldsymbol{x}_t^c \end{bmatrix}, \quad A = \begin{bmatrix} A_p + d_{cy} B_p C_p & B_p C_c \\ B_{cy} C_p & A_c \end{bmatrix},$$
$$B = \begin{bmatrix} d_{ce} B_p \\ B_{ce} \end{bmatrix}, \quad C = \begin{bmatrix} C_p & 0_{n_c}^T \end{bmatrix}$$

$A \in \mathbb{R}^{n\times n}$, $B \in \mathbb{R}^n$ and $C \in \mathbb{R}^{1\times n}$ for all $n = n_p + n_c$.

Assumption 1: It is important that the controller (2) is designed such that A is a Hurwitz matrix and $\lim_{t\to 0} e_t = 0$.

For real-time applications of a power converter, one-bit control and an NCS with one-bit communication channels, some signals inside (3) are converted to binary signals. These signals can be either control signals in power converters, controller states in one-bit control processing or transmitted signals in the NCS. Depending on the applications, these signals that are to be converted are defined here as:

$$\boldsymbol{w}_t := E \boldsymbol{x}_t + F\ e_t \tag{4}$$

where $\boldsymbol{w}_t \in \mathbb{R}^m$, $E \in \mathbb{R}^{m\times n}$ and $F \in \mathbb{R}^m$. Note that E and F depend on several factors, including the intended real-time applications and types of signals to be converted.

Thus, combining (3) with (4) yields the following augmented system

$$\dot{\boldsymbol{\chi}}_t = \mathcal{A}\boldsymbol{\chi}_t + \mathcal{B}e_t \tag{5a}$$
$$\mathcal{Y}_t = \mathcal{C}\boldsymbol{\chi}_t \tag{5b}$$

where $\boldsymbol{\chi}_t^T = \begin{bmatrix}\boldsymbol{x}_t^T & \boldsymbol{w}_t^T\end{bmatrix} \in \mathbb{R}^N$ with $N = n + m$, $\mathcal{A} = \begin{bmatrix}A_{11} & A_{12}\\ A_{21} & A_{22}\end{bmatrix}$, $\mathcal{B} = \begin{bmatrix}B_1\\ B_2\end{bmatrix}$, and $\mathcal{C} = \begin{bmatrix}C & \mathbf{0}_m^T\end{bmatrix}$ in which $A_{11} \in \mathbb{R}^{n\times n}, A_{12} \in \mathbb{R}^{n\times m}, A_{21} \in \mathbb{R}^{m\times n}$, $A_{22} \in \mathbb{R}^{m\times m}$, $B_1 \in \mathbb{R}^n$ and $B_2 \in \mathbb{R}^m$. It should be stressed here that (3) is only a new form of (5); that is, both systems (3) and (5) represent the same control system with the only difference being the insertion of dependent vectors.

In the following example, we show how the values of the matrices $\mathcal{A}, \mathcal{B}, \mathcal{C}, E$ and F depend on the nature of the control problem to be solved. This in turn changes the various matrices in the augmented system.

Example: Consider the problem of an NCS where the communication channel with one-bit information is located between the sensors and the controller. Thus, the feedback signal y_t is converted to a binary signal to be transferred through the communication channel. For simplicity, let us consider an output-feedback control problem with $r = 0$ in this example.

In this example, we want to represent $\boldsymbol{w}_t = \boldsymbol{y}_t$. Therefore, $E = C$ and $F = 0$ in (4). We consider *ideal* conversion where, as a result, the controller (2) can be rewritten as:

$$\dot{\boldsymbol{x}}_t^c = A_c\boldsymbol{x}_t^c + \left(B_{cy} - B_{ce}\right)\boldsymbol{w}_t \tag{6a}$$
$$u_t = C_c\boldsymbol{x}_t^c + \left(d_{cy} - d_{ce}\right)\boldsymbol{w}_t \tag{6b}$$

The various matrices in the augmented system (5) are defined as follows. From (1a), and (6), it follows that

$$\dot{\boldsymbol{x}}_t = A_{11}\boldsymbol{x}_t + A_{12}\boldsymbol{w}_t \tag{7}$$

where $A_{11} = \begin{bmatrix}A_p & B_pC_c\\ 0_{n_c\times n_p} & A_c\end{bmatrix}$, and $A_{12} = \begin{bmatrix}\left(d_{cy} - d_{ce}\right)B_p\\ B_{cy} - B_{ce}\end{bmatrix}$. Furthermore, using (5a) and (7), it can be shown that

$$\begin{aligned}\dot{\boldsymbol{w}}_t &= C\dot{\boldsymbol{x}}_t\\ &= A_{21}\boldsymbol{x}_t + A_{22}\boldsymbol{w}_t\end{aligned} \tag{8}$$

where $A_{21} = CA_{11} = \begin{bmatrix}C_pA_p & C_pB_pC_c\end{bmatrix}$, and $A_{22} = \left(d_{cy} - d_{ce}\right)C_pB_p$. Additionally, $\mathcal{B} = \mathbf{0}_N$ and $\mathcal{C} = \begin{bmatrix}C_p & \mathbf{0}_{n_c}^T & \mathbf{0}_m^T\end{bmatrix}$.

In this subsection, we only consider ideal conversion from conventional signals to binary signals with *zero* quantization error. Next, we introduce one-bit CT control where ΔΣ-Q is embedded to convert $\boldsymbol{w}_t$ defined in (4) to binary signals.

B. ONE-BIT CT CONTROL SYSTEMS EMBEDDED WITH THE ΔΣ-Q

In this section, we apply the ΔΣ-Q to convert

$$\hat{\boldsymbol{w}}_t = E\hat{\boldsymbol{x}}_t + F\,\hat{e}_t \tag{9}$$

to binary signals.[2] The dynamic function of the ΔΣ-Q, which operates here as a map $\hat{\boldsymbol{w}}_t \in \mathbb{R}^m \rightarrow \boldsymbol{\delta}_t \in \left[\{-1, 1\}, \cdots, \{-1, 1\}\right]^T \in \mathbb{Z}^m$, is given by

$$\dot{\boldsymbol{s}}_t = \hat{\boldsymbol{w}}_t - \phi\,\boldsymbol{\delta}_t \tag{10}$$

where $\boldsymbol{s}_t$ is the state-variable of the ΔΣ-Q, $\hat{\boldsymbol{w}}_t$ is the input of the ΔΣ-Q, $\boldsymbol{\delta}_t\ \boldsymbol{\mathcal{D}}\ \mathbf{sgn}(\boldsymbol{s_t}) = \left[\mathrm{sgn}(s_1), \cdots, \mathrm{sgn}(s_m)\right]^T$ is the binary output of the ΔΣ-Q and ϕ is the quantizer gain. The quantizer gain (ϕ) can be judicially chosen to be greater that the upper bound of (4), i.e., $\left\|\hat{\boldsymbol{w}}_t\right\|_\infty \leq \phi$, (see [30], [31]).

The one-bit CT control systems are obtained by replacing $\hat{\boldsymbol{w}}_t$ with $\boldsymbol{\delta}_t$ using (10) such that

$$\dot{\hat{\boldsymbol{\chi}}}_t = \bar{\mathcal{A}}\begin{bmatrix}\hat{\boldsymbol{x}}_t\\ \boldsymbol{\delta}_t\end{bmatrix} + \mathcal{B}\hat{e}_t \tag{11a}$$
$$\hat{\mathcal{Y}}_t = \mathcal{C}\hat{\boldsymbol{\chi}}_t \tag{11b}$$

where $\hat{\boldsymbol{\chi}}_t^T = \begin{bmatrix}\hat{\boldsymbol{x}}_t^T & \hat{\boldsymbol{w}}_t^T\end{bmatrix}$ and $\bar{\mathcal{A}} = \mathcal{A} \times \mathrm{diag}\{I_n, \phi I_m\}$.

Theorem 1: For the CT control system (3) with assumption 1, one-bit CT control systems (11), embedded with the oversampling ΔΣ-Q described by (10), converges to the nominal control system (5) using ECB-SMC if ϕ is designed such that

$$\Omega_t = \left\{\boldsymbol{w}_t \in \mathbb{R}^m \ \mid\ \|\boldsymbol{w}_t\|_\infty \leq \Psi_t < \phi\right\} \tag{12}$$

in which $\Psi_t = \sqrt{m}\left(\|E\|\,\|x_t\| + \|F\|\,|e_t|\right)$.

Proof: Consider the dynamic function of the ΔΣ-Q given by (10), and let us define the Lyapunov function as $V_t = \frac{1}{2}\boldsymbol{s}_t^T\,\boldsymbol{s}_t$. The derivative of V_t with respect to time is expressed by $\dot{V}_t = \boldsymbol{s}_t^T\dot{\boldsymbol{s}}_t$. It follows from (10) that

$$\dot{V}_t = \boldsymbol{s}_t^T\,\hat{\boldsymbol{w}}_t - \phi\boldsymbol{s}_t^T\,\boldsymbol{\delta}_t \tag{13a}$$
$$= \boldsymbol{s}_t^T\,\hat{\boldsymbol{w}}_t - \phi\,\|\boldsymbol{s}_t\|_1 \tag{13b}$$
$$\leq -\|\boldsymbol{s}_t\|\left(\phi - \left\|\hat{\boldsymbol{w}}_t\right\|_\infty\right) \tag{13c}$$

since $\|\boldsymbol{s}_t\|_2 \leq \|\boldsymbol{s}_t\|_1$. It is also obvious that (13c) is negative, i.e., V_t decreases to ensure sliding mode, if $\left\|\hat{\boldsymbol{w}}_t\right\|_\infty < \phi$. As a result, ECB-SMC can be taken into account to characterize one-bit CT control systems. For the equivalent control, the ΔΣ-Q operates at an arbitrary high frequency, the so-called oversampling ΔΣ-Q, which gives $\dot{\boldsymbol{s}}_t \doteq 0_m$. This in turn implies that

$$\hat{\boldsymbol{w}}_{\boldsymbol{t}_{(\boldsymbol{eq})}} = \phi\boldsymbol{\delta}_{t_{(eq)}} \tag{14}$$

in (10), where $\hat{\boldsymbol{w}}_{\boldsymbol{t}_{(\boldsymbol{eq})}}$ and $\boldsymbol{\delta}_{t_{(eq)}}$ are the equivalent signals for $\hat{\boldsymbol{w}}_t$ and $\boldsymbol{\delta}_t$, respectively. Both $\hat{\boldsymbol{w}}_{\boldsymbol{t}_{(\boldsymbol{eq})}}$ and $\boldsymbol{\delta}_{t_{(eq)}}$ are obtained by filtering $\hat{\boldsymbol{w}}_t$ and $\boldsymbol{\delta}_t$ through a low-pass filter. [3]

[2] Here, $\hat{()}$ indicates quantized signals. Thus, we change the notation from $\boldsymbol{w}_t$ and $\boldsymbol{x}_t$ and the nominal signals in Section II to their associated quantized signals $\hat{\boldsymbol{w}}_t$ and $\hat{\boldsymbol{x}}_t$.

[3] The equivalent signal (i.e., average) of the discontinuous function $\boldsymbol{\delta}_t$, denoted as $\boldsymbol{\delta}_{t_{(eq)}} \in [-\mathbf{1_m}, \mathbf{1_m}]$, can be obtained by passing $\boldsymbol{\delta}_t$ through a first-order low-pass filter such that $\boldsymbol{\delta}_{t_{(eq)}} := \boldsymbol{\delta}_t - \tau\dot{\delta}_{t_{(eq)}}$, where τ is the time constant [32].

From a geometric point of view and during ideal sliding motion, ECB-SMC implies that the high-switching-frequency binary signals $\phi\boldsymbol{\delta}_t$ in one-bit CT control systems (11) can be replaced by their equivalent signals in (14) [30]–[32]. As a result, this gives

$$\dot{\boldsymbol{\chi}}_t^* = \mathcal{A}\boldsymbol{\chi}_t^* + \mathcal{B}e_t^* \tag{15}$$

where $\boldsymbol{\chi}_t^* = \begin{bmatrix} \boldsymbol{x}_t^* \\ \hat{\boldsymbol{w}}_{t_{(eq)}} \end{bmatrix}$ and e_t^* denote the states and tracking error of the system under the equivalent control, respectively. It follows from (15) that $\boldsymbol{w}_t \equiv \hat{\boldsymbol{w}}_{t_{(eq)}} \equiv \hat{\boldsymbol{w}}_t$. Hence, the quantizer gain ϕ can be suitably designed using the upper bounds of $\boldsymbol{w}_t$ defined in (4) in the original control system, such that

$$\Omega_t = \{\boldsymbol{w}_t \in \mathbb{R}^m \mid \|\boldsymbol{w}_t\|_\infty \leq \Psi_t < \phi\} \tag{16}$$

where $\Psi_t = \sqrt{m}\,(\|E\|\,\|x_t\| + \|F\|\,|e_t|)$.

It is straightforward to see that if $\hat{\boldsymbol{\chi}}_t$ tends to $\boldsymbol{\chi}_t$, then $\hat{\mathcal{Y}}_t$ tends to $\mathcal{Y}_t$ accordingly. Thus, we can conclude that the one-bit CT control system (11) converges to its nominal control system (5) with ECB-SMC if (16) holds. ■

Remark 1: In our analysis, we consider the *ideal* sliding mode, where sufficiently high-frequency switching devices should be implemented. However, this requirement is not necessarily valid for some power electronic converters with a low switching frequency, digital platforms with bandwidth constraints, and networks with a bandwidth-limited channel.

In what follows, we extend our analysis of one-bit CT control systems to the more realistic case of one-bit DT control systems where the switching frequency is finite.

III. ONE-BIT DT CONTROL SYSTEM

A. NOMINAL DT-CONTROL SYSTEM DESCRIPTION

The DT transformation of (3), is described as:

$$\rho\boldsymbol{x}_k = A_d\boldsymbol{x}_k + B_d e_k \tag{17a}$$

$$\mathrm{y}_k = C_d\boldsymbol{x}_k \tag{17b}$$

by defining $\rho \triangleq zI_n - I_n$ and for all $t \in [kh, (k+1)h]$, where $h > 0$ denotes the sampling period, $\boldsymbol{x}_k$, u_k and y_k represent $\boldsymbol{x}(kh)$, $u(kh)$ and $y(kh)$, respectively. Euler's discretization method gives $A_d = hA$, $B_d = hB$ and $C_d = C$. Let $\hat{A}_d = I_n + A_d$, which implies that h should be chosen in the range $0 \leq h \leq h_M$ such that rank $\left\{\hat{A}_d\right\} = n$ and $\varrho\left(\hat{A}_d\right) \leq 1$; $\varrho\left(\hat{A}_d\right)$ is the spectral radius of $\hat{A}_d$ in which $\varrho\left(\hat{A}_d\right) = \max\left\{\left|\lambda_i\left(\hat{A}_d\right)\right|\right\}$ for $(i = 1, \cdots, n)$. Note that the maximum sampling period h_M results in a marginally stable system where $\varrho\left(\hat{A}_d\right) = 1$.

The DT equivalent of (4) is defined as:

$$\boldsymbol{w}_k := E\boldsymbol{x}_k + Fe_k. \tag{18}$$

The DT representation of the augmented nominal system (5) has the form

$$\rho\boldsymbol{\chi}_k = \mathcal{A}_d\boldsymbol{\chi}_k + \mathcal{B}_d e_k \tag{19a}$$

$$\mathcal{Y}_k = \mathcal{C}_d\boldsymbol{\chi}_k \tag{19b}$$

where $\boldsymbol{\chi}_k^T = \left[\boldsymbol{x}_k^T\ \boldsymbol{w}_k^T\right]$, $\mathcal{A}_d = h\mathcal{A}$, $\mathcal{B}_d = h\mathcal{B}$, and $\mathcal{C}_d = \mathcal{C}$ for all $N = n + m$.

Note that both (17) and (19) are equivalent; i.e. they convey the same information. Next, we consider the Euler's discretization of the CT control system embedded with the ΔΣ-Q.

B. ONE-BIT DT CONTROL SYSTEM EMBEDDED WITH THE ΔΣ-Q

The dynamic function in (10) is discretized as follows:

$$\rho\boldsymbol{s}_k = \hat{\boldsymbol{w}}_k - \phi\,\boldsymbol{\delta}_k \tag{20}$$

where $\hat{\boldsymbol{w}}_k \in \mathbb{R}^m$ and $\boldsymbol{\delta}_k \in \mathbb{Z}^m$ are the input and output of the ΔΣ-Q, respectively, and ϕ denotes the quantizer gain.

Replacing the intended signals $\hat{\boldsymbol{w}}_k$ by their associated binary signals $\boldsymbol{\delta}_k$ using (20) gives

$$\rho\hat{\boldsymbol{\chi}}_k = \bar{\mathcal{A}}_d\begin{bmatrix}\hat{\boldsymbol{x}}_k \\ \boldsymbol{\delta}_k\end{bmatrix} + \mathcal{B}_d\hat{e}_k \tag{21a}$$

$$\hat{\mathcal{Y}}_k = \mathcal{C}_d\hat{\boldsymbol{\chi}}_k \tag{21b}$$

where $\hat{\boldsymbol{\chi}}_k^T = \left[\hat{\boldsymbol{x}}_k^T\ \hat{\boldsymbol{w}}_k^T\right]$, $\bar{\mathcal{A}}_d = h\bar{\mathcal{A}} = h\mathcal{A} \times \mathrm{diag}\,\{I_n, \phi I_m\}$ and $\boldsymbol{\delta}_k = \mathbf{sgn}(\boldsymbol{s}_k) = \left[\mathrm{sgn}(s_1), \cdots, \mathrm{sgn}(s_m)\right]^T$.

Lemma 1: Consider (20) with $\boldsymbol{s}_0 = \mathbf{0}_m$. If the quantizer gains ϕ is selected as

$$\left\|\hat{\boldsymbol{w}}_k\right\|_\infty < \phi, \tag{22}$$

then the following results are valid.

1) The dynamic function (20) is stable, and $\boldsymbol{s}_k$ is confined by $\|\boldsymbol{s}_k\| \leq \epsilon$ where $\left\|\hat{\boldsymbol{w}}_k\right\|_\infty + \phi < 2\phi \leq \epsilon$.

2) It can be verified that

$$\phi\boldsymbol{\delta}_{(eq)_N} = \hat{\boldsymbol{w}}_{(eq)_N} \tag{23}$$

where $\boldsymbol{\Xi}_{(eq)_N} = \lim_{N\to\infty}\frac{1}{N}\sum_{i=0}^{N-1}\boldsymbol{\Xi}_i$, denotes the N-moving average for all $\boldsymbol{\Xi} \in \left\{\hat{\boldsymbol{w}}, \boldsymbol{\delta}\right\}$.

Proof: Consider the scalar system of (20)

$$s_{j_{k+1}} = s_{j_k} + \hat{w}_{j_k} - \phi\,\delta_{j_k} \tag{24}$$

where $\hat{w}_j \in \mathbb{R}$ and $\delta_j = 1$ if $s_j \geq 0$ and -1 if $s_j < 0$ for $j = 1, \cdots, m$.

In what follows, the dynamical behavior and stability of (24) are studied in both possible cases: $s_{j_k} \geq 0$, and $s_{j_k} < 0$. For the case of $s_{j_k} \geq 0$, it can be shown that $s_{j_{k+1}} = s_{j_k} + \hat{w}_{j_k} - \phi \leq s_{j_k}$ if $\left|\hat{w}_{j_k}\right| < \phi$. It can also be verified that $s_{j_k} > s_{j_{k+1}} > -\left|\hat{w}_{j_k}\right| - \phi > -2\phi \geq -\epsilon$. Similarly, $s_{j_k} < 0$ implies that $s_{j_{k+1}} > s_{j_k}$ and $\epsilon > s_{j_{k+1}} > s_{j_k}$ if $\left|\hat{w}_{j_k}\right| < \phi$ holds.

From the above analysis, it clear that s_{j_k} will be attracted to $s_{j_k} \in [-\epsilon, \epsilon]$ if $\left|\hat{w}_{j_k}\right| < \phi$ holds. This completes the proof of the first part.

Next, assume that (20) is stable. The addition of N iterations for (20) with $\boldsymbol{s}_0 = \mathbf{0}_m$ yields

$$\boldsymbol{s}_N = \sum_{i=0}^{N-1}\hat{\boldsymbol{w}}_i - \phi\sum_{i=0}^{N-1}\boldsymbol{\delta}_i \tag{25}$$

Given that $\|s_k\| \leq \epsilon$, then $\lim_{N\to\infty} \frac{s_N}{N} = \mathbf{0_m}$, which yields ECB-SMC (23). ■

Definition 1: Given that $\|\boldsymbol{\chi}_k\| < \infty$, the one-bit DT control system is said to be stable if there exists $\boldsymbol{\xi}_k = \boldsymbol{\chi}_k - \hat{\boldsymbol{\chi}}_k$ such that $\|\boldsymbol{\xi}_k\| < \infty$.

In the following theorem, the necessary conditions for the stability and convergence of the one-bit DT control system embedded with the ΔΣ-Q described by (20), are investigated.

Theorem 2: If the system (17) is asymptotically stable, i.e., $\varrho(A_d) < 1$, then there exist sampling periods h_m such that $0 \leq h \leq h_m < h_M$, where the one-bit DT control system (11), embedded with the oversampling ΔΣ-Q described by (20) converges to the nominal control system (5) given that ϕ satisfies

$$\Omega_k = \left\{ \boldsymbol{w}_k \in \mathbb{R}^m \mid \|\boldsymbol{w}_k\|_\infty \leq \Psi_k < \phi \right\} \tag{26}$$

where $\Psi_k = \sqrt{m}\left(\|E\|\,\|\boldsymbol{x}_k\| + \|F\|\,|e_k|\right) + \mathcal{O}(h)$ with $\lim_{h\to 0} \mathcal{O}(h) = 0$.

Proof: Assume that the ΔΣ-Q described by (20) is *initially* designed to be a stable, i.e., Lemma (1) holds. The quantization error generated by the ΔΣ-Q (20) is defined as the difference between the input and the output

$$\boldsymbol{\varepsilon}_k = \hat{\boldsymbol{w}}_k - \phi\boldsymbol{\delta}_k. \tag{27}$$

Substituting (27) into one-bit DT control system (21) gives

$$\rho\hat{\boldsymbol{\chi}}_k = \mathcal{A}_d\hat{\boldsymbol{\chi}}_k + \mathcal{B}_d\hat{e}_k + \boldsymbol{\xi}_k \tag{28}$$

with

$$\boldsymbol{\xi}_k = -\bar{\mathcal{A}}_d \begin{bmatrix} 0_n \\ \phi^{-1}\boldsymbol{\varepsilon}_k \end{bmatrix} = -h\mathcal{A} \begin{bmatrix} 0_n \\ \boldsymbol{\varepsilon}_k \end{bmatrix} \tag{29}$$

where $\boldsymbol{\xi}_k$ denotes the chattering behavior as per Definition 1. Notice that both one-bit DT control system (21), or equivalently (28), and the nominal system (19) should behave identically if $\boldsymbol{\xi}_k = \mathbf{0}_{\mathcal{N}}$. Hence, from (28) and (29), one can see that there exist sampling periods h_m such that $0 < h \leq h_m \leq h_M$, where the one-bit DT control system (21) converges to the nominal system (19) since $\lim_{h\to 0}\boldsymbol{\xi}_k = \mathbf{0}_{\mathcal{N}}$. It is, also, straightforward to see that if $\hat{\boldsymbol{\chi}}_k$ tends to $\boldsymbol{\chi}_k$, then $\hat{\mathcal{Y}}_k$ tends to $\mathcal{Y}_k$ accordingly.

Consider ECB-SMC as per Lemma 1, it can be assumed that $\hat{\boldsymbol{w}}_{k_{(eq)}} \equiv \hat{\boldsymbol{w}}_k \equiv \boldsymbol{w}_k$. Thus, ϕ can be suitably designed using the upper bounds of $\boldsymbol{w}_k$ defined in (18) to satisfy the stability condition (26). ■

Remark 2: It follows from (27) that $\|\boldsymbol{\varepsilon}_k\|_\infty < 2\phi$ if $\|\hat{\boldsymbol{w}}_k\|_\infty < \phi$. It is then easy to verify that

$$\|\boldsymbol{\xi}_k\|_\infty < 2\phi\, h\, \|\mathcal{A}\| \tag{30}$$

From (30), the chattering $\boldsymbol{\xi}_k$ can be reduced with a minimum quantizer gain ϕ, short sampling period h, and small negative eigenvalues of $\mathcal{A}$, which result in slow dynamics such that the control system can effectively act as a low-pass filter. Roughly speaking, the optimal quantizer gain ϕ can be selected, appropriately to be as close as possible to $\|\boldsymbol{w}_k\|_\infty$. Thus, special care must be taken to judiciously select the optimal quantizer gain ϕ, which ensures both the stability and performance (i.e., less chattering) of the one-bit DT control system.

IV. ONE-BIT GPI CONTROLLER

This section illustrates the effectiveness of the proposed approach of designing a one-bit control system by implementing a GPI controller using an experimental prototype of a DC motor.

A. DESIGN OF THE GPI CONTROLLER FOR A DC MOTOR

The DC motor presented in this paper is modeled as a first-order system. The transfer function, with control input u_t and output angular speed ψ_t^r, is given by

$$\frac{\psi_t^r}{\mathrm{u}_t} = \frac{\ell}{\tau_s s + 1} \left(\text{with units of } \frac{rad/s}{Volt} \right)$$

where ℓ and τ_s denote the DC gain and rise time, respectively. The position control θ_t of the DC motor is described by a second-order linear system of the form

$$\mathcal{P}_t : \begin{cases} \dot{x}_t^{p_1} &= a x_t^{p_1} + b\mathrm{u}_t \\ \dot{x}_t^{p_2} &= x_t^{p_1} \\ \mathrm{y}_t^{p} &= x_t^{p_2} \end{cases} \tag{31}$$

where $a = -1/\tau_s$, $b = \ell/\tau_s$, $x_t^{p_1} = \omega_t^r$ and $x_t^{p_2} = \theta_t$.

The GPI controller is designed so that the closed-loop characteristic polynomial is:

$$\begin{aligned} 1p(s) &= s^4 + k_3 s^3 + k_2 s^2 + k_1 s + k_0 \\ &= \left(s^2 + 2\zeta_r\omega_n s + \omega_n^2\right)^2 \end{aligned}$$

in which $k_0 = \omega_n^4$, $k_1 = 4\zeta_r\omega_n^3$, $k_2 = 4\zeta_r^2\omega_n^2 + 2\omega_n^2$ and $k_3 = 4\zeta_r\omega_n$, where ω_n and ζ_r are design parameters that denote the natural frequency and damping ratio of the transient response, respectively. The GPI controller is designed as $\mathrm{u}_t = u_t^{cy} + u_t^{ce}$, where u_t^{cy} and u_t^{ce} are given by

$$\mathcal{C}_t^y : \begin{cases} \dot{x}_t^{c_1 y} = -\bar{b}u_t^{cy} \\ u_t^{cy} = x_t^{c_1 y} + \bar{a}\mathrm{y}_t^p \end{cases} \tag{32a}$$

$$\mathcal{C}_t^e : \begin{cases} \dot{x}_t^{c_1 e} = \dfrac{k_0}{b} e_t \\ \dot{x}_t^{c_2 e} = x_t^{c_1 e} - \bar{b}u_t^{ce} + \dfrac{k_1}{b} e_t \\ u_t^{ce} = x_t^{c_2 e} + \dfrac{1}{b} e_t \end{cases} \tag{32b}$$

where $\bar{a} = \left(1 - a^2 - k_2 - ak_3\right)/b$, and $\bar{b} = k_3 + a$.

From (31)-(32), the closed-loop control system can take the form of (3), such that

$$\boldsymbol{x}_t^p = \left[x_t^{p_1}\ x_t^{p_2}\right]^T, \boldsymbol{x}_t^c = \left[x_t^{c1y}\ x_t^{c1e}\ x_t^{c2e}\right]^T,$$

$$A_p = \begin{bmatrix} a & 0 \\ 1 & 0 \end{bmatrix}, \quad B_p = \begin{bmatrix} 1 \\ 0 \end{bmatrix},$$

$$C_p = \begin{bmatrix} 0 \\ 1 \end{bmatrix}^T, \quad A_c = \begin{bmatrix} -\bar{b} & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 1 & -\bar{b} \end{bmatrix},$$

$$B_{cy} = \begin{bmatrix} -\bar{b}\bar{a} \\ -k_0/b \\ -\left(k_1 - \bar{b}\right)/b \end{bmatrix}, B_{ce} = \begin{bmatrix} 0 \\ k_0/b \\ \left(k_1 - \bar{b}\right)/b \end{bmatrix},$$
$$C_c = \begin{bmatrix} 1 & 0 & 1 \end{bmatrix}, \quad d_{cy} = \bar{a} - 1/b \text{ and } d_{cr} = 1/b.$$

Using Euler's discretization, the discrete-time model for the the position control of the DC motor is given by

$$\mathcal{P}_k : \begin{cases} \rho x_k^{p_1} = hax_k^{p_1} + hb\mathrm{u}_k \\ \rho x_k^{p_2} = hx_k^{p_1} \\ \mathrm{y}_k^p = x_k^{p_2} \end{cases} \tag{33}$$

Similarly, the GPI controller is designed as $\mathrm{u}_k = u_k^{cy} + u_k^{ce}$ in which u_k^{cy} and u_k^{ce} are given by

$$\mathcal{C}_k^y : \begin{cases} \rho x_k^{c_1 y} = -h\bar{b}u_k^{cy} \\ u_k^{cy} = x_k^{c_1 y} + \bar{a}\mathrm{y}_k^p \end{cases} \tag{34a}$$

$$\mathcal{C}_k^e : \begin{cases} \rho x_k^{c_1 e} = h\dfrac{k_0}{b}e_k \\ \rho x_k^{c_2 e} = hx_k^{c_1 e} - h\bar{b}u_k^{ce} + h\dfrac{k_1}{b}e_k \\ u_k^{ce} = x_k^{c_2 e} + \dfrac{1}{b}e_k \end{cases} \tag{34b}$$

where e_k denotes the output tracking error $e_k = r - \mathrm{y}_k^p$.

B. DC MOTOR CONTROL SYSTEM WITH THE ONE-BIT GPI CONTROLLER

To meet the practical constraints of the ON/OFF power converter and further reduce the computational burden, the controller is implemented using one-bit techniques. Thus, we design (4) such that $\boldsymbol{w}_t = \begin{bmatrix} \mathrm{u}_t & u_t^{cy} & u_t^{ce} & e_t \end{bmatrix}^T$,

$$E = \begin{bmatrix} 0 & \left(\bar{a} - \dfrac{1}{b}\right) & 1 & 0 & 1 \\ 0 & \bar{a} & 1 & 0 & 0 \\ 0 & -\frac{1}{b} & 0 & 0 & 1 \\ 0 & -1 & 0 & 0 & 0 \end{bmatrix}, \text{ and } F = \begin{bmatrix} \dfrac{1}{b} \\ 0 \\ \dfrac{1}{b} \\ 1 \end{bmatrix}.$$

Given that $\hat{e}_t = r - \hat{y}_t^p$ and $\hat{u}_t = \hat{u}_t^{ce} + \hat{u}_t^{cy}$, the CT ΔΣ-Q in (10) is designed to convert its input signals $\hat{\boldsymbol{w}}_t$ to binary signals $\boldsymbol{\delta}_t$, where

$$\hat{\boldsymbol{w}}_t = \begin{bmatrix} \hat{u}_t \\ \hat{u}_t^{cy} \\ \hat{u}_t^{ce} \\ \hat{e}_t \end{bmatrix} \overset{\Delta\Sigma-Q}{\Longrightarrow} \boldsymbol{\delta}_t = \begin{bmatrix} \delta_t^u \\ \delta_t^{cy} \\ \delta_t^{ce} \\ \delta_t^e \end{bmatrix}. \tag{35}$$

The one-bit CT control subsystem counterparts of (31)-(32b) are then expressed as

$$\hat{\mathcal{P}}_t : \begin{cases} \dot{\hat{x}}_t^{p1} = a\hat{x}_t^{p1} + b\phi\ \delta_t^u \\ \dot{\hat{x}}_t^{p2} = \hat{x}_t^{p1} \\ \hat{y}_t^p = \hat{x}_t^{p2} \end{cases} \tag{36}$$

$$\hat{\mathcal{C}}_t^y : \begin{cases} \dot{\hat{x}}_t^{c1y} = -\bar{b}\phi\delta_t^{cy} \\ \hat{u}_t^{cy} = \hat{x}_t^{c1y} + \bar{a}\hat{y}_t^p \end{cases} \tag{37}$$

$$\hat{\mathcal{C}}_t^e : \begin{cases} \dot{\hat{x}}_t^{c1e} = \dfrac{k_0}{b}\phi\delta_t^e \\ \dot{\hat{x}}_t^{c2e} = \hat{x}_t^{c1e} + \dfrac{k_1}{b}\phi\delta_t^e - \bar{b}\phi\delta_t^{ce} \\ \hat{u}_t^{ce} = \hat{x}_t^{c2e} + \dfrac{1}{b}\phi\delta_t^e. \end{cases} \tag{38}$$

In what follows, we extend our design of one-bit CT control systems to the more realistic case of one-bit DT control systems. It follows from (35) that we can similarly use ΔΣ-Q in (20) to convert the input signals $\hat{\boldsymbol{w}}_k$ to binary signals $\boldsymbol{\delta}_k$,

$$\hat{\boldsymbol{w}}_k = \begin{bmatrix} \hat{u}_k \\ \hat{u}_k^{cy} \\ \hat{u}_k^{ce} \\ \hat{e}_k \end{bmatrix} \overset{\Delta\Sigma-Q}{\Longrightarrow} \boldsymbol{\delta}_k = \begin{bmatrix} \delta_k^u \\ \delta_k^{cy} \\ \delta_k^{ce} \\ \delta_k^e \end{bmatrix}. \tag{39}$$

where $\hat{e}_k = r - \hat{y}_k^p$ and $\hat{u}_k = \hat{u}_k^{ce} + \hat{u}_k^{cy}$. The one-bit DT control subsystem counterparts of (33) and (34) are then expressed as

$$\hat{\mathcal{P}}_k : \begin{cases} \rho\hat{x}_k^{p1} = ha\hat{x}_k^{p1} + hb\phi\ \delta_k^u \\ \rho\hat{x}_k^{p2} = h\hat{x}_k^{p1} \\ \hat{y}_k^p = \hat{x}_k^{p2} \end{cases} \tag{40}$$

$$\hat{\mathcal{C}}_k^y : \begin{cases} \rho\hat{x}_k^{c1y} = -h\bar{b}\phi\delta_k^{cy} \\ \hat{u}_k^{cy} = \hat{x}_k^{c1y} + \bar{a}\hat{y}_k^p \end{cases} \tag{41}$$

$$\hat{\mathcal{C}}_k^e : \begin{cases} \rho\hat{x}_k^{c1e} = h\dfrac{k_0}{b}\phi\delta_k^e \\ \rho\hat{x}_k^{c2e} = h\hat{x}_k^{c1e} + h\dfrac{k_1}{b}\phi\delta_k^e - h\bar{b}\phi\delta_k^{ce} \\ \hat{u}_k^{ce} = \hat{x}_k^{c2e} + \dfrac{1}{b}\phi\delta_k^e. \end{cases} \tag{42}$$

Next, the simulations and experimental results for the DC motor control system with the one-bit GPI controller are presented in the following section.

V. RESULTS

The effectiveness of the proposed formulated one-bit DT control system embedded with the ΔΣ-Q is illustrated via both a numerical simulation and the real-time implementation of a GPI controller for position control of the DC motor.

A. GPI DESIGN REQUIREMENT

The physical parameters for the DC motor are $\tau_s = 0.023$ sec and $\ell = 27.3$. The parameters a and b in (31) are accordingly obtained such that $a = -43.4783$ and $b = 1.182 \times 10^3$. The desired response is chosen to satisfy $\zeta_r = 5$ and $\omega_n = 42.8$ (rad/sec). As a result, we obtain the GPI controller gains: $k_0 = 3.3556 \times 10^6$, $k_1 = 1.5680 \times 10^6$, $k_2 = 1.8684 \times 10^5$, $k_3 = 856$ and accordingly $\bar{a} \approx -128$.

Substituting the system parameters and GPI controller gains into (31) and (32), respectively, gives A, B and C in (3), in which A has five eigenvalues: -812.5 (single),-4.3 (double) and -423.7 (double). Thus, the sampling period h for the formulated DT control scheme has to satisfy $0 < h \leq h_M$, with $h_M = 2/812.5 = 2.5\ m$ sec, where the eigenvalues of A_d are all within the unit circle. From a practical point of view, h is chosen to be considerably smaller than h_M (roughly speaking, $0 < h \leq h_M/5$) to

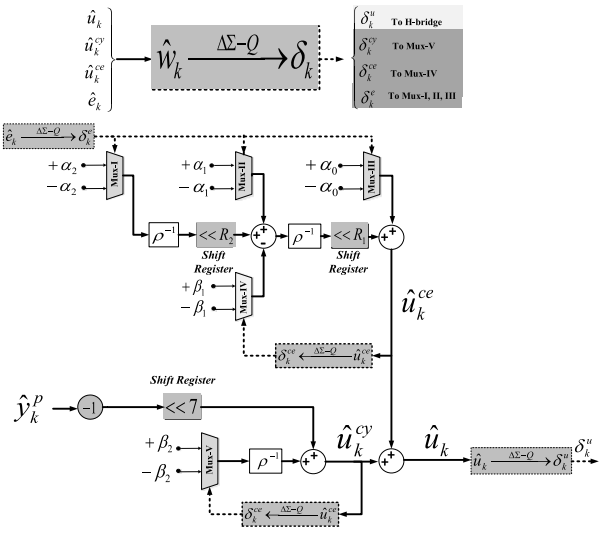

FIGURE 1. Realization of one-bit GPI controller.

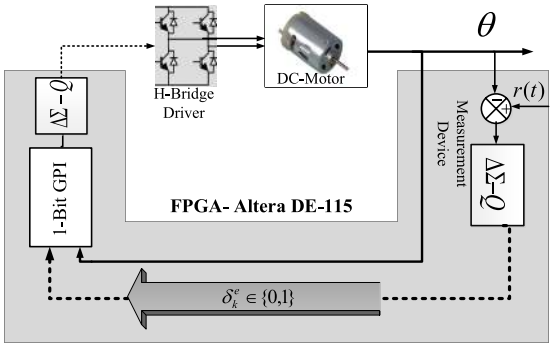

FIGURE 2. The experimental prototype of one-bit control systems.

avoid high noise or overheating the motor. The reference signal to be tracked is a square wave in which the amplitude alternates between π and $-\pi$ every 10 sec. Using a numerical simulation, we find that this gives $\|\boldsymbol{w}_k\|_\infty = 10.21$. Hence, ϕ is set to $\phi = 12$ as per Remark 2.

B. HARDWARE SAVINGS

The one-bit GPI realization is shown in Fig. 1, and the other scaled parameters are given in Table 1. It is straightforward to see that α_2 is $\mathcal{O}\left(h^2\right)$ and α_1, β_1, and β_2 are all $\mathcal{O}(h)$ (see Table 1). Therefore, as $h \to 0$, these coefficients, i.e., α_1, α_2, β_1, and β_2, tend to zero. Representing parameters with very small values demands a long FWL. To alleviate the effects related to sensitivity or overflow, scaling parameters, 2^{R_1} and 2^{R_2} where R_1, $R_2 \in \mathbb{N}$, are embedded in the controller realization to scale the sampling period h and prevent the drawbacks associated with small values [15]. In this work, we let $R_1 = 0$ and $R_2 = 8$ at $h = 1/5k$ sec and $R_1 = 1$ and $R_2 = 12$ at $h = 1/20\ m$ sec. Additionally, $\bar{a} \approx -128$ can be replaced by a *sign* converter and a shift register with 7-bits to the right.

Note that the one-bit GPI controller uses $\Delta\Sigma$-Qs to convert $\hat{\boldsymbol{w}}_k$ to $\boldsymbol{\delta}_k$ (see Fig. 1). Both the GPI and one-bit GPI controllers are described in the VHSIC Hardware Description Language (VHDL) and then compiled by an Altera DE2-115 FPGA by means of Quartus II. Fig. 2 shows the experimental prototype of the one-bit control DC motor system. Table 2 shows the hardware consumption for both the conventional GPI and one-bit GPI controllers. We successfully design a *multiplier-less* one-bit GPI controller with a high cost savings in terms of hardware with approximately 75% of the DSP elements. As an immediate advantage of one-bit processing, the six multipliers in the conventional GPI controller are replaced by six simple multiplexers in the one-bit GPI controller. Furthermore, the conventional GPI controller requires PWM

TABLE 1. One-bit GPI parameters.

Controller parameter	Value
α_0	ϕ/b
α_1	$h\phi k_1 2^{R_1}/b$
α_2	$h^2\phi k_0 2^{R_2}/b$
β_1	$h\phi b$
β_2	$-h\phi\bar{b}$

TABLE 2. Hardware Resource Consumption.

General Hardware Resources		
Controller	Multiplier	Multiplexers
Standard GPI	6	0
One-bit GPI	0	6

FPGA Hardware Resources		
Controller	DSP - LE	DSP 18×18
Standard GPI	48	24
One-bit GPI	12	0

to convert the control signals to switch signals to drive the switch components of the H-bridge. In the one-bit GPI controller, the $\Delta\Sigma$-Q replaces the conventional PWM to convert $\hat{u}_k$ to δ_k^u for the same purpose, i.e,. control the switch components in the H-bridge (LMD18200). This results in a significant reduction of the overall implementation costs.

C. SIMULATION RESULTS

To verify the effectiveness of the one-bit GPI controller in a real-time implementation, a conventional GPI controller is utilized and compared with the one-bit GPI controller with two sampling periods, i.e., 5 *kHz* and 20 *kHz*. The comparison is carried out for both types of GPI controllers in terms of performance. Therefore, some specifications of the transient response, e.g., the settling time t_s, peak time t_p and overshoot M_p are considered in this comparison.

Fig. 3 shows the simulation results at sampling frequencies of 5 *kHz* and 20 *kHz*. For one-bit GPI controllers, we can easily notice the significant reduction in the free oscillations (limit cycles) in both the position and speed responses by increasing the sampling frequency from 5 *kHz* to 20 *kHz*. Nevertheless, both the conventional and one-bit GPI controllers

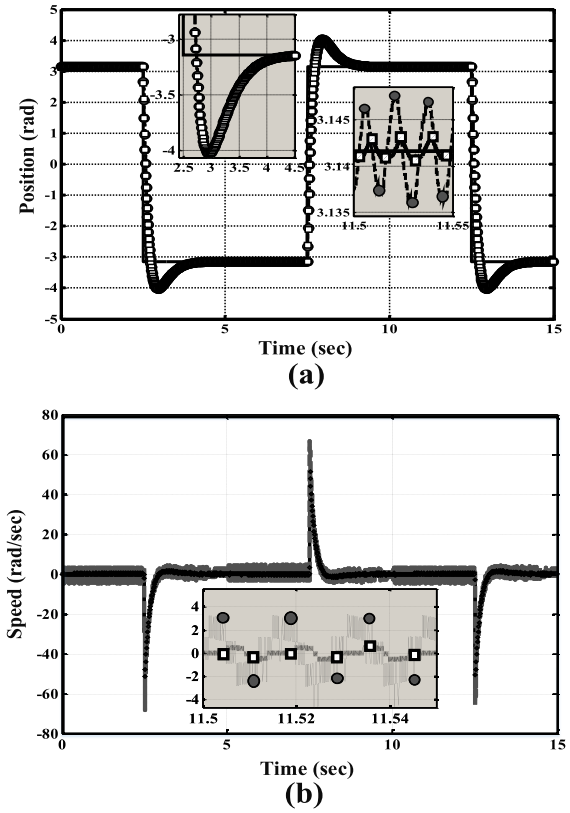

FIGURE 3. Simulation results of (a) position control at sampling frequency 5 *kHz* (dashed line with circle points) and 20 *kHz* (solid line with square points) and (b) speed response at 5 *kHz* (gray line with circle points) and 20 *kHz* (solid line with square points).

exhibit similar specifications during the transient response with $t_p = 0.4$ sec, $t_s = 1.7$ sec and $M_p = 25\%$.

D. EXPERIMENTAL RESULTS

The control system from the signal measurement (shaft position) to the power converter is fully implemented using the FPGA platform. The output of the system, i.e., the shaft position, is estimated using a quadrature encoder attached to the shaft of the DC motor. The results of tracking the reference signal for the GPI controllers with sampling frequencies of 5 *kHz* and 20 *kHz* are shown in Fig. 4.

In accordance with Fig. 4(a)-(b), the one-bit GPI controller performs satisfactorily in the tracking performance of the position reference with a 5 *kHz* sampling frequency. Notice that the one-bit GPI controller exhibits different transient response characteristics than the desired transient response characteristics. As shown in Fig. 4(a), there is a reduction in both the peak time ($t_p = 0.2$ sec) and settling time ($t_s = 0.4$ sec) and a higher overshoot with $M_p = 35\%$. This implies that the one-bit GPI controller yields high dither (noise) in the system bandwidth, as depicted in the measured angular speed response of the one-bit GPI controller in Fig. 4(b). As shown in Fig. 4(c)-(d), the one-bit GPI controller successfully achieves the desired response with transient response specifications of $t_p = 0.4$ sec, $t_s = 1.7$ sec and $M_p = 25\%$ using a sampling frequency of 20 *kHz*.

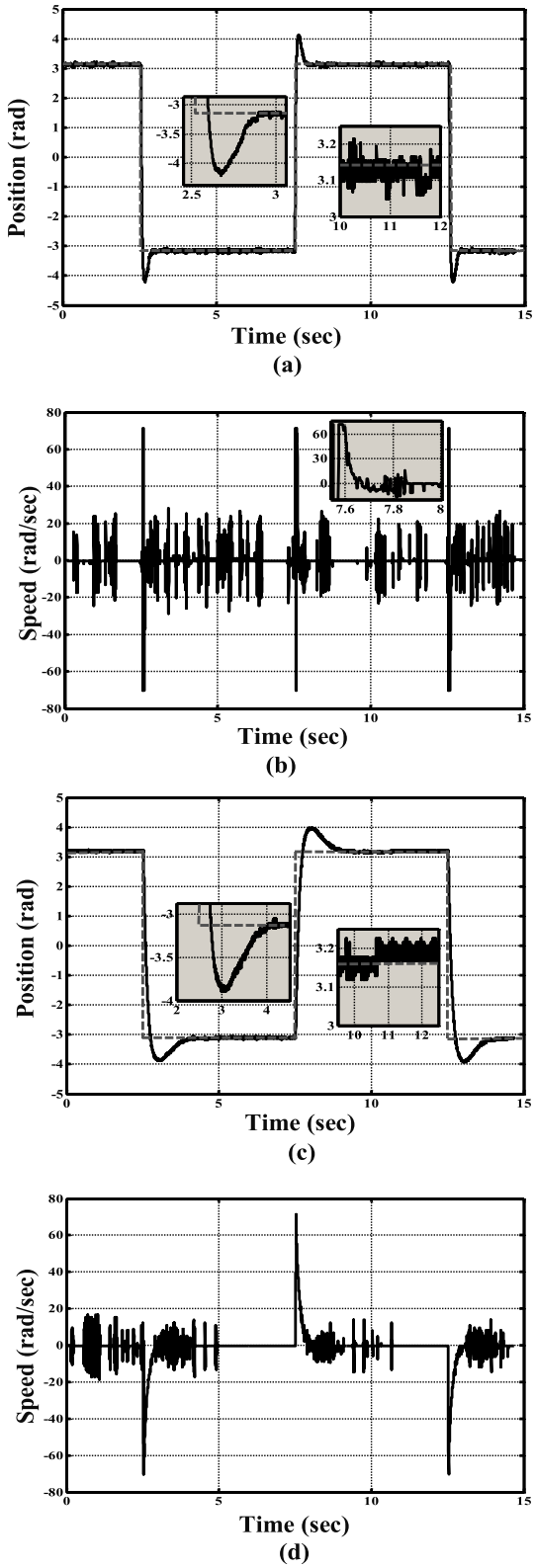

FIGURE 4. The results of experiment for (a) position control and (b) speed response for one-bit GPI at 5 *kHz*. The results of experiment for (c) position control and (d) speed response for one-bit GPI at 20 *kHz*.

Remark 3: From realization and implementation point of view, it is worth noting that proportional and integral (PI) control strategy can be considered as a special

case of the GPI, see [27]–[29]. Hence, the methodology we consider in this work for designing one-bit GPI controller, can be adopted to implement a one-bit PI control strategy.

Remark 4: Some pioneering works show that for a given sampling period h, the PCMs such as $\Delta\Sigma$-Q significantly reduce the network bandwidth (data rate) by transmitting a single bit every sample time (i.e., 1 bit/h) over the communication network [9], [33]. Although in this work, we restrict our analysis to the one-bit control system with traditional time-triggered mechanisms (TTMs), i.e., periodic sampling, it is of interest to consider one of the new event-triggered mechanisms (ETMs) [9], [34]–[36]. More precisely, the $\Delta\Sigma$-Q can be effectively applied to periodic-event-triggered control, where the event triggering conditions are synchronized to a periodic clock such that data are transmitted and the control law is executed periodically only if the event takes place. Thus, it is important to consider the performance and stability analysis of the control system using an event-triggered $\Delta\Sigma$-Q, which will be investigated thoroughly in subsequent work.

VI. CONCLUSION

In this paper, a generalized one-bit control system has been presented. We have applied ECB-SMC to study the stability and performance of the proposed system motivated by the fact that one-bit control system is a differential inclusion in the sense of Filippov solutions. We show that the binary signals in a one-bit control system are equivalent to their counterpart signals in the conventional control system during ideal sliding motion. The feasibility and effectiveness of the use of $\Delta\Sigma$-Qs in both CT and DT control systems, where a multiplier-less one-bit GPI controller structure for realizing Euler's discretization, is demonstrated through a numerical simulation and a real-time implementation using an example of a DC motor. We successfully show that the one-bit control system achieves the desired steady and transient response specifications, while offering significantly high costs savings in terms of hardware resources compared to the standard control system. The results of the simulation and experiment demonstrate that the one-bit control system effectively controls the system and achieves the desired specifications while consuming fewer hardware resources than the standard control system.

REFERENCES

[1] S. Qiao, J. Wu, X. Zhan, and T. Han, "Performance limitation of networked control systems with networked delay and two-channel noises constraints," *Syst. Sci. Control Eng.*, vol. 7, no. 1, pp. 28–35, 2019. doi: 10.1080/21642583.2018.1558421.

[2] H. Sira-Ramírez, "Sliding mode-Δ modulation control of a 'buck' converter," in *Proc. 42nd IEEE Int. Conf. Decis. Control*, vol. 3, Dec. 2003, pp. 2999–3004.

[3] X. Wu, Z. Xie, X. Bai, and T. Kwan, "Design of a 1-bit MEMS gyroscope using the model predictive control approach," *Sensors*, vol. 19, no. 3, p. 730, 2019.

[4] A. J. Frazier and M. K. Kazimierczuk, "DC-AC power inversion using $\Sigma - \Delta$ modulation," *IEEE Trans. Circuits Syst. I, Fundam. Theory Appl.*, vol. 47, no. 1, pp. 79–82, Jan. 2000.

[5] J. Roh, "Digital PWM controller with one-bit noise-shaping interface," *Analog Integr. Circuits Signal Process.*, vol. 49, pp. 11–17, Oct. 2006. doi: 10.1007/s10470-006-8698-0.

[6] J. Paramesh and A. von Jouanne, "Use of sigma-delta modulation to control EMI from switch-mode power supplies," *IEEE Trans. Ind. Electron.*, vol. 48, no. 1, pp. 111–117, Feb. 2001.

[7] D. Almakhles, "Two-level quantised control systems: Sliding-mode approach," *Int. J. Control*, pp. 1–9, Jun. 2018. [Online]. Available: https://www.tandfonline.com/doi/citedby/10.1080/00207179.2018.1484569?scroll=top&needAccess=true. doi: 10.1080/00207179.2018.1484569.

[8] D. Almakhles, A. K. Swain, A. Nasiri, and N. Patel, "An adaptive two-level quantizer for networked control systems," *IEEE Trans. Control Syst. Technol.*, vol. 25, no. 3, pp. 1084–1091, May 2017.

[9] U. Premaratne, S. K. Halgamuge, and I. M. Y. Mareels, "Event triggered adaptive differential modulation: A new method for traffic reduction in networked control systems," *IEEE Trans. Autom. Control*, vol. 58, no. 7, pp. 1696–1706, Jul. 2013.

[10] T. Li and Y. Fujimoto, "Control system with high-speed and real-time communication links," *IEEE Trans. Ind. Electron.*, vol. 55, no. 4, pp. 1548–1557, Apr. 2008.

[11] M. A. Aldajani and A. H. Sayed, "Adaptive predictive power control for the uplink channel in DS-CDMA cellular systems," *IEEE Trans. Veh. Technol.*, vol. 52, no. 6, pp. 1447–1462, Nov. 2003.

[12] S. Tatikonda and S. Mitter, "Control under communication constraints," *IEEE Trans. Autom. Control*, vol. 49, no. 7, pp. 1056–1068, Jul. 2004.

[13] A. C. Thompson, P. O'Shea, Z. M. Hussain, and B. R. Steele, "Efficient single-bit ternary digital filtering using sigma-delta modulator," *IEEE Signal Process. Lett.*, vol. 11, no. 2, pp. 164–166, Feb. 2004.

[14] C.-W. Ng, "Bit-stream signal processing on FPGA," Ph.D. dissertationn, Dept. Elect. Electron. Eng., Univ. Hong Kong, Hong Kong, 2008.

[15] X. Wu, V. A. Chouliaras, J. L. Nunez-Yanez, and R. M. Goodall, "A novel $\Delta\Sigma$ control system processor and its VLSI implementation," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 16, no. 3, pp. 217–228, Mar. 2008.

[16] D. J. Almakhles, A. K. Swain, and N. D. Patel, "Stability and performance analysis of bit-stream-based feedback control systems," *IEEE Trans. Ind. Electron.*, vol. 62, no. 7, pp. 4319–4327, Jul. 2015.

[17] E. Monmasson, L. Idkhajine, M. Cirstea, I. Bahri, A. Tisan, and M. W. Naouar, "FPGAs in industrial control applications," *IEEE Trans. Ind. Informat.*, vol. 7, no. 2, pp. 224–243, May 2011.

[18] E. Monmasson, L. Idkhajine, and M. W. Naouar, "FPGA-based controllers," *IEEE Ind. Electron. Mag.*, vol. 5, no. 1, pp. 14–26, Mar. 2011.

[19] N. Wong and T.-S. Ng, "A generalized direct-form delta operator-based IIR filter with minimum noise gain and sensitivity," *IEEE Trans. Circuits Syst.*, vol. 48, no. 4, pp. 425–431, Apr. 2001.

[20] G. C. Goodwin, R. H. Middleton, and H. V. Poor, "High-speed digital signal processing and control," *Proc. IEEE*, vol. 80, no. 2, pp. 240–259, Feb. 1992.

[21] D. A. Johns and D. M. Lewis, "Design and analysis of delta-sigma based IIR filters," *IEEE Trans. Circuits Syst. II. Analog Digit. Signal Process.*, vol. 40, no. 4, pp. 233–240, Apr. 1993.

[22] J. Kauraniemi, T. I. Laakso, I. Hartimo, and S. J. Ovaska, "Delta operator realizations of direct-form IIR filters," *IEEE Trans. Circuits Syst. II. Analog Digit. Signal Process.*, vol. 45, no. 1, pp. 41–52, Jan. 1998.

[23] R. H. Middleton and G. C. Goodwin, *Digital Control and Estimation: A Unified Approach*. Englewood Cliffs, NJ, USA: Prentice-Hall, 1990.

[24] H. Fujisaka, R. Kurata, M. Sakamoto, and M. Morisue, "Bit-stream signal processing and its application to communication systems," *IEE Proc. Circuits, Devices Syst.*, vol. 149, no. 3, pp. 159–166, 2002.

[25] C.-W. Ng, N. Wong, H. K.-H. So, and T.-S. Ng, "On IIR-based bit-stream multipliers," *Int. J. Circuit Theory Appl.*, vol. 39, no. 2, pp. 149–158, Feb. 2011.

[26] A. F. Filippov, *Differential Equations With Discontinuous Righthand Sides*. Norwell, MA, USA: Kluwer, 1998.

[27] X. Zhou, Z. Gu, and F. Yang, "Resilient event-triggered output feedback control for load frequency control systems subject to cyber attacks," *IEEE Access*, vol. 7, pp. 58951–58958, 2019.

[28] J. A. Juárez-Abad, J. Linares-Flores, E. Guzmán-Ramírez, and H. Sira-Ramírez, "Generalized proportional integral tracking controller for a single-phase multilevel cascade inverter: An FPGA implementation," *IEEE Trans. Ind. Informat.*, vol. 10, no. 1, pp. 256–266, Feb. 2014.

[29] E. W. Zurita-Bustamante, J. Linares-Flores, E. Guzman-Ramirez, and H. Sira-Ramirez, "A comparison between the GPI and PID controllers for the stabilization of a DC–DC 'buck' converter: A field programmable gate array implementation," *IEEE Trans. Ind. Electron.*, vol. 58, no. 11, pp. 5251–5262, Nov. 2011.
[30] H. Sira-Ramírez, *Sliding Mode Control: The Delta-Sigma Modulation Approach*. Basel, Switzerland: Birkhäuser Verlag, 2015.
[31] D. Almakhles, A. K. Swain, and A. Nasiri, "The dynamic behaviour of data-driven Δ-M and ΔΣ-M in sliding mode control," *Int. J. Control*, vol. 90, no. 11, pp. 2406–2414, 2017. doi: 10.1080/00207179.2016.1250160.
[32] V. I. Utkin, *Sliding Modes in Control and Optimization*. Berlin, Germany:Springer, 1992.
[33] C. Canudas-de-Wit, F. Gomez-Estern, and F. R. Rubio, "Delta-modulation coding redesign for feedback-controlled systems," *IEEE Trans. Ind. Electron.*, vol. 56, no. 7, pp. 2684–2696, Jul. 2009.
[34] W. P. M. H. Heemels, M. C. F. Donkers, and A. R. Teel, "Periodic event-triggered control for linear systems," *IEEE Trans. Autom. Control*, vol. 58, no. 4, pp. 847–861, Apr. 2013.
[35] J. Lunze and D. Lehmann, "A state-feedback approach to event-based control," *Automatica*, vol. 46, no. 1, pp. 211–215, Jan. 2010.
[36] D. E. Quevedo and V. Gupta, "Sequence-based anytime control," *IEEE Trans. Autom. Control*, vol. 58, no. 2, pp. 377–390, Feb. 2013.

DHAFER J. ALMAKHLES (M'13) received the B.E. degree in electrical engineering from the King Fahd University of Petroleum and Minerals, Dhahran, Saudi Arabia, in 2006, and the master's (Hons.) and Ph.D. dgerees from The University of Auckland, New Zealand, in 2011 and 2016, respectively. Since 2016, he has been with Prince Sultan University, Saudi Arabia, where he is currently an Assistant Professor with the Department of Communications and Networks Engineering and the Director of Science and Technology Unit. He is also the Leader for the Renewable Energy Research Team and Laboratory, Prince Sultan University. His research interests include the hardware implementation of control theory, signal processing, networked control systems, and sliding mode.

R. SAKTHIVEL (M'97–SM'13) received the B.Sc., M.Sc., M.Phil., and Ph.D. degrees in mathematics from Bharathiar University, Coimbatore, India, in 1992, 1994, 1996, and 1999, respectively. From 2000 to 2001, he was a Lecturer with the Department of Mathematics, Sri Krishna College of Engineering and Technology, Coimbatore. From 2001 to 2003, he was a Postdoctoral Fellow with the Department of Mathematics, Inha University, Incheon, South Korea. He was a Visiting Fellow with the Max Planck Institute, Magdeburg, Germany, in 2002. From 2003 to 2005, he was a Japan Society for the Promotion of Science Fellow with the Department of Systems Innovation and Informatics, Kyushu Institute of Technology, Kitakyushu, Japan. He was a Research Professor with the Department of Mathematics, Yonsei University, Seoul, South Korea, until 2006. From 2006 to 2008, he was a Postdoctoral Fellow (Brain Pool Program) with the Department of Mechanical Engineering, Pohang University of Science and Technology, Pohang, South Korea. From 2008 to 2013, he was an Assistant Professor and an Associate Professor with the Department of Mathematics, Sungkyunkwan University, Suwon, South Korea. From 2013 to 2016, he was a Professor with the Department of Mathematics, Sri Ramakrishna Institute of Technology, India. He is currently a Professor with the Department of Applied Mathematics, Bharathiar University. He has published over 260 research papers in reputed Science Citation Index journals. His current research interests include systems and control theory, optimization techniques, and nonlinear dynamics. He has been on the Editorial Board of international journals, including the IEEE Access, *Journal of the Franklin Institute*, *Neurocomputing*, *Advances in Difference Equations*, and *Journal of Electrical Engineering & Technology*.

AKSHYA SWAIN (M'97–SM'13) received the B.Sc.Eng. and M.Sc.Eng. degrees from Sambalpur University, India, in 1985 and 1988, respectively, and the Ph.D. degree from the Department of Automatic Control and Systems Engineering, The University of Sheffield, in 1997. He joined the Department of Electrical and Computer Engineering, The University of Auckland, in September 2002. His research interests include nonlinear system identification and control, biomedical signal processing, sensor networks, and control applications to power systems and inductive power transfer systems. He is currently a member of the Editorial Board of the *International Journal of Automation and Control* and *International Journal of Sensors, Wireless Communications and Control*.

UMASHANKAR SUBRAMANIAM (M'97–SM'13) has more than 15 years of teaching, research, and industrial Research and Development experience. He was an Associate Professor and the Head of VIT Vellore and Senior Research and Development and Senior Application Engineer in the fields of power electronics, renewable energy, and electrical drives. He is currently an Associate Professor with the Renewable Energy Laboratory, College of Engineering, Prince Sultan University, Saudi Arabia. He has published more than 250 research papers in national and international journals and conferences. He has also authored/coauthored/contributed 12 books/chapters and 12 technical articles on power electronics applications in renewable energy and allied areas. He is also a member of IACSIT, IDES, and ISTE. He was an Executive Member, from 2014 to 2016. He has taken charge as the Vice Chair of IEEE Madras Section and the Chair of the IEEE Student Activities, in 2018. He has been the Vice Chair of the IEEE MAS Young Professional of the IEEE Madras Section, since 2017. He is also an Editor of *Heliyon* (Elsevier). He received the Danfoss Innovator Award-Mentor, from 2014 to 2015 and 2017 to 2018, and the Research Award from VIT University, from 2013 to 2018. He also received the INAE Summer Research Fellowship for the year 2014. Under his guidance, 24 P.G. students and more than 25 U.G. students completed the senior design project work, and also, six Ph.D. scholars completed Doctoral thesis as a Research Associate. He is also involved in collaborative research projects with various international- and national-level organizations and research institutions.

KHALED ALMUSTAFA received the B.E.Sc. degree in electrical engineering and the M.E.Sc. and Ph.D. degrees in wireless communication from the University of Western Ontario, London, ON, Canada, in 2003, 2004, and 2007, respectively. He is currently an Associate Professor with the Department of Information Systems (IS), College of Computer Science and Information Systems (CCIS), Prince Sultan University (PSU), Riyadh, Saudi Arabia. He is also a General Supervisor of the Information Technology and Computer Services Center (ITCS), PSU, the Chairman of the Department of Communication and Networks Engineering (CME), and the Vice Dean for the College of Engineering, PSU, and the Director of the Research and Initiatives Center, PSU. His research interests include error performance evaluation of MIMO communication systems in partially known channels, adaptive modulation, channel security, text recognition models, control systems with renewable energy applications, as well as features selections and data prepossessing.