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A generic interface chip for capacitive sensors in low-power multi-parameter microsystems

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Abstract

This paper presents a generic low-power sensor interface chip compatible with smart microsystems and a wide range of capacitive transducers. The interface chip is highly programmable, can communicate with an external microcontroller using a nine-line sensor bus standard, contains a switched-capacitor readout circuit, supports sensor self-test, and includes a temperature sensor. The circuit can interface with up to six external sensors and contains three internal programmable reference capacitors in the range of 0.15–8 pF. The chip measures 3.2×3.2 mm in a standard 3-μm single-metal double-poly p-well process, dissipates less than 2.2 mW from a single 5 V supply, and can resolve input capacitance variations of less than 1 fF in 10 Hz bandwidth. © 2000 Elsevier Science S.A. All rights reserved.

Keywords: Interface circuit; Microsystem; Sensor bus; Capacitive sensors

1. Introduction

As the MicroElectroMechanical Systems (MEMS), or Microsystems, industry continues to experience accelerating growth, there has been an obvious trend toward combining MEMS transducers with increasingly sophisticated circuits. One step in this evolution is to integrate circuitry and transducers to form ''smart'' sensors, yet the low cost and wide availability of present signal processing electronics make it possible to go one step further and form entire smart microsystems. These microsystems, which combine multiple microsensors and/or microactuators with signal processing circuitry on a common substrate, are capable of gathering electronic data from the physical world, processing and acting on the information, and transferring the data to other electronic systems which gain intelligence from this process [1]. It is precisely these capabilities which ensure that microsystems will have a pervasive impact on the future of the microelectronics industry in application fields ranging from automotive systems to health care. A significant subset of such microsystems will be small, portable, autonomous units [2,3] that can be distributed to collect data over a long period of time. Because these portable microsystems will be battery powered, one of their key constraints is the overall power consumption, which must be minimized without sacrificing performance. A low-power transducer front-end is vital to this effort, yet most of the devices being manufactured today are piezoresistive and consume large amounts of power. Capacitive microsensors provide an attractive alternative since they have no intrinsic power dissipation and can be read out using relatively low-power circuit techniques while offering high sensitivity and self-test capabilities [4,5]. However, the various capacitive transducers that have been reported display a wide range of base capacitances and sensitivities depending on the technology and structure of each device [6]. This variation among transducers places a challenging requirement on the sensor interface circuit, especially in microsystems with multiple sensors such as the one shown in Fig. 1 [5]. For systems such as this, there is a significant advantage to using a generic interface circuit capable of reading out multiple microsensors, each of which may have a different base capacitance and sensitivity. Furthermore, a generic interface circuit should provide a standard communication link to the main microsystem controller, support sensor self-test and self-calibration, support multi-ranging within a single sensor, dissipate low power, and occupy very small die area with no external

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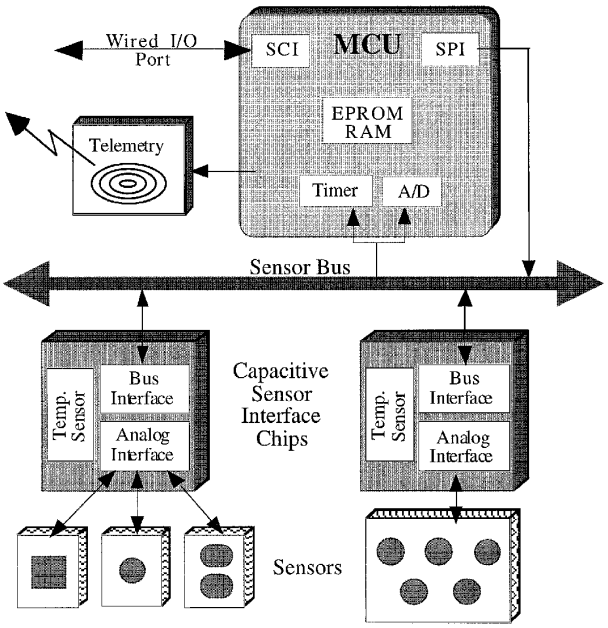

Fig. 1. Block diagram of a microsystem that utilizes the generic capacitive sensor interface chip and multiple microsensors to measure a variety of physical parameters.

components. While numerous readout circuits for capacitive microsensors have been introduced [7–11] and some have even been commercialized [12,13], to date, a generic interface with all of these features has not been reported. A novel universal transducer interface is reported in Ref. [11] that can read out capacitive sensors with a wide range of base capacitances, however it does not support standard communication with a microcontroller, self-test and self-calibration.

This paper describes a generic capacitive sensor interface for multi-parameter microsystems which satisfies all the aforementioned requirements. First, a brief description of a microsystem that utilizes this interface circuit is presented to highlight both the requirements and the application of the circuit. Then, the interface chip architecture is presented, followed by a description of its major building blocks. Finally, measurement and test results for the fabricated chip are presented.

2. Microsystem description

The microsystem shown in Fig. 1 utilizes an open architecture with a standard sensor bus which allows the system to be populated with sensors and actuators as required by various applications such as, weather monitoring or electronic systems health monitoring for condition-based maintenance. Such applications require that an array of parameters be measured, and the generic capacitive interface chip is a critical component of the overall system because it allows a standard microcontroller to communicate with, and collect data from, a wide variety of sensors. For instance, the currently developed microsystem accommodates sensors for measuring a variety of environmental parameters including temperature, barometric pressure, relative humidity, and acceleration/vibration [4,5]. As shown in Table 1, these sensors display a wide range of base capacitance and sensitivity, which must be covered by the interface chip.

The heart of the microsystem is a microcontroller unit (MCU) that provides stored program control and data handling as well as sensor-specific software routines for in-module sensor calibration, digital compensation, and self-test. The MCU communicates with the front-end transducers via the sensor interface chips and a nine-wire sensor bus. Once sensor data has been collected and compensated in-module, it can be stored in-module or output through either a hardwired serial I/O port or an on-board RF transmitter.

The sensor bus is a central part of the microsystem architecture that provides access to multiple sensors/actuators while using a limited number of interconnects. This bus is based on a standard used at the University of Michigan and was chosen for its functionality as well as its compatibility with existing systems. Although a variety of bus standards are still being used throughout the sensor industry, this sensor bus provides a reduced line count without requiring complex signal decoding, and it is a predecessor to the very similar and recently adopted IEEE P1451 standard. It consists of nine lines: three power leads, four lines for synchronous serial communication, a data output line, and a data valid/interrupt signal [4]. The three power leads are the system supply, ground reference, and a switched reference voltage for devices that can be powered-down during a low-power system sleep mode. For synchronous communication with the front-end devices, chip enable and data strobe signals provide handshaking for use with a programmable-frequency clock and a serial data line. The data out line is used for sensor data output that can be either an analog voltage, a frequency encoded set of pulses, or a serial bitstream. The last line of the sensor bus is data valid, which signals the MCU when valid data is present on the data out line. Data valid is also used as an interrupt from the interface chip that can initiate an event triggered sensor readout when the bus is otherwise idle.

Table 1
Base capacitance and sensitivity of several sensors employed in the microsystem

Sensor	Base capacitance (pF)	Full scale °C (pF)	Sensitivity
Barometric pressure	4–8	1.5	7.5 fF/Torr
Relative humidity	6	0.25	4 fF/% RH
Acceleration	0.8	0.16	40 fF/g

3. Chip architecture

Fig. 2 shows the block diagram of the interface chip. Communication with the MCU is performed over the sensor bus and is handled by the bus interface unit. Serial data transmitted over the bus is received, decoded, and applied to control various interface chip blocks. The readout circuit utilizes a low-noise front-end charge integrator to read out the difference between the sensor capacitance and a reference capacitor [8]. An input multiplexer enables the chip to interface with up to six capacitive sensors. Furthermore, the chip can be digitally programmed to operate with one of three external and/or internal reference capacitors. The on-chip reference capacitors are laser trimmable in a range of 0.15–8 pF in 0.15-pF capacitance steps. The programmability of the reference capacitors allows the chip to interface with capacitive sensors having a wide range of base capacitance and also provides input offset control.

The chip analog signal path consists of an input multiplexer, the input charge integrator, a gain stage, an output sample/hold circuit, and an output multiplexer. The gain stage can be programmed on-line to one of three preset gain values each set by laser-trimming. Also the gain can be adjusted at the first stage by laser trimming the charge integration capacitor. A digital gain control at this stage is not used to avoid using additional switches in the charge integration path at the input stage. Note that the thermal noise of the series switches contributes to the total input-referred noise. These gains can be used to accommodate sensors with different sensitivities or for multi-ranging a single sensor and can be adjusted by laser trimming the on-chip capacitors. The overall readout sensitivity can be varied from 0.23 to 73.5 mV/fF using both digital programming and laser trimming, which gives an effective gain variation from 1 to 312. The output multiplexer provides access to the sensor bus for both the capacitive readout circuitry and the on-chip temperature sensor.

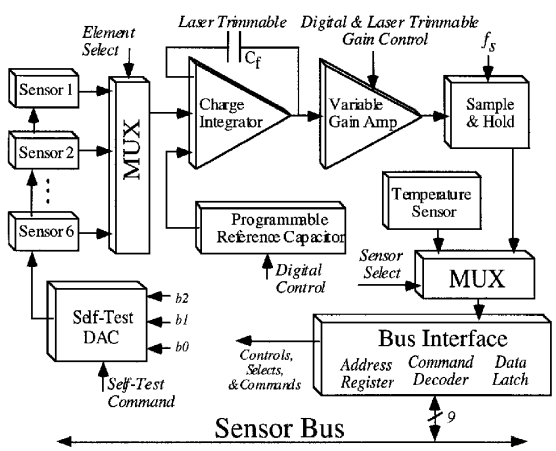

Fig. 2. Block diagram of the capacitive sensor interface chip.

The interface chip also supports self-test and self-calibration. A 3b on-chip DAC is utilized to generate a variable-amplitude two-phase clock for driving the sense and reference capacitors in each input charge integration cycle. The variable amplitude clock can be used to apply a programmable dc voltage and electrostatic force to the sensor for self-test and self-calibration. In self-test mode, the programmable electrostatic force is used to move a sensor structure and generate a change in the sensor's output. In self-calibration mode, the sensor response can be tracked and calibrated while a set of predetermined electrostatic forces are applied. The variable amplitude clock also provides additional control of the overall readout circuit sensitivity by setting the input charge transferred to the front-end charge integrator.

4. Circuit building blocks

4.1. Sensor bus interface unit

The sensor bus interface unit, illustrated in Fig. 3, handles the communication between the microsystem controller and the capacitive interface chip through the sensor bus. The bus interface unit consists of a series of shift registers that load the input serial data, logic circuitry that decodes incoming instructions, on-chip memory to store data written to the interface chip, and an output multiplexer. Each interface chip contains a 4b laser-programmable chip address and a 4b comparator that checks the chip address of an incoming instruction. The selected chip then loads in a 3b command code and a 5b element address as set by the sensor bus data format, which allows for eight individual commands to be issued to each of 32 read (e.g., sensor) or write (e.g., actuator or memory register) elements. On the generic capacitive sensor interface, during a read command, three of the element address bits are decoded to select one of six external capacitive sensors or the on-chip temperature sensor. The remaining two element address bits are used to select one of three on-chip reference capacitors used by the switched-capacitor readout circuit block. During a write command, data from the microsystem controller is stored in one of three on-chip registers. This data is used to control several other circuit blocks on the chip such as the gain stage of the switched-capacitor readout circuit and the DAC. Based on the input instruction, the output multiplexer selects which sensor data will be put on the shared data out line of the sensor bus and ensures that the output signal is disabled at the end of a sensor read command.

4.2. Switched-capacitor readout circuit

The readout circuit is a switched-capacitor circuit consisting of a low-noise charge integrator, a digitally-programmable gain stage and a sample/hold circuit as shown

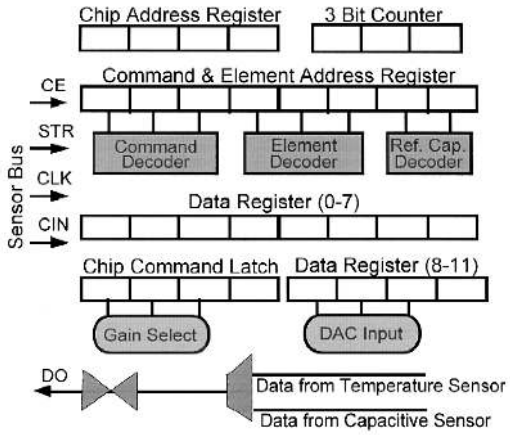

Fig. 3. Diagram of the sensor bus interface unit of the capacitive sensor interface chip. The four signals of this nine-wire bus, which are not shown, are three power leads and a data valid line.

in Fig. 4. Since the circuit operates from a single supply, an internal analog ground reference level, half way between the supply level and ground, is generated on-chip and is shown as Vref in Fig. 4. A switched-capacitor front-end is selected for the capacitance readout because the gain of this circuit is less sensitive to variations in input parasitic capacitance. In addition, the dc reference voltage is preferred because a low noise reference can be more easily generated on chip as compared to a low-noise ac source. Note that any noise in the reference voltage couples directly to the input. For instance, in an ac bridge with a 10-kHz source voltage, an amplitude of 1 V, and 10 pF sense capacitor, a noise level of 1 $\mu V/\sqrt{Hz}$ on the source voltage is equivalent to 1 fF input capacitance change. In a charge integrator using a 1 V switched dc source with 1 μV noise, the equivalent input capacitance change due to the voltage source noise is 10 af. In our case, the front-end circuit has a calculated resolution of 0.4 fF in 500 Hz bandwidth considering 10 pF sense capacitor, 10 pF reference capacitor, 2 pF charge integrator capacitor, 30 pF parasitic capacitance, total input amplifier noise of 10 μV from dc to 1 kHz and a thermal noise of 50 $nV/\sqrt{Hz}$, a dc noise of 20 μV on a 5-V sensor charging voltage, and a sampling frequency of 50 kHz. The kT/C noise of the front-end charge integrator is reduced by using a large integrating capacitor (2–8 pF, depending on the gain setting). Clock switching noise is reduced by using sized dummy switches at the high-impedance nodes; a fully differential circuit is not utilized in order to save power and die area. The control clocks of the dummy switches are slightly delayed [14] since better charge compensation occurs when the actual switches are first turned off completely.

The input switches are controlled so that at each instant only one of the sense capacitors (Cs) and one of the reference capacitors (Cref) are connected to the circuit. During $\phi 1$, the reset switch of the charge integrator is closed and Cs is charged through the charge integrator output. Once $\phi 1$ goes low, a packet of charge proportional to the difference between Cs and Cref is integrated on the feedback capacitor of the first stage (Cf1). Subsequently $\phi 2$ goes high, the second stage integrator is reset and either Cg1, Cg2, or both Cg1 and Cg2 charge to the output level of the first stage. The gain of the second stage is determined by the ratio of the total capacitance switched into its input to the feedback capacitance (Cf2). Clock phases $\phi 3$ and $\phi 4$ are slightly delayed $\phi 1$ and $\phi 2$ clocks, which become active only when gain 1 or 3 is selected. Similarly, $\phi 5$ and $\phi 6$ are delayed $\phi 1$ and $\phi 2$ clock phases that are active only when digital gain 2 or 3 is set. Therefore, the gain of the second stage is selected by controlling switching of Cg1 and Cg2 at its input. During $\phi 3$ ($\phi 5$) clock phase, the charge stored on Cg1 and Cg2 capacitors is integrated on Cf2. Finally, the output of the second stage is sampled and held at the input of the third stage during ϕs. The circuit is designed to operate with a 50-kHz clock. The non-overlap time of the clock phases and the clock delays are both 250 ns.

Fig. 5 shows the schematic of the opamp used in the switched-capacitor circuit. The opamp is designed to provide low noise and good high frequency PSRR with low power dissipation and to drive capacitive loads over a wide range. Transistors M1–M5 form the input differential stage, with large PMOS transistors (M1–M2) used to reduce noise. The amplifier noise is primarily determined by the noise of the input transistors. The main gain stage is a

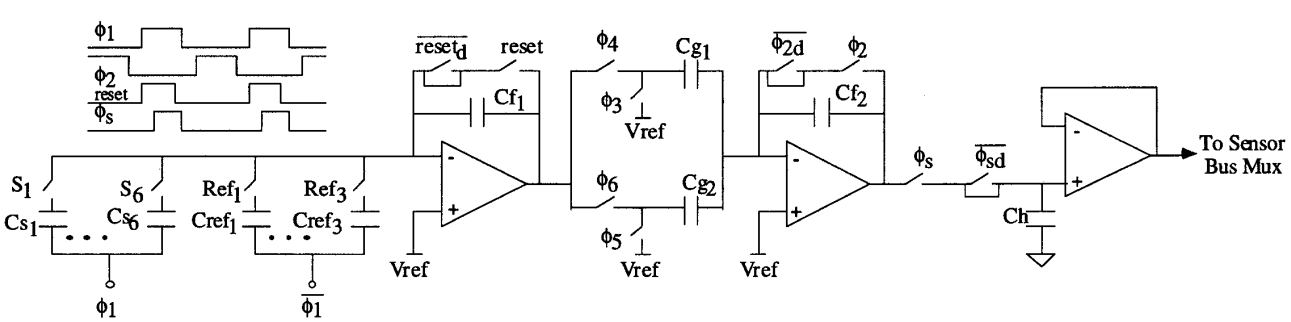

Fig. 4. Schematic diagram of the switched-capacitor readout circuit.

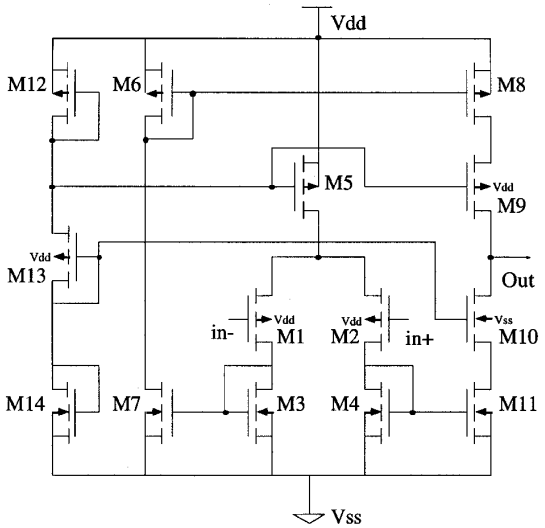

Fig. 5. Schematic diagram of the low-noise operational amplifier used in the readout circuit front-end.

cascode output stage consisting of M8–M11. The dominant pole is determined by the load capacitance, which eliminates the need for a compensation capacitor and effectively improves the high frequency PSRR. Also, the load capacitance can vary over a wide range without causing stability problems and is driven efficiently by the output stage. The opamp dissipates less than 420 μW from a 5-V supply and has a slew rate of 1 V/μs with a 50-pF capacitive load.

4.3. Digital-to-analog converter

Fig. 6 shows a schematic diagram of the self-test current-mode DAC. The 3b DAC consists of three selectable current mirrors (Mp0–Mp3) driving an on-chip polysilicon resistor (R) to obtain voltage-mode output. This configuration is used for the DAC due to its simplicity while satisfying the 3b self-testing requirements. The DAC output voltage is buffered and is available at one of the chip output pads. The DAC output also modulates the amplitude of the clocks that drive the sense and reference capacitors ($\phi 1$ and $\overline{\phi 1}$). The amplitude modulation of these clock lines is performed by four transmission-gate switches (S1–S4) which function as a multiplier. An output multiplexer formed by switches (S5–S8) chooses between the amplitude modulated clock lines or the input digital clocks. Hence, when the output multiplexer select line (var) is set, a variable amplitude two phase clock will be provided to the input capacitive sensors. In a self-testing or self-calibration mode of operation, this clock will be applied for a sufficiently long period of time to generate a controllable electrostatic force on the input sensors.

4.4. Temperature sensor

To measure the temperature in close proximity to the other sensors on the microsystem, a temperature sensor is integrated on the interface chip. This provides data that can be used to digitally compensate for the temperature sensitivity of any other sensors connected through this interface chip. The temperature sensor exploits the temperature dependence of the drain current of an MOS transistor in weak inversion [15] as shown in Fig. 7. Here, the charging current of the capacitively-loaded ring oscillator input stage is set by a PMOS transistor biased for subthreshold operation. Feedback from the ring oscillator is used to discharge the input capacitor and maintain the oscillation. Since the charging current is temperature dependent, the frequency of the oscillator provides a measure of the local temperature. Although there are secondary temperature sensitivities within this circuit (e.g., switching point of the Schmitt trigger, bias voltages, etc.), they will not have a substantial effect on the overall response. Furthermore, any secondary sensitivity will be accounted for during calibration of the temperature sensor, which is necessary because this sensor does not provide a direct (linear) temperature output as discussed in Section 5. While many integrated circuit temperature sensors exist [16], this technique was selected because it provides a direct digital output with a low-power circuit that is accurate enough (± 1°C) to compensate the temperature dependence of other transducers in

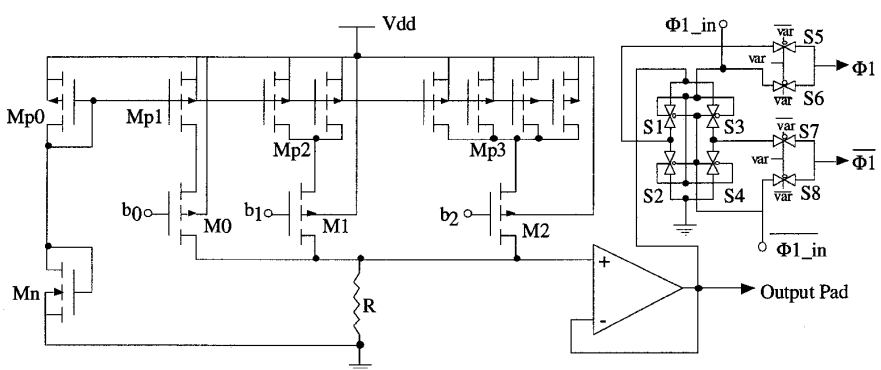

Fig. 6. Schematic diagram of self-test digital-to-analog converter.

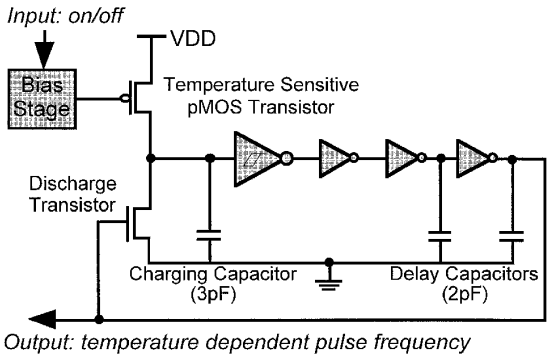

Fig. 7. A temperature-sensitive oscillator used to measure temperature in close proximity to the other sensing elements on the microsystem.

the system. In addition, it can easily be implemented in a standard CMOS process and does not require any bipolar devices.

5. Test results

The chip has been fabricated using a standard 3-μm, single metal, double poly, p-well, CMOS process at the University of Michigan [17]. Fig. 8 shows a photograph of the chip, which measures 3.2×3.2 mm and dissipates less than 2.2 mW from a single 5-V supply. Approximately 85% of the power dissipation is due to the quiescent currents of the five opamps integrated on the chip. Table 2 summarizes the chip specifications. Test results have shown full circuit functionality with an input capacitance resolution better than 1 fF in a 10-Hz bandwidth, and a maximum readout clock rate of 50 kHz. Although carefully sized dummy switches are used in the switched-capacitor circuit, the resolution is still limited by the clock switching noise and the noise-coupling to the sense and reference capacitor charging voltage lines rather than kT/C and input amplifier flicker noise. Fig. 9 shows the output of the

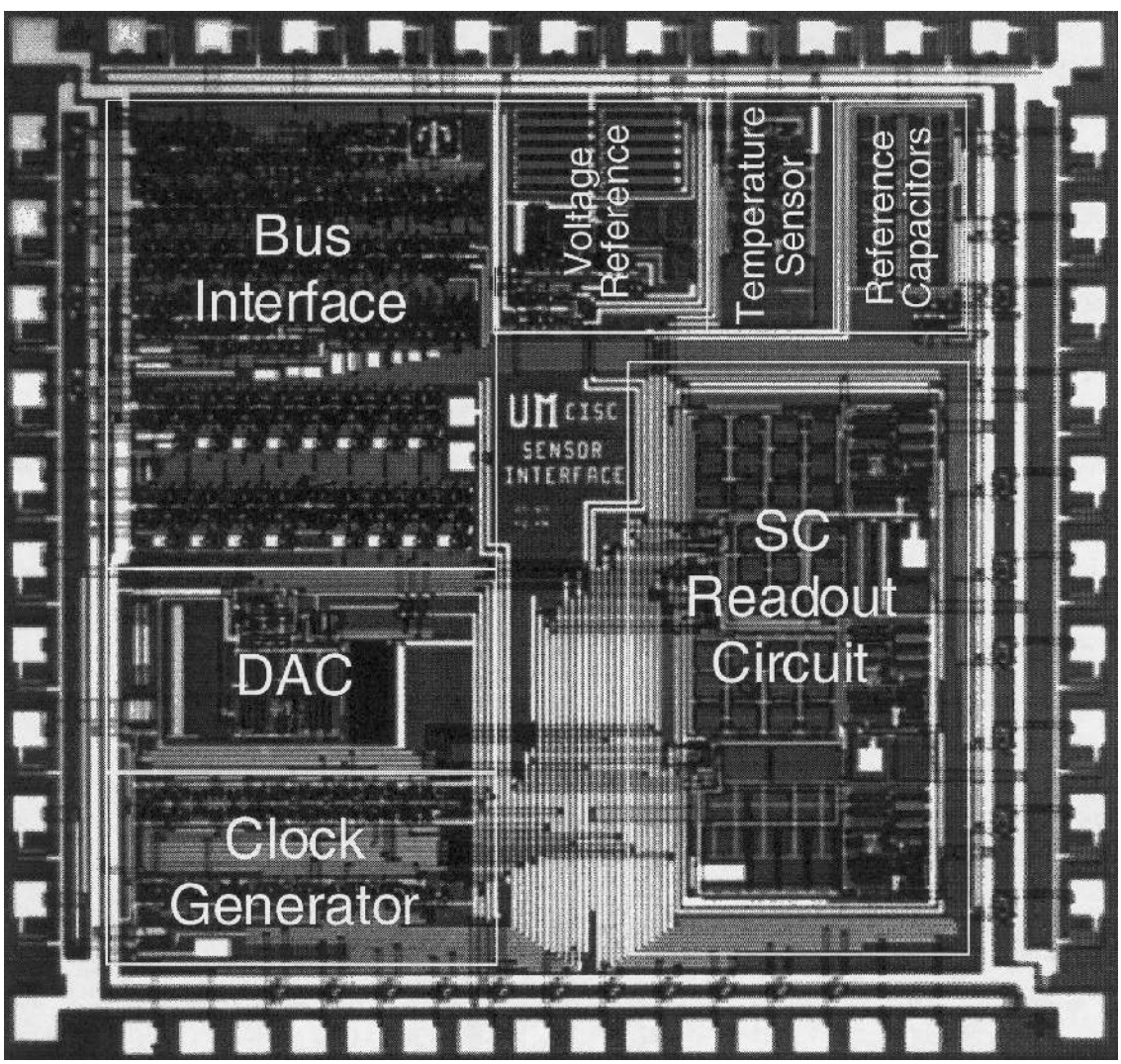

Fig. 8. Die photograph of the generic capacitive sensor interface.

Table 2
Summary of the interface chip specifications

Number of Sensing Channels	Six Capacitive + Temperature
Reference Capacitor Channels	Three Internal/External, Internal Capacitor Programmable 0.15–8 pF
Chip Address	4 bits
Bus Interface Clock	< 10 MHz
Complete Read/Write Instruction Transfer Rate over the Sensor Bus	> 500 kHz
Sensitivity 1 [mV/fF]	0.23–22.3
Sensitivity 2 [mV/fF]	0.23–50.9
Sensitivity 3 [mV/fF]	0.47–73.5
Resolution	< 1 fF Input Capacitance (in 10 Hz BW)
Readout Clock	< 50 kHz
DAC	3 bits for Self-Testing
Supply	Single 5 V
Power Dissipation	< 2.2 mW
Temperature: Dependence of Offset	< 0.16 fF/°C (input referred capacitance variation)
Temperature Sensor Range	−20°C to +60°C
Temperature Sensor Resolution	1°C

charge integrator with a 6-pF reference capacitor as the sensor capacitance is varied from 3 to 8 pF. Fig. 10 illustrates the output of the readout circuit as the input capacitance changes in 0.5-pF steps. The programmability of the gain is illustrated in Fig. 11, where the measured output is plotted for various digital gain selections of 2.66, 6, and 8.66. These gains result in the overall sensitivity of 2, 4.5, and 6.5 V/pF, as shown in Fig. 11. The overall output linearity is better than 4% in the range of 0.6–3.8 V.

The temperature dependence of the readout circuit offset and sensitivity has been measured over the range 0–60°C. The circuit sensitivity is not significantly affected by its operating temperature and in all measurements the temperature dependence of the output voltage has been dominated by that of offset. The main source of offset temperature dependence is due to junction leakage current of the reset switches in parallel with the charge integrating capacitors and the first stage opamp offset. The maximum temperature dependence of offset is equivalent to less than 0.16 fF/°C input-referred capacitance. Note that the temperature dependence of the readout circuit does not adversely affect the performance of the overall microsystem since it can easily be compensated as temperature compen-

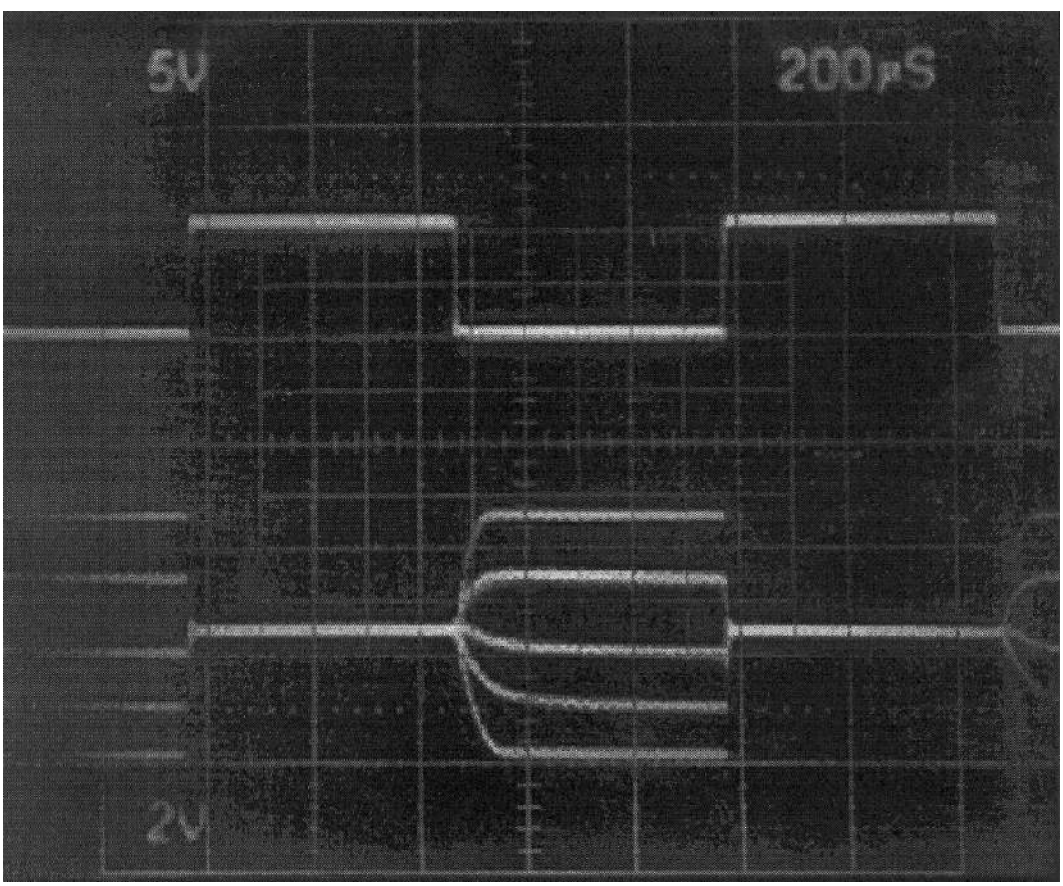

Fig. 9. Upper trace: Reset control of the input charge integrator. Lower trace: Output of the charge integrator with a 6-pF reference capacitor as the sensor capacitance changes from 3 to 8 pF.

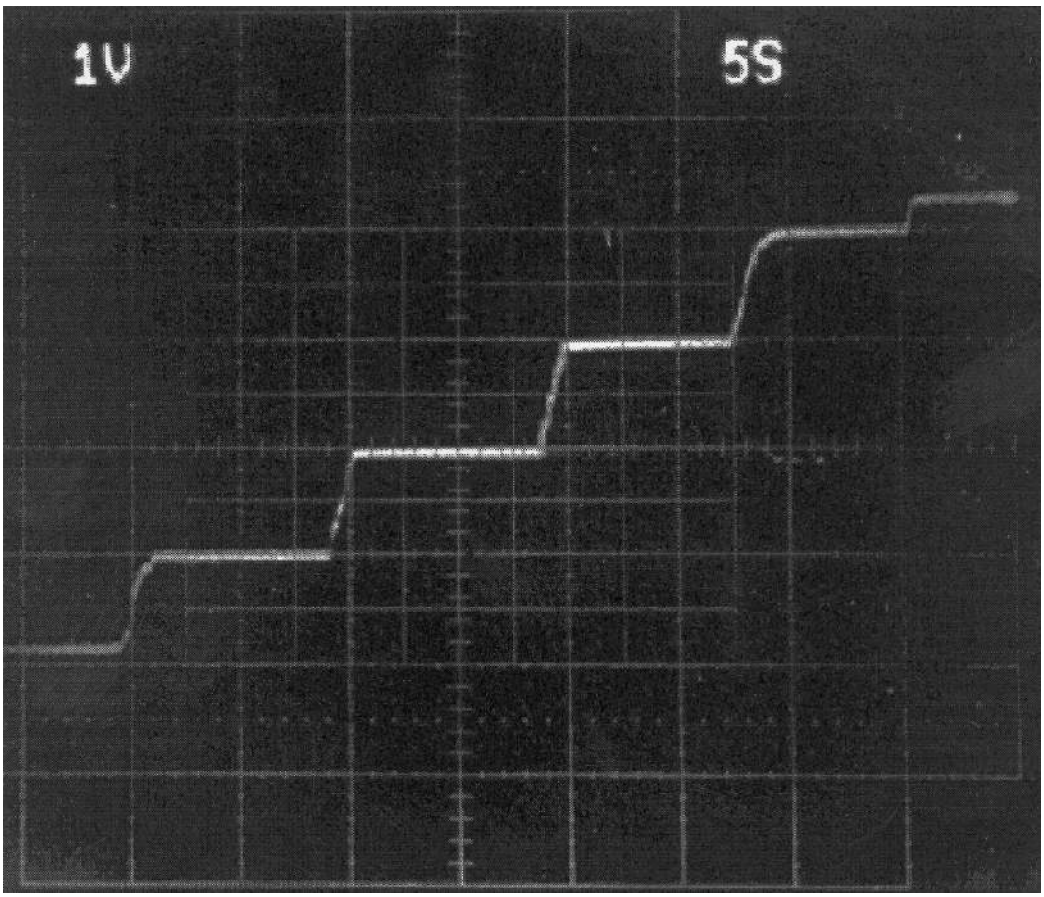

Fig. 10. Readout circuit output as the input capacitance changes in 0.5 pF steps; no laser trimming for gain adjustment is performed and lowest second-stage gain is selected.

sation of the sensor is performed using the on-chip temperature sensor data and the microcontroller of the system.

The temperature sensor was tested over the range of −20°C to 60°C and the output oscillation period was measured. The results for a representative device are plotted in Fig. 12 which illustrates a sensitivity from 4 ms/°C at high temperatures to 33 ms/°C at low temperatures. A device tested for 1 month demonstrated a stable resolution better than 1°C over its entire range of operation. In order to calibrate the temperature sensor, the non-linear response

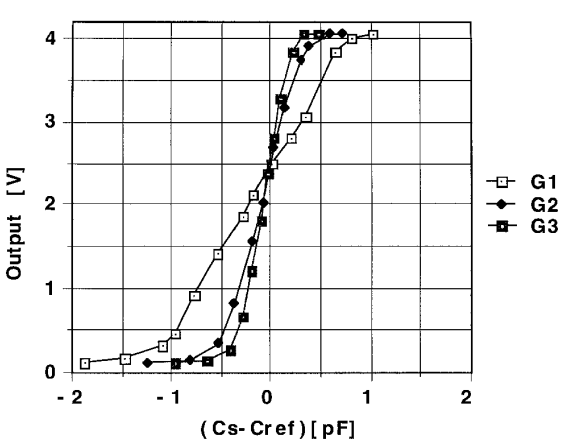

Fig. 11. Measured output of the chip as a function of the input capacitance for different second-stage gain settings. The three programmed gains are: G1 = 2.66, G2 = 6, and G3 = 8.66.

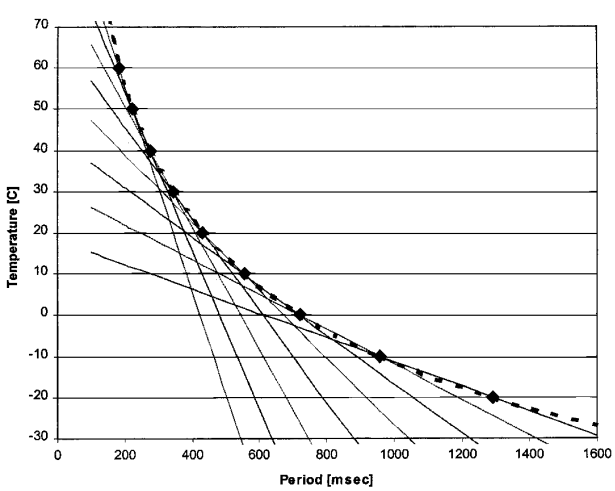

Fig. 12. Measured response of the temperature sensor (diamonds at 10°C intervals), and polynomial best fit to measured data (dashed curve). Also shown are the linear approximations used for calibration of this sensor in steps of 10°C.

is approximated by eight piecewise linear intervals as shown in Fig. 12. Using this method, the temperature is obtained by evaluating a linear equation in-module, the slope and y-intercept of which are determined by the measured sensor output frequency. This provides a temperature measurement accurate to within ± 1°C that is stored in the microsystem controller and used to digitally compensate other sensors for temperature cross sensitivities. In all tested cases, this accuracy was adequate for digital compensation using polynomial evaluation.

The microsystem shown in Fig. 13 is an example of a multi-parameter sensing system in which the generic capacitive sensor interface chip plays a key role [5]. This microsystem utilizes four interface chips to link a commercially available MCU to 22 sensor elements for measuring temperature, pressure, humidity, and acceleration [4,5]. The interface chip can operate with a sensor bus clock speed up to 10 MHz. With a minimum of 12b required for an input read command, the instruction can be issued in less than 2 μs including time for the strobe and chip enable signals. The bus clock speed of the implemented microsystem is 1 MHz bounded by the system microcontroller (MCU) speed. The maximum speed for issuing consecutive read commands in the microsystem is slightly greater than 10 kHz, which is mainly limited by the switched-capacitor readout circuit, the MCU and interface chip communication, and off-chip A/D conversion. If additional commands (such as gain selection or DAC settings) to the interface chip are required, an additional 2–3 μs is necessary, but a-10 kHz readout speed could still be maintained.

6. Conclusions

In this paper, a generic interface circuit for capacitive sensors for smart multielement microsystems has been presented. This chip satisfies all the requirements of such microsystems: It can interface with a large variety of capacitive sensors with base-capacitance and sensitivity spread over a wide range, supports communication with any microcontroller over a standard sensor bus, has programmable gain and offset control, and supports sensor self-test. In addition, the interface circuit integrates a temperature sensor on-chip. It dissipates less than 2.2 mW from a single supply, resolves input capacitance variations better than 1 fF in 10 Hz bandwidth, and has a 1°C temperature resolution. A number of these generic capaci-

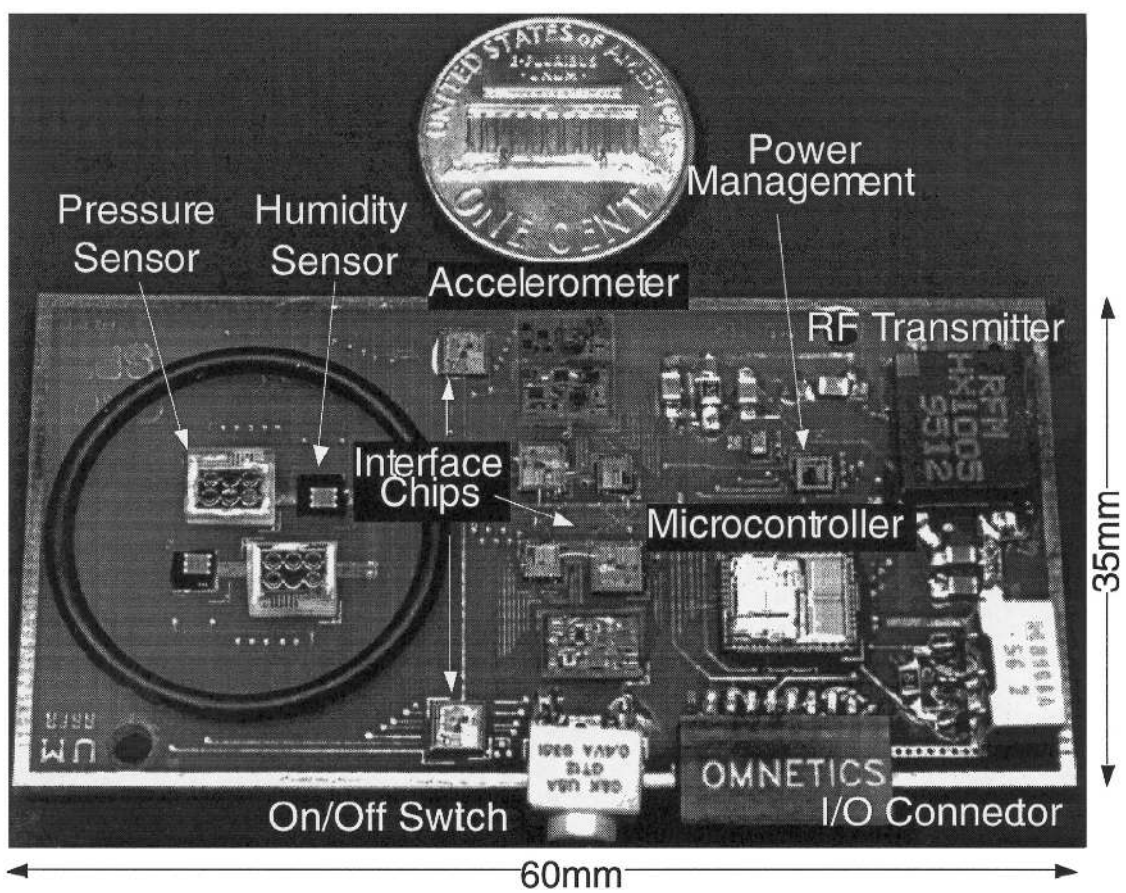

Fig. 13. Photograph of a working microsystem for environmental monitoring that uses several generic capacitive sensor interface chips.

tive interface circuits are currently employed in a low-power wireless multielement microsystem for environmental monitoring. While this wireless battery-powered system provides a prototype for future small portable microsystems, the presented generic interface chip and its combined features will be essential for the successful realization of similar microsystems of the future. The steady push toward low-power high-performance electronics, combined with the increasing attention being given to MEMS-based microsystems, will likely lead to improved versions of the interface chip that still need to combine and implement many of the same functions. Future designs are expected to have expanded range and programmability (to improve gain and offset trim resolution), as well as improved bus interface modules with more on-chip memory and the ability to interface with a larger number of sensors and actuators.

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