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November 1978

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A GERMANIUM FIELD-EFFECT TRANSISTOR MADE FROM A HIGH-PURITY SUBSTRATE*

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Abstract

Field effect transistors have been fabricated on high-purity germanium substrates using low-temperature technology. The aim of this work is to preserve the low density of trapping centers in high-quality starting material by low-temperature (< 350°C) processing. The use of germanium promises to eliminate some of the traps which cause generation-recombination noise in silicon field-effect transistors (FET's) at low temperatures. Typically, the transconductance (g_m) in the germanium FET's is 10 mA/V and the gate leakage can be less than 10^{-12} A. Our present devices exhibit a large 1/f noise component and most of this noise must be eliminated if they are to be competitive with silicon FET's commonly used in high-resolution nuclear spectrometers.

Introduction

When a silicon junction FET used as the input stage of a charge sensitive preamplifier is cooled below ambient temperature, the signal-to-noise ratio generally improves. This improvement can be anticipated due partly to the normal KT term in the Nyquist noise equation and also due to the increase in g_m which results from the temperature dependence of the carrier mobility. However, at temperatures below about 120 K the noise increases through a series of peaks so that a minimum is found in the range of 140 to 180°K. The origin of this excess noise has been shown to be due to: 1) process-induced deep impurity traps and 2) a fundamental fluctuation in the charge state of majority impurity atoms which occurs in the temperature range of carrier

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freeze-out.[1] By using germanium, with its narrow bandgap instead of silicon, it appears that these noise sources should be much smaller or negligible at temperatures down to 77°K.

The problem of majority carrier freeze-out in silicon is fundamental and cannot be affected by design or processing. This means that silicon FET's must always be operated above about 140°K for best noise performance. Because the Group III and V impurities are much shallower in germanium than silicon, germanium FET's should have their minimum noise at about 20°K.

The dominance of silicon as the material for low-noise transistors is due mainly to the characteristics of SiO_2 and the SiO_2-Si interface. Silicon dioxide provides a very convenient method of masking for diffusion operations. Furthermore, the SiO_2-Si interface can be made to contain a very low density of fixed or mobile charges and at the same time it can mask surface junctions while processing is performed to getter deep traps. These benefits are somewhat offset by the higher processing temperatures required for silicon and these gettering steps are more necessary. In the case of germanium, even the best passivating films[2,3] contain too many charges to be useful for low-noise transistors. Our work with high-purity germanium for nuclear radiation detectors has shown that deep traps are irreversibly introduced if the crystal is heated much about 350°C.[4] Since the best passivating films for germanium required at least 600°C for their stabilization,[2,3] a truly low-noise germanium transistor demands low-temperature processing and bare junctions.

Design of Germanium FET

The constraint of low-temperature processing severely limits the design possibilities for a germanium FET. In particular, multiple masking for geometry control is not possible. This means that the source, drain and gate geometries must be defined with a single photolithographic mask. One possible design which meets these criteria is the vertical, self-aligned gate configuration shown in Fig. 1. In this design, the source metallization acts as an etching mask for the gate metallization and the back of the wafer serves as the drain contact. The over-hanging source metal remaining after etching the gate valley acts as a shadow for the gate metallization which then behaves as a self-aligned gate.

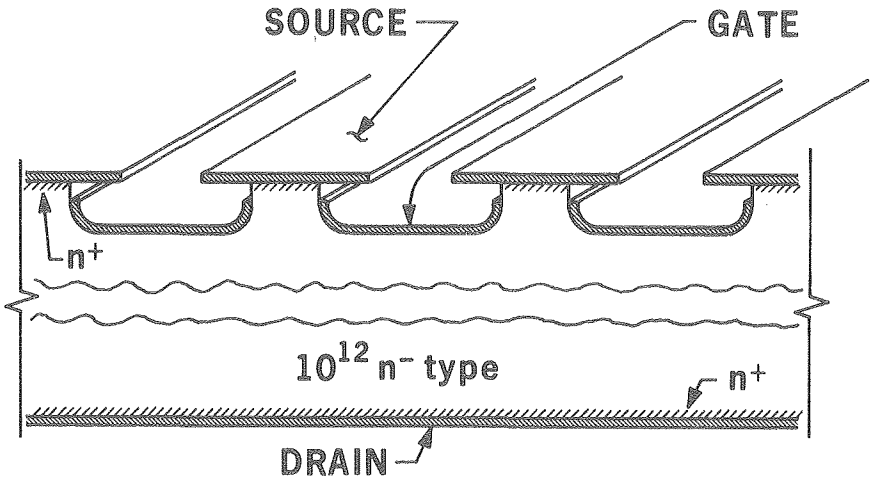

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Fig. 1. Vertical FET showing method of forming self-aligned gate.

The operation of this device may be roughly analyzed with reference to the idealized structure shown in Fig. 2. Selecting an n-type substrate with a donor concentration of $10^{12}/cm^3$ and a wafer thickness of 100 μ, the device will be totally depleted to the drain contact at a gate bias of -4 V with respect to the drain. This means that the injected source current will be contained to a narrow channel between the gate fingers, and the device acts as an analog transistor; i.e., instead of acting as a voltage controlled resistor (the model usually assumed for a lateral FET at low voltages), the vertical FET (VFET) acts as an injection control device.

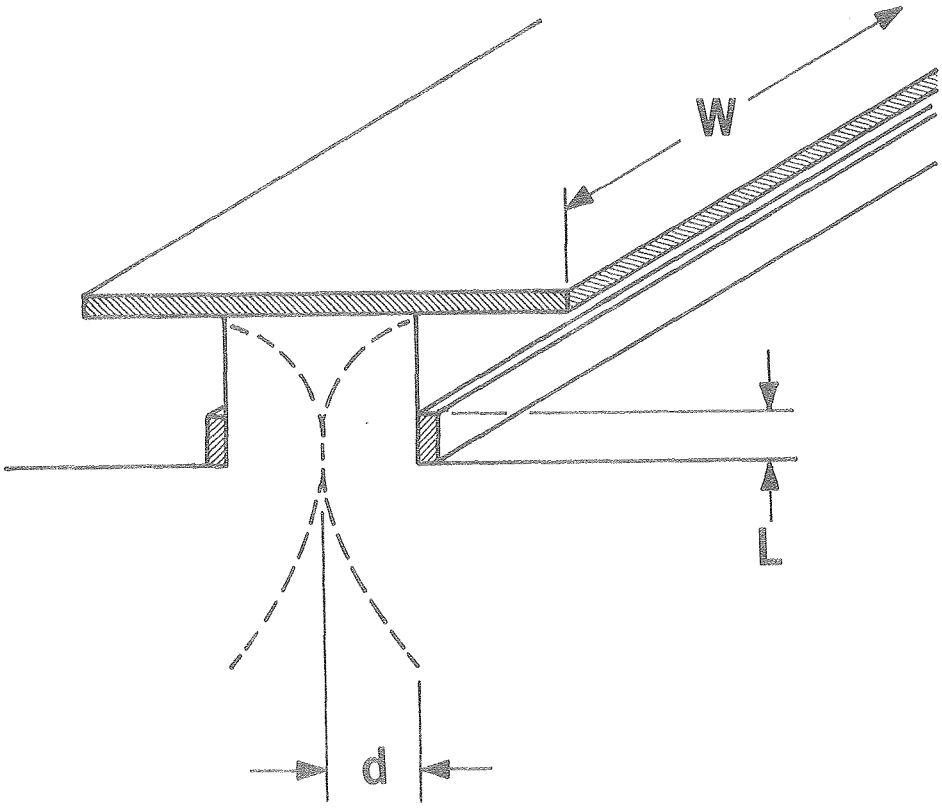

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Fig. 2. 'Idealized' VFET structure.

Many analyses of the operation of a VFET have appeared in the literature,[5-8] however, a simplification can be made by restricting the analysis to the case where electrons injected into the channel between the gates has the saturation velocity, v_s while traveling through the control region. In this case, the charge, Q, in transit through the control region is

$$Q = i\,L/v_s \tag{1}$$

where i is the current and L is the length of the control region, then

$$\partial Q/\partial i = L/v_s \tag{2}$$

If the capacity between the gate electrode and the current sheath in the control region is C then we also have:

$$\partial Q = \partial V.C \tag{3}$$

where ∂V is the incremental change in gate voltage and ∂Q is the resulting change in the charge in transit. Now the transconductance

$$g_m = \partial i/\partial V = C\,v_s/L \tag{4}$$

but

$$C = \varepsilon\varepsilon_o\,LW/d \tag{5}$$

where $\varepsilon\varepsilon_o$ is the dielectric constant of the material, W the long gate dimension (i.e. the integrated length of the fingers) and, d, the distance of the gate electrode to the electron sheath. Therefore,

$$g_m = \varepsilon\varepsilon_o\,W/d\,v_s \tag{6}$$

In the voltage saturation region, which is the usual operating point for VFET's, the g_m therefore depends only on the dielectric constant and the gate spacing and width. The saturation velocity v_s is roughly the same for the common covalent semiconductors and is about 10^7 cm/s. For W = 1 cm and d = 10 μm, this simple calculation yields g_m = 20 mA/V. For a control region length, L, of 2 μ, control capacity (i.e. gate to electron sheath) C_{SG}, is 0.2 pF. Extraneous gate capacity increases this value but, even for this very undemanding geometry, the figure of merit g_m/C is much better than the best lateral FET's.

The above analysis fairly accurately estimates the g_m of a VFET but is not at all applicable to a conventional or lateral FET. In any FET the intrinsic or geometrical transconductance, g_m', is reduced by the source or channel resistance, R_S, so that $g_m = g_m'/(1 + R_S.g_m')$.[8] In the conventional FET $R_S\ g_m'$ is $>> 1$ so that $g_m' \simeq 1/R_S$ and the current saturates. This negative feedback through the source resistance is the origin of the pentode-like characteristics of the normal FET. For the VFET, however, $R_S\ g_m' < 1$ so that no current saturation occurs and the device shows triode-like characteristics. From this point of view the conventional FET acts as a voltage controlled resistor and the VFET as a current injection control device.

For constant geometry and electrode potentials, the magnitude of the injected current in the VFET is determined mainly by the substrate impurity concentration. The g_m, however, is controlled principally by the gate geometry, in accordance with Eq. 7.

Device Fabrication

In attempting to realize the structure of Fig. 1 it must be decided whether to use p-channel or n-channel. They should exhibit equivalent performance since electrons and holes have the same mobility at 77 K. For ease of fabrication it would be convenient to use a Schottky barrier for the gate so that an n-channel is preferred (metals all behave as p-type contacts against germanium). Source and drain contacts can be made by phosphorous ion implantation using the techniques of Ref. 9.

A variety of metallization systems were tried for the source fingers and only pure gold was found to be reasonably satisfactory. The problem with using metal etch masks on n^+ germanium is that a galvanic couple is formed which rapidly undercuts the metal in any electrolyte. For example, 50 μ wide gate fingers are removed in 2 min. in 0.1 N NaOH. Based on the etching analysis of Schartz and Robbins [10], it was possible to devise satisfactory masking using an etch of 20:1 (HNO_3:HF). A further problem with germanium-metal systems is that germanium has a high solubility in most of the metals which are resistant to germanium etches. For example, the gold masked devices must be limited to short times above 200°C if the implanted layer is to be preserved. Chromium is an exception to this rule, however, the germanium-chromium couple passivates chromium etches.

In selecting the physical dimensions of the device we are limited by the availability of headers (TO-18) to a maximum of a 1.3 mm square chip. Given this constraint, a chip of 1.2 mm square is used with source fingers 50 μ wide with 25 μ spacing. After etching and metallizing the base fingers, an adjustable base spacing d of 10 to 30 μ results with a total width W of 1 cm and a length, L, of 2-6 μ.

The chip is bonded to the header with silver-epoxy and the source is contacted by the use of an overlay chip. The overlay chip is made from heavily doped germanium which is indium coated on one side and subsequently bonded to the source fingers at 200°C in an enert atmosphere. An SEM photo of a mounted device is shown in Fig. 3. More detailed processing steps are given in the Appendix.

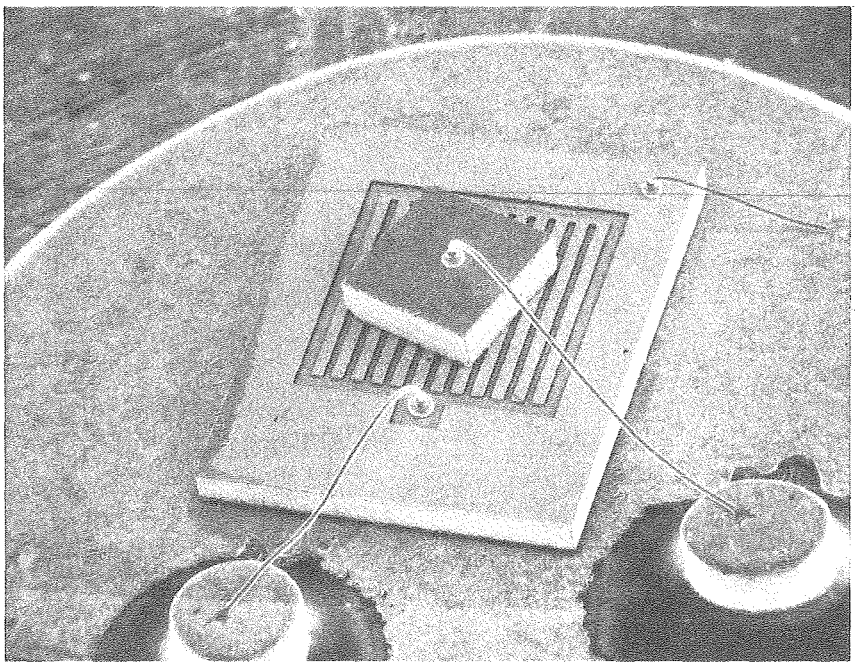

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Fig. 3. VFET mounted on TO-18 header showing over-lay chip for source contact.

Results

Typical dc transfer characteristics at 77 K are shown in Fig. 4 and the expected triode-like characteristics are found. The gate spacing d is measured to be 20 $\pm$ 5 μ which, from Eq. 7, gives a g_m of 10 mA/V in agreement with Fig. 4. The fabricated devices initially exhibit excessive gate leakage (μA) but a short wash in methanol results in the gate leakage shown in Fig. 5. The gate leakage is quite stable and no changes are observed after several months of ambient storage.

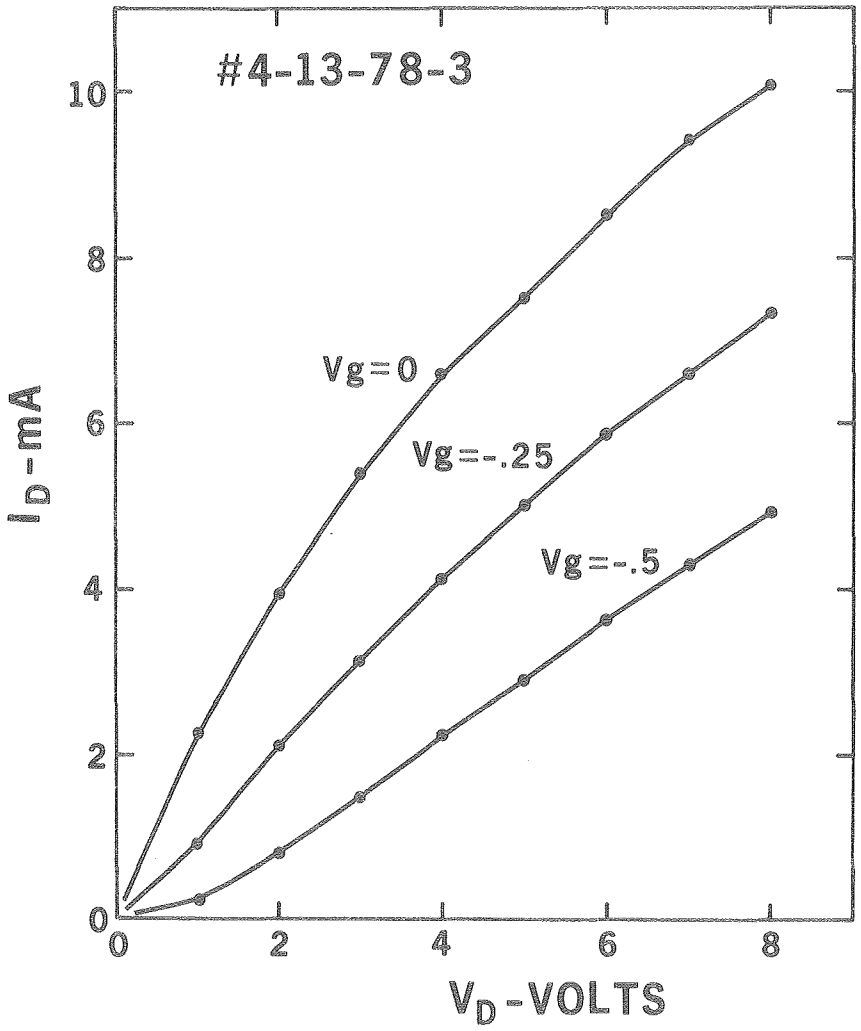

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Fig. 4. Transfer characteristic of typical Ge VFET.

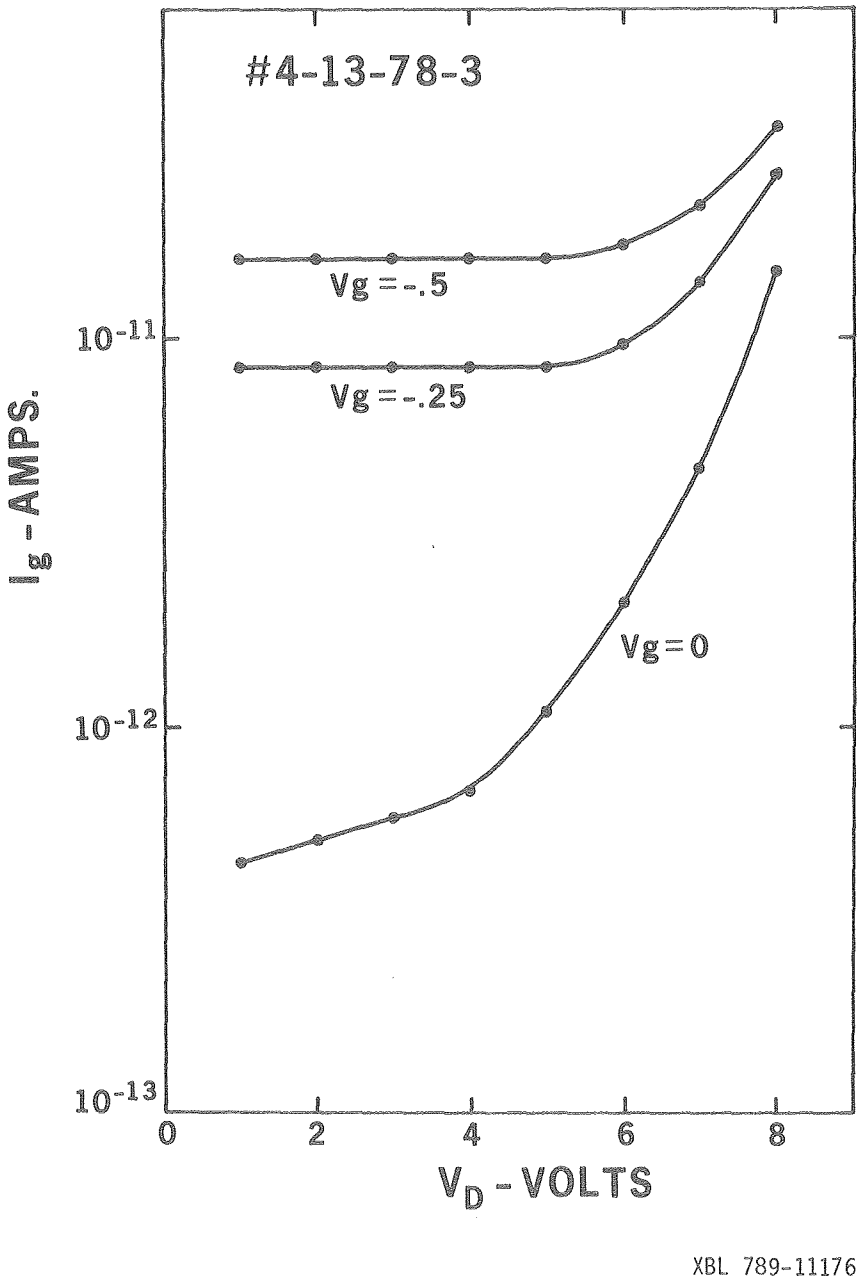

Fig. 5. Gate current of typical VFET with Schottky barrier gate. Ion implanted gates have about two orders of magnitude less current.

While the dc characteristics are close to those predicted, the transistor, when used as the input stage of an amplifier, shows excessive noise with a large 1/f component. The spot noise figure in the grounded gate configuration was measured with a Hewlett-Packard* Model 4470B Transistor Noise Analyzer and is shown in Fig. 6 together with a comparison selected 2N4416 at 20°C. In an attempt to see the effect of a strong accumulation or depletion layer on the source-gate interelectrode surface, a device which had been stored at ambient for two months was exposed alternately to ammonia and iodine--treatments which are known to give strong n-type and p-type surfaces respectively. No change was seen in either the gate leakage or the noise figure.

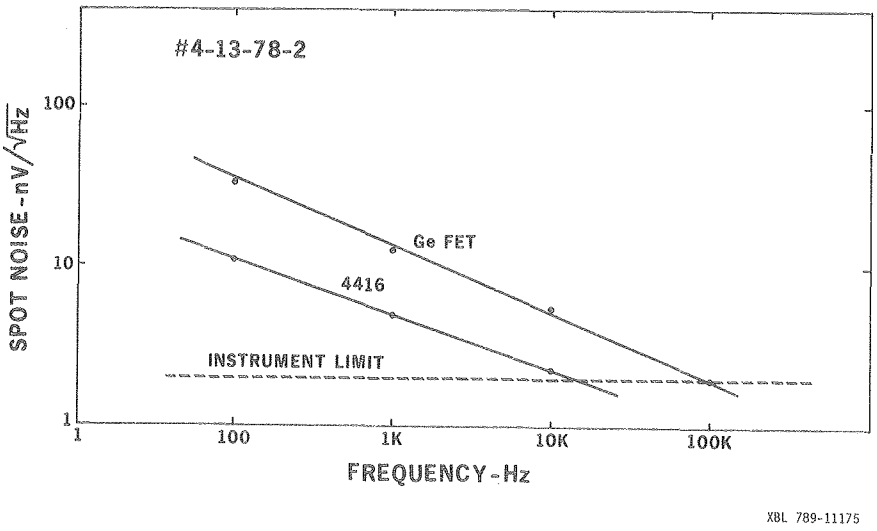

Fig. 6. Grounded gate spot noise of Ge FET at 77 K compared with 2N4416 at 20°C.

*Reference to a company or product name does not imply approval or recommendation of the product by the University of California or the U.S. Department of Energy to the exclusion of others that may be suitable.

Using a calibrated capacitor, the germanium equivalent noise line width (NLW) was measured using the germanium FET as the input stage of a normal charge-sensitive preamplifier. The result (see Fig. 7) shows noise in excess to that of a good silicon FET.

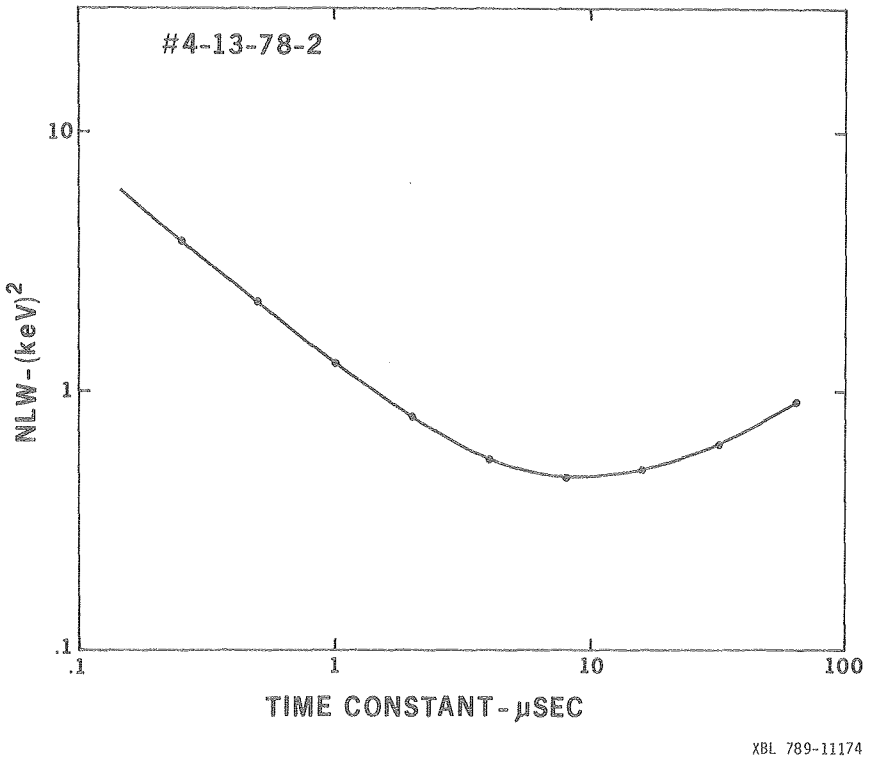

Fig. 7. Noise line width of Ge VFET used as the input stage of a charge-sensitive preamplifier. The minimum noise is about 700 eV at 10 μs time constant.

Discussion

The g_m of a germanium VFET is adequately described by a single geometrical relation (Eq. 7). The reason for this simplicity for a VFET as against a lateral FET is due to the low value of the source resistance, R_S, such that no current saturation occurs. This low value of R_S results in a low voltage gain, μ, (or what is the same thing, a low output impedance, R_p) such that some provision must be made for this low gain in the preamplifier design so as not to see the noise of the second stage. However, the low value of R_p (about 1 KΩ in the devices shown here) is not related to the poor noise performance seen in Figs. 6 and 7. It will be noticed that the frequency dependence of the noise voltage is different in the case of grounded grid operation (Fig. 6) and open grid operation (Fig. 7). This suggests that an additional noise source is present with a high impedance gate (Fig. 7) than in the case of channel current noise (Fig. 6).

Many noise sources are possible in this device but no significant source has as yet been isolated. Noise sources which are unlikely to be dominant are: 1) generation-recombination through deep traps in the substrate, 2) minority carrier injection from source and drain, 3) voltages induced in the gate by leakage currents on the bare surfaces and 4) gate voltages induced by surface states in the Schottky gate contact.

Noise source 1) may be dismissed, as the low-temperature processing should produce very few deep traps. Noise source 2) would result in large gate currents which are not observed. Noise source 3) would be largely suppressed by grounded gate measurements and no suppression is observed (Fig. 6). FET's have been made with boron implanted gates, and while the gate currents are lower (10^{-14}A.range), no noise improvement is found. However, measurements on devices with ion-implanted gates do give a clue to a possible noise source.

When devices are made with ion-implanted gates it is possible to measure the source-gate diode forward characteristic which is not possible with Schottky barrier gate devices. At 300 K the source-gate diode has the ideal forward voltage drop of 60 mV per decade of current but at 77 K has 30 mV per decade instead of the ideal 15 mV. This result suggests that the low temperature annealed, ion-implanted n^+-n contact is not ideal at 77 K. One could postulate that the ion-implanted contact has a p-type damage layer deeper than

the ions which becomes extrinsic at low temperatures and results in a forward double-diode voltage. Attempts will be made to fabricate devices with low-temperature solid-phase epitaxy to test this idea.

Acknowledgments

We would like to thank R. Cordi, R. Davis, and J. Mraz for their assistance in the project.

Appendix

The processing steps are shown schematically in Fig. 8.

a) The use of high-purity germanium doped with arsenic to $10^{12}/cm^3$. Lap and optically polish to 100 μ using colloidal silica with hydrogen peroxied.

b) Implant $10^{15}/cm^2$ phosphorus at 77 K and 25 KV. Anneal 48 hours at 150°C and ramp up to 350°C.

c) Sputter off in Ar for 30 sec then sputter 3 μ Au on both sides.

d) Define source fingers with KTFR photoresist and etch in KI + I_2. Remove photoresist in activated H_2SO_4.

e) Etch 90 sec in 20:1 HNO_3:HF; quench in CH_3OH.

f) Angle evaporate 3000Å Au for gate. Follow by 15 sec etch as in (e).

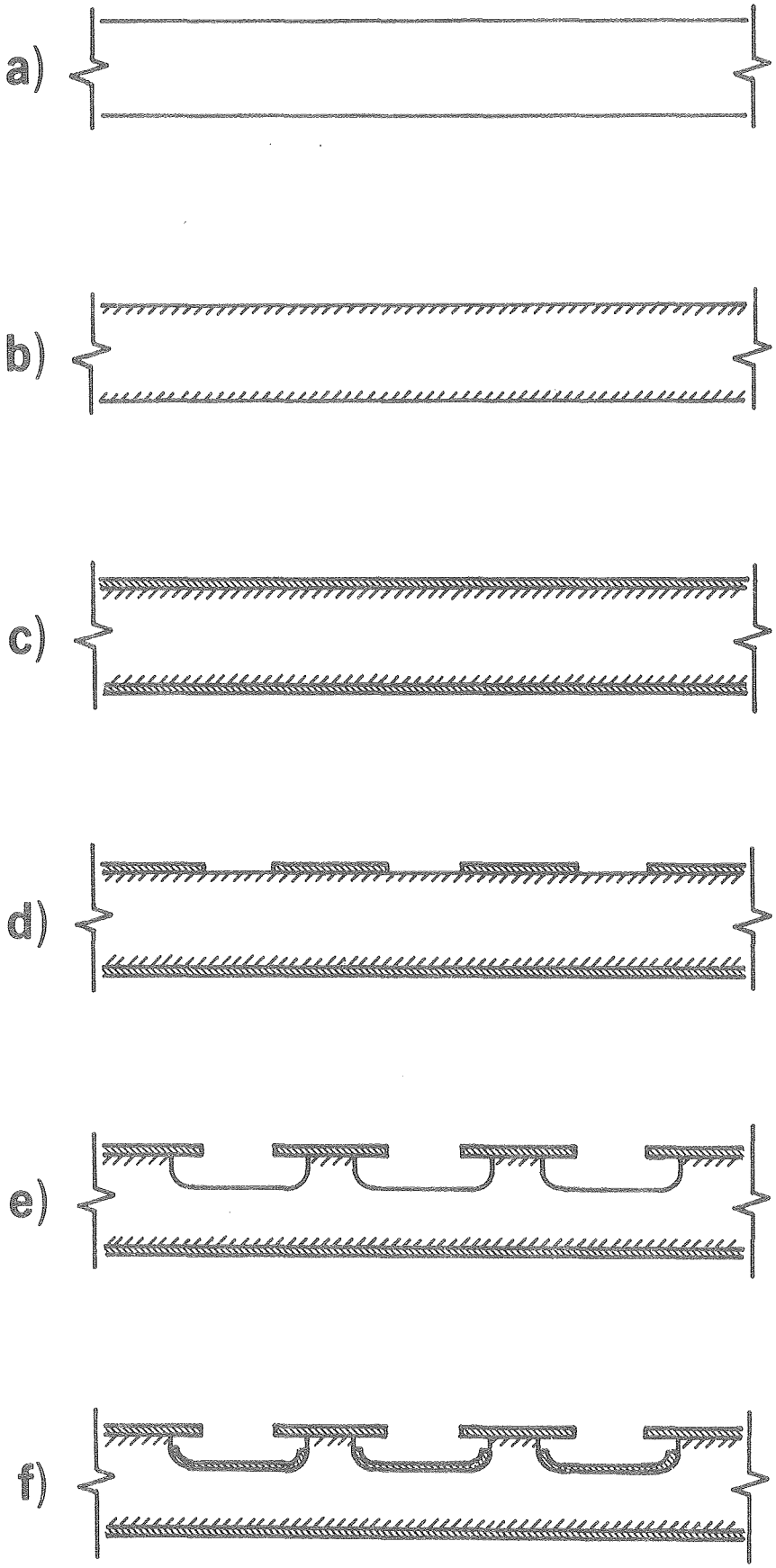

Fig. 8
Schematic of processing steps

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