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I am submitting herewith a dissertation written by Benjamin Matthew McCue entitled "A GHz-range, High-resolution Multi-modulus Prescaler for Extreme Environment Applications." I have examined the final electronic copy of this dissertation for form and content and recommend that it be accepted in partial fulfillment of the requirements for the degree of Doctor of Philosophy, with a major in Electrical Engineering.

Benjamin J. Blalock, Major Professor

We have read this dissertation and recommend its acceptance:

Charles Britton, Jeremy Holleman, Jayson Hayward

Accepted for the Council:

Carolyn R. Hodges

Vice Provost and Dean of the Graduate School

(Original signatures are on file with official student records.)

A GHz-range, High-resolution Multi-modulus Prescaler for Extreme Environment Applications

A Dissertation Presented for the

Doctor of Philosophy

Degree

The University of Tennessee, Knoxville

Benjamin Matthew McCue

August 2015

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In loving memory of

Larry T. Petrowski & David D. McCue

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ABSTRACT

The generation of a precise, low-noise, reliable clock source is critical to developing mixed-signal and digital electronic systems. The applications of such a clock source are greatly expanded if the clock source can be configured to output different clock frequencies. The phase-locked loop (PLL) is a well-documented architecture for realizing this configurable clock source. Principle to the configurability of a PLL is a multi-modulus divider. The resolution of this divider (or prescaler) dictates the resolution of the configurable PLL output frequency. In integrated PLL designs, such a multi-modulus prescaler is usually sourced from a GHz-range voltage-controlled oscillator. Therefore, a fully-integrated PLL ASIC requires the development of a high-speed, high-resolution multi-modulus prescaler.

The design challenges associated with developing such a prescaler are compounded when the application requires the device to operate in an extreme environment. In these extreme environments (often extra-terrestrial), wide temperature ranges and radiation effects can adversely affect the operation of electronic systems. Even more problematic is that extreme temperatures and ionizing radiation can cause permanent damage to electronic devices. Typical commercial-off-the-shelf (COTS) components are not able withstand such an environment, and any electronics operating in these extreme conditions must be designed to accommodate such operation.

This dissertation describes the development of a high-speed, high-resolution, multi-modulus prescaler capable of operating in an extreme environment. This prescaler has been developed using current-mode logic (CML) on a 180-nm silicon-germanium (SiGe) BiCMOS process. The prescaler is capable of operating up to at least 5.4 GHz over a division range of 16-48 with a total of 27 configurable moduli. The prescaler is designed to provide excellent ionizing radiation hardness, single-event latch-up (SEL) immunity, and single-event upset (SEU) resistance over a temperature range of −180°C to 125°C.

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CHAPTER 1: INTRODUCTION AND GENERAL INFORMATION

1.1 Motivation

A principle requirement of many electronic systems, such as data acquisition systems, data converters, and many other systems, is the generation of a reliable clock signal. Many methods for generating such a signal have been developed over the years, with each method tailored to the specific application. Many electronic systems (particularly mixed-signal) require a very precise, low-noise clock signal. Piezo-electric crystals (quartz) can be manufactured to act as resonant LC tank circuits with a very high quality factor (Q) [1]. The high-Q parameter of quartz allows these crystals to be used to generate very low phase noise clock sources. In the time domain, phase noise manifests as jitter, or timing uncertainty associated with edge transitions of a periodic signal. One drawback to using crystal oscillator circuits as clock sources is that the oscillation frequency of these circuits cannot be changed without a physical change to the crystal. Moreover, the intrinsic quality factor of a crystal is inversely proportional to crystal resonant frequency and internal losses of the crystal limit the resonant frequency of quartz crystals to the low MHz range [1]. Therefore, there is a frequency "window" for crystal resonators before internal losses degrade performance where the maximum quality factor can be obtained. This limitation on the frequency range of crystal resonators highlights the need for a configurable system that allows user-selectable clock frequencies to be generated from a single (or set of) crystal(s). A phase-locked loop (PLL) is a well-established electronic system for accomplishing this variable frequency selection functionality [2], [3]. Figure 1 shows the basic concept of a phase-locked loop.

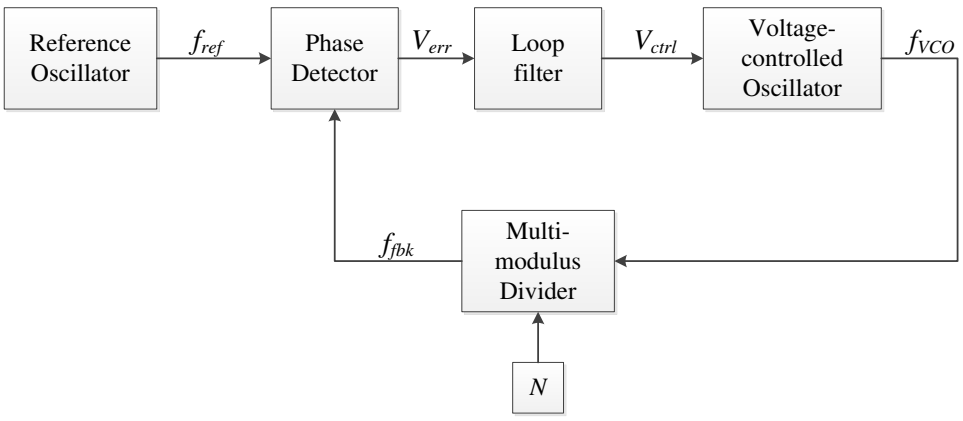

Figure 1. Basic functionality of a phase-locked loop

In a PLL circuit, a reference oscillator (usually a crystal oscillator) provides a reference frequency (f_{ref}) for the PLL system. Another oscillator in the PLL system, a voltage-controlled oscillator (VCO), generates a second oscillation frequency (f_{VCO}), significantly higher than the reference frequency. The phase detector, together with the feedback action of the control loop, forces the feedback frequency (f_{fbk}) at the output of the multi-modulus divider to match the reference frequency. Therefore, the VCO is forced to oscillate at a frequency equal to the reference frequency multiplied by the division ratio (N) of the multi-modulus divider (provided this frequency is within the VCO tuning range). This PLL system allows the precision of the crystal resonant frequency to be extended to generate precise oscillation at frequencies other than the resonant frequency of the crystal. It is evident from the previous PLL functional description that a principle section of PLL architecture (and the section that dictates the PLL output frequency relative to the crystal frequency) is the multi-modulus divider. The set of configurable output frequencies for a given crystal frequency is determined by the available moduli of this divider. This multi-modulus divider (or prescaler) is often required to operate at very high speeds, as the nominal oscillation frequency of the VCO is usually designed to be relatively high (a desirable trait for a wide tuning range, tuning linearity, and small on-chip, passive components) [3]. It is now evident that user-configurable, precision clock generation requires an integrated, high-speed, multi-modulus divider solution.

Extreme environment applications, such as space exploration, satellite systems, and defense systems, have led to the need for the development of highly-reliable, extreme environment capable electronic systems [4], [5]. Electronics operated in space are inevitably exposed to extreme cold temperatures (often −180°C or lower) and high temperatures (often 125°C or higher) [5]. Extreme cold temperatures present several problems for electronic circuit operation, particularly precision frequency generation circuits. Reliability of semiconductor devices in extreme cold temperature is also of noted concern due to the increased generation of hot carriers that occurs at low temperatures. Specifically, the degradation of silicon MOSFET devices via hot carrier effects is a well-established phenomenon. Hot carrier injection into the oxide layer of a MOSFET can accumulate and induce transconductance degradation and permanent threshold voltage shifts [6]. Analog electronics rely on precise matching of device parameters for proper performance; threshold voltage shifts can result in drastic mismatch of these critical device parameters. Moreover, hot carrier injection and carrier trapping result can

cause damage to the oxide layer that manifests as subthreshold leakage current [6]. These effects present significant concerns regarding the long-term performance and reliability for MOSFET-based electronics operated in this cold-temperature environment (particularly analog electronics).

In addition to these extreme temperatures, extra-terrestrial environments harbor much higher levels of radiation than observed on Earth, both in terms of single-event effects (SEE) and total-ionizing dose (TID) irradiation [4]. The effects of this radiation are often catastrophic for electronics not specifically designed to tolerate such radiation. TID radiation incident upon a silicon cross-section has been demonstrated to induce electron-hole pairs in the insulating oxide layer [7], [8]. In the presence of an electric field, low-mobility holes slowly drift through the oxide layer while high-mobility electrons are quickly removed by the electric field. The result is a trapped charge of holes at the oxide-Si interface. This trapped charge causes variability in I-V characteristic of the device, particularly subthreshold leakage current and threshold voltage shifts [7] – [10]. Single-event transients (SETs) are voltage transients at a circuit node induced by an ion strike transecting a *pn*-junction resulting in charge deposition. SETs can be mitigated with a variety of design and layout techniques, but SETs can never be completely eliminated. Single-event upsets (SEUs) induced by SETs are most concerning in digital systems such as dividers/prescalers. An SEU is defined as an SET-induced alteration of a logic level at a particular digital circuit node. SEUs are often responsible for bit errors in digital systems and frequently result in erroneous operation.

The design challenges associated with these extreme environments may render the use of commercial-off-the-shelf (COTS) components impossible for extra-terrestrial electronic systems, and therefore, an application-specific integrated circuit (ASIC) must be developed for this specific purpose. The development and manufacturing of an ASIC is a costly, time-consuming process that is greatly exacerbated if the ASIC is required to be capable of extreme environment operation. Therefore, whenever possible, it is highly desirable to develop scalable, adaptable ASICs for extreme environment applications. The development of a fixed frequency, non-configurable frequency synthesizer for a specific extreme environment application would offer a very low return on investment. A more attractive solution would be to develop a user-configurable frequency synthesizer ASIC that can provide a wide range of precise clock frequencies for a myriad of extreme environment applications.

Table 1. Attributes required of extreme environment, precision frequency synthesizer

Criteria	Description
Radiation hard	TID radiation tolerance in excess of 1 Mrad/Si, SEL immune, SEU resistant
Temperature range	Robust and fully operational from −180°C to 125°C
Frequency stable	High frequency stability, low noise attained from high-Q, extreme environment crystal resonator (developed by FMI)
Configurable	Able to generate wide range of clock frequencies from a single crystal frequency, selectable clock logic types (CMOS & LVDS)
Compact/self-contained	Complete system-in-a-package solution, single power supply, contains all required components, small size (under 0.7 cc)
Reliable	Able to withstand thermal cycles, robust, reliable start-up over temperature
System compatible	Compatible with existing (and upcoming) supply voltage standards, compatible with existing logic standards (CMOS & LVDS)
Low cost	Lower cost than hybrid solutions using individual elements for clock source generation

A system that allows a high-Q, precision crystal to be packaged with a programmable, extreme environment capable frequency synthesizer ASIC would provide a complete, compact solution to clock generation needs for a wide range of space flight and other extreme environment applications. Presently, no such system exists. Table 1 outlines the frequency synthesizer design criteria required to meet the demands of extreme environment frequency generation.

1.2 Research goals

The development of the described frequency synthesizer system was a significant undertaking that required parallel design paths. Frequency Management International (FMI) has developed the extreme environment capable, high-Q crystal resonators for use in the frequency generation system. The Integrated Circuits and Systems Laboratory (ICASL) group at the University of Tennessee was responsible for designing the extreme environment capable, configurable frequency synthesizer ASIC. Central to the design of this frequency synthesizer ASIC was the development of a high-frequency, multi-modulus divider (prescaler). This prescaler is the building block of the frequency synthesizer ASIC that allows a wide range of

user-selected output frequencies to be generated from a set of crystal frequency. This fact illustrates the importance of the prescaler design in a highly-configurable frequency generation system with a wide range of potential applications.

The focus of this dissertation is the design, implementation, and testing of such a prescaler capable supporting the described frequency synthesizer system. Moreover, this work was tasked with determining the performance requirements of such a prescaler that allowed the described frequency synthesizer system to be realized. The prescaler design is embedded as part of the frequency synthesizer ASIC as well as implemented as a discrete component on a test ASIC to allow for expanded testing of the multi-modulus prescaler and potential implementation in future, stand-alone applications. The multi-modulus prescaler design has been fully tested and characterized both as a stand-alone design and embedded as part of the frequency synthesizer ASIC.

1.3 Dissertation overview

Chapter 2 of this dissertation details the problem description and outlines the specific requirements of the frequency synthesizer ASIC. Furthermore, Chapter 2 details the design requirements and outlines design challenges associated with the development of a highly-configurable prescaler for precision clock frequency generation in extreme environment applications.

Chapter 3 examines IC fabrication technology as it pertains to extreme environments and high-speed operation. A comparison between standard silicon-CMOS and silicon-germanium (SiGe) technologies is made as it pertains to the development of the described frequency synthesizer ASIC of this research work. The high-speed limitations of CMOS logic are explored, and the speed advantage of current-mode logic is examined. Fractional-N division and dual-modulus prescaler design (an important concept in highly-configurable dividers) is reviewed. Chapter 3 also explores prior art demonstrating frequency generation systems and prescaler designs (and frequency dividers in general) with specific attention paid to reports highlighting extreme environment capability or high configurability.

Chapter 4 describes the design approach of the multi-modulus prescaler of this dissertation. A functional description of the multi-modulus prescaler design is presented, and the block-level diagrams of the components of the multi-modulus prescaler are analyzed. The error correction scheme used for the dividers of the multi-modulus prescaler is described. Chapter 4

also presents schematic-level design details for the critical blocks of multi-modulus prescaler, and demonstrates the functionality of the dividers of the multi-modulus prescaler with block-level timing simulations. Lastly, Chapter 4 illustrates the physical implementation of multi-modulus prescaler as well as the physical implementation of the frequency synthesizer ASIC.

Chapter 5 describes the functionality of the prescaler test ASIC and the printed-circuit board (PCB) used to facilitate testing of the multi-modulus prescaler. The initial functionality testing of the developed multi-modulus prescaler is shown. Prescaler measurement results are presented demonstrating input frequency locking range and supply current draw over temperature and supply voltage. Phase noise and jitter measurements are shown and analyzed for both the stand-alone VCO/prescaler test structure and the entire frequency synthesizer ASIC system. Finally, the method used for testing the prescaler error correction scheme is outlined, and measurement results demonstrating error correction of the multi-modulus are presented and analyzed.

Chapter 6 summarizes the research work performed for this dissertation. The original contributions of this research as well as possible directions for future work are also discussed in Chapter 6.

CHAPTER 2: PROBLEM DESCRIPTION

2.1 Extreme environment frequency synthesizer overview

As mentioned in Chapter 1, the goal of this research was to design and develop a fully-integrated, extreme environment capable, multi-modulus prescaler for use in a PLL-based frequency synthesizer ASIC. To better understand the requirements of this prescaler, the operation and design requirements of the frequency synthesizer ASIC must first be examined. The frequency synthesizer system was developed with the following set of targeted, technical objectives defined in Table 2. The technical objectives defined in Table 2 were established based on experience from previous and on-going projects with space-flight application users, discussions with energy exploration users, and established requirements for military-grade electronic systems.

Table 2. Frequency synthesizer ASIC technical objectives

Performance parameter	Design goal	
Crystal frequency range	15 to 25	MHz
Output frequency range	0.08 to 250	MHz
Output frequency resolution	10	kHz
Operating temperature range	−180 to 125	°C
Supply voltage range	3.0 to 3.6	V
Output logic type	CMOS (3.3 V)	
	LVDS	

Figure 2 shows the frequency synthesizer ASIC functional block diagram; the frequency synthesizer ASIC is separated into two main sections, the PLL core and the output core. The output core serves two main functions: to allow user-controlled division of the PLL core output frequency to extend the lower end of the ASIC output frequency range, to allow user-controlled selection of the ASIC output logic type. Since the output core of the frequency synthesizer is outside of the PLL loop, any frequency division and/or signal conditioning performed in the output core will not alter the performance of the PLL core. Consequently, for the analysis of the prescaler design within the frequency synthesizer ASIC, the output core can be neglected. The subsequent analysis will be limited to the PLL core. In the PLL core, the oscillator frequency (f_{osc}) is generated from the external crystal and integrated crystal oscillator. A Schmitt trigger digitizes the analog output signal of the crystal oscillator to establish the reference frequency (f_{ref}). The phase-frequency detector together with the charge pump compares the phase difference between the reference signal (f_{ref}) and the feedback signal (f_{fbk}) and generates a sourcing/sinking current pulse (i_{cp}) for a positive/negative phase difference.

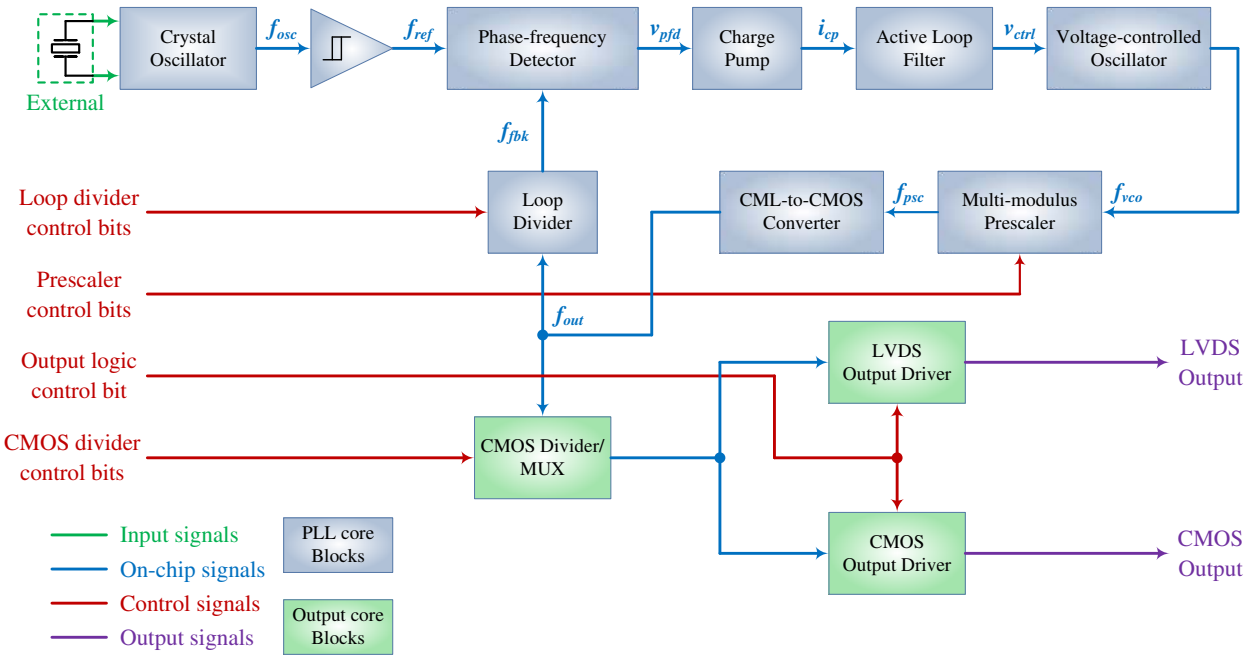

Figure 2. Frequency synthesizer ASIC functional diagram

The active loop filter reduces the bandwidth of the PLL control loop (thereby establishing the dynamic performance of the loop) and generates a stable control voltage (v_{ctrl}) for the voltage-controlled oscillator by suppressing noise and voltage ripple from the charge-pump. This control voltage regulates the oscillation frequency of the VCO (f_{vco}). By design, the VCO oscillation frequency is much higher than the reference frequency and must be reduced to allow the control loop to lock and reach stable operation. The prescaler provides the majority of this frequency division with high-speed, current-mode logic (CML). The CML signal of the prescaler output (f_{psc}) is converted to CMOS logic via a CML-to-CMOS logic converter. The output of the CML-to-CMOS converter is taken as the output of the PLL core (f_{out}). The CMOS loop divider provides the remaining frequency division and generates the feedback signal for the phase-frequency detector.

In lieu of a detailed PLL transfer function analysis, a simplified, linear approximation of the PLL control loop will be performed as this analysis is sufficient for understanding the operation of the prescaler within the PLL control loop. Shown in Figure 3 is a simplified diagram of the PLL core used for the subsequent PLL analysis. Here, N_{PSC} is the prescaler division ratio and N_{LD} is the loop divider division ratio. In this analysis, it is assumed that the loop is operating in a locked condition, and the chosen crystal determines the reference frequency, f_{ref}. Under these assumptions, the feedback frequency is forced to match the reference frequency. Therefore, we see that

$$f_{out} = f_{ref} N_{LD} \qquad \{2.1\}.$$

Substituting the maximum values of output frequency (250 MHz) and crystal frequency (25 MHz) from Table 2 into {2.1} gives the maximum required loop divider ratio of 10. To limit the tuning range required of the VCO, a minimum loop divider ratio of 4 is used. Therefore, the PLL core output frequency range is 80 MHz to 250 MHz. Observing Figure 3 once more, we find that

$$f_{vco} = f_{out} N_{PSC} \qquad \{2.2\}.$$

As mentioned in Chapter 1, there are several advantages to operating the VCO within a PLL at high frequencies. To this end, a nominal VCO frequency of 4 GHz was chosen with ±10% tuning range. Substituting this nominal VCO frequency and the stated 80 MHz to 250 MHz output frequency range into {2.2} results in a required prescaler division ratio range of ~ 16 to 48.

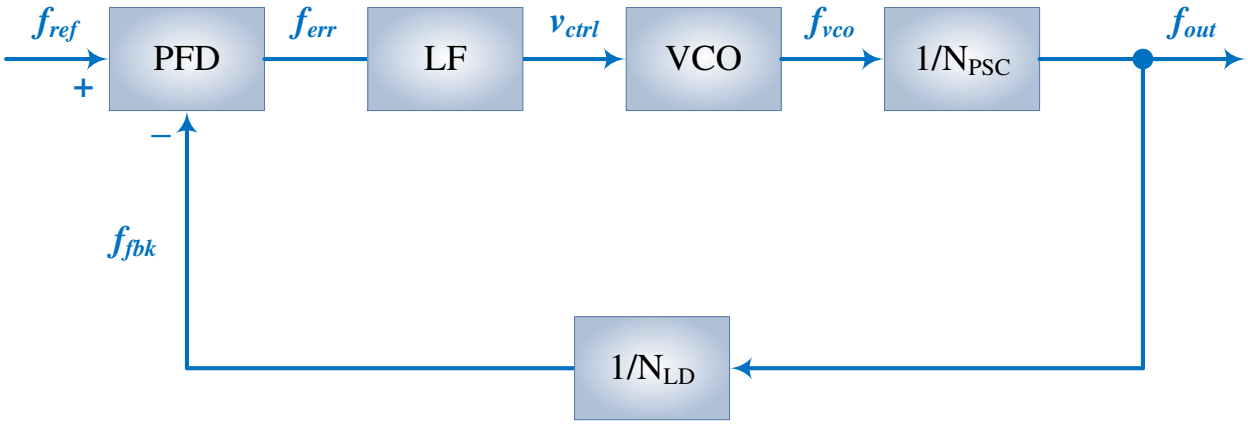

Figure 3. PLL core functional diagram (simplified)

2.2 Multi-modulus prescaler design considerations

From the analysis of the frequency synthesizer ASIC in the previous section, the performance requirements of the extreme environment, multi-modulus prescaler designed to support the frequency synthesizer ASIC can be established. The VCO tuning range, output frequency range, and output frequency resolution of the frequency synthesizer ASIC dictate the operating frequency and resolution specifications required of the multi-modulus prescaler. A summary of the design specifications of the multi-modulus prescaler are outlined in Table 3. The VCO output signal is a differential, ground-referenced, sinusoidal signal in the range of 3.6 GHz to 5 GHz. The VCO output signal must be buffered and level-shifted to the CML logic level required by the multi-modulus prescaler. To allow tuning linearity and configurability, the prescaler must be able to divide the buffered VCO signal in the range of 16 to 48 with high resolution (27 total moduli with the division range). The differential, CML output of the prescaler must be converted to a 1.8 V CMOS signal capable of operating up to at least 250 MHz. As stated in the previous sections, the prescaler must operate reliably over a temperature range of −180°C to 125°C and supply voltages from 3.0 V to 3.6 V. To be able to provide extreme environment capability, the prescaler must be TID radiation tolerant up to 1 Mrad/Si as well as SEL immune and SEU resistant. The definition of SEU resistant established for this research work is that the circuit is able to “quickly and gracefully” recover from SEUs.

Table 3. Multi-modulus prescaler design specifications

Performance parameter	Design specification	
Input frequency	3.6 to 5	GHz
Output frequency	80 to 250	MHz
Output logic	1.8 V CMOS	-
Division range	16 to 48	-
Total moduli	27	-
Operating temperature range	−180 to 125	°C
Supply voltage range	3.0 to 3.6	V

2.3 Frequency synthesizer ASIC development

The frequency synthesizer ASIC was developed on a SiGe BiCMOS process. This reasoning behind this design choice will be explained in Chapter 3. The frequency synthesizer ASIC is a fully-integrated design (except for the external crystal resonator). The frequency synthesizer ASIC, along with the crystal, is configured at the packaging stage to provide a complete frequency synthesizer system-in-a-package solution. To achieve the stated TID radiation tolerance requirement, the frequency synthesizer ASIC leverages the SiGe hetero-junction bipolar transistor (HBT) and avoids the use of the TID-sensitive NMOS device [9], [10]. The development of the frequency synthesizer ASIC (and therefore the prescaler) used a commercially-available, 180-nm SiGe BiCMOS fabrication process. This process offers HBT devices capable very high-speed operation which facilitated the design of the high-frequency portion of the PLL core.

CHAPTER 3: LITERATURE REVIEW

3.1 Introduction

Chapter 2 of this dissertation outlined the design requirements for the extreme environment capable prescaler developed for use in the frequency synthesizer ASIC. Chapter 2 states that the frequency synthesizer ASIC was developed on a 180-nm SiGe BiCMOS process. The first section of this chapter examines this technology and provides reasoning for this design choice. Additionally, this chapter reviews the limitations of lower-speed logic families (such as the well-known static CMOS logic) and explores high-speed digital logic families (such as CML). This chapter also examines methods of achieving fractional-N division, including the common dual-modulus approach. Lastly, this chapter covers a review of prior art demonstrating prescalers capable of high-speed operation, high-resolution moduli, and/or extreme environment capability.

3.2 Silicon Germanium (SiGe) technology overview

Bulk-silicon CMOS technology has long dominated the semiconductor market place for a number of reasons including: ease of growing a high-quality dielectric (SiO_2); silicon can be grown in large, single crystals; silicon is capable of high levels of integration; silicon has excellent heat dissipation qualities; silicon has a wide doping range for both *n*- and *p*-type impurities, cost of bulk-silicon technology remains considerably lower than other process technologies [11]. While all of these attributes of bulk-silicon are certainly desirable for any semiconductor material used as an integrated circuit (IC) development platform, silicon has several notable limitations to consider. These limitations include: relatively low carrier mobility (both electrons and holes), low saturation velocity, and susceptibility to extreme environment effects (both temperature and radiation) [11] – [13].

Over the years, there has been considerable advancement in the area of extreme environment electronics. Developments in process technology as well as circuit design techniques have led to a wide range of extreme environment capable electronics. One such process technology that has demonstrated excellent performance in extreme environments is silicon-germanium (SiGe) bipolar-CMOS (BiCMOS) technology. SiGe BiCMOS technology leverages a heterojunction between silicon and silicon-germanium materials to form a *pn*-junction.

For extreme environment applications, the susceptibility of silicon CMOS ICs to hot-carrier and TID radiation effects is of particular concern. As previously explained, the underlying cause of the damaging effects of both hot-carrier injection and TID radiation on silicon devices is the generation and trapping of charge in an oxide layer of a device (most notably the shallow-trench isolation (STI) used to terminate the edges of the MOSFET conduction channel) [7] – [10]. Several radiation-hardening by design (RHBD) techniques have been demonstrated to be very effective in preventing this damaging trapped charge from accumulating along the STI edge. Unfortunately, these RHBD techniques (most notably annular-gate NMOS structures) invariably require design trade-offs, particularly a reduction in device speed and an increase in required chip area and power. Since SiGe HBT devices do not require this oxide layer, generation of trapped charge is not an issue in these devices. The damaging effects of low temperature operation and TID radiation observed in silicon CMOS devices are not seen in SiGe HBTs [14]. This feature of SiGe HBTs allows SiGe BiCMOS technology to provide a wide-temperature, radiation-tolerant design platform for IC development.

In addition to the extreme environment benefits of SiGe BiCMOS, SiGe HBTs are also capable of operating at much higher speeds than both silicon BJTs and silicon CMOS. Both the low carrier mobility and saturation velocity of silicon reduce speed achievable by silicon-based devices [15]. Many compounds from the III-V semiconductor family offer drastically higher motilities and saturation velocities than those of silicon; however, these compounds offer none of the benefits of silicon in terms of ease of fabrication, high-integration level, high yield, and low fabrication cost [11]. SiGe HBTs are inherently very high-speed devices and exhibit excellent performance at low temperature. In fact, many important bipolar device parameters (such as current gain and cut-off frequency) improve as temperature decreases [14], [16]. Additionally, since SiGe technology is developed from bulk-silicon CMOS technology, SiGe HBTs can be developed on existing silicon CMOS processes. SiGe HBT technology, therefore, offers operating speed performance that is competitive with that of the III-V compounds while maintaining compatibility with easy to fabricate, low-cost silicon CMOS [14]. The result is that SiGe BiCMOS processes offer a complete bulk-silicon CMOS design platform with the addition of high-speed, radiation-hard HBTs.

The previous discussion on SiGe technology highlights why SiGe BiCMOS technology is a very attractive choice for high-speed, extreme environment capable electronic systems. With no modification to the existing technology, SiGe BiCMOS has several qualities ideally-matched to the development of an extreme environment capable frequency synthesizer ASIC. The key benefits of SiGe BiCMOS technology within the scope of this research include:

- Compatibility with low-cost, high-yield silicon CMOS processes
- SiGe HBT devices are capable of very high-speed operation (f_T ~ 60 GHz)
- SiGe HBT devices offer excellent low-temperature performance and resistance to hot-carrier injection
- SiGe HBT devices are inherently resistant to TID radiation

3.3 High-speed digital logic review

Many logic families have been developed through the years from the early resistor-transistor logic (RTL) to the ubiquitous CMOS logic and to more exotic logic families such as dynamic logic. Most of these logic families focus on taking advantage of the high integration capacity and high scalability of MOSFET devices. While MOSFET devices are distinctly advantaged in these areas, bipolar devices have always been and remain capable of much higher switching speeds than comparable MOSFETs. To this end, logic circuits for high-speed applications often implement current-mode logic (CML) as opposed to CMOS or other logic families. CML is a generalized logic structure that encompasses emitter-coupled logic (ECL), positive emitter-coupled logic (PECL), and source-coupled logic (SCL). All of these logic families have specific definitions for logic levels that may not be applicable to this design effort. For this reason, the generalized term, CML, will be used throughout this dissertation.

3.3.1 Speed limitations of CMOS logic

To understand why CML logic offers such a significant speed advantage over other logic families, we first examine the limiting factor in standard CMOS logic speed capability. As illustrated, the active devices in the CMOS inverter shown in Figure 4 can be modeled with switched constant current sources. In this analysis, the load capacitance includes all parasitic capacitance associated with the output of the inverter.

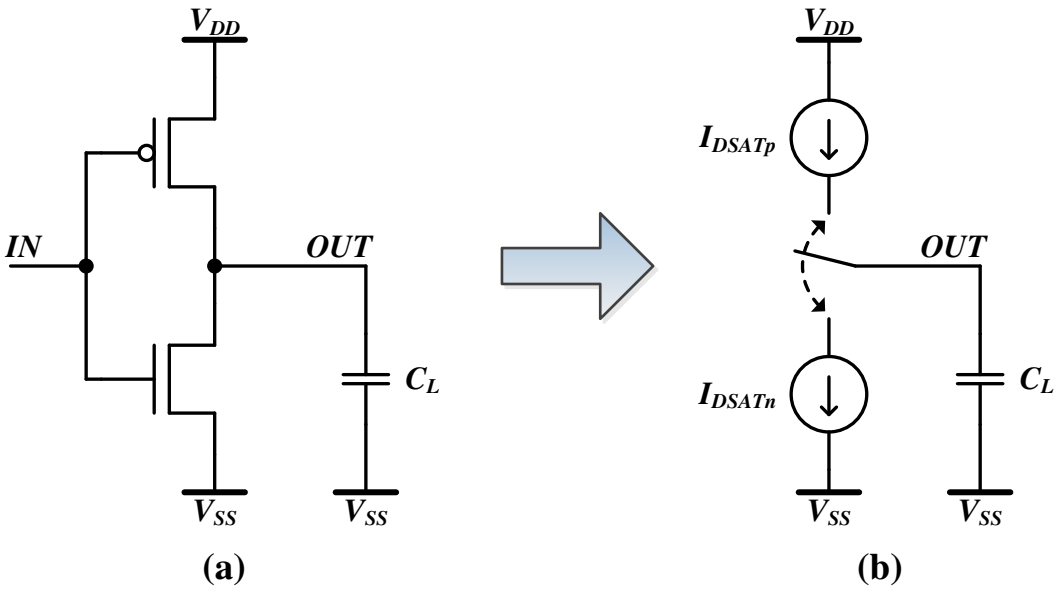

Figure 4. Standard CMOS inverter (a) with equivalent model (b)

The stored charge of a capacitor is a linear function of capacitor voltage as given by

$$Q = CV \qquad \{3.1\}.$$

The inverter propagation delay from output high to low (t_{phl}) of the CMOS inverter is defined as the time required for the output voltage to fall from V_{DD} to ½V_{DD}. Using this definition in {3.1}, the initial charge at the inverter output is given by

$$Q_{L\,(t=0)} = C_L V_{DD} \qquad \{3.2\}.$$

Similarly, the charge at the inverter output at time $t = t_{phl}$ is given by

$$Q_{L\,(t=t_{phl})} = C_L \frac{V_{DD}}{2} \qquad \{3.3\}.$$

Universally for capacitors, the total charge transferred between times t_1 and t_2 is a function of current flow as defined by

$$Q_{(t=t_2)} = \int_{t_1}^{t_2} I\, dt \qquad \{3.4\}.$$

For constant current, I, {3.4} can be evaluated as

$$t_2 - t_1 = \frac{Q_{(t=t_2)} - Q_{(t=t_1)}}{I} \qquad \{3.5\}.$$

Substituting {3.2}, {3.3}, and the saturated NMOS current source (negative current because it discharges the load capacitance) into {3.4} where $t_1 = 0$ and $t_2 = t_{phl}$, we find that

$$t_{phl} = \frac{C_L \frac{V_{DD}}{2} - C_L V_{DD}}{-2I_{DSATn}} = \frac{C_L V_{DD}}{2I_{DSATn}} \qquad \{3.6\}.$$

Substituting the expression for NMOS saturation current into {3.6} we see that

$$t_{phl} = \frac{C_L V_{DD}}{\frac{W_n}{L_n} \mu_n C_{ox} (V_{DD} - V_{TN})^2} \qquad \{3.7\}.$$

A similar analysis can be performed for inverter output low to high propagation delay; however, CMOS inverters are usually designed such that NMOS and PMOS saturation currents (and therefore rising and falling propagation delays) closely match [17].

The CMOS inverter equivalent model and subsequent analysis illustrate that the propagation delay for a CMOS inverter is determined by MOSFET saturation current, load capacitance at the inverter output, and supply voltage. Because the total charge of a capacitor is proportional to capacitor voltage and the fact that CMOS logic swings the full range of supply voltage, large amounts of charge must be continually supplied and removed from the inverter load capacitance. Also, the relatively low saturation current of MOSFET devices limits the rate that this load capacitance can be charged/discharged. These factors combine to limit the speed of CMOS logic circuits. In short, static CMOS logic is most well-suited for large-scale, low power, lower-speed applications, but applications requiring high-speed digital logic will not be able leverage the benefits of CMOS logic due to the prohibitive speed limitations inherent to CMOS logic.

3.3.2 Current-mode logic (CML) review

Having noted that CMOS logic speed is limited in large part because CMOS logic outputs must swing the full range of the supply rail, CML aims to improve speed by restricting the logic levels to a portion of the supply rail. Additionally, CML using BJT devices can improve on CMOS speed by replacing the relatively low speed MOSFET devices with higher-speed devices. The essential concept underlying CML logic is to use inherently high-speed bipolar devices in a differential pair configuration with a constant tail current (I_{EE}). In CML, the input and output logic levels are defined such that the bipolar devices are never driven into the

saturation region. This is an important concept in CML design since bipolar devices exhibit slow turn-off behavior in the saturation region [18]. Figure 5 shows a simplified CML inverter/buffer with parasitic load capacitance. Using the bipolar collector current equation

$$I_C = I_S\left(e^{V_{BE}/U_T} - 1\right) \qquad \{3.8\}$$

where U_T is the thermal voltage, we can express the ratio of collector currents of Figure 5 as

$$\frac{I_{C1}}{I_{C2}} = e^{(V_{i+}-V_{i-})/U_T} \qquad \{3.9\}.$$

The exponential relationship of this ratio to the input voltage difference shows that only very small input voltage difference is needed to force nearly all current through one bipolar transistor and negligible current through the other bipolar transistor. For example, an input voltage difference of only 100 mV results in a current ratio of 50 at room temperature; an input voltage difference of 200 mV results in a current ratio of over 2000.

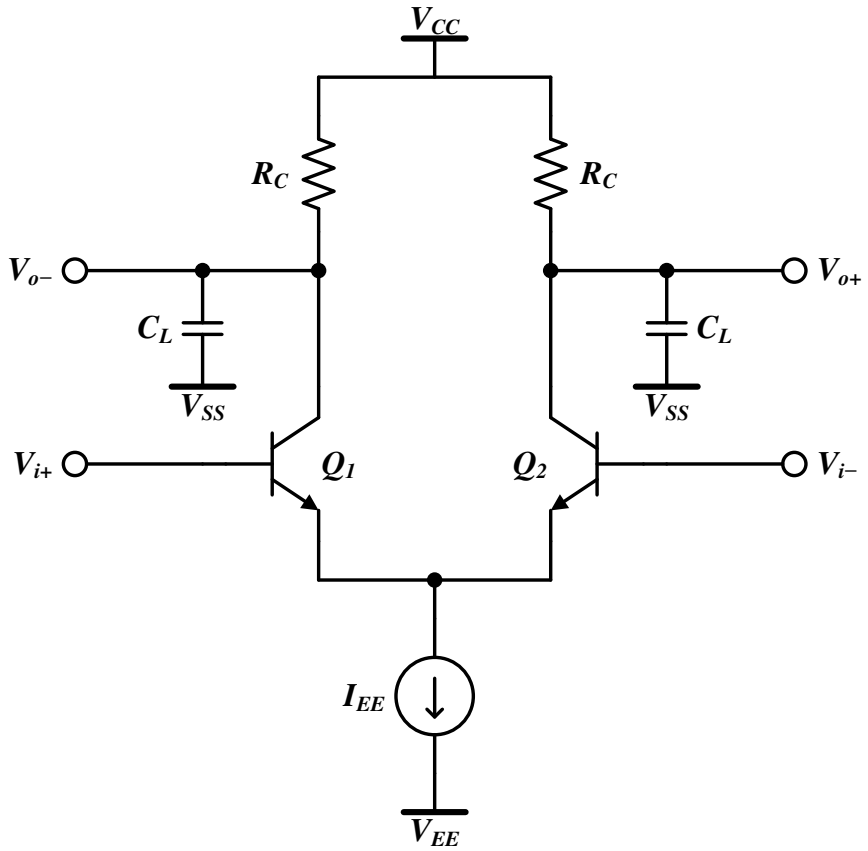

Figure 5. CML inverter/buffer (simplified)

This current ratio is high enough to approximate the differential pair as current-steering switch (all current flows through either Q_1 or Q_2 at any given time). Using this approximation, the CML inverter output logic levels can be defined as

$$V_{OL} = V_{CC} - I_{EE}R_C \qquad V_{OH} = V_{CC} \qquad \{3.10\}.$$

The differential input voltage is the same as the differential output voltage, so the differential logic levels can be defined as

$$V_{o/i+} - V_{o/i-} = V_{OH} - V_{OL} = I_{EE}R_C \qquad \{3.11\}$$

and the emitter current and collector resistor are chosen to induce a relatively small voltage differential. Therefore, the common-mode voltage of the differential pair can be set to ensure that both Q_1 and Q_2 remain in the forward-active region throughout operation and the slow turn-off behavior of the saturation region is avoided. By restricting Q_1 and Q_2 to the forward-active region of operation, small-signal estimations for the cut-off frequency (f_T) of Q_1 and Q_2 are valid. As stated earlier in this chapter, current SiGe BiCMOS technology offers well-established HBTs with cut-off frequencies of 60 GHz or more. The high f_T of these HBT devices allows the time constant associated with the parasitic load capacitance and collector resistor to dominate the CML inverter transient response, so Q_1 and Q_2 can be approximated as ideal switches. Figure 6(a) shows the resulting equivalent model for one side of the differential CML inverter/buffer. Figure 6(b) shows the state of the inverter with the output LOW, just before the output transitions HIGH; Figure 6(c) shows the equivalent model of the inverter just after switching from output LOW to HIGH. From Figure 6(c), KVL reveal the time domain output voltage response is governed by

$$I(t)R_C + V_o(t) = V_{CC} \qquad \{3.12\}.$$

Using the time domain expression relating capacitor current to voltage

$$I_C(t) = C\frac{dV_C(t)}{dt} \qquad \{3.13\}$$

and realizing that $V_C(t) = V_o(t)$ and $I_C(t) = I(t)$, {3.12} can be rearranged to show that

$$R_C C_L \frac{dV_o(t)}{dt} + V_o(t) = V_{CC} \qquad \{3.14\}.$$

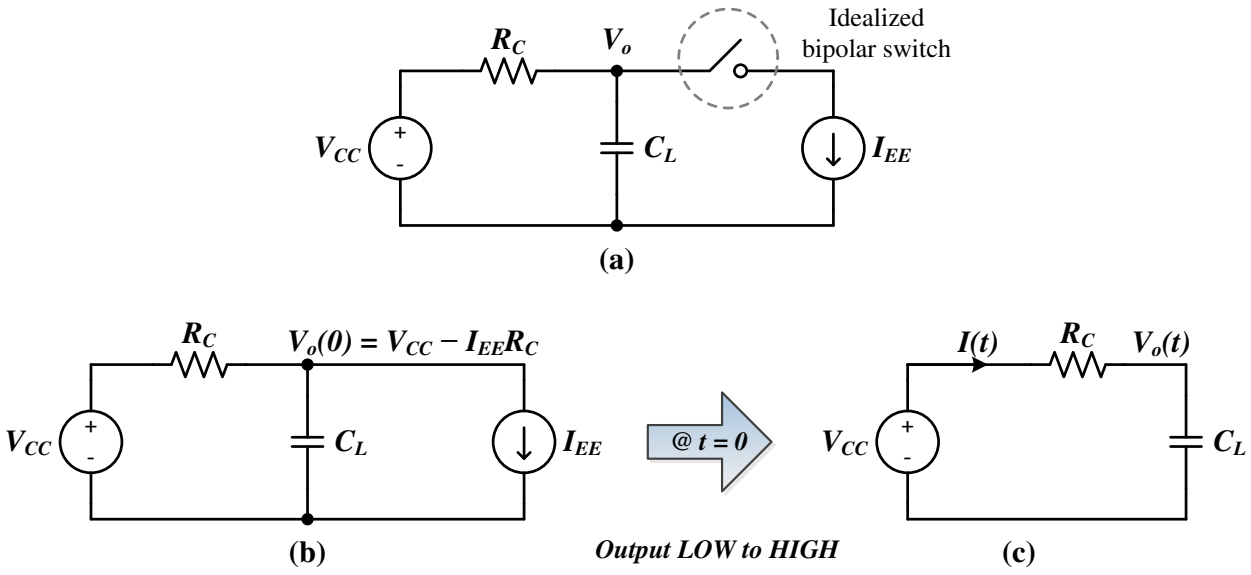

Figure 6. CML inverter/buffer (a) equivalent model using ideal switch, (b) equivalent model just before output LOW to HIGH, (c) equivalent model after output LOW to HIGH

Equation {3.14} is a first-order, differential equation that can be solved as

$$V_o(t) = V_{CC} + Ke^{-t/R_C C_L} \qquad \{3.15\}$$

where *K* is an unknown constant of integration that can be found using the initial condition of the inverter output voltage shown in Figure 6(b).

$$V_o(0) = V_{CC} - I_{EE}R_C = V_{CC} + Ke^0$$
$$\text{or} \qquad \{3.16\}$$
$$K = -I_{EE}R_C$$

The final expression for the CML inverter output LOW to HIGH transient response is then

$$V_o(t) = V_{CC} - I_{EE}R_C e^{-t/R_C C_L} \qquad \{3.17\}.$$

Defining output LOW to HIGH propagation delay (t_{plh}) as the time required for the output to swing from V_{OL} to $(V_{OL}+V_{OH})/2$ and substituting these values into {3.17}, we arrive at

$$V_o(t_{plh}) = \frac{V_{CC} + (V_{CC} - I_{EE}R_C)}{2} = V_{CC} - I_{EE}R_C e^{-t_{plh}/R_C C_L} \qquad \{3.18\}.$$

Solving {3.18} for the LOW to HIGH propagation delay, we find that

$$t_{plh} = R_C C_L ln2 \qquad \{3.19\}.$$

A similar analysis for the CML inverter output HIGH to LOW transient response can be performed to find that

$$V_o(t) = V_{CC} - I_{EE} R_C \left(1 - e^{t/R_C C_L}\right) \qquad \{3.20\}$$

Solving {3.20} for output HIGH to LOW propagation delay reveals that

$$t_p = t_{phl} = t_{plh} = R_C C_L ln2 \qquad \{3.21\}.$$

where t_p is defined as the average of t_{plh} and t_{phl}. In this first-order analysis, it is revealed that the CML inverter propagation delay depends only on the parasitic load capacitance and the size of the collector resistor. The dependence of the inverter propagation delay on supply voltage observed with the CMOS inverter is not seen in the CML inverter. Moreover, the propagation delay of the CML inverter is not limited by the switching speed or saturation current of the active device. Judicious choice of I_{EE} and R_C in the CML inverter design allows this logic structure to operate at speeds approaching the limit of the HBT device itself; however, static power dissipation of CML circuits is proportional to I_{EE}. In summary, the previous CML/CMOS logic comparison indicates that CML is capable of significantly higher operating speeds than CMOS, but this benefit comes at the expense static power dissipation. CMOS logic does not consume static power as observed with CML and can allow for lower power designs.

3.4 Fractional-N division review

Chapter 1 of this dissertation introduced the concept of fractional-N division as a method for obtaining greater frequency resolution in frequency synthesizer designs. Other methods exist for increasing frequency resolution that include: separation of PLL loop divider and output divider, use of multiple-loop synthesizers, pulse-swallowing techniques, and others [3]. All of these techniques have distinct advantages and disadvantages that must be considered in the design of any PLL-based frequency synthesizer. This research focuses on the most common techniques for increasing frequency resolution, fractional-N division. In Figure 7, a basic, integer-N PLL structure is shown. The integer-N PLL configuration operates such that the phase-locking of the phase detector requires that $f_{out} = Nf_{ref}$. Therefore, the output frequency is a selectable, integer-multiple of the reference frequency. To suppress output ripple and ensure loop stability, the bandwidth of the loop must be substantially smaller than the phase detector

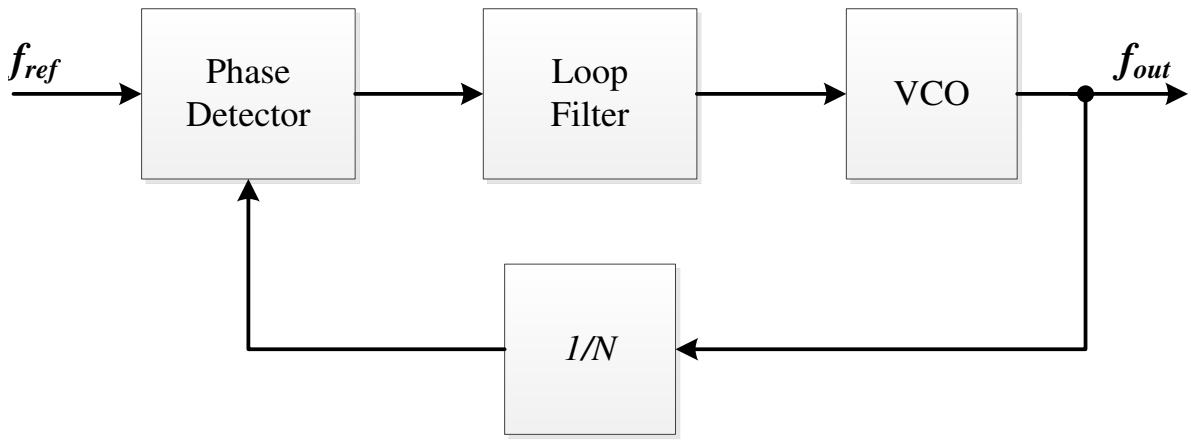

Figure 7. Integer-N phase-locked loop

comparison frequency, f_{ref}. If it is desired that the output frequency increments be small, then the PLL bandwidth must extremely small. This narrow bandwidth requirement opposes the benefits of rapid frequency acquisition and stabilization of VCO jitter achieved with higher loop bandwidths. It is now evident that a conflict exists in PLL design between simultaneously obtaining narrow frequency resolution and fast PLL loop response time. A useful technique for alleviating this conflict is using fractional-N division as opposed to integer-N division. A fractional-N divider narrows the output frequency resolution without compromising loop bandwidth. One method for realizing fractional-N division is the use of a dual-modulus prescaler as shown in Figure 8. The dual-modulus prescaler in Figure 8, divides by *P* or *P+1* as dictated by the modulus control. The division ratios of the *N* and *A* counters are externally controlled. The dual-modulus prescaler can best be conceptualized as a counter that divides the VCO frequency by *P* for *N−A* cycles and by *P+1* for *A* cycles. For example, assume that counters *N* and *A* are each externally preset to some value and the prescaler initially divides by *P+1*. After each cycle of the prescaler (*P+1* cycles of the VCO), the *N* and *A* counters are decremented by 1. This continues until the *A* counter reaches zero, after which, the *P* counter division ratio is changed from *P+1* to *P*. At this point, the *N* counter has completed *A* counts. The *N* and *A* counters continue to decrement with every cycle of the prescaler (*P* cycles of the VCO) until the *N* counter reaches zero, at which point, both counters and the prescaler reset and the cycle repeats. One complete cycle as described above consists of *A* cycles of *P+1* VCO sub-cycles and *N−A* cycles of *P* VCO sub-cycles.

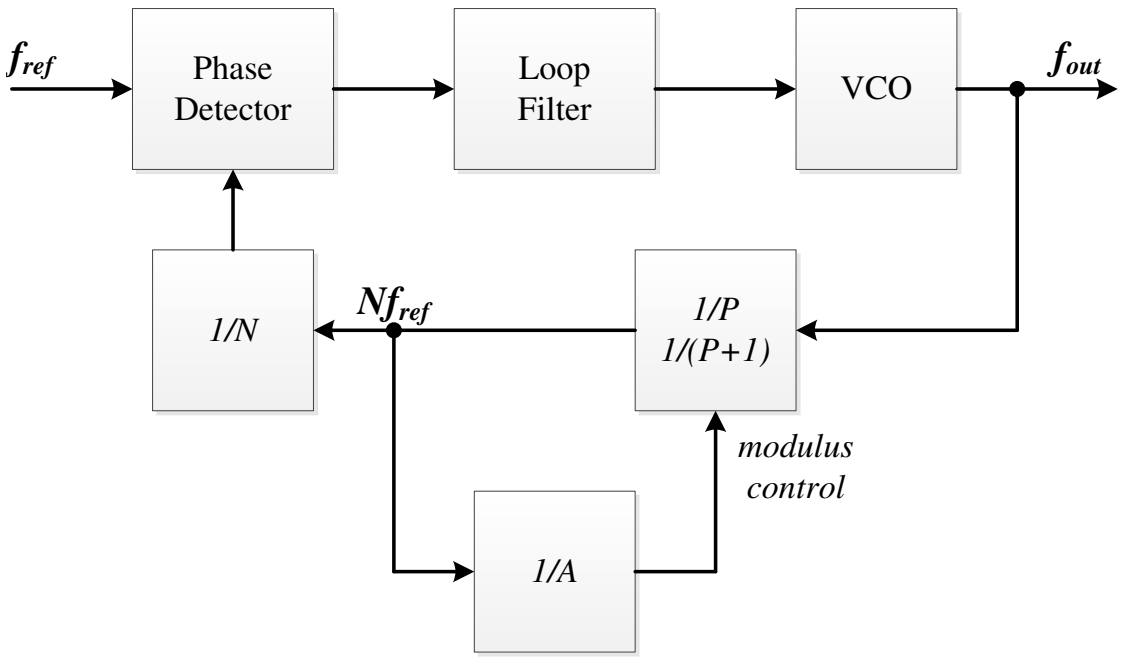

Figure 8. Phase-locked loop with dual-modulus prescaler

The total resulting count can be expressed as

$$N_{tot} = A(P+1) + (N-A)P = NP + A \qquad \{3.22\}.$$

While this counting structure is not truly fractional-N division since N_{tot} must be a whole number, multiplying N by P allows the addition of a count, A, to effectively result in a fractional divider. Dual-modulus prescalers are not able to operate with any choice of N, P, and A; they are restricted by the limits $A < P$ and $N \geq A$. These restrictions imply that N_{tot} must be greater than $P(P-1)$ to achieve the channel spacing advertised, otherwise gaps in the channel spacing exist. This shows that a dual-modulus prescaler cannot achieve high division resolution for low-range moduli. The consequences of this point as it pertains to this dissertation will be addressed later in this chapter. Another drawback to a dual-modulus prescaler approach is that the periodicity introduced by the varying prescaler modulus appears as sidebands or spurs around the operating frequency. These sidebands and spurs can be suppressed by dithering techniques, but this usually requires complex delta-sigma techniques to avoid an increase in the noise floor. These limitations of the conventional dual-modulus prescaler design indicates the need for this research work to explore alternative methods of achieving narrowly-spaced moduli for over a low division range of 16 to 48.

3.5 Prescaler prior art

The previous sections of Chapter 3 highlight the need for a literature review to examine the prior art for prescaler designs. A considerable amount of literature has been published on a wide variety of prescaler designs. Many of these prescaler designs offer specifications that meet those required of this research effort, but none of the designs encompass all of the requirements for this multi-modulus prescaler design effort. The prior art applicable to such a prescaler design will now be examined, and the knowledge and design techniques of this examination will be incorporated into the development of a novel prescaler solution capable of meeting the specifications provided in Table 3. Special attention will be paid to prescaler designs with one or more of the following attributes: high-speed operation, high division resolution, and extreme environment operation capable.

3.5.1 High-speed prescaler prior art

Prescaler designs operating at frequencies over 40 GHz have been reported in literature [19] – [21]. These high-speed designs utilize current-mode logic with inductor peaking to achieve high switching speeds, but inductor peaking results in highly-tuned digital cells that can operate only in a narrow frequency band. Other digital design techniques have been demonstrated that allow high-speed operation without requiring highly-tuned circuits. One such example is the 21 GHz, 8-modulus prescaler CMOS design described in [22], see Figure 9.

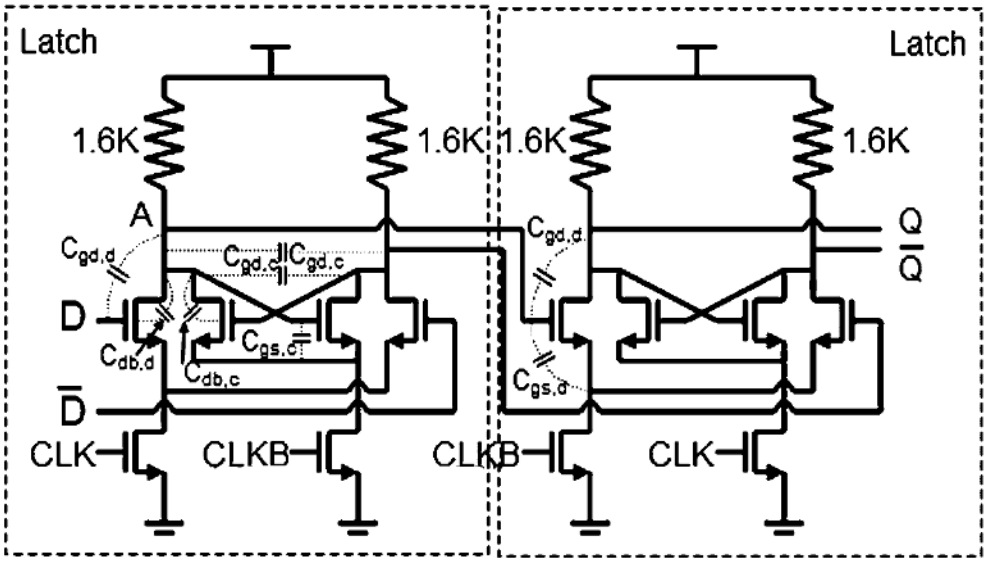

Figure 9. D-flip-flop used in prescaler in [22]

This prescaler design uses NMOS-based, CML D-flip-flops to achieve a 21-GHz maximum operating frequency. This 21-GHz prescaler design consists of a 4/5, synchronous counter and a divide-by-64, asynchronous counter. This configuration allows for external control of the prescaler division ratio in the range of 256-263 with 8 selectable output frequencies. The block diagram of the prescaler reported in [22] is shown in Figure 10. While this 21-GHz prescaler design meets the required 5 GHz operating frequency of this research, this prescaler was designed in a "stacked" configuration along with the VCO of the PLL. By stacking the VCO and prescaler, the VCO and prescaler can share current and parasitic capacitance at these critical, high-speed circuit nodes can be reduced, allowing for very high-speed designs. The drawback to this technique is that the VCO and prescaler must be designed and optimized in conjunction; therefore, the prescaler design as intellectual property (IP) cannot be used with another VCO without major redesign effort. Another tradeoff of this technique is that this VCO/prescaler design requires a significant amount of bench tuning to achieve the desired operation. As discussed in Chapters 1 and 2, this research is focused on developing a highly-configurable ASIC that (once configured at the bonding/packaging stage) requires no tuning or user configuration. Any design solution requiring post-fabrication tuning or optimizing is not viable for this research effort. Moreover, the dual-modulus approach used for this design limits the division range of this prescaler (256-263) to well outside the range required of this research.

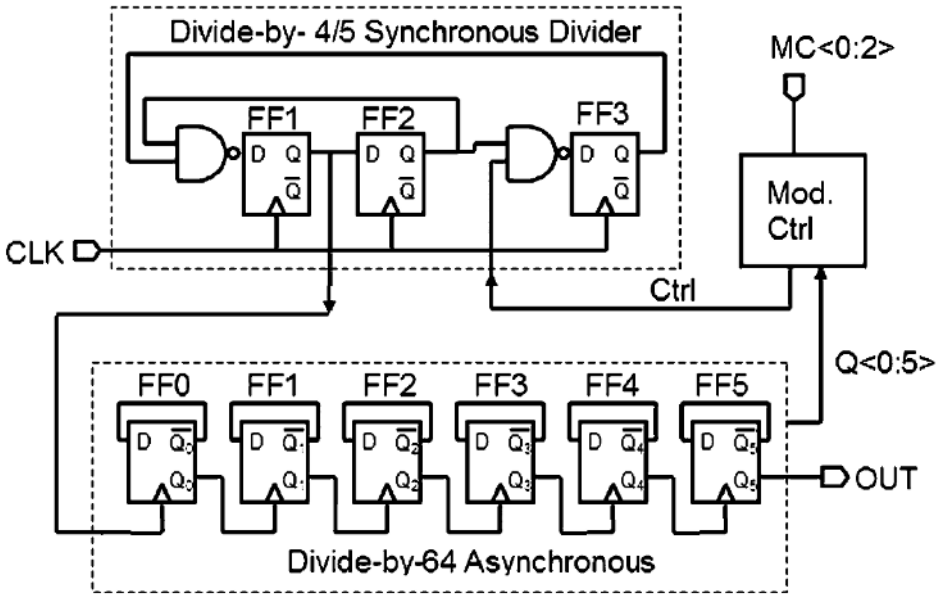

Figure 10. Diagram of 8-modulus prescaler in [22]

Additionally, the range of division ratios for the 21-GHz prescaler design is quite restricted and will limit the range of frequency synthesizer output frequencies possible with this prescaler. Lastly, frequency synthesis using this 21-GHz prescaler is limited to a maximum output frequency determined by the maximum prescaler input frequency and the minimum prescaler division ratio, found to be 82 MHz. The 82-MHz output frequency limit for this prescaler is well below the 250 MHz maximum output frequency required for this research. Another consideration with respect to this prescaler design is the extensive use of NMOS devices in the CML D-flip-flops (the essential building block of this prescaler). NMOS devices have a well-documented sensitivity to ionizing radiation (see Chapter 1) that prohibits the use of such a design in a radiation-rich environment. Due to the sensitivity of NMOS devices to ionizing radiation, any prescaler design utilizing NMOS devices without using RHBD techniques is not viable for this research work.

Another high-speed prescaler design that leverages HBTs instead of NMOS as the principle active device attains an 8 GHz maximum operating frequency as reported in [23].

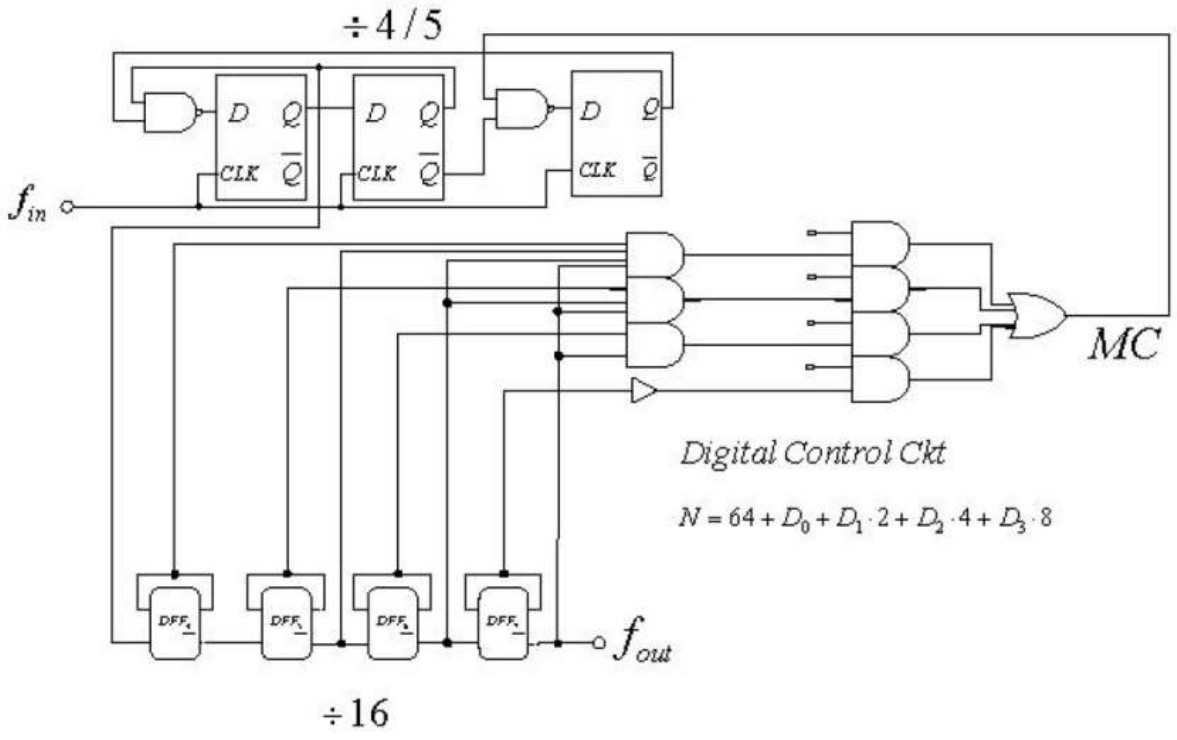

Figure 11. Diagram of divide-by-64~79 prescaler of [23]

This prescaler uses HBT-based CML D-flip-flops to achieve this high-speed operation. This design uses a synchronous, divide-by-4/5 counter followed by a divide-by-16, asynchronous counter (Figure 11). In this configuration, division ratios of any integer in the range of 64-79 can be achieved with this prescaler design, but as with the prescaler in [22] this division range is insufficient for the goals of this research. These D-flip-flops are incorporated with merged NAND gates as shown in Figure 12. By merging the NAND gates with the D-flip-flops, the gate delay associated with a separate NAND gate is diminished and the operating frequency range is extended. The HBT-based, CML D-flip-flops used throughout this prescaler design allow for the reported 8 GHz operation. While this paper does not present any specific information on this design with respect to extreme environment reliability, the SiGe HBT has been established as an extreme environment capable device and designs leveraging HBTs could potentially take advantage of this inherent quality. Extreme environment capability notwithstanding, the division range 64-79 is insufficient (both out of required range and width of range too narrow) to allow such a design topology to be used in this research work.

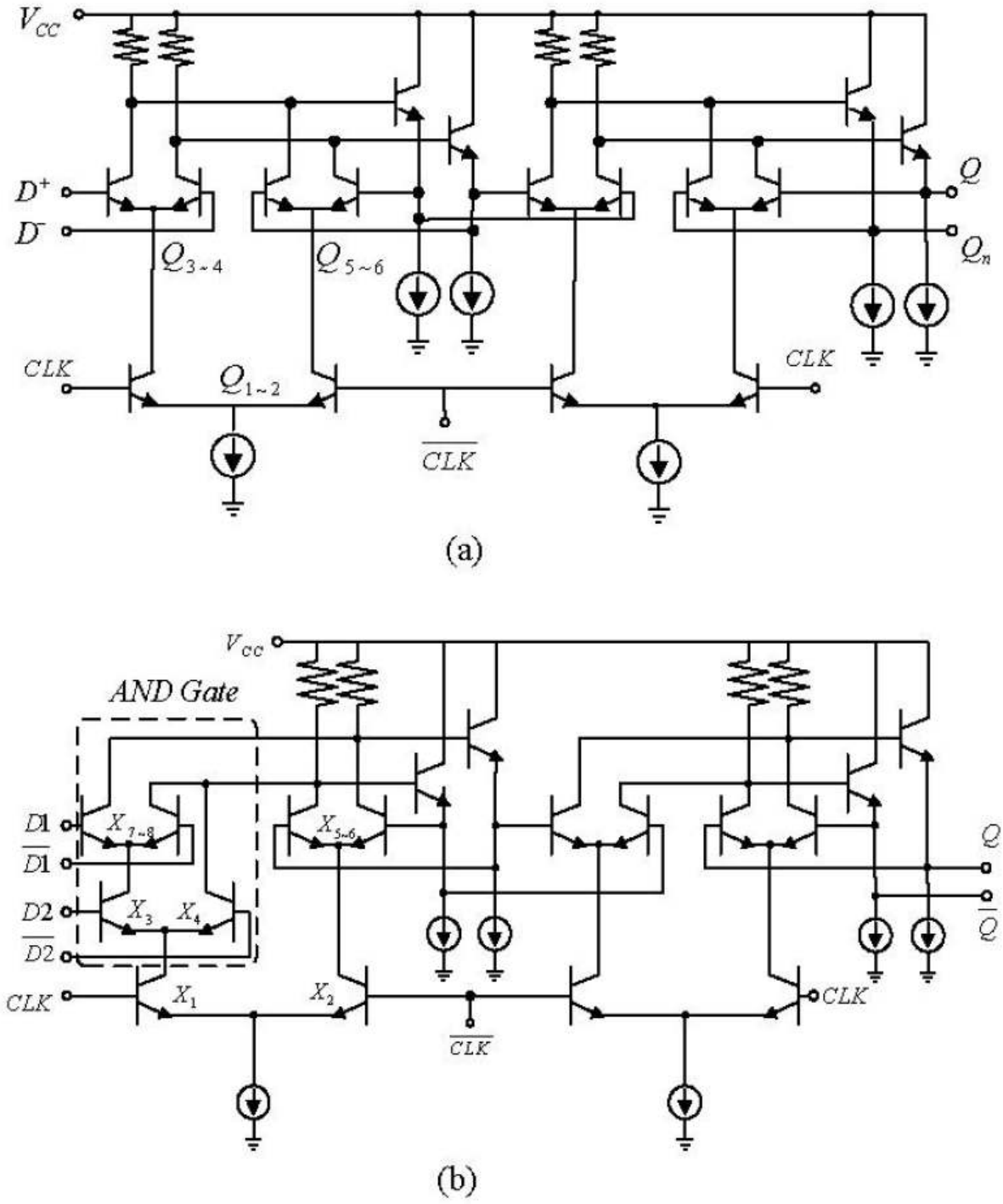

Figure 12. D-flip-flop designs of [23] (a) without and (b) with merged NAND gate

High-speed prescaler designs are not necessarily limited to CML structures, and this fact is demonstrated in the work described in [24]. This paper reports a multi-modulus prescaler design using a modified, enhanced, true-single phase clock (METSPC), dynamic CMOS logic gates developed on 90-nm CMOS technology capable of operating at frequencies as high as 5 GHz. However, this paper only reports simulation data and presents no experimental results. This design consists of a divide-by-2/3, synchronous counter followed by a divide-by-16, asynchronous counter and allows for divisions by 32/33/39/40/47/48. The prescaler described in [24] is demonstrated in Figure 13. As with the previous prescaler designs examined, this prescaler is subject to a narrow division range, in addition to widely-spaced moduli. As with the prescaler described in [22], this prescaler leverages NMOS devices throughout and is therefore potentially sensitive to ionizing radiation.

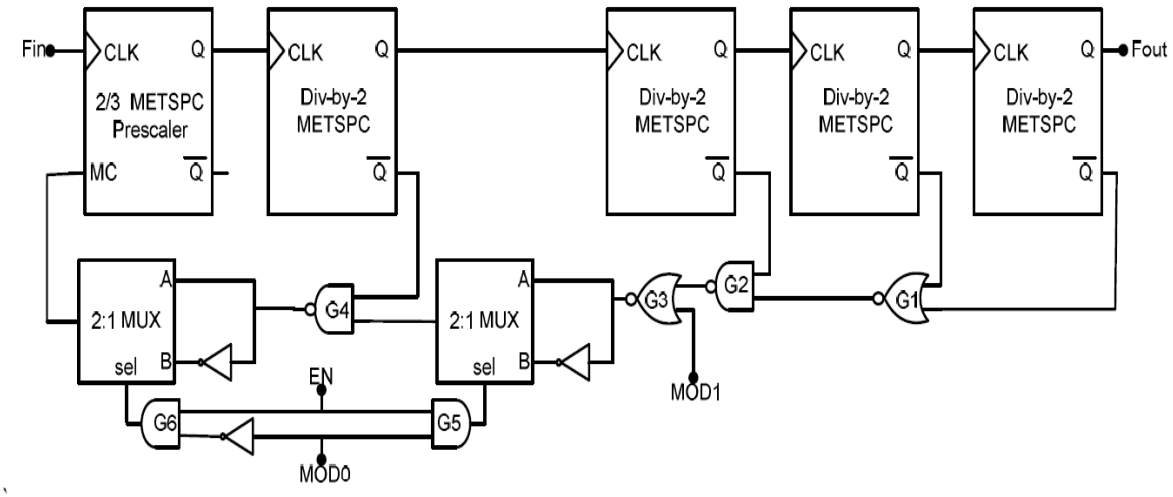

Figure 13. Diagram of multi-modulus 32/33/39/40/47/48 prescaler of [24]

3.5.2 High-resolution prescaler prior art

From the review of high-speed prescaler prior art, we saw that these prescaler designs have relatively narrow division ranges. These dual-modulus designs utilize a synchronous, dual-modulus divider followed by an asynchronous divider. As explained in section 3.4, this architecture cannot provide narrowly-spaced division over a low range of moduli. From Chapter 2, this research requires the design of prescaler capable of narrowly-spaced moduli from 16 to 48. A conventional, dual-modulus structure is, therefore, not viable for this prescaler and other avenues must be explored.

To illustrate the previous point, the frequency divider described in [25] is now examined. This frequency divider is composed of a 32/33 synchronous dual-modulus prescaler, a 5-bit swallow counter, an asynchronous 11-bit programmable counter, and a control circuit as seen in Figure 14. This frequency divider is arranged in the dual-modulus configuration seen previously and is capable of operating at clock frequencies from 0.5 to 3.5 GHz. The 11-bit programmable counter and the 5-bit pulse swallow counter allow this divider configuration to achieve an extremely wide range of moduli, from 1024 to 65536. A consequence of this wide division range is that the minimum division ratio must be quite high. This example of the frequency divider topology of [25] illustrates the point that a conventional dual-modulus prescaler approach (or any resolution narrowing method that uses varying moduli) is not well-suited for the development of a high-resolution frequency divider for a low range of moduli.

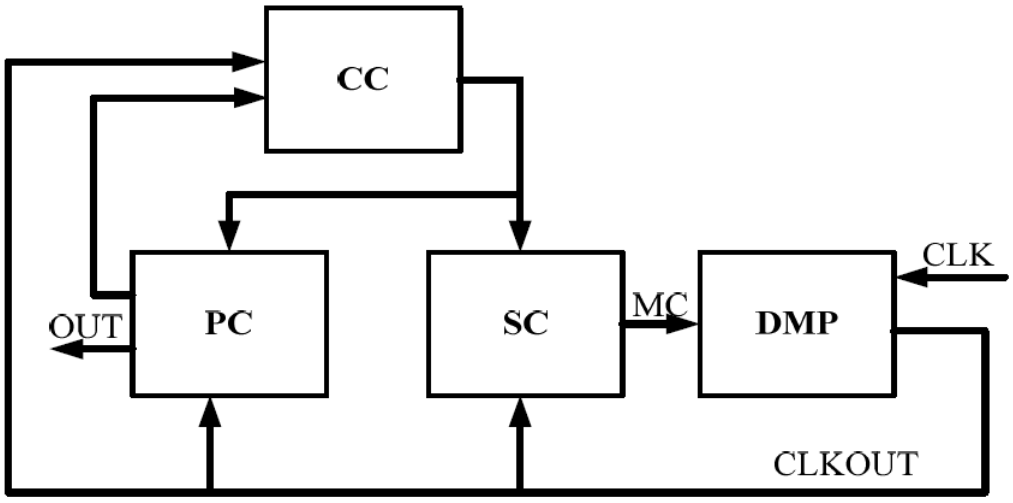

Figure 14. Diagram of frequency divider described in [25]

The prescaler described in [26] describes a multi-modulus prescaler design used to generate narrowly-spaced moduli over a low-range. The prescaler of [26] was developed using a 0.35-µm SiGe BiCMOS process. A maximum operating frequency of 4.6 GHz was achieved by leveraging high-speed, ECL D-latches as the principle building block. As opposed to the dual-modulus approach seen in the previous examples, this design cascades a series of divide-by-2/3 cells as illustrated in Figure 15. For this design, each control signal C_n is used to control the modulus of each stage divide-by-2/3 cell. A feedback signal, generated in the subsequent stage of each cell, is used to ensure that each cell divides by 3 only once during the prescaler cycle. This work used six divide-by-2/3 cells configured as seen in Figure 15, which results in a division range of 64 to 127. This range of moduli is much closer to the range required of the prescaler for this research work (16 to 48). Using five 2/3 cells would allow a prescaler to attain moduli of 16 to 31, but this division range is still not adequate for the prescaler design of this work. Another tradeoff to consider with this design is that the input frequency to each stage changes drastically for different configurations. To maintain adequate input operating frequency of all stages of the cascade-based prescaler for all division configurations, each cell must either be biased for the highest input frequency possible (wastes power for all other configurations) or an adaptive bias scheme must be used (adds complexity, uses more power and space). The cascaded prescaler structure used in the precaler of [26] is not a complete solution to the prescaler design challenge of this research work but shows promise as tool for the development of a complete solution.

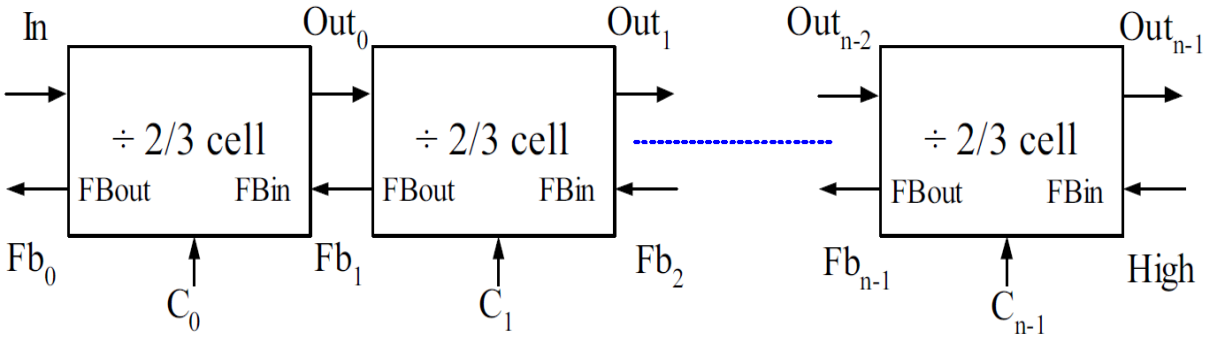

Figure 15. Diagram of cascade-based prescaler of [26]

Another promising prescaler design was described in [27]. This prescaler was developed on a 0.25-µm BiCMOS process and consists of two main parts, the ECL programmable divider and the CMOS divide-by-16 divider (see Figure 16). A maximum input frequency of 12.8 GHz was reported for this prescaler for a range of moduli from 128 to 368. Just as with the prescaler described in [26], the programmable divider part of [27] is a cascade division cells, however, [27] implements triple-modulus dividers for these cells as opposed to dual-modulus dividers. These triple-modulus dividers are capable of division by 1, 2, or 3. The programmable part of the prescaler of [27] cascades three of these triple-modulus prescalers, and the result is a programmable divider capable of division from 9 to 23. If four such prescalers were cascaded, a division range of 17 to 47 would be possible (very close to the range required of this research work). As with the prescaler of [26], the input frequency of each stage is a function of the division ratio, and the resulting biasing considerations apply to [27] as well.

The prescaler of [27] shows that the use of cascaded, triple-modulus divider cells allows for narrowly-spaced division over a low range of divisors, which is the goal of this research work. A prescaler composed of cascaded, multi-modulus dividers is a departure from the much more common, dual-modulus prescaler approach. However, the cascaded, multi-modulus divider approach does not impose the low-range frequency resolution design challenges seen in varying moduli approaches.

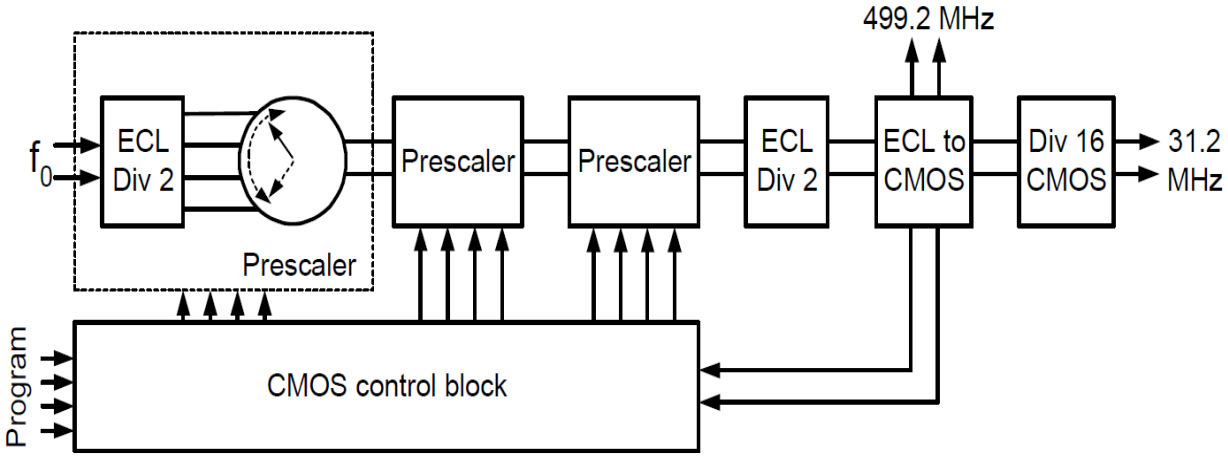

Figure 16. Diagram of programmable frequency divider of [27]

Other high-resolution prescaler designs have been demonstrated in literature. The odd-modulus divider described in [28] is capable of operating at frequencies as high as 7 GHz and division by odd-moduli through the use of current-switchable, CML D-flip-flops. The resulting D-flip-flop triggers on both positive and negative clock edges, which enables division by odd-moduli. However, this prescaler is designed to be implemented for a fixed modulus and does not allow for external configuration. Another design leveraging double-edge triggering (DET) is reported in [29]. The design of [29] modifies a conventional divide-by-128/129 prescaler by using DET DFFs to implement a divide-by-64/64.5. This modification allows the PLL output to be taken directly from the VCO output instead of passing through a divide-by-2 cell. Therefore, the operating frequency of the modified VCO and prescaler is reduced by two, which reduces the power consumption. However, the PLL of [29] is designed to operate at a fixed frequency, and consequently, the prescaler of this design is not configurable. In [30], a dual-modulus prescaler design using an imbalanced phase-switching technique is reported. This technique relies on the fact that 50% duty cycle is not required for proper operation of edge-triggered DFFs. As long as the triggering-edges occur at the correct time and set-up and hold times are not violated, the prescaler will operate properly. Lastly, [31] reports a "time-borrowing" technique for designing multi-modulus prescalers. The first section of this prescaler uses divide-by-2 cells to generate four 90°-spaced clock phases. A phase selector is then used to switch between these phases as dictated by a phase-switching control logic circuit. By shifting this phase for a single clock cycle, the instantaneous divide ratio can be reduced by one. This technique achieves the same end result as conventional dual-modulus prescalers, where a divider provides division-by-N for some amount of cycles, then division-by-N−1 for the remaining number of cycles. All of the high-resolution prescaler design techniques reviewed provided valuable insights into achieving a prescaler capable of meeting the requirements of this research work.

3.5.3 Extreme environment capable prescaler prior art

Extreme-environment capable electronics represent a very small portion of the electronics field as whole, and as such, electronics demonstrating extreme environment capability are quite sparse. Nevertheless, phase-locked loops have become such a ubiquitous circuit for so many electronic systems that a limited amount literature reporting radiation-hardened phase-locked loops is available. Most of this literature focuses on the most radiation-sensitive circuit blocks of a PLL, the VCO and the charge-pump, and as a result, literature reporting extreme environment

capable prescaler designs is even further limited. Therefore, we will examine general frequency dividers for extreme environment applications as well as PLLs for extreme environment applications.

One example of a radiation-hardened frequency divider is reported in [32]. The frequency divider described in [32] was developed and simulated on a 0.18-µm CMOS process, however, the design was not fabricated and no measurement data is available. This frequency divider is composed of cascaded divide-by-2 cells and control circuit logic. SEU mitigation within the latch circuits of this design is achieved by a latch that stores its output state at three nodes (*PDH*, *NDH*, *DH*) as opposed to the usual single node as shown in Figure 17. When an SEU event destroys the logic value at one of these nodes, the value is restored by the value at the remaining two nodes. This mitigation technique only prevents SEU-induced errors for single-event transients (SETs) induced within the latch cell itself.

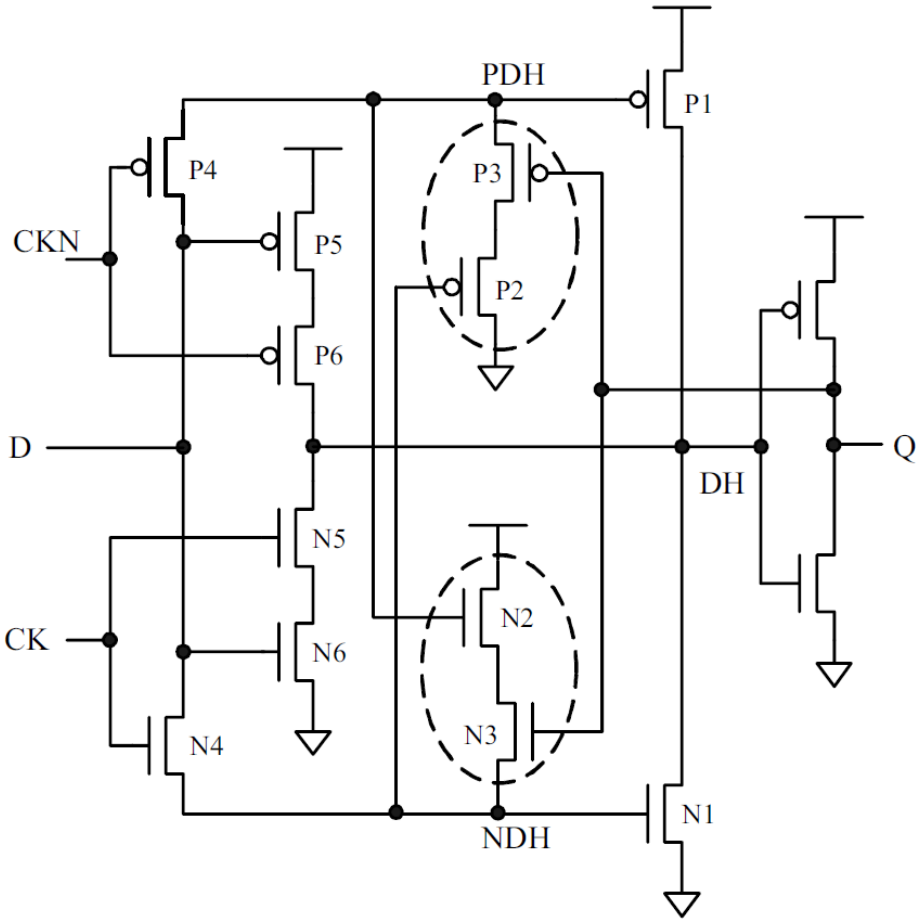

Figure 17. SEU-tolerant latch circuit proposed in [32]

A separate design technique is used in this frequency divider to mitigate SEUs induced by transients at the input to one of the divider stages. Each divide-by-2 cell is implemented with the two negative output signals (*QN* and *QN'*) of the slave latch fedback to the inputs of the master latch as shown in Figure 18. In this configuration, *QN* and *QN'* must change simultaneously due to an SET to induce an SEU within the divide-by-2 cell. The mitigation strategy relies on the improbability of both of the nodes changing state due to the same SET. This frequency divider also uses an enable signal to load the preset division ratio of the programmable divider. An SET on this enable signal can also induce an SEU on the frequency divider. Therefore, this design uses complementary enable signals (*EN* and $\overline{EN}$). As with the divide-by-2 output signals, both enable and its complement must change simultaneously to induce an SEU. For this reason, the enable signal and its complement must be generated via parallel paths to ensure that an SET does not induce an SEU on both signals simultaneously. The divide-by-2 cell is therefore tolerant to SETs by the use of redundancy. Redundancy is a common method of SEU mitigation in many digital cells. All SEU mitigation strategies that leverage redundancy come at the expense of an increase of required chip area (often by 2 to 4 times). This SEU mitigation strategy increases the required chip area by a factor of 1.8. Another limitation of this design is that no radiation hardening with respect to ionizing radiation is explored; this CMOS design uses TID radiation-sensitive NMOS devices.

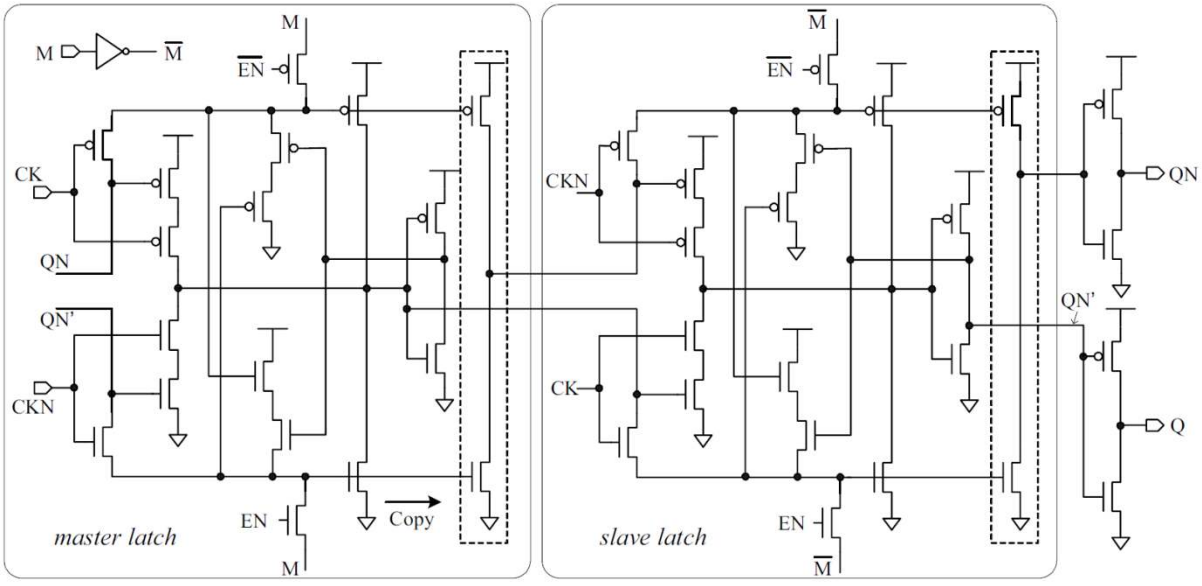

Figure 18. SEU-tolerant divide-by-2 cell of [32]

Another SEU tolerant frequency divider reported in literature is described in [33]. This frequency divider was developed and simulated using a 0.13-µm CMOS process and achieves a maximum operating frequency of 3.6 GHz. This frequency divider was not fabricated, and therefore, no measurement data is reported. This frequency divider is composed of cascaded divide-by-2 cells that operate asynchronously. The SEU mitigation strategy reported in [33] uses triple-modular redundancy (TMR) with error detection and correction. TMR is a common SEU mitigation strategy for digital circuits where three, redundant copies of a circuit are implemented. A majority vote of the three copies is carried out to determine the proper output. A single event upset induced on one of the three frequency dividers will be "voted out" by the other two copies. Due to the sequential nature asynchronous frequency dividers, an SEU on a bit of the state machine can cause an erroneous state that continues to propagate indefinitely. Eventually, an SEU could be induced in one of the two correctly-operating frequency dividers. If this occurs, the majority vote can no longer mask the erroneous state, and the SEU mitigation strategy fails. To combat this problem, the frequency divider of [33] incorporates an error correction circuit as seen in Figure 19. According to [33], the error correction circuit in Figure 19 counts and compares the number of rising edges of the three frequency dividers as well as the majority voter output. The number of rising edges of a given frequency divider being less than that of the majority vote usually implies that the given frequency divider has entered a faulty state that must be corrected. The error correction circuit will then reset the faulty counter to the correct state and the process continues. Because the error correction circuit itself is subject to SET-induced errors, the error correction circuit ignores the error the first time it is observed. When the error is detected a second time in succession, the error correction circuit resets the faulty frequency divider. The number of rising edges for a given frequency divider being greater than that of the majority vote usually implies that the output of the given frequency divider is corrupted by an SET, but the state of the frequency divider is unchanged. This type of SET-induced error will not propagate through-out the circuit operation, and the error correction circuit ignores this fault.

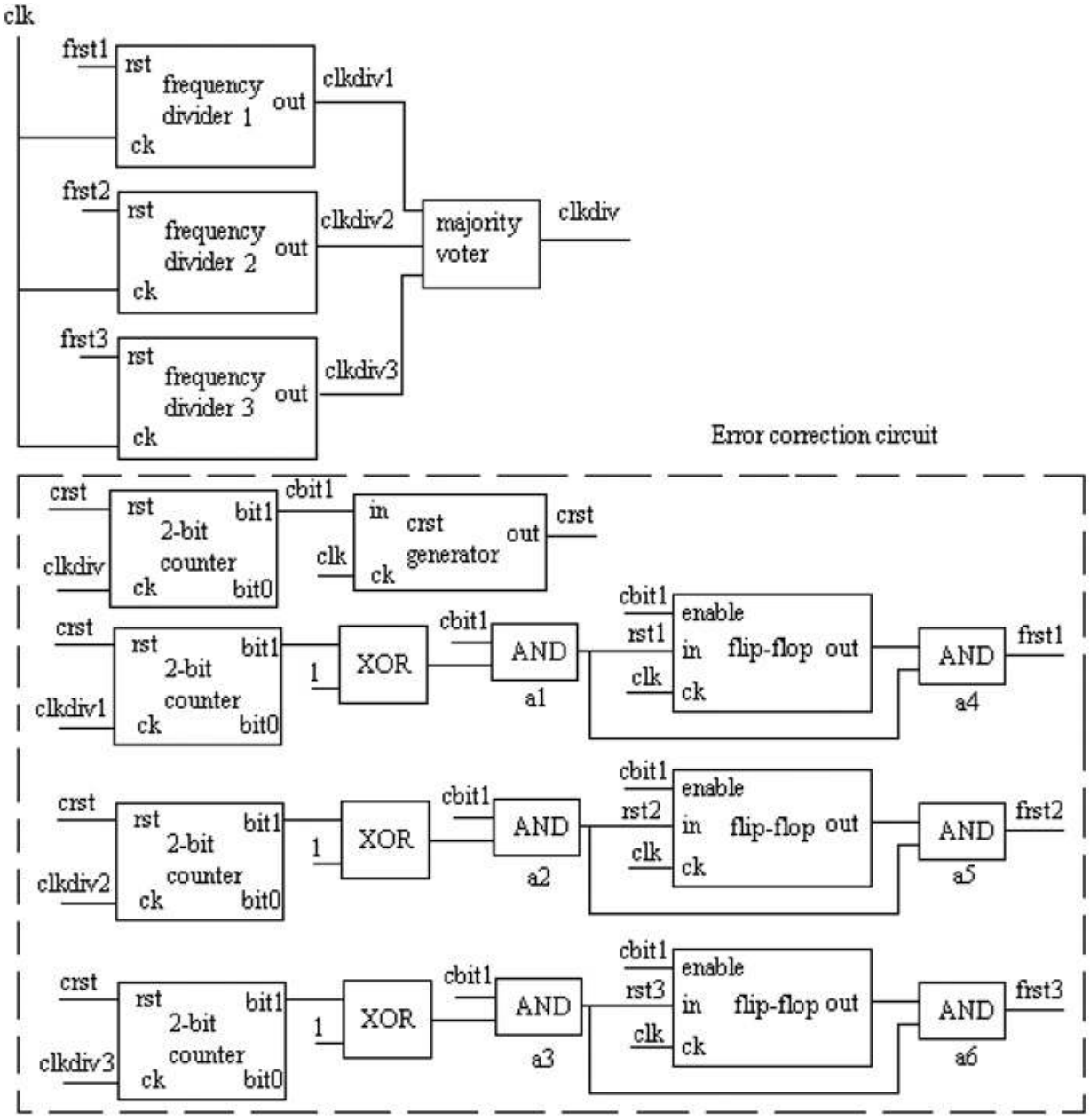

Figure 19. SEU-tolerant frequency divider of [33]

The state machine for the error correction circuit described in [33] is illustrated in Figure 20. One of the major drawbacks to TMR as an SEU mitigation strategy is the substantial chip area penalty required to implement such a scheme. The addition of the error correction circuitry described in [33] consumes even more chip area than TMR alone. While the frequency divider in [33] reports a very robust design in terms SEU mitigation, the frequency divider requires 3.5 times the chip area when compared to an unhardened frequency divider implementation. Moreover, this radiation-hardening scheme does not address the concerns of ionizing radiation. However, the concept of error detection and correction in [33] for state-based frequency dividers is a valuable concept that will be further examined in Chapter 4 of this dissertation.

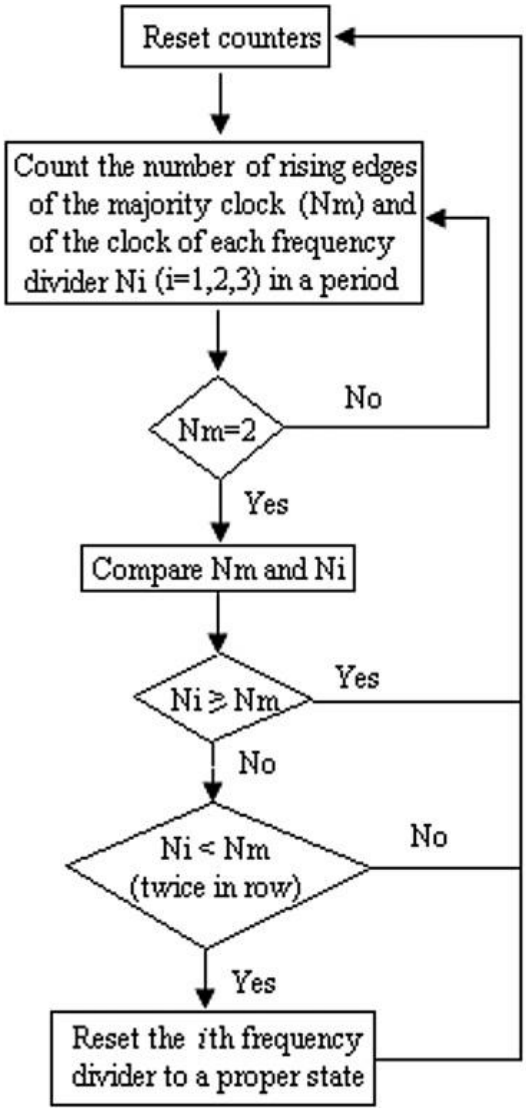

Figure 20. State machine of the error correction circuit of [33]

The patent of [34] describes a divide-by-1 to 8, programmable frequency divider developed for deep sub-micron CMOS implementation. This design is composed of 3 D-flip-flips and combinational logic and is capable operation in the GHz frequency range. The D-flip-flops of [34] are implemented with two pairs of complementary inputs and outputs. The combinational logic circuits of this design leverage the complementary outputs of the D-flip-flops in such a way that only one pair of complementary inputs to any D-flip-flop will be affected by a given SEU. The first part of the SEU-hardened D-flip-flop of [34] is composed of a radiation-hardened master latch with a clock input, complementary data inputs, complementary feedback signals, and complementary data outputs as shown in Figure 21. In this configuration, the master latch is immune to SEUs affecting at most one of the four complementary data inputs to the master latch. In a manner similar to the master latch of [34], a radiation-hardened slave latch is implemented with complementary data inputs, feedback signals, and data outputs as seen in Figure 22.

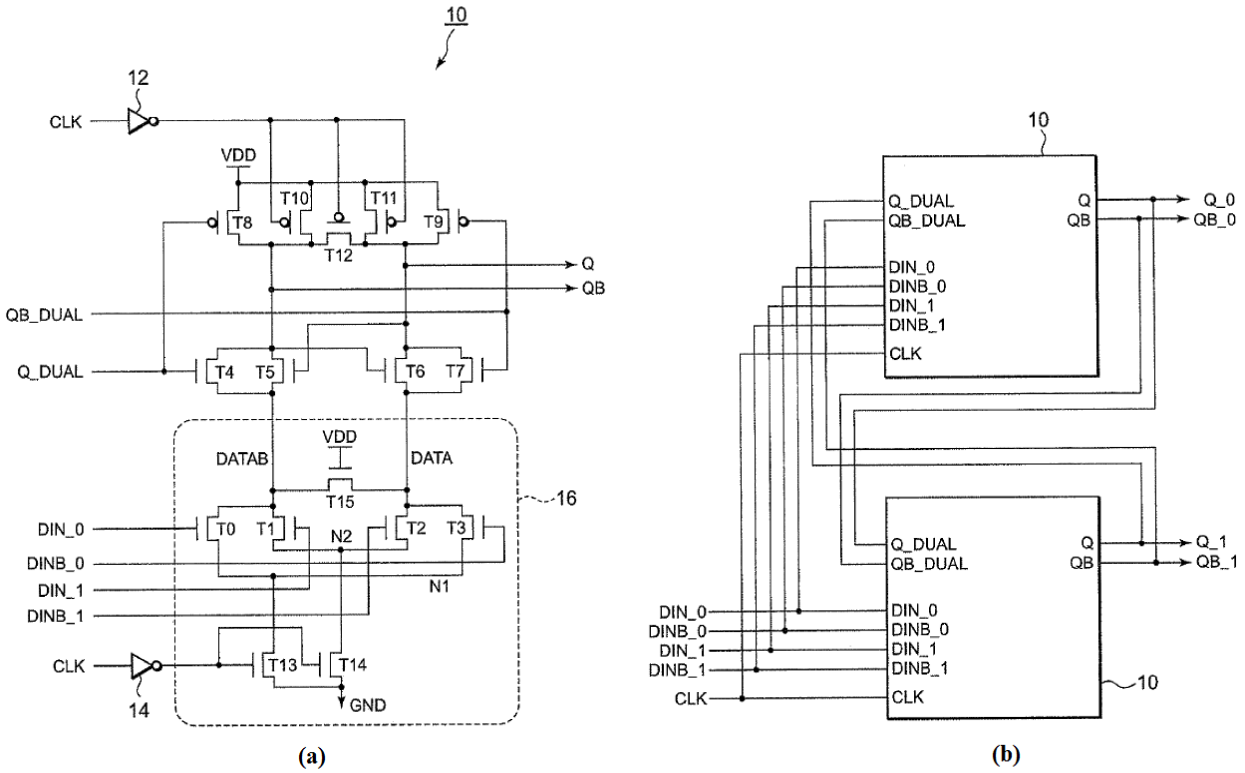

Figure 21. Radiation-hardened master latch of [34] (a) schematic of one half of master latch (b) diagram of master latch using two half circuits (a)

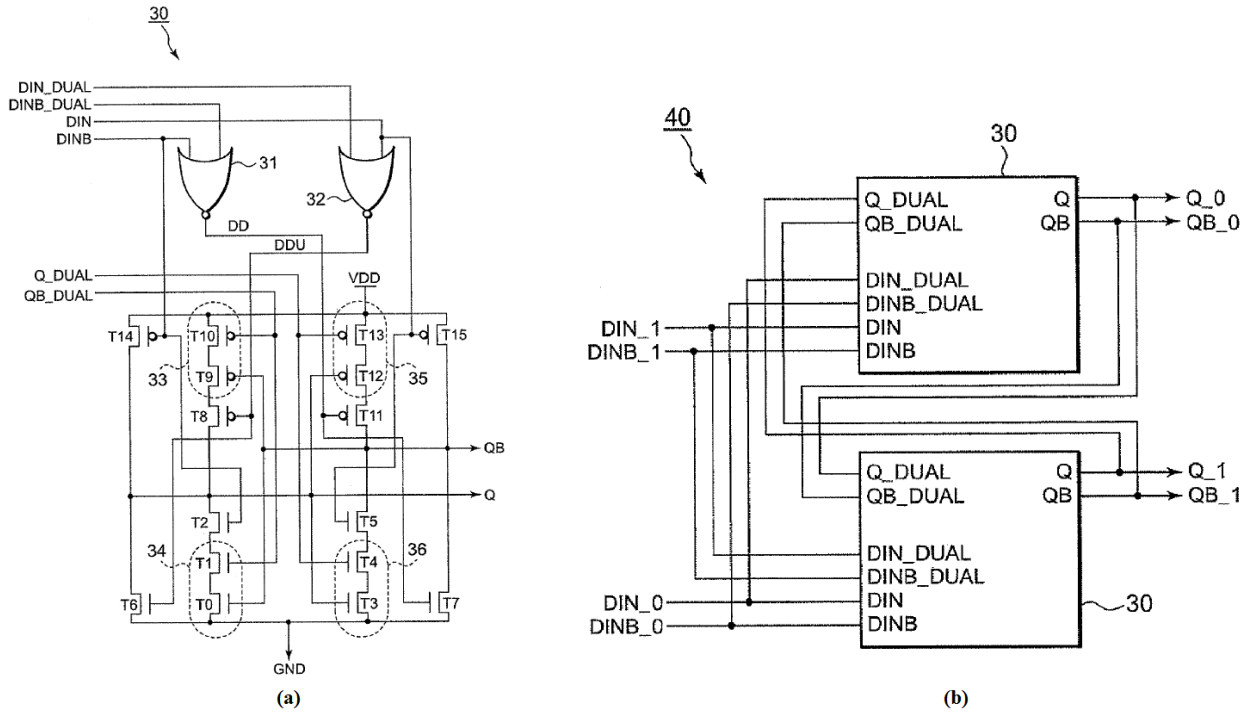

Figure 22. Radiation-hardened slave latch of [34] (a) schematic of one half of slave latch (b) diagram of slave latch using two half circuits of (a)

The concept of the radiation-hardened slave latch shown in Figure 22 is similar to that of the master latch. Operation of the slave latch is immune to a SEU affecting at most one of the four complementary data inputs to the slave latch. Due to the SEU mitigation of the master and slave latches, the D-flip-flop of [34] is immune to SEU affecting at most one of the four complementary data inputs to the slave latch or master latch. The described SEU mitigation strategy is similar that of [32], in that, redundancy within the latch circuits of the D-flip-flop is used to mask SEU errors induced on a single node. As mentioned previously, any SEU mitigation scheme using circuit redundancy is subject to a significant chip area penalty.

A radiation-hard, 2-3 GHz integer-N CMOS phase-locked loop has been demonstrated in [35] that shows only modest performance degradation for 100 kRad(Si) TID exposure. This paper also reports excellent SEE tolerance and temperature stability. To achieve this radiation tolerance, this design relied on the inherent radiation hardness of the 0.5-µm silicon-on-sapphire (SOS) process on which it was developed. This process uses local oxidation of silicon (LOCOS) for transistor isolation, thin gate oxide, lightly-doped drains, and other techniques for radiation-hardening by process. A major drawback to this design is that the ionizing radiation hardness of

this process is achieved mainly by the use of thin gate oxide. Reducing the gate dielectric thickness of an NMOS device does allow the device to tolerate a higher radiation dose, but the NMOS device is still potentially sensitive to TID radiation, and designs leveraging the NMOS device will be subject to its limitations.

Several other papers have been published reporting radiation hardened phase-locked loop designs implemented on an SOS-CMOS process, [36] – [39]. SOS-CMOS technology is known for its inherent SEE immunity compared to bulk-CMOS technology, but fabrication on SOS-CMOS is drastically more expensive than bulk-CMOS fabrication. Additionally, the NMOS device in SOS-CMOS is still a concern with respect to TID radiation. Silicon-on-insulator (SOI) technology (with the insulator usually being SiO_2) is a generalized version of SOS and also possesses inherent immunity to SEE. Several papers have been published reporting radiation-hardened by process phase-locked loops developed on SOI-CMOS technology including [40]. One paper, [41], describes a radiation-hard phase-locked loop developed on an SOI-BiCMOS technology. This PLL design reports no significant performance degradation for TID irradiation up to 10 MRad(Si).

3.6 Limitations of prescaler prior art

After reviewing the state of the art of high-speed, wide-ratio, extreme environment capable prescalers and frequency dividers, we can see that no design encompasses all of the requirements of the prescaler targeted for this research work. Most of the literature available on prescaler design uses some version of dual-modulus prescaler topology, which, as explained previously, does not lend itself to narrow division resolution over a low range of moduli. Many of the prescaler designs examined are implemented with TID-sensitive CMOS technology that precludes their implementation for this research work. Other designs may be able to provide the division range required, but are not capable of the 5 GHz operating frequency required for this research work. However, valuable insights to prescaler design can be found in the literature presented in Chapter 3, and many of the concepts outlined in this literature were used to develop a novel prescaler design that meets all of the design requirements presented in Chapter 2.

CHAPTER 4: DESIGN OF THE MULTI-MODULUS PRESCALER

4.1 Prescaler design approach

Many of the design approaches and insights explored in Chapter 3 were leveraged in the design of the prescaler of this research work; however, a novel design approach was required to meet all of the design requirements of this research work. The fabrication process for this research work was chosen to be a 180-nm SiGe BiCMOS process. As examined in Chapter 3, SiGe BiCMOS technology offers several, distinct advantages over bulk-CMOS in terms of ionizing radiation hardness, wide-temperature capable operation, and the availability of the high-speed HBT that justify the choice of technology. High-speed, digital design for this prescaler leverages the HBT device in a CML structure. As explored in Chapters 2 and 3, CML logic is capable of much higher operating frequencies than CMOS logic and other logic types. To meet the project requirement of a configurable prescaler capable of dividing by narrowly-spaced moduli from 16 to 48, a cascade of multi-modulus dividers is used to form the multi-modulus prescaler. Chapter 3 explains how this structure allows for narrowly-spaced moduli over a low range of divisors. The remainder of Chapter 4 outlines the design approach used to develop a novel multi-modulus prescaler design to meet the demanding requirements of the extreme environment capable frequency synthesizer system described in Chapter 2.

4.2 Multi-modulus prescaler functional description

Synchronous frequency division requires more cells to operate at high-frequency (and therefore increased power consumption) when compared to asynchronous division; however, synchronous division results in less jitter accumulation at the divider output [3]. For precision clock generation such as the focus of this research work, minimizing jitter (and consequently phase noise) is of the utmost importance. To this end, this prescaler design is composed of two cascaded, synchronous, multi-modulus divider cells. To reduce power consumption, the first divider cell is composed of as few cells as possible. A consequence of this design choice is that a limited number of moduli are available for the first divider; this restricts the input frequency variation of the second divider allowing for more optimal design. The majority of the resolution capability comes from the second, low-speed frequency divider. Figure 23 illustrates the prescaler design achieved by cascading a 4/5/6 modulus divider with a 3.5-8 modulus divider.

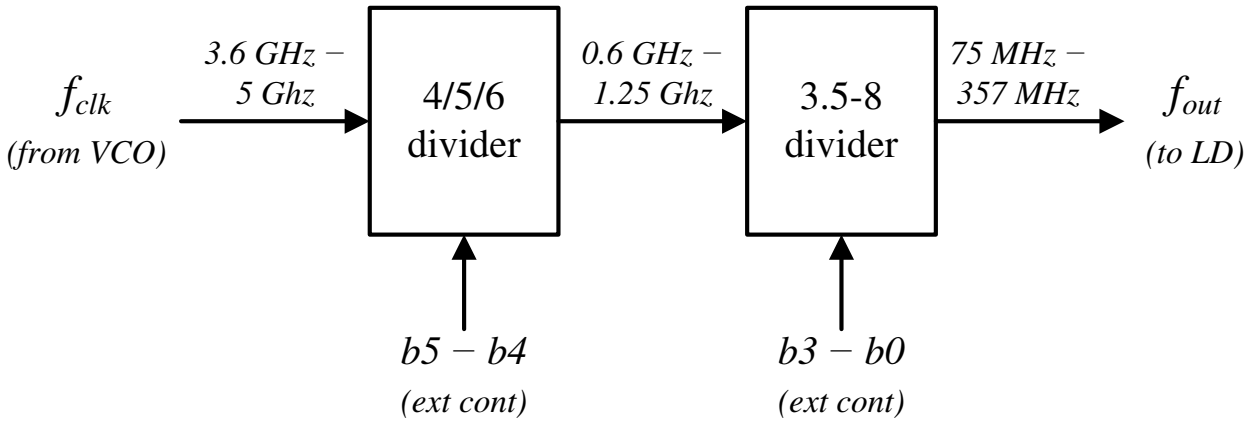

Figure 23. Multi-modulus prescaler block diagram with external control bits b5 - b0

The result shown in Figure 23 is a prescaler design capable of dividing by moduli between 14 and 48 with a total of 28 configurable moduli. This achieves the division range and resolution required of this prescaler for integration within the frequency synthesizer ASIC. External control bits *b5* and *b4* are used to configure the modulus of the 4/5/6 divider and *b3 – b0* are used to configure the modulus of the 3.5-8 divider. The 4/5/6 divider must be able to operate at clock frequencies over the full VCO tuning range, 3.6 to 5 GHz. The 3.5-8 divider must be capable of operating at input frequencies from 600 MHz to 1.25 GHz. The defined VCO tuning range and range of prescaler moduli result in a prescaler output frequency range of 75 to 357 MHz, which exceeds the requirements outlined in Chapter 2. The prescaler solution in Figure 23 is a simple approach that allows for robust, low-jitter, reliable prescaler design for frequency synthesizers in extreme environments. The remaining challenge for this prescaler design is the development and verification of these two synchronous divider cells.

4.2.1 4/5/6 divider design

Synchronous dividers, like the 4/5/6 divider of this prescaler, implement edge-triggered D-flip-flops (DFFs), with combinational logic and external control to achieve the desired functionality. For synchronous operation, the DFFs of these dividers are clocked from a common signal. In contrast, asynchronous dividers clock each DFF from the output of the DFF of the previous stage. The result for asynchronous dividers is that propagation delay accumulates through each divider stage, which results in each stage transitioning at slightly different times. An external event occurring close to a transition between states (some but not all DFFs have changed state) could induce a bit error into the divider. This problem is of particular

concern for extreme environment applications where single-event effects are a noted concern. Synchronous divider operation eliminates the propagation delay between DFFs associated with asynchronous dividers. In a synchronous divider, all DFFs transition simultaneously which reduces the time window of vulnerability of the divider. The 4/5/6 divider design is composed of DFFs, multiplexers, and combinational logic gates as shown in Figure 24. For the moment, the error correction circuit and DFF reset signal of Figure 24 can be ignored. The 4/5/6 divider of Figure 24 functions by allowing two static control bits, *b5* and *b4*, to control the signal path between the DFFs. This controllability is achieved by using two multiplexers to control the signal flow between the DFFs of the divider. Assume *b5* is LOW and *b4* is HIGH. In this condition, the multiplexer controlled by *b5* feeds $\overline{Q_1}$ to the input of the first DFF. Because the multiplexer controlled by *b4* feeds Q_1 to the input of the last DFF, Q_2 will simply follow Q_1, but delayed by one clock cycle. The end result is a synchronous, divide-by-4 circuit as seen in Figure 25(a). Now assume *b5* is HIGH and *b4* is LOW. Here, the multiplexer controlled by *b5* feeds $\overline{Q_2}$ to the input of the first DFF, and the multiplexer controlled by *b4* feeds the output of the AND gate to the input of the last DFF.

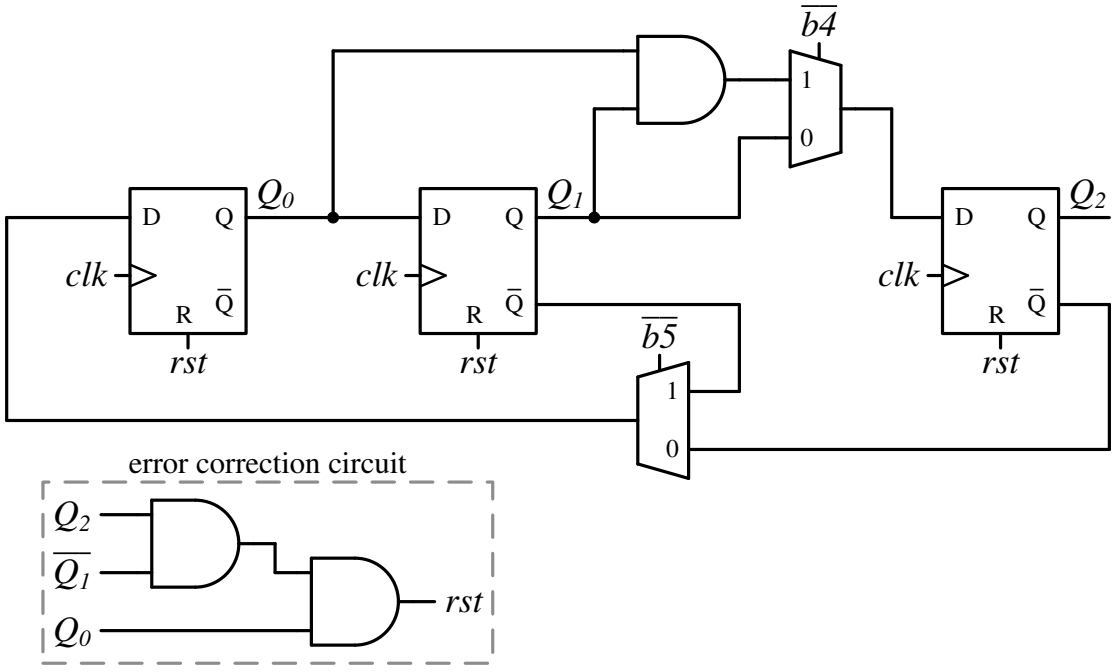

Figure 24. 4/5/6 divider block diagram

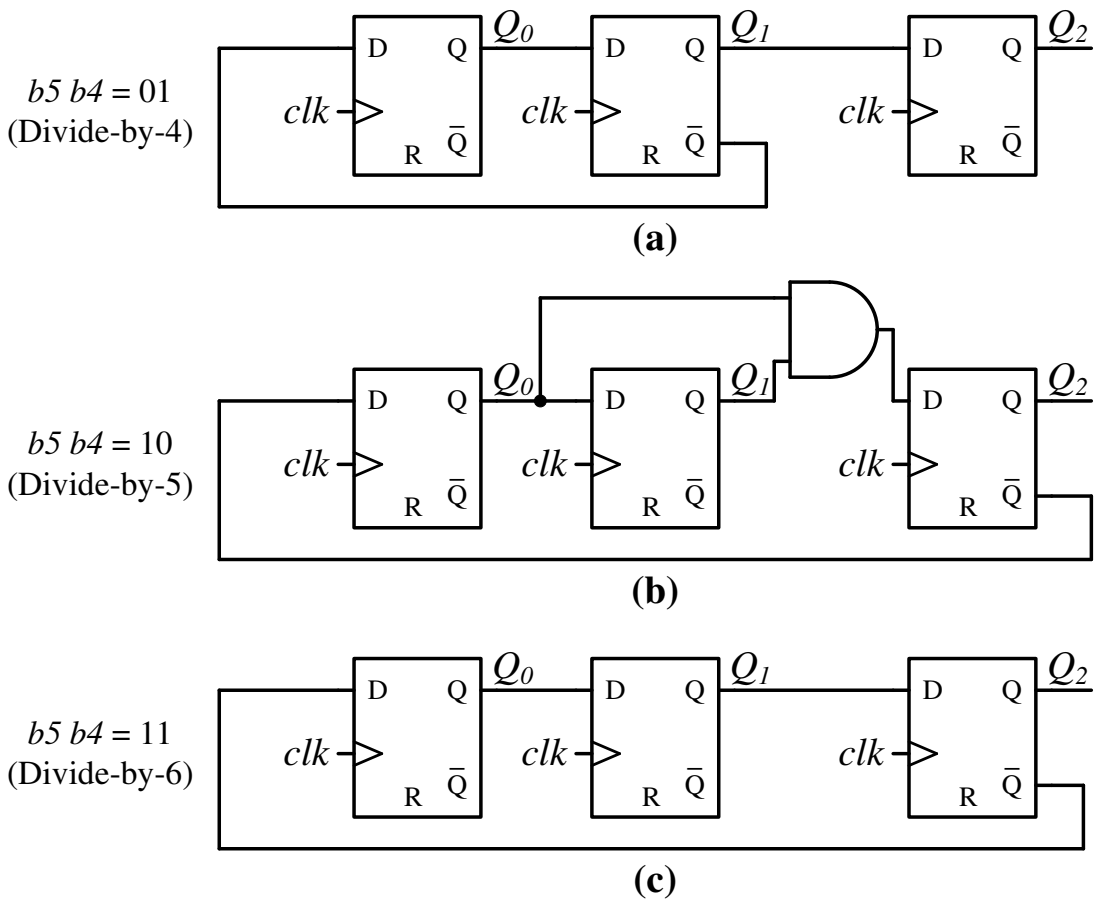

Figure 25. 4/5/6 divider diagram for (a) divide-by-4, (b) divide-by-5, and (c) divide-by-6 configurations (simplified)

The resulting circuit is a divide-by-5 circuit as represented in Figure 25(b). Lastly, with *b5* and *b4* HIGH, the multiplexer controlled by *b5* feeds $\overline{Q_2}$ to the input of the first DFF, and Q_1 feeds the input of the last DFF. This three DFF circuit is illustrated in Figure 25(c) and performs the desired divide-by-6 function. The output of the 4/5/6 divider is taken from a buffered Q_2 signal. The output for the 4/5/6 divider was taken from the last DFF to ensure comparable loading conditions for all divider configurations.

To verify the operation of the 4/5/6 divider for each configuration in Figure 25, the state tables must be examined. The state tables for each of the moduli of the 4/5/6 divider are outlined in Table 4.

Table 4. 4/5/6 divider state tables for each configuration

	Divide-by-4 (*b5 b4* – 01)			**Divide-by-5 (*b5 b4* – 10)**			**Divide-by-6 (*b5 b4* – 11)**		
	Present State	Next State		Present State	Next State		Present State	Next State	
	$Q_2Q_1Q_0$	$Q_2Q_1Q_0$	Out	$Q_2Q_1Q_0$	$Q_2Q_1Q_0$	Out	$Q_2Q_1Q_0$	$Q_2Q_1Q_0$	Out
1	000*	001	0(1)	000	001	0	000	001	0
2	001	011	0	001	011	0	001	011	0
3	011	110	0	011	111	0	011	111	0
4	110	100	1	111	110	1	111	110	1
5	---	---	-	110	000	1	110	100	1
6	---	---	-	---	---	-	100	000	1

* For the divide-by-4 case, states 000 and 100 are equivalent because state table is independent of Q_2, state 000 only occurs when counter is initiated

Observing the state tables of Table 4, we can see that the desired functionality for the 4/5/6 divider is achieved. For the divide-by-4 case, the counting sequence is provided by the first two DFFs and the last DFF follows the second DFF with one clock cycle delay. For the divide-by-5 case, an AND gate allows the counting sequence to increment sequentially, but when the counting sequences decrements, the 100 state is skipped. This pulse-swallowing technique allows the 4/5/6 divider to be configured for odd moduli as observed in Table 5. For the divide-by-6 case, the AND gate output is not used, and no pulse-swallowing occurs. Here, the divider cycles through every state resulting in a division of the clock signal by a factor of 6.

The previous discussion was carried out assuming that the divider is initiated to the 000 state at the beginning of operation. This condition cannot be guaranteed, however. Moreover, we cannot guarantee that the 4/5/6 divider will remain in the states listed in Table 4. The divider could initiate to (e.g. at start-up) or be induced by a disturbance (a single event or other disturbance) to a faulty state. For the remainder of this dissertation the term "faulty state" will be used to refer to any state not appearing in the state table of a correctly operating, configured divider. For a divider composed of three DFFs, eight total states are possible. The 4/5/6 divider

uses at most six of these states. We must now ask the question, what happens if the divider enters one of these faulty states? The states 010 and 101 do not appear in Table 4 for any of the three configurable moduli. Also, for the divide-by-4 case, the state 111 does not appear in Table 4; for the divide-by-5 case, the state 100 does not appear Table 4. Table 5 summarizes these faulty states and the subsequent state for each. For the divide-by-4 case, Table 5 shows that the subsequent state for each of the three possible faulty states is a correct state for the divide-by-4 configuration. In other words, the 4/5/6 divider will automatically correct any faulty state for the divide-by-4 configuration, and no error correction is required. For the divide-by-5 case, the subsequent state for both 010 and 100 are correct states of the divide-by-5 configuration; the subsequent state for 101 is the faulty state 010, however this state leads to a correct state as previously mentioned. As with the divide-by-4 configuration, the divide-by-5 configuration of the 4/5/6 divider will automatically correct any faulty state and no intervention is required. Lastly, for the divide-by-6 configuration we have two faulty states, 010 and 101. The subsequent state for each of these faulty states is in fact the other faulty state. If the 4/5/6 divider, configured to divide-by-6, enters either of these two states, the 4/5/6 divider will remain in this erroneous operation indefinitely. The result is that the 4/5/6 divider will provide divide-by-2 functionality as opposed to the configured, divide-by-6 operation. For reliable operation over time, this erroneous behavior must be detected and corrected.

Table 5. Faulty states for each configuration of the 4/5/6 divider

Divide-by-4			**Divide-by-5**			**Divide-by-6**	
Present State	Next State		Present State	Next State		Present State	Next State
$Q_2Q_1Q_0$	$Q_2Q_1Q_0$		$Q_2Q_1Q_0$	$Q_2Q_1Q_0$		$Q_2Q_1Q_0$	$Q_2Q_1Q_0$
010	**100**		**010**	**001**		**010**	**101**
101	**011**		**100**	**000**		**101**	**010**
111	**110**		**101**	**010**		n/a	n/a

faulty state
correct state
faulty state leading to correct state

For the remainder of this dissertation, the term "erroneous state" will be defined as a faulty state that is not auto-correcting and forms a closed, erroneous state table. Because one erroneous state of the divide-by-6 configuration leads to the other erroneous state, all erroneous 4/5/6 divider operation can be corrected by checking for only one the two erroneous states. Referring back to Figure 24, the realization of an error correction circuit capable of correcting this erroneous operation is visible. The combinational logic of the error correction circuit monitors the DFF outputs for the state 101, and once detected, all DFFs are reset to 0. This simple error correction circuit is able to correct for any erroneous divider operation with minimal increase to design complexity, chip area, and power requirements. The error correction circuit is able to correct any error within two clock cycles. The fast recovery from erroneous operation of the 4/5/6 divider meets the requirement from Chapter 2 that the prescaler recovers "quickly and gracefully" from any single-event upset (or other error-inducing disturbance). An SEU induced within the error correction circuit itself could potentially result in a 4/5/6 divider reset when the divider was in fact operating correctly. However, even if an unnecessary reset was induced, the 4/5/6 divider DFFs are reset and returns to normal operation just as if the error occurred within the divider itself.

4.2.2 3.5-8 divider design

The output of the 4/5/6 divider is subsequently used to clock a second synchronous divider, the 3.5-8 divider. To achieve half-bit division resolution, the 3.5-8 divider is realized using double-edge triggered (DET) DFFs. These DET DFFs along with combinational logic and multiplexers can be used to design the 3.5-8 divider as demonstrated in Figure 26. The error correction circuit and DFF reset signal can be ignored for the moment. The 3.5-8 divider is constructed in a manner very similar to the 4/5/6 divider. Multiplexers are used to control signal flow between the DFFs. The half-bit resolution is accomplished by a pulse-swallowing method similar to that seen in the 4/5/6 divider. In Figure 26, control bits *b3-b0* are set externally and control the division ratio of the 3.5-8 divider.

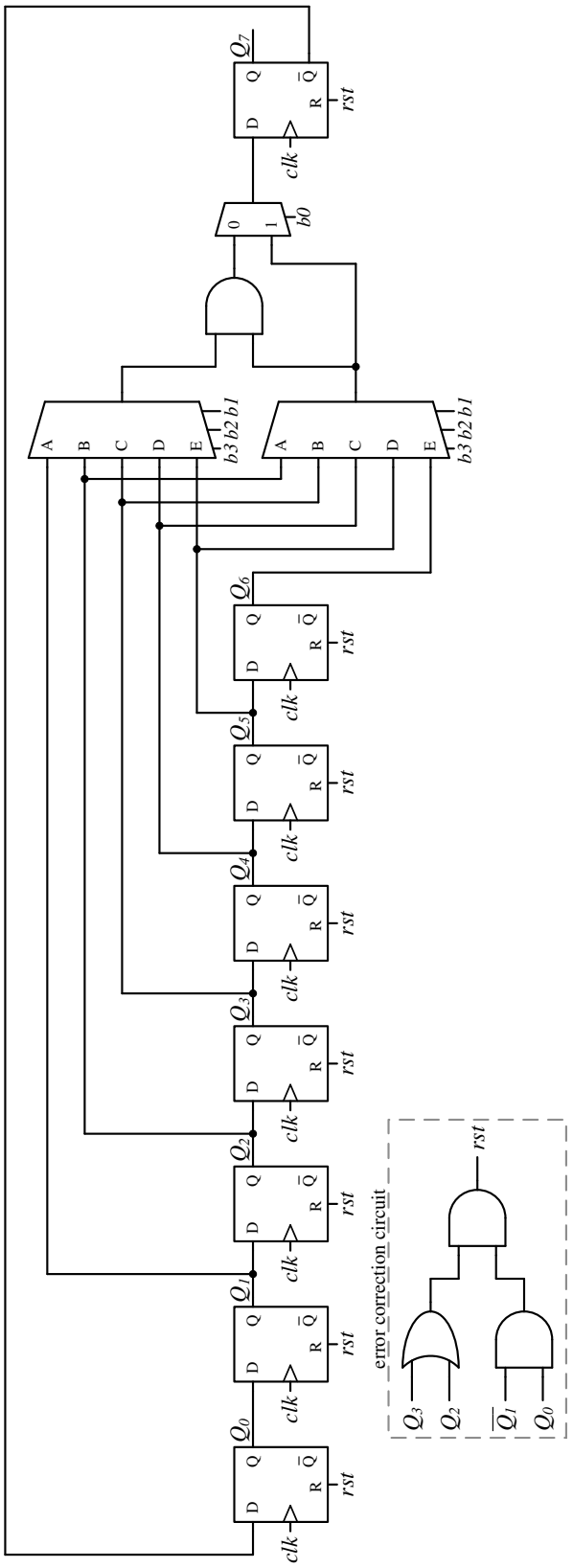

Figure 26. 3.5-8 divider block diagram

Consider the case where the control bits, *b3-b0*, are set to 0000. In this case, the A input of both 5-input multiplexers and the 0 input of the 2-input multiplexer will be taken as the multiplexer outputs. Figure 27(a) shows the simplified diagram for the described configuration. Remembering that each DFF in the 3.5-8 divider is triggered on both clock edges, it is evident that the configuration of Figure 27(a) results in division-by-3.5. Now, consider the case where *b3-b0* are set to 0001. In this case, the A input of both 5-input multiplexers and the 1 input of the 2-input multiplexer are taken as the output. This configuration is illustrated in Figure 27(b) and results in a divide-by-4 operation. The divide-by-4.5 configuration, Figure 27(c), is very similar to the divide-by-3.5 configuration except for an additional DFF. The functionality of the 3.5-8 divider can be described as follows: the least significant control bit, b0, determines if ½ bit division occurs via the pulse-swallowing AND gate.

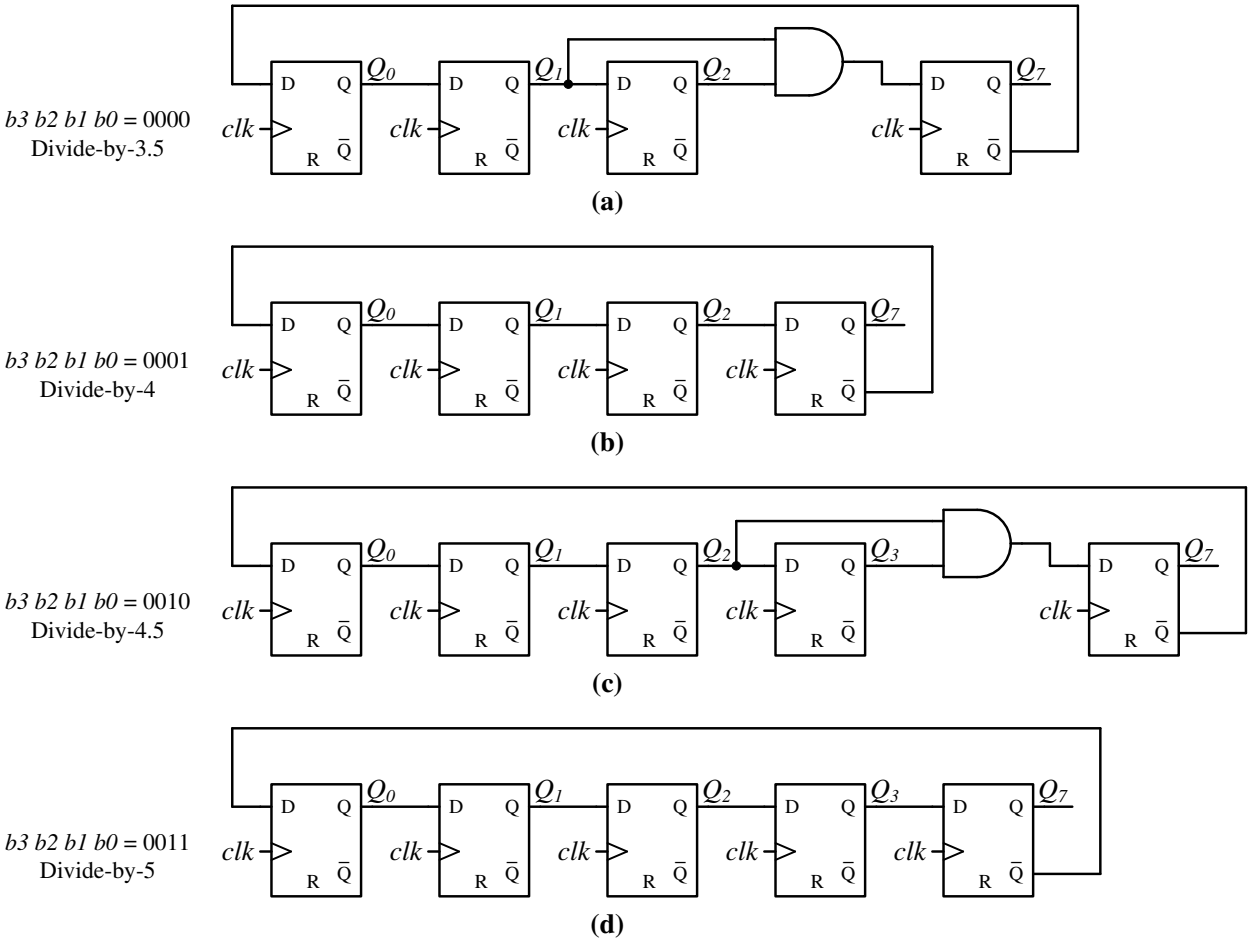

Figure 27. 3.5-8 divider diagram for (a) divide-by-3.5, (b) divide-by-4, (c) divide-by-4.5, and (d) divide-by-5 configurations (simplified)

The remaining three control bits, b3-b1, add a DFF to the divider chain each time the divider control bit word is incremented. As was the case with the 4/5/6 divider, the possible faulty states of the 3.5-8 divider must be examined. The increased complexity of the 3.5-8 divider leads to significantly more faulty states than observed in the 4/5/6 divider analysis. As the modulus of the 3.5-8 divider increases, the amount of possible faulty states for the 3.5-8 divider increases. The analysis of all possible faulty states for each configuration of the 3.5-8 divider is too lengthy to include in this dissertation, so a qualitative description of this analysis is provided.

For each division configuration of the 3.5-8 divider, the following procedure was performed via a Matlab script. The state table for correct divider operation is generated. A list of all possible faulty states is compiled. For each of these faulty states, the subsequent state is calculated. These faulty states are then arranged into faulty state tables. In some cases, these faulty state tables lead to the correct state table, and all faulty states within that table are auto-correcting and do not require intervention from the error correction circuit. The problematic states are those that form closed loops and result in an erroneous state table.

Table 6. Divide-by-4.5 configuration example of faulty and erroneous state analysis

Correct state table	Faulty state table	Erroneous state table
00000	00010	00110
00001	00101	01101
00011	01011	11011
00111	00111	00110
01111	Correct state Faulty state Erroneous state	
11111		
11110		
11100		
11000		
00000		

Only the faulty states present in an erroneous state table must be monitored for and corrected by the error correction circuit. As an example, the divide-by-4.5 configuration will be examined. The correct state table for the divide-by-4.5 configuration is shown in the left column of Table 6. One example of an auto-correcting faulty state is illustrated by beginning with the state 00010. The second column of Table 6 shows that this faulty state passes through two more faulty states before reaching a correct state. Therefore, all three faulty states in the second column will occur only once before the error is automatically corrected. In contrast, the erroneous state table seen in the third column is a closed state table. If the 3.5-8 divider is induced to any of the states seen in the third column of Table 6, the divider will remain in this erroneous operation, indefinitely. These erroneous states must be monitored for and corrected when observed. The complete list of erroneous states for all 3.5-8 divider configurations is far too long for the error correction circuit to monitor for every erroneous state. For example, the divide-by-8 configuration alone consists of 240 erroneous states across 15 erroneous state tables. Because each erroneous state table forms a closed loop, a much more efficient approach is to monitor for only one erroneous state in each erroneous state table. The efficiency of the error correction circuit can be further improved by finding commonality between the erroneous state tables. Because the 4 LSBs of the 3.5-8 divider are used in every divider configuration (not the case for the 4 MSBs), monitoring these 4 bits alone is necessary and sufficient (and therefore the minimal solution) to provide error correction for all divider configurations. A Matlab script was written to search for commonality and find the minimum number of bit sequences that can be monitored and successfully detect all erroneous state tables. At least one state in each erroneous state table was found to contain at least one of these three bit sequences for the four LSBs: 0101, 1001, and 1101. None of these three bit sequences appear in any of the correct state stables for any of the 3.5-8 divider configurations, so monitoring these sequences will not corrupt any of the correct state tables. The resulting solution is the simple error correction circuit seen in Figure 26. This error correction solution contributes minimal complexity and does not affect normal operation for any divider configuration. The maximum recovery time for an erroneous state of the 3.5-8 divider is dictated by the longest erroneous state table of the 3.5-8 divider. This occurs for the divide-by-8 configuration where all state tables are composed of 16 states. Therefore, the maximum recovery time from an induced error of the 3.5-8 divider will be 16 clock cycles where the clock is the output of the 4/5/6 divider.

4.3 Prescaler 4/5/6 divider cell development

Now that high-level designs of the 4/5/6 and 3.5-8 dividers have been developed, we turn our attention to the development of the cells to be used in these dividers. The main building block of the 4/5/6 divider is the DFF. To achieve the high operating frequency required of the 4/5/6 divider, the DFF of the 4/5/6 divider is implemented with current-mode logic using the high-speed SiGe *npn*-HBT device. The 4/5/6 divider design of Figure 24 also requires the development of an AND gate and a multiplexer. The design of these supplemental cells will follow the design DFF. The same differential logic voltage, bias current, and collector resistor will be used in all cells of the 4/5/6 divider, with only structural changes made to realize different functionality.

To minimize the area and power consumption of the 4/5/6 divider, minimum-sized HBTs (1 µm x 0.24 µm emitter area) were used for all cells of the 4/5/6 divider. Many different techniques have been reported in literature for estimating propagation delay in CML structures for designs using bipolar devices [42]-[45] as well as CMOS devices [46]. Many of these publications aim to minimize propagation delay by optimizing device geometry, resistor size, and bias current. Rather than minimizing propagation delay as is the aim in many designs [43], [45], and [46], the goal of the 4/5/6 divider for this dissertation is to achieve 5 GHz operation over a very wide temperature range (−180°C to 125°C). Since the HBT device geometry is minimized for all cells of the 4/5/6 divider, the two remaining design choices for the development of these cells is the choice of resistor size and bias current. As reported in [44], biasing CML latches to only 40% of the peak unity gain-bandwidth (f_T) of the device, allows these structure to achieve ~ 80% of their maximum speed corresponding to the peak f_T. Below the 40% maximum f_T benchmark, CML latch delay increases sharply. The optimal range for biasing CML latches in terms of power/speed tradeoff is in the range of 40% to 60% of the peak f_T [44]. The technology specification manual for the 180-nm SiGe BiCMOS process used for this design states a peak f_T of the HBTs for emitter current densities of 1.65 mA/µm^2. Therefore, the peak f_T of the 0.24 µm^2 HBT used in this design is achieved for an emitter current of ~ 400 µA. To optimize power/speed tradeoff while leaving margin for variation over temperature, 50% peak f_T (200 µA) was used for the emitter current of the 4/5/6 divider cells. Recalling {3.11} from Chapter 3, the differential logic level is set by the bias current and resistor size of the CML structure. For noise immunity and to ensure complete current steering, the differential logic level

of the 4/5/6 divider was chosen to be 200 mV. This logic level provides a room temperature CML current ratio of over 2000 and a worst case (125°C) current ratio of over 330. With the emitter current and differential logic voltage chosen, the required resistor size is 1 kΩ.

4.3.1 4/5/6 divider DFF

The realization of the CML DFF of the 4/5/6 divider is composed of a master and slave latch as shown in Figure 28. The function of the 4/5/6 divider DFF can best be understood by analyzing the function of the master latch. Current-mode logic is, in essence, a cascade of current-steering differential pairs. The concept of CML hinges on the assumption that all bias current is steered through only one branch of a given differential pair at a time; this assumption will be validated later in this chapter. When *clk* switches LOW, all bias current of Q_3 flows through Q_4 and no current flows through Q_5. If the D input is HIGH, then all current will flow through Q_6 and none through Q_7. During the time *clk* is LOW, any input to D will appear as an inversion at the base of Q_{11}. In this state, the base of Q_{12} is at V_{CC}, and the base of Q_{11} is at V_{CC} minus the voltage drop across R_2. So, the voltage at the base of Q_8 is higher than at Q_9. When *clk* switches HIGH, all bias current of Q_3 flows through Q_5 and no current flows through Q_4. Since the base of Q_8 is at a higher voltage than Q_9, all bias current will flow through Q_8 and no current will flow through Q_9. Therefore, when *clk* switches from LOW to HIGH, the data at the D input is stored at the base of Q_8.

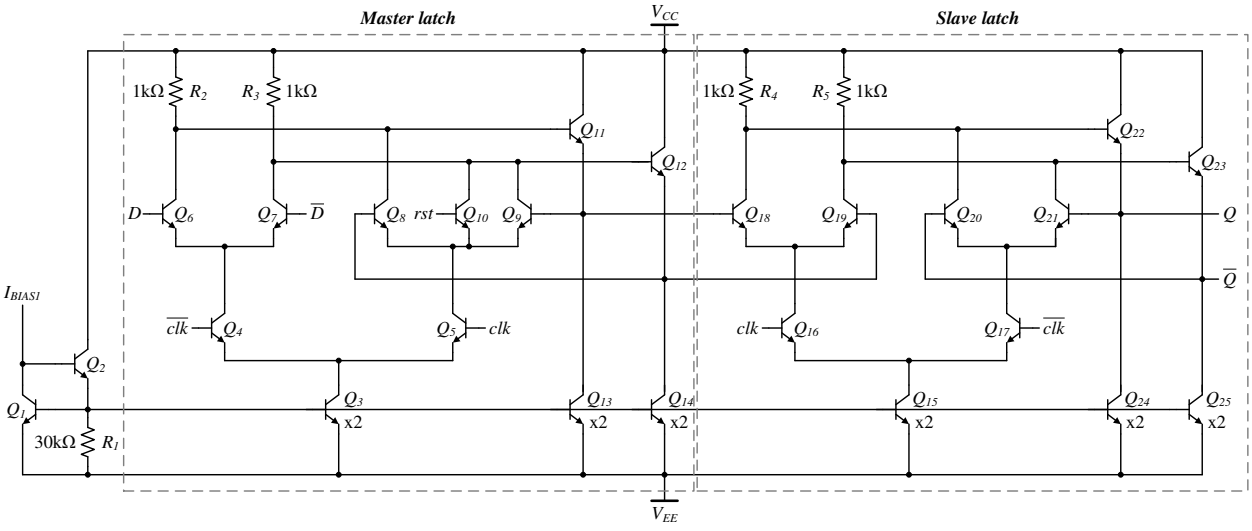

Figure 28. DFF of 4/5/6 divider (all bipolars – npn-HBTs of 1 µm x 0.24 µm emitter area, all resistors – polysilicon type, I_{BIAS1} = 100 µA)

This data will remain stored until *clk* switches from HIGH to LOW. By cascading the master latch with a slave latch with inverted *clk* signals, data is transferred from the master latch to slave latch only when *clk* transitions from LOW to HIGH. Essentially, the master latch stores the data at the *D* input while *clk* is LOW, and the slave latch samples the stored data when *clk* is HIGH. The result is a storage element whose output only changes state during a rising clock edge, a positive-edge triggered DFF.

4.3.2 4/5/6 divider combinational logic

In addition to the DFF, the 4/5/6 divider development also requires the design of CML AND gate and multiplexer. These gates must be able to operate at 5 GHz and have the same logic levels as previously discussed for the DFF design. Therefore, the device sizing and biasing choices defined for the DFF are carried over to the other cells of the 4/5/6 divider. The same cascade structure seen in the DFF of the 4/5/6 divider can be arranged to realize an AND function as demonstrated in Figure 29. The function of the 4/5/6 divider AND gate can be described as follows. When *A* and *B* are both LOW, the bias current of Q_7 will be forced through Q_9 and through Q_{12}. The voltage drop induced across R_3 pulls the base of Q_{15} LOW and results in the output *O* being pulled LOW. If A is HIGH and B is LOW, the bias current of Q_7 will now be forced through Q_8 and through Q_{11}. The bias current still induces a voltage drop across R_3, so the output will be LOW in this case as well. With A held LOW and B held HIGH, the bias current will be forced through Q_9, then through Q_{13}. Just as with the other two cases, the bias current is forced through R_3, which results in *O* being pulled LOW. Only when both A and B are HIGH will the bias current be forced through Q_8 and Q_{10} and a voltage drop will be induced across R_2. With no voltage drop across R_3, the output *O* will be HIGH. The described functionality is the sought CML AND gate. Note that by simply interchanging the outputs, the AND gate becomes a NAND gate. In fact, any CML gate inherently provides its complement with no additional overhead in terms of chip area, power, or design time.

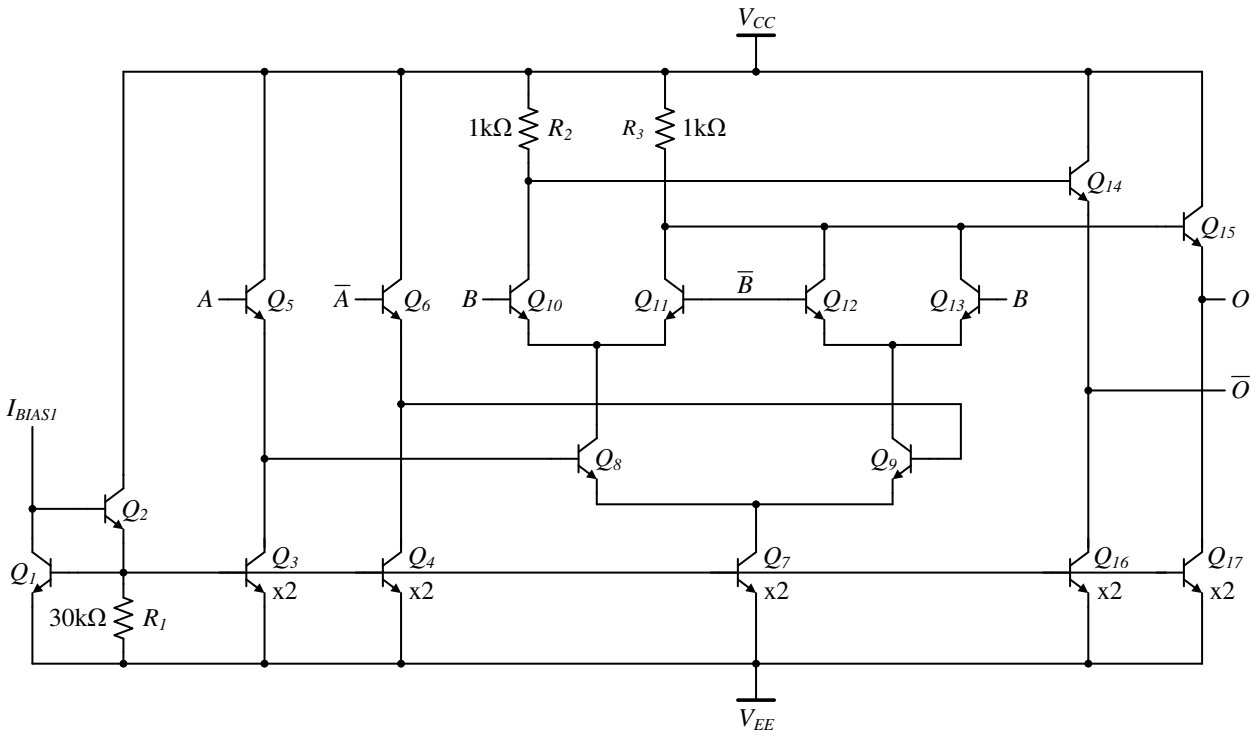

Figure 29. AND gate of 4/5/6 divider (all bipolars – npn-HBTs of 1 µm x 0.24 µm emitter area, all resistors – polysilicon type, I_{BIAS1} = 100 µA)

The final gate required to develop the 4/5/6 divider is the 2-input multiplexer. Recalling that the essence of CML is the current steering principle, it would stand to reason that a CML multiplexer could be realized by simply controlling the bias currents of the differential input pairs. The device sizing and biasing of the 4/5/6 divider multiplexer is consistent with that of the DFF and AND gate. A simple realization of the described CML multiplexer is shown in Figure 30. In this multiplexer, PMOS devices are used as the tail current switches for the data input pairs. PMOS devices were used because they allow standard CMOS logic to be used for the external control, and PMOS devices do not exhibit the TID sensitivity of NMOS devices [10]. Because the external control signals for this multiplexer is static, the PMOS devices do not perform any dynamic switching, and their high-frequency limitations do not limit the multiplexer operating speed. When *s* is LOW, M_1 is turned "on" and M_2 will be "off". In this case, the bias current is forced through either Q_4 or Q_5, depending on the state of the D_0 input. With M_2 "off", no current can flow through Q_6 or Q_7, no matter what the state of the D_1 input. Therefore, the multiplexer output follows the D_0 input while *s* is LOW.

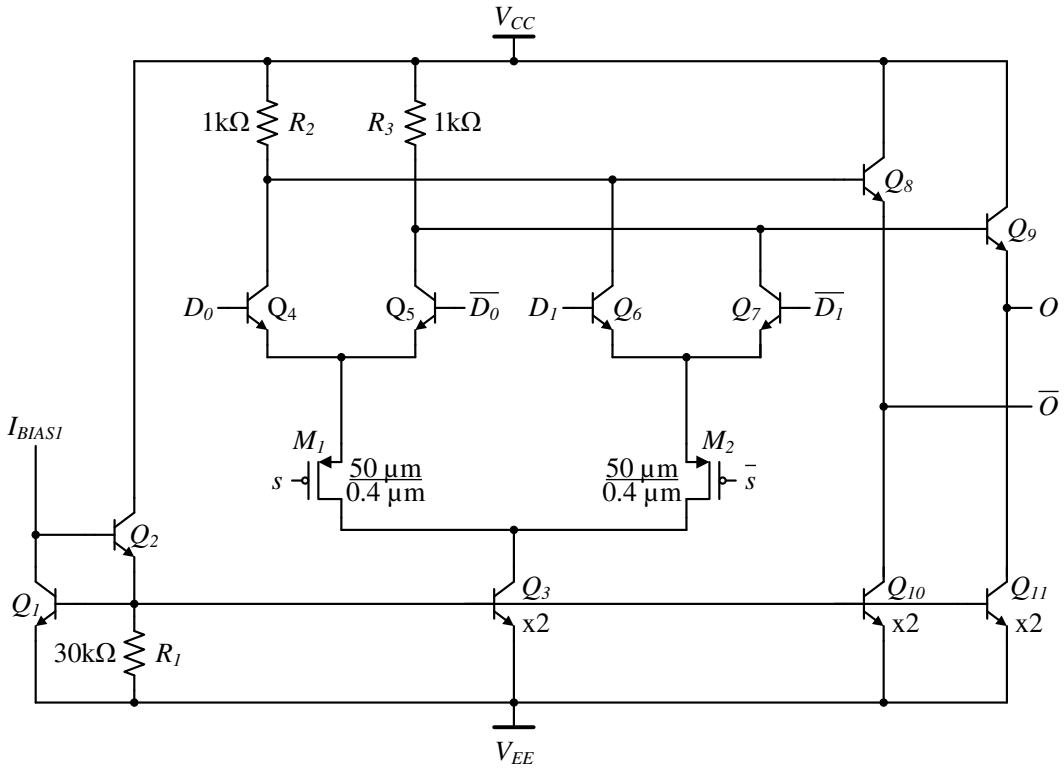

Figure 30. Multiplexer of 4/5/6 divider (all bipolars – npn-HBTs of 1 µm x 0.24 µm emitter area, all resistors – polysilicon type , I_{BIAS1} = 100 µA, all MOSFETs – 3.3 V PFETs)

When *s* is HIGH, M_1 is turned "off" and M_2 is "on". In this case, all bias current flows through either Q_6 or Q_7 and no current flows through Q_4 or Q_5. Therefore, the multiplexer follows the D_1 input when *s* is HIGH. The simple circuit of Figure 30 is essentially a CML buffer with selectable input pairs, which is exactly the function required by the 4/5/6 divider.

4.4 Prescaler 3.5-8 divider cell development

The development 3.5-8 divider of Figure 26 required the design of several building blocks. The main building block of the 3.5-8 divider is a double-edge triggered DFF. To support the configurability required of the 3.5-8 divider, a 2-input AND gate, a 2-input multiplexer, and a 5-input multiplexer were developed. The 2-input AND gate and the 2-input multiplexer are nearly identical to those used in the 4/5/6 divider, with only the choice bias current and collector resistor differing. The 5-input multiplexer is simply an extension of 2-input multiplexer that has 5 input pairs and PMOS static current switches. The same differential logic voltage is used in the 3.5-8 divider as was used in the 4/5/6 divider. To reduce power

consumption in the 3.5-8 divider, the resistor size was increased by a factor of 2 while the bias current was reduced by a factor of ½.

4.4.1 3.5-8 divider DFF

The 3.5-8 divider of Figure 26 requires a CML, double-edge triggered DFF to achieve ½-integer resolution. The CML, positive-edge triggered DFF of Figure 28 uses a master latch followed by a slave latch to achieve positive-edge triggered functionality. If instead, two master latches were operated with opposite clock polarities, one latch would change state only when *clk* is LOW and the other only when *clk* is HIGH. By multiplexing the outputs of these two latches at the clock frequency, a DFF that changes state on both positive and negative clock edges is realized. The designed double-edge triggered DFF of the 3.5-8 divider is shown in Figure 31.

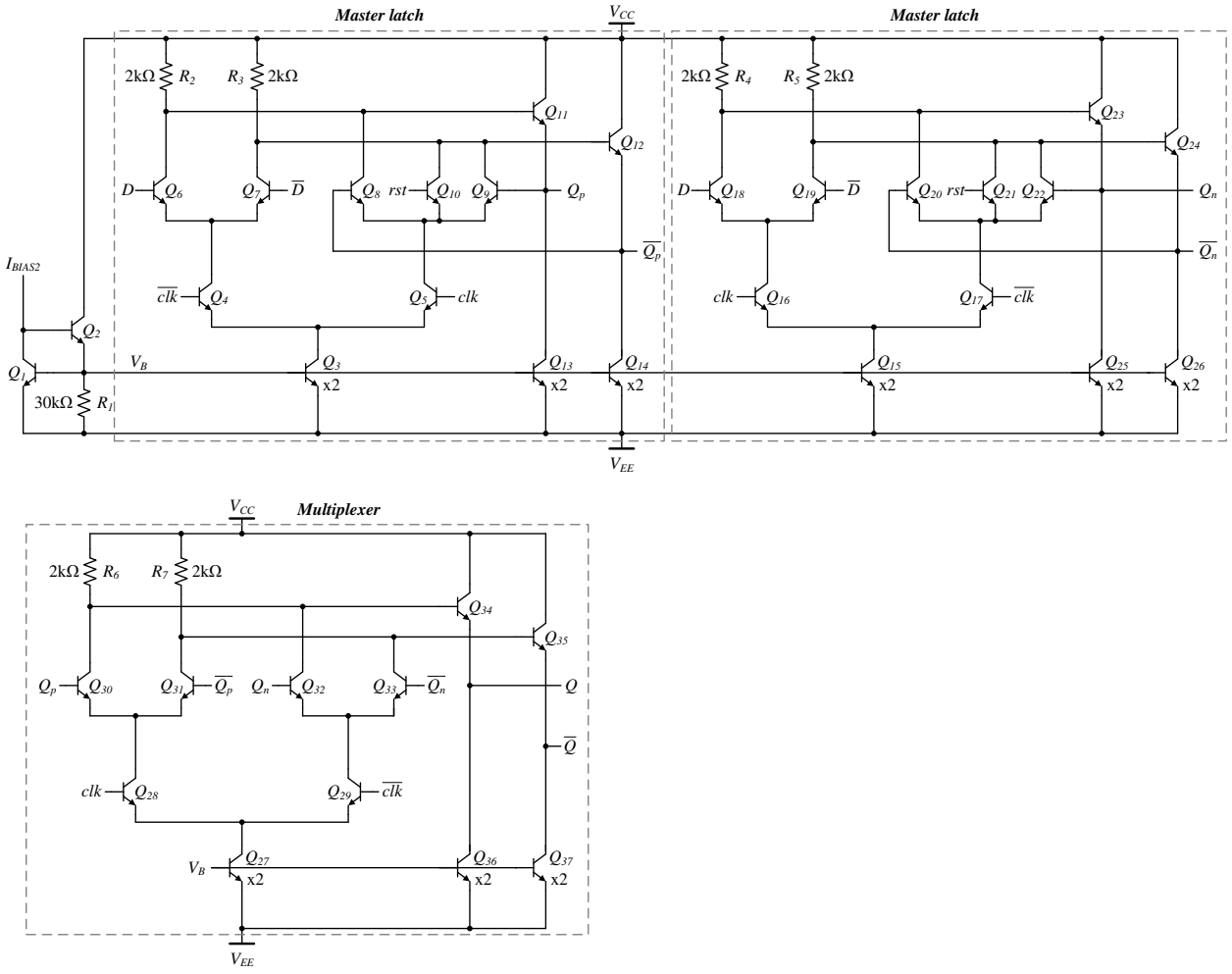

Figure 31. DFF of 3.5-8 divider (all bipolars – npn-HBTs of 1 µm x 0.24 µm emitter area, all resistors – 2-µm width, polysilicon type, I_{BIAS2} = 50 µA)

4.5 Multi-modulus prescaler simulations

To verify the functionality of the complete multi-modulus prescaler, block-level simulations of the 4/5/6 divider and the 3.5-8 divider have been performed. These simulations used ideal, digital elements and serve as a means to verify and illustrate the functionality of the prescaler design. Spectre simulations over a wide range operating conditions and device models have also been performed to verify the functionality of the divider cells and the multi-modulus prescaler as a whole. For clarity, these simulation waveforms are not included in this dissertation. The following idealized timing diagram simulations provide a more clear and understandable visualization of the functionality of the multi-modulus prescaler.

4.5.1 4/5/6 divider simulation results

The timing diagram simulations of the 4/5/6 divider are displayed in Figure 32 for the three configurable moduli of this divider. Recall that the output of the 4/5/6 divider is taken from Q_2, regardless of the divider configuration. Observing Figure 32(a), Q_0 and Q_1 can be seen to exhibit the expected divide-by-4 operation. As expected, the 4/5/6 divider output, Q_2, follows Q_1 but delayed by one clock cycle. In Figure 32(b), we can see that Q_0, Q_1, and Q_2 transition HIGH on successive rising clock edges. Once all DFF outputs are HIGH, the next rising clock edge triggers the Q_0 output to transition LOW. On the following clock rising edge, the pulse swallowing action of this configuration causes both Q_1 and Q_2 to transition LOW. Therefore, one period of the divider output, Q_2, can be described as LOW for three clock pulses and HIGH for two clock pulses, divide-by-5. Lastly in Figure 32(c), the pulse-swallowing observed in Figure 32(b) is absent and the 4/5/6 divider passes through each state in the full sequence, which results in the divide-by-6 waveforms.

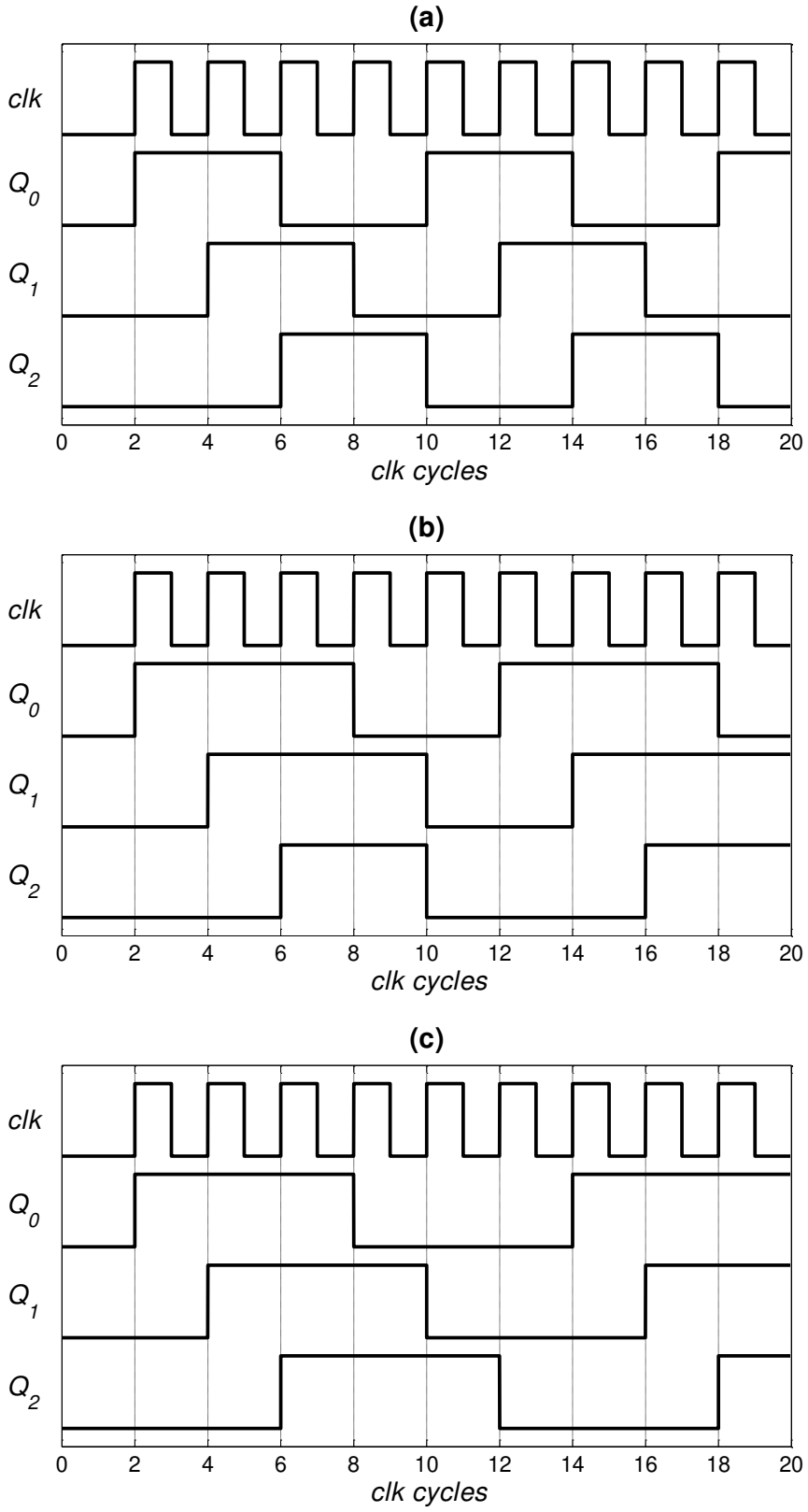

Figure 32. 4/5/6 divider block-level simulation timing diagram for (a) divide-by-4, (b) divide-by-5, and (c) divide-by-6 configurations

4.5.2 3.5-8 divider simulation results

The timing diagram simulations of the 3.5-8 divider are illustrated in Figure 33 for four divider configurations. The output of the 3.5-8 divider is taken from the output of the final DFF, Q_7, regardless of the configuration. Remembering that the 3.5-8 divider utilizes double-edge triggered DFFs, Figure 33(a) shows how half-integer division is achieved. In Figure 33(a), each DFF output successively transitions HIGH on every clock edge (rising or falling). After two clock periods all DFF outputs are HIGH. Once all DFF outputs are HIGH, the first two DFF outputs transition LOW on successive clock edges, while pulse swallowing forces the last two DFF outputs to transition LOW on the same clock edge. The described cycle repeats every seven clock edges (rising or falling), which results in division by 3.5. Figure 33(b) shows the timing diagram for the divide-by-4 configuration, where the only difference from the divide-by-3.5 configuration is that the divide-by-4 removes the pulse swallowing. Division by 4.5 can be achieved by inserting a DFF just before the output DFF, Q_7, as evident from Figure 33(c). Lastly, the divide-by-5 configuration of Figure 33(d) is achieved by removing the pulse swallowing of the divide-by-4.5 configuration. Division by higher moduli (up to 8) is achieved by continuing to insert DFFs into the 3.5-8 divider. The simulation results for moduli of 5.5-8 show the expected results, but for brevity, these results have not been included in this dissertation.

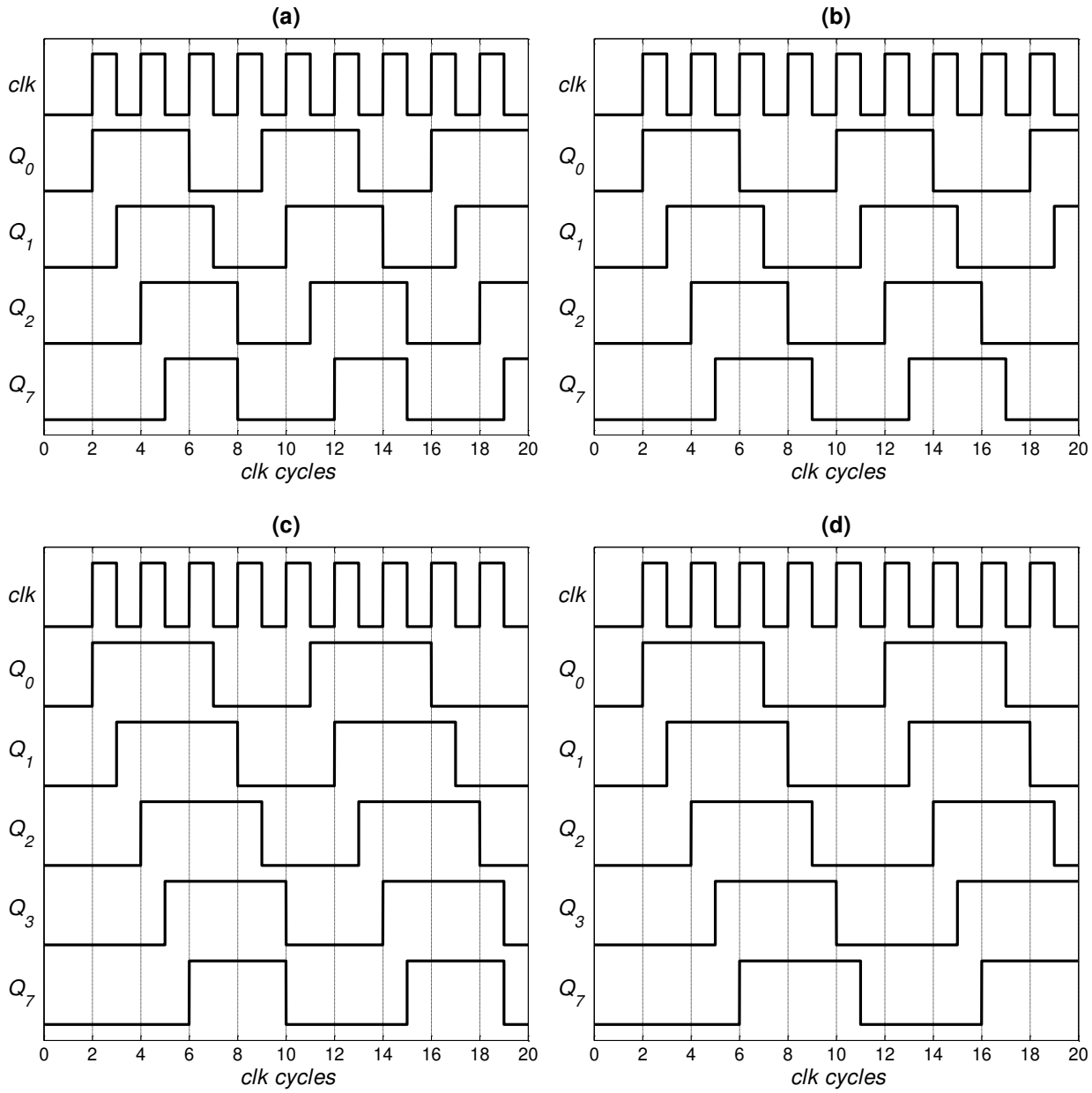

Figure 33. 3.5-8 divider block-level simulation timing diagram for (a) divide-by-3.5, (b) divide-by-4, (c) divide-by-4.5, and (d) divide-by-5 configurations

4.6 Physical implementation of the multi-modulus prescaler

The multi-modulus prescaler was implemented on a 180-nm SiGe BiCMOS process using the *npn*-HBT as the main active device. The HBT device in the process has generous spacing rules that result in significantly less dense layout (and therefore more required chip area) than seen with CMOS layout. Also contributing to the required chip area was the liberal use of guard-rings in an effort to mitigate charge sharing between devices in the event of a single-event ion strike. In spite of these factors, the use of minimum-sized HBT devices as well as minimum spacing allowed the complete multi-modulus prescaler to be implemented in a 750 µm by 460 µm area as shown in Figure 34. As explained in Chapter 3, implementation of common error correction schemes, such as triple-modular redundancy, typically require a 100-200% increase in chip area. The required chip area of the complete multi-modulus prescaler is approximately 0.345 mm^2. Of this area, the combined chip area of the error correction circuits of the 4/5/6 divider and the 3.5-8 divider is a modest 31,800 μm^2. Therefore, the implementation of the prescaler error correction scheme requires a chip area increase of only 10%.

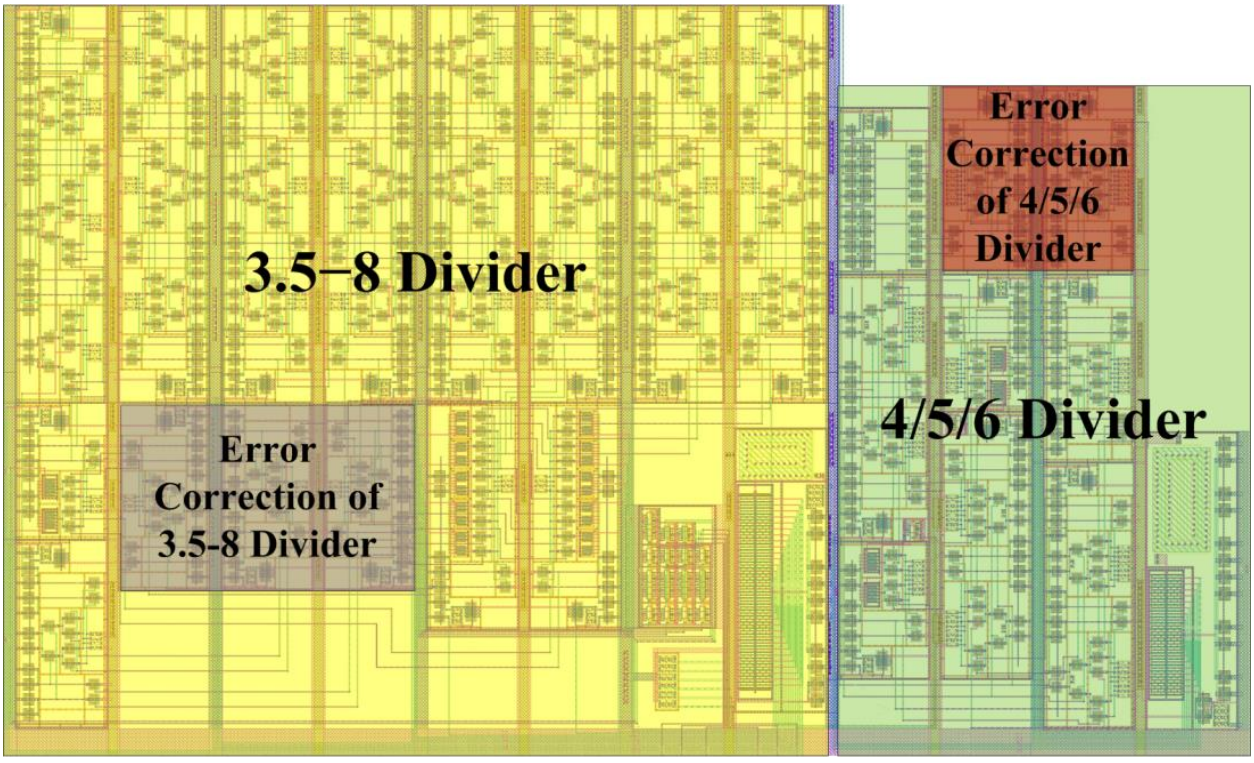

Figure 34. Layout of complete multi-modulus prescaler (750 µm x 460 µm)

The minimal chip area overhead of the error correction scheme of this multi-modulus prescaler is an attractive solution in many systems where chip area is a valuable resource. As described previously, the multi-modulus prescaler is designed to be implemented within a PLL core to support development of a frequency synthesizer ASIC. The implementation of this frequency synthesizer ASIC is shown in Figure 35 with the embedded multi-modulus prescaler highlighted. In addition to the frequency synthesizer ASIC, the multi-modulus prescaler was also integrated into a prescaler test ASIC as shown in Figure 36. This prescaler test ASIC consists of two copies of the multi-modulus prescaler that facilitate functional and performance testing of the designed multi-modulus prescaler. The functional details of the prescaler test ASIC will be explained in Chapter 5. Both the frequency synthesizer ASIC and the prescaler test ASIC were packaged in an 8 mm x 8 mm, 56-pin QFN ceramic packages.

4.7 Tools used in this research

The following tools were used in this research:

- Cadence 5.1.0 was used with a 180-nm SiGe BiCMOS process
- Assura 4.10 is used for LVS, DRC, and post-layout netlist extraction
- Cadence Virtuoso Analog Design Environment is used with Spectre for both schematic and extracted netlist simulations
- Matlab 2012 is used to develop the code for the 3.5-8 divider faulty state table analysis
- Eagle Layout Editor 5.9.0 was used to develop the printed circuit board for testing the prescaler ASIC and the frequency synthesizer ASIC
- An Agilent MSO6034A Mixed-Signal Oscilloscope was used for functional prescaler testing and prescaler error correction testing
- An Agilent N9010A Spectrum Analyzer was used for phase noise and jitter measurements of the VCO, prescaler, and frequency synthesizer

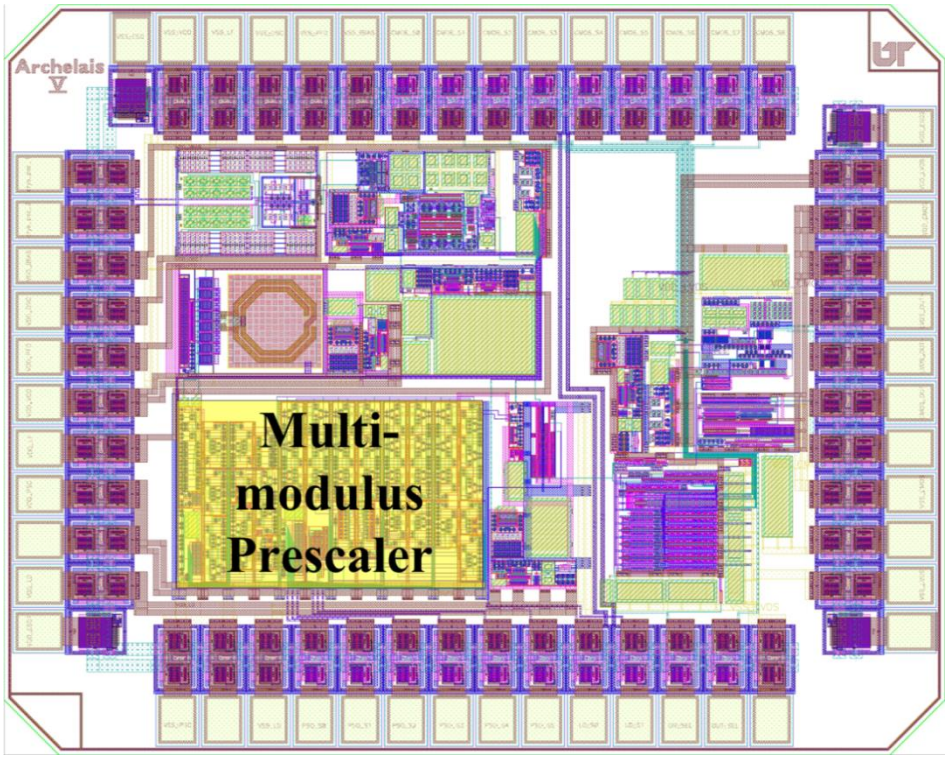

Figure 35. Layout of frequency synthesizer ASIC, with integrated prescaler (2.2 mm x 1.8 mm)

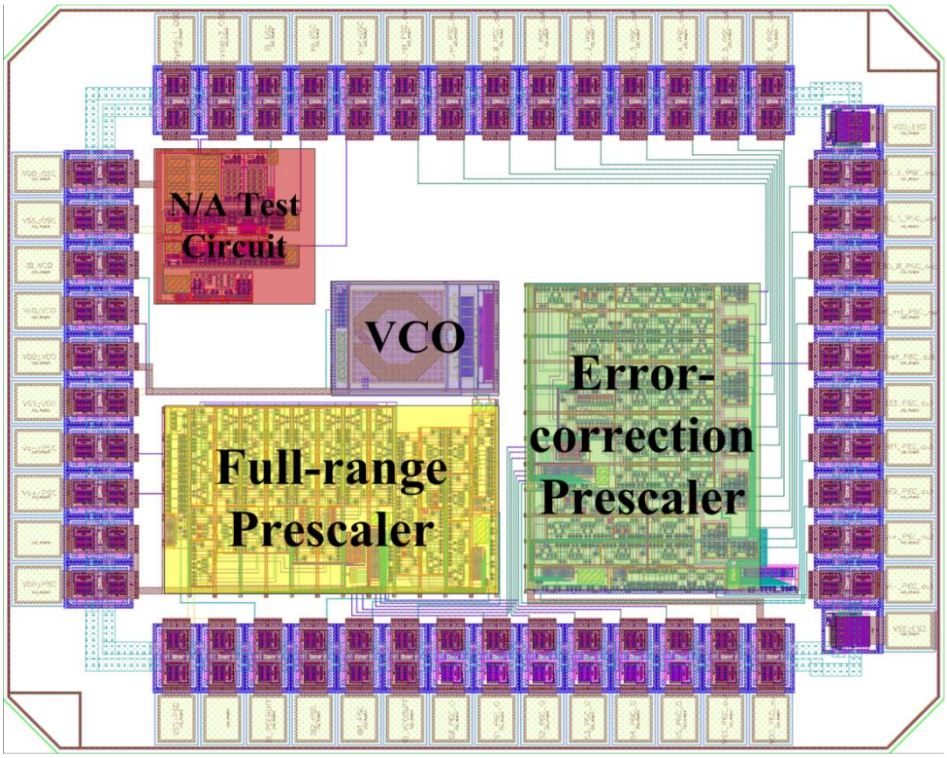

Figure 36. Layout of prescaler test ASIC (2.2 mm x 1.8 mm)

4.8 Concluding remarks

Chapter 4 of this dissertation examined the development of a multi-modulus prescaler design capable of operating at high frequency with high division resolution and well-suited for extreme environments. Chapter 4 also detailed the block-level design and analysis of the multi-modulus prescaler. The designed multi-modulus prescaler achieves high division resolution by utilizing cascaded, multi-modulus dividers. Next, the 4/5/6 divider design was presented and the functionality of this divider was examined. Detailed analysis of the state tables of the 4/5/6 has been performed, and this analysis revealed that an erroneous state table exists for this 4/5/6 divider. An error correction circuit for the 4/5/6 divider was described that is able to monitor the 4/5/6 divider and reset the divider if an error is detected. The error correction circuit was designed such that it does not affect normal operation of the 4/5/6 divider. Subsequently in Chapter 4, the 3.5-8 divider design and functionality was detailed. An exhaustive analysis of the erroneous state tables that exist for the 3.5-8 was performed. All erroneous state tables of the 3.5-8 divider were found to contain at least one of three LSB sequences. A simple, three-gate error correction circuit is able to monitor for and correct all erroneous state tables without affecting normal operation of the 3.5-8 divider. The transistor-level schematics for the components of the 4/5/6 divider and 3.5-8 divider have been presented and analyzed to validate their use in design of the multi-modulus prescaler. A first order propagation delay estimate was shown to determine the device sizing and biasing required of cells for each divider that would allow them to meet the requirements of the multi-modulus prescaler. Chapter 4 of this dissertation also presented timing diagram simulation results from each of the dividers for several configured moduli. These state table simulations validate the functionality of the designed multi-modulus prescaler. Lastly in Chapter 4, the physical implementation of the multi-modulus prescaler as well as the prescaler test ASIC and frequency synthesizer ASIC was described.

CHAPTER 5: TESTING AND ANALYSIS OF THE MULTI-MODULUS PRESCALER

5.1 Description of multi-modulus prescaler testing

Two ASICs have been fabricated with integrated, multi-modulus prescalers: the frequency synthesizer ASIC and a prescaler testing ASIC. A total of three prescaler test ASICs and two frequency synthesizer ASICs were packaged and available to be tested. The majority of multi-modulus prescaler testing reported in this dissertation was performed on the prescaler testing ASIC; however, extensive testing of the frequency synthesizer ASIC with the integrated, multi-modulus prescaler has also been performed.

5.1.1 Prescaler test ASIC description

Each prescaler test ASIC (Figure 37) consists of a full-range prescaler test structure and an error-correction testing prescaler structure. The prescalers in each of these test structures are identical, and the only difference is the supporting structures used to facilitate their testing.

The full-range prescaler structure is driven by the same on-chip VCO with buffer used in the frequency synthesizer ASIC. The prescaler output was buffered with a simple CML buffer, which uses larger HBTs and bias current than the prescaler cells to allow this prescaler buffer to drive off-chip, capacitive loads (stray capacitance, oscilloscope probes, etc.). The full-range prescaler test structure allows prescaler testing over the full VCO tuning range (3.7 GHz to 5.4 GHz), temperature (−180°C to 125°C), supply voltage (3.0 V to 3.6 V), and bias current. Using the full-range prescaler test structure functionality, phase noise, and power consumption measurements can be taken.

The error-correction prescaler test structure is driven by the same VCO buffer as the full-range prescaler; however, an external, differential clock signal drives this buffer as opposed to the VCO. In the error-correction prescaler test structure, the outputs of all DFFs in the 3.5-8 divider are buffered and brought off-chip to allow the error-correction scheme of the prescaler to be demonstrated. To allow simultaneous monitoring of all error-correction prescaler digital outputs, this test structure is operated at much lower frequencies than the full-range prescaler.

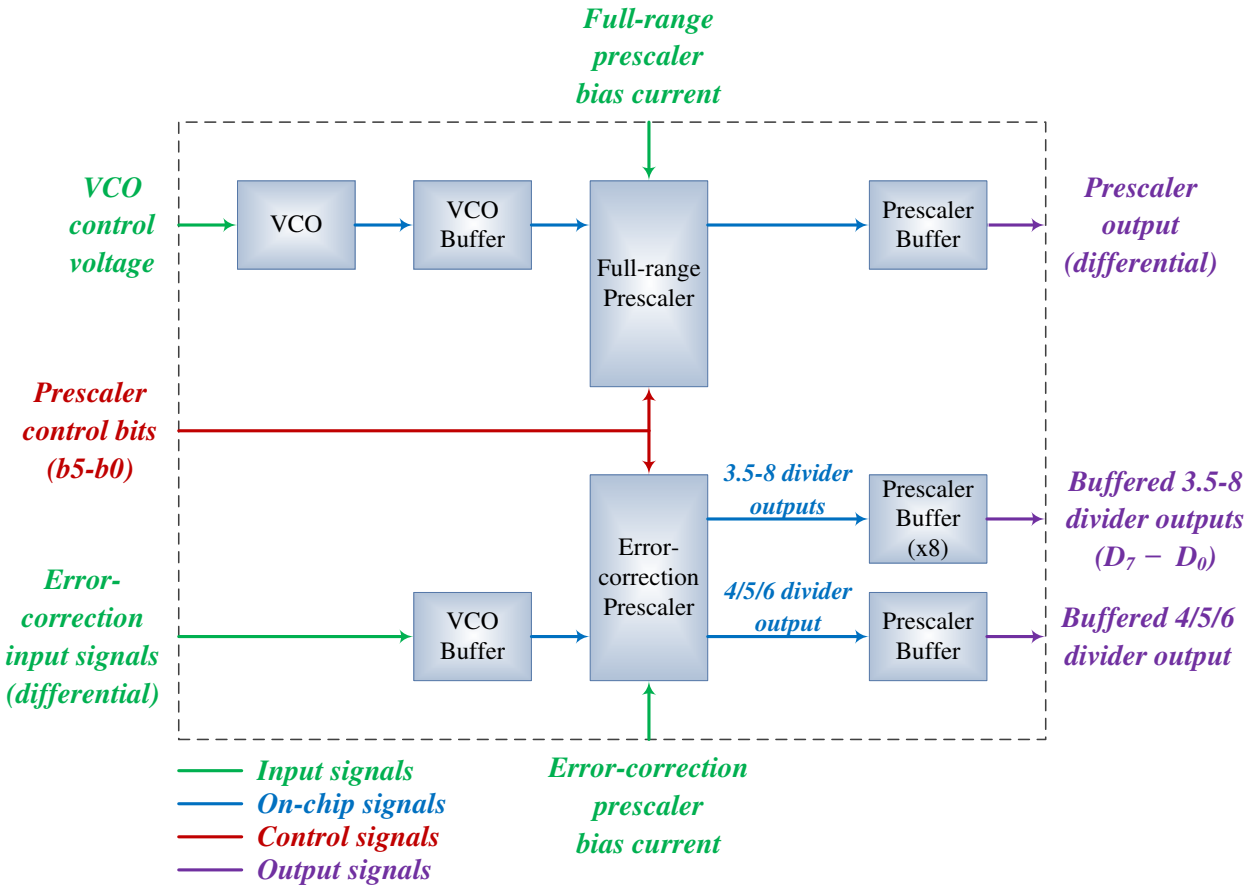

Figure 37. Prescaler test ASIC diagram

5.1.2 Test board and set-up description

A 4-layer test board was developed to support testing of the prescaler test ASIC as seen in Figure 38. The device under test (DUT) is housed in high-frequency, 8 mm x 8 mm QFN socket. Due to the high operating frequency of the prescaler test ASIC, minimizing parasitic inductance on the power supplies was critical to ensure proper operation of the DUT on the test board. The two internal PCB layers were used as power planes for the chip power supplies and ground. This arrangement minimizes parasitic resistance and inductance on the chip power supplies. High-frequency, ceramic bypass capacitors (on the bottom of the test board) provide a power supply filtering for each test structure of the prescaler test ASIC. This test board allows both on-board and external control of bias currents and prescaler control bits. External control is used to facilitate testing while the test board is sealed in the temperature chamber.

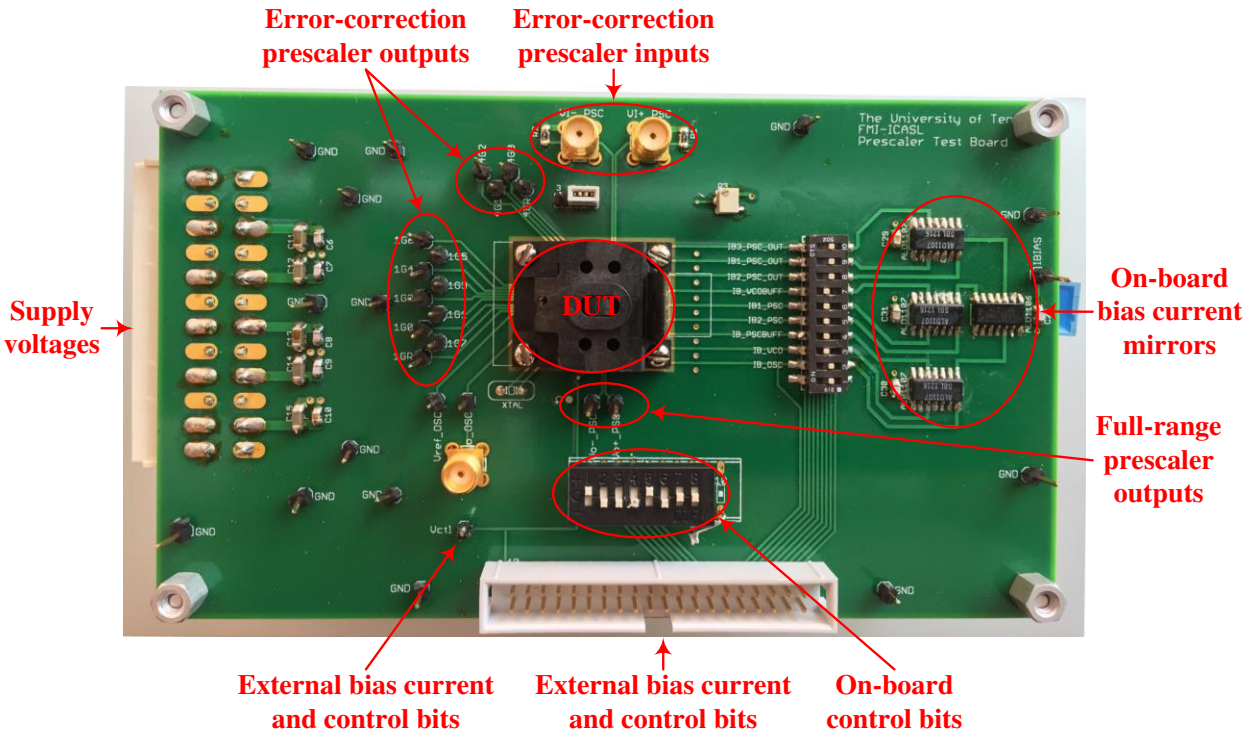

Figure 38. Prescaler test board, 4-layer PCB design, 8 mm x 8 mm, 56-pin QFN chip socket

For room temperature testing, a Keithley 2400 current source is used to bias on-board current mirrors, which provide the bias currents required for each test structure of the DUT.

5.2 Room-temperature functionality testing

Initial testing of the full-range prescaler consisted of room-temperature, nominal supply voltage (3.3 V) testing of the prescaler over the full range of the on-chip VCO for prescaler division ratios of 16, 24, 32, and 48. Due to one high-speed probe being available for testing, only one of the prescaler differential outputs was monitored for these tests. These tests were performed on all three prescaler test ASICs.

5.2.1 Prescaler functionality demonstration

All three prescaler test chips demonstrated proper functionality over the full VCO tuning range for the 4 division ratios tested. The result of one such test is shown below in Figure 39 with the prescaler configured to divide-by-48 and operating at the maximum VCO frequency. Measurements taken at division ratios of 24 and 32 showed results consistent with the measurement shown in Figure 39.

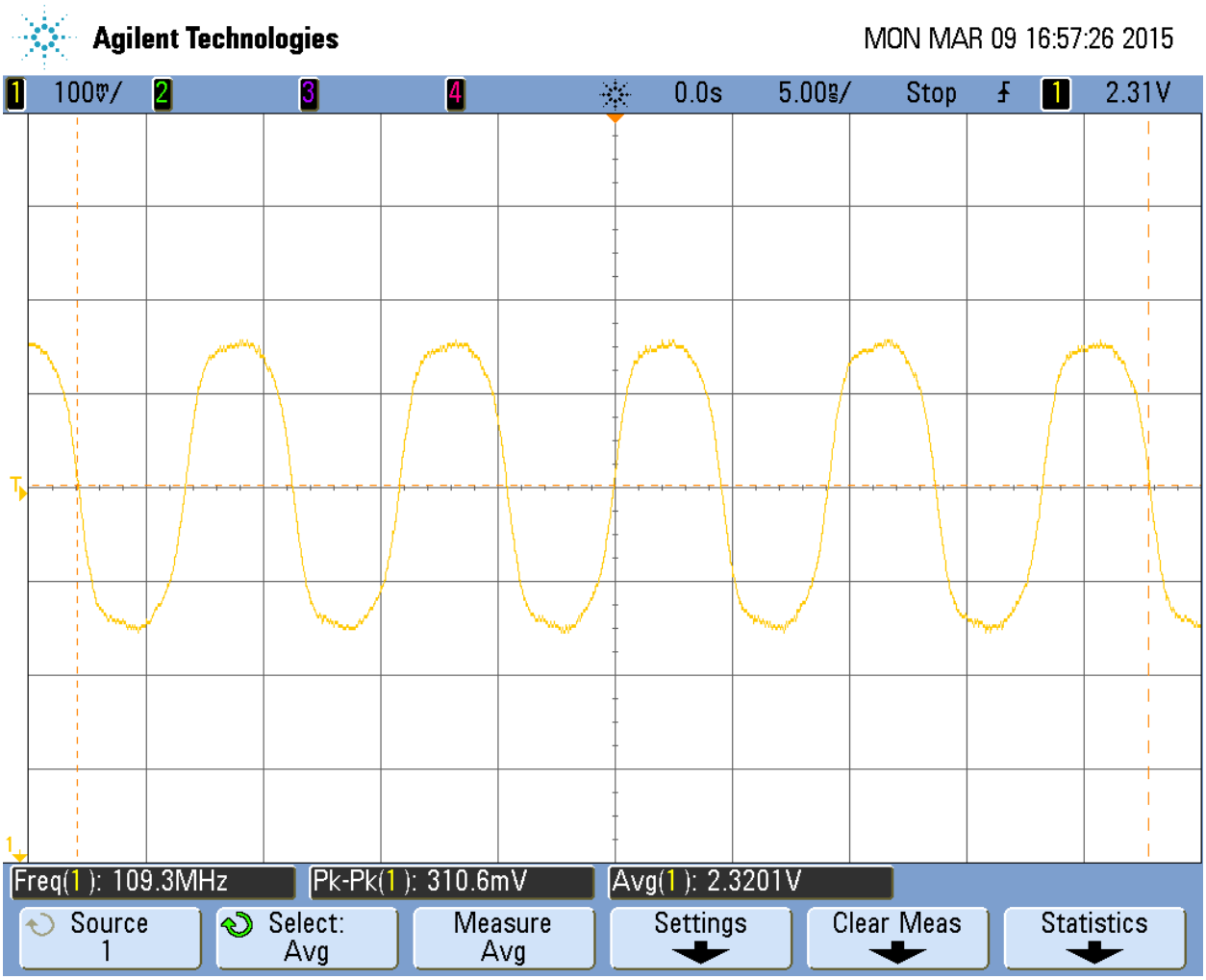

Figure 39. Chip #1 prescaler output at room temperature driven by on-chip VCO, input frequency of 5.25 GHz, prescaler division ratio – 48, V_{DD} = 3.3 V, I_{BIAS} = 40 µA

Another example of prescaler functionality at room temperature is shown in Figure 40. This measurement was taken with prescaler operating at the minimum VCO frequency in a divide-by-48 configuration. Measurements were also taken with the minimum VCO frequency for the lower prescaler division ratios. No faulty operation of any kind was observed during these initial functionality tests. Measurements taken for division ratios of 16, 24, and 32 showed results consistent with the result observed in Figure 40.

The measurements results observed for the initial prescaler functionality serve the purpose to verify proper functionality of both dividers of the prescaler. Additionally, the external control bits of the prescaler were observed to provide the correct configurability.

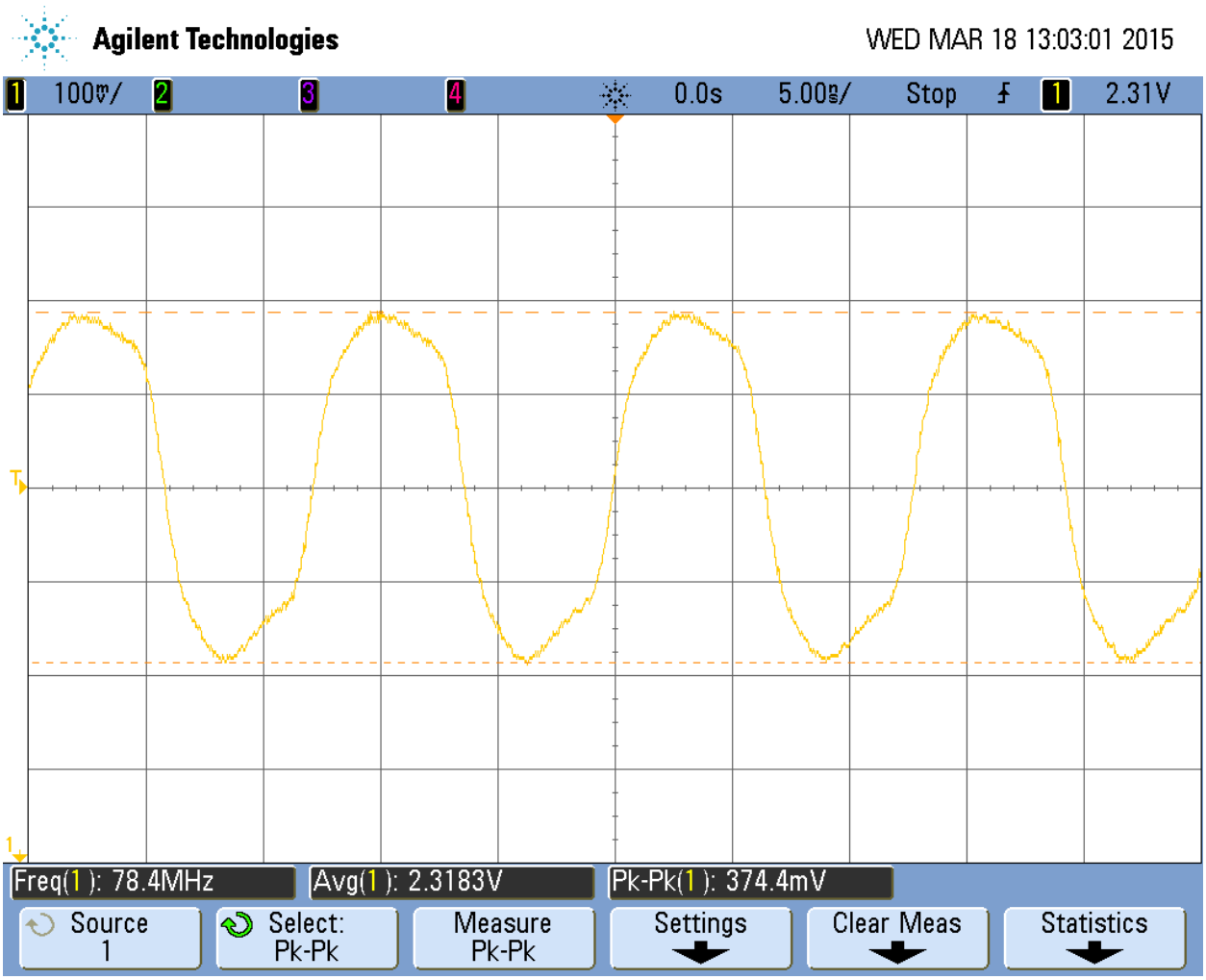

Figure 40. Chip #1 prescaler output at room temperature driven by on-chip VCO, input frequency of 3.74 GHz, prescaler division ratio – 48, V_{DD} = 3.3 V, I_{BIAS} = 40 µA

5.2.2 Prescaler input frequency locking range

The maximum input frequency locking range of the prescaler in divide-by-48 configuration was tested as a function of prescaler bias current. Each chip was tested over the full supply voltage range, but no variation in maximum input frequency was observed for different supply voltages, a benefit of the current-mode logic of the prescaler. A summary of the prescaler input locking range as a function of prescaler bias current is shown in Figure 41. All three test chips were able to operate at the maximum VCO frequency with a prescaler bias current of 37 µA or less. The maximum input frequency of the prescaler was observed to be linearly dependent on input bias current for all three test chips.

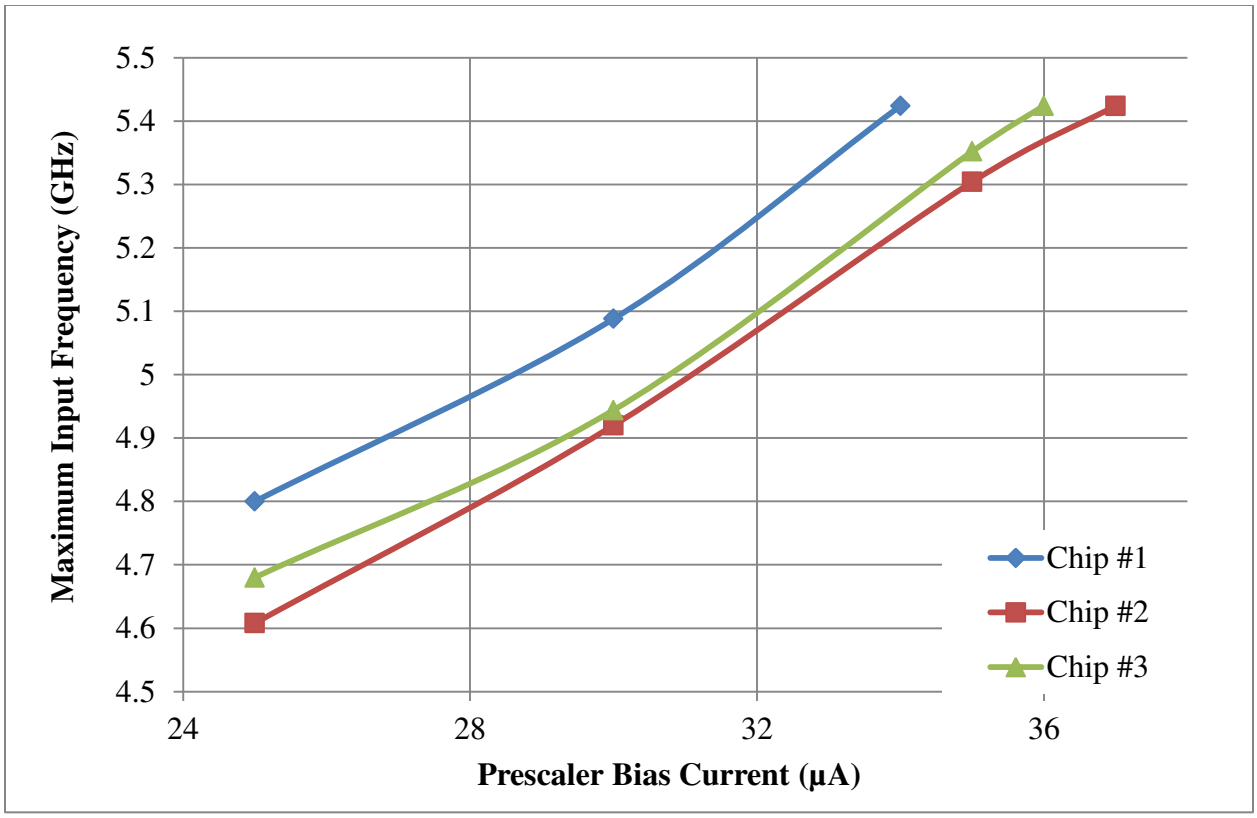

Figure 41. Maximum prescaler input frequency over prescaler bias current, room temperature, prescaler division ratio – 48 (valid for 3.0 V to 3.6 V supply voltage range)

5.3 Temperature and supply voltage testing

Chip #2 was tested over the full operating temperature range and supply voltage range. Chip #2 was chosen for this test as this chip demonstrated the highest bias current requirement for a given input frequency. Due to temperature chamber limitations, the minimum temperature achieved was limited to −175°C. At each temperature, supply voltage, and input frequency tested, the minimum bias current required for proper operation of the prescaler was supplied and the total prescaler current consumption was measured. This test was performed for prescaler division ratios of 16, 24, 32, and 48 with only modest differences in prescaler current consumption observed. The minimum VCO frequency was observed to be slightly dependent on temperature, ranging from 3.86 GHz at −175°C to 3.64 GHz at 125°C. Due to the 300 MHz bandwidth limitation of the oscilloscope used during testing, the 5.0 GHz, divide-by-16 test point was omitted. Figure 42 summarizes the results observed for these tests. As expected, Figure 42 shows that prescaler current consumption increases with temperature.

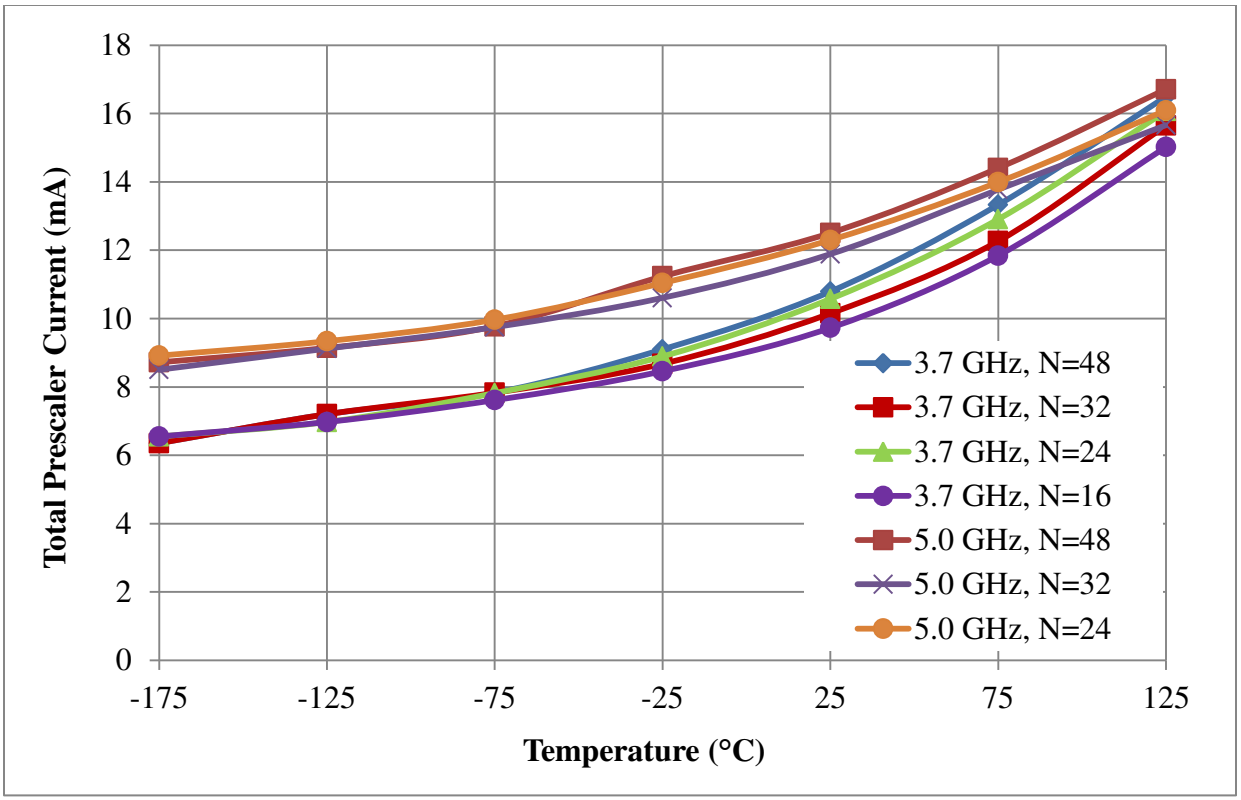

Figure 42. Chip #2 total prescaler current consumption over temperature and division ratio (valid for 3.0 V to 3.6 V supply voltage)

The maximum prescaler current consumption was observed to be 16.7 mA at 125°C with a 5 GHz input frequency and a division ratio of 48. The prescaler demonstrated proper functionality from 3.0 V to 3.6 V supply voltage over the full temperature range, but as mentioned previously, supply voltage variation has negligible impact on current consumption. Therefore, supply voltage variation is applicable but not reflected in Figure 42.

5.4 Prescaler and VCO phase noise measurements

Since the on-chip VCO is used to clock the full-range prescaler test structure, phase noise measurements at the prescaler output include the VCO phase noise in addition to the prescaler phase noise. In fact, the VCO phase noise dominates these measurement results. To allow the phase noise contribution of the prescaler itself to be inferred, the phase noise of the VCO alone was first measured. A separate test chip from an earlier fabrication contains an integrated VCO loaded by the same VCO buffer used on the prescaler test ASIC. This VCO test chip is used to establish a base line VCO phase noise measurement. To minimize external interference of

measurement results, all phase noise measurements for both the VCO and the prescaler were taken with power to the test chips supplied by alkaline batteries. Also, to reduce external interference of phase noise measurements, the bias currents for the VCO and the prescaler were provided by a resistor to the supply voltage as opposed to the Keithly 2400 source meter. These measurements were taken at a typical lab bench with no special radiative noise isolation implemented. An Agilent N9010A spectrum analyzer was used to conduct all phase noise and jitter measurements.

5.4.1 VCO phase noise measurements

Several, repeated, low-frequency VCO phase noise measurements were taken and showed fairly consistent results. An example of one of these VCO phase noise measurements is shown in Figure 43.

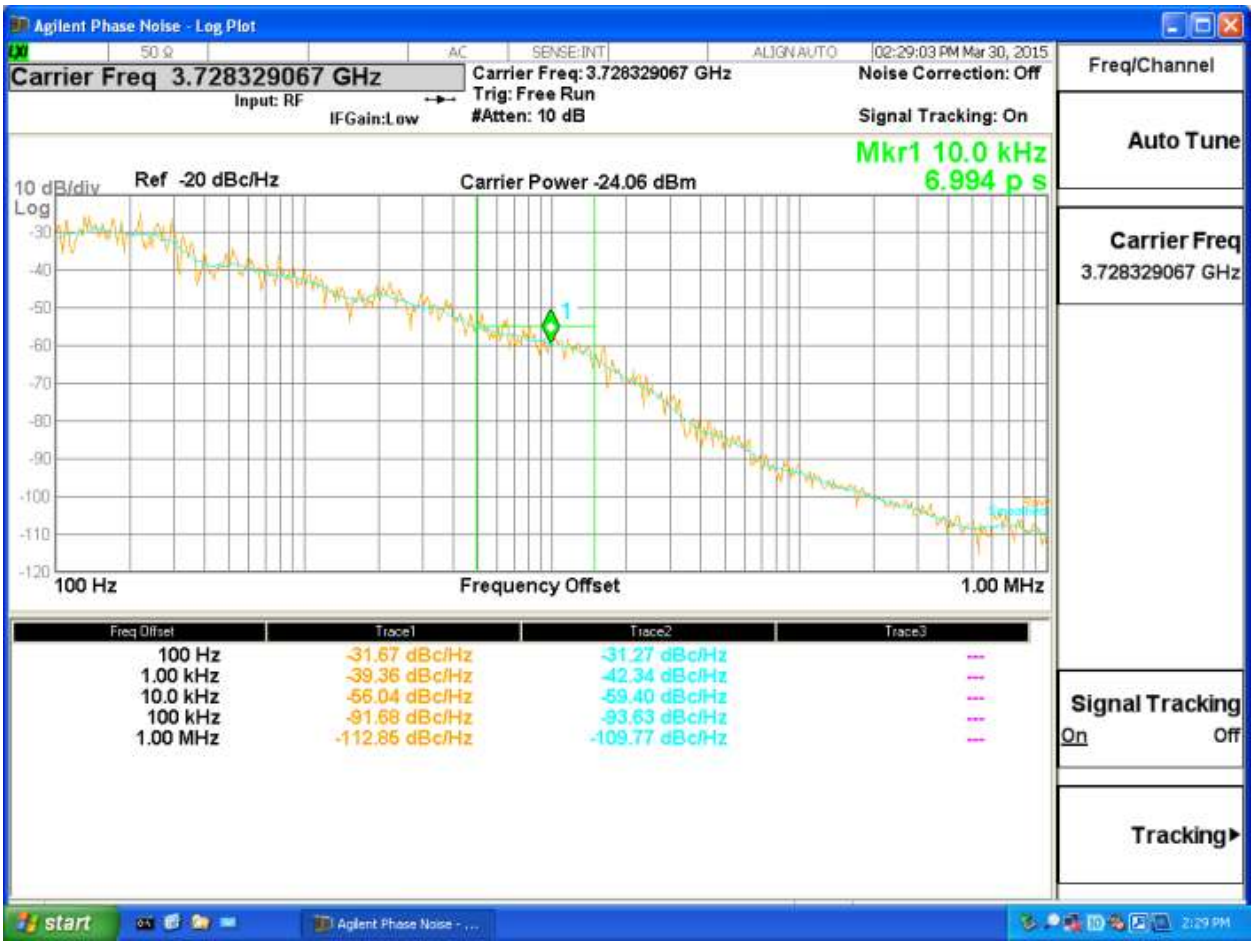

Figure 43. VCO phase noise measurement, room temperature, nominal supply voltage, minimum VCO frequency

Phase noise measurements taken at 10 kHz offset frequency ranged from −60.8 to −58 dBc/Hz for the 13 measurements taken. Attempts to measure VCO phase noise at 5.0 GHz oscillation frequency showed low carrier power and inconsistent phase noise measurements due to limitations in the drive capability of the VCO buffer. From the data gathered from the stand-alone VCO phase noise tests, an approximate VCO phase noise value at 10 kHz offset frequency was found to be ~ −60 dBc/Hz.

5.4.2 Prescaler phase noise measurements

Having established an approximate VCO phase noise value of −60 dBc/Hz at 10 kHz offset, the same, room temperature test set-up was used to measure the phase noise of the prescaler driven by the on-chip VCO and buffer. An example of one such measurement is shown in Figure 44.

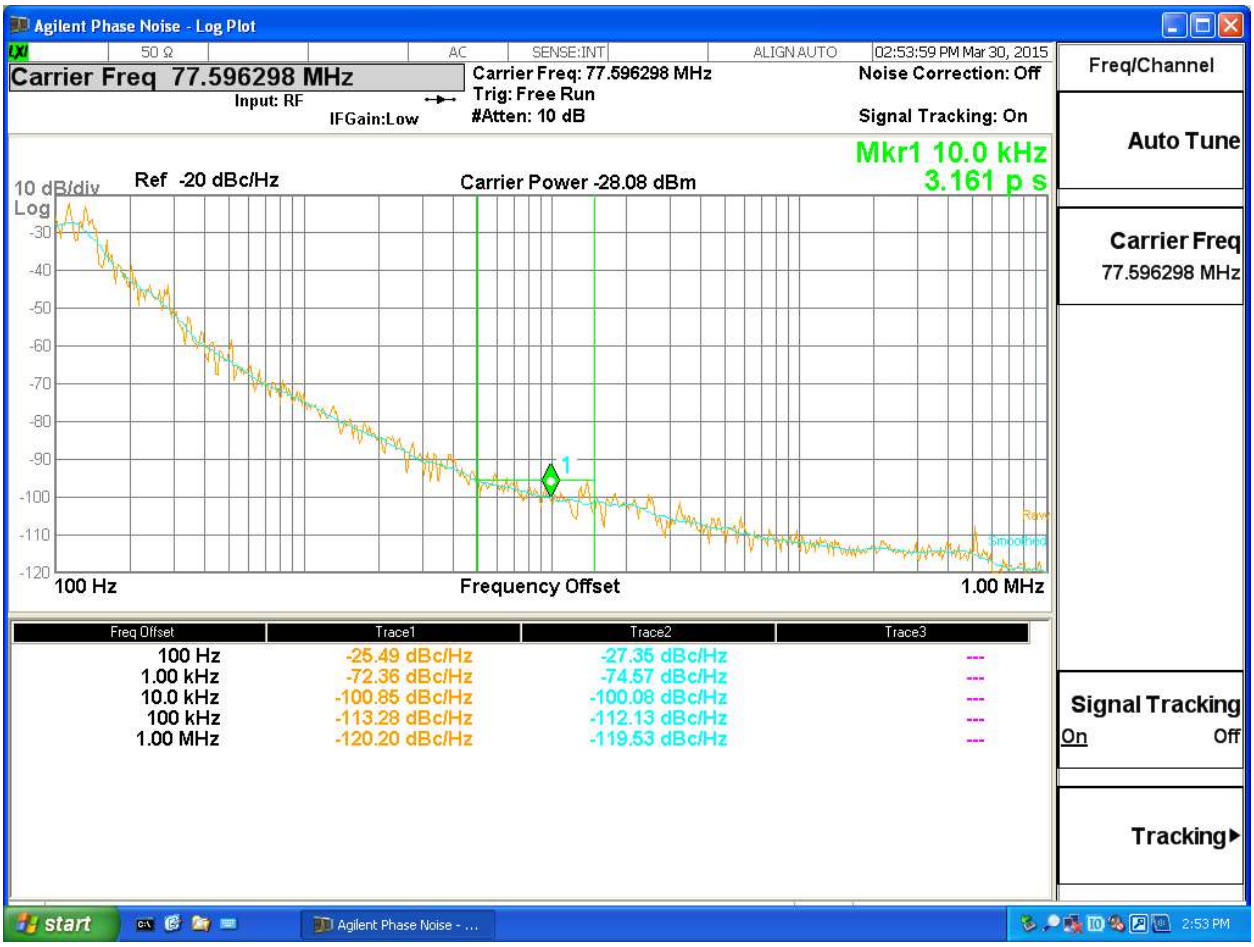

Figure 44. Chip #1 prescaler phase noise measurement, room temperature, 3.3 V supply voltage, 3.7 GHz VCO frequency, prescaler division ratio – 48

Several, repeated measurements were taken at each test point described above and these measurements showed very consistent results. These measurements were performed on all three test chips for prescaler division ratios of 16, 24, 32, and 48 and for both 3.7 GHz and 5.0 GHz VCO frequencies. With a 3.7 GHz VCO frequency and the prescaler configured to divide-by-48, phase noise measurements taken at 10 kHz offset ranged from −100.1 to –99 dBc/Hz. A summary of all VCO-driven prescaler phase noise measurements at 10 kHz offset is shown in Figure 45. As observed in Figure 45, the measured phase noise was approximately linearly related to division ratio with measured phase noise decreasing as division ratio increases. All three test chips showed consistent results and only a modest increase in phase noise for higher VCO frequency. The approximate effect of frequency dividers on input phase noise is a reduction in phase noise by $20log_{10}(N)$ where N is the division ratio of the frequency divider [3]. Using this approximation, the phase noise reduction due to frequency division can be added to the measured output phase noise.

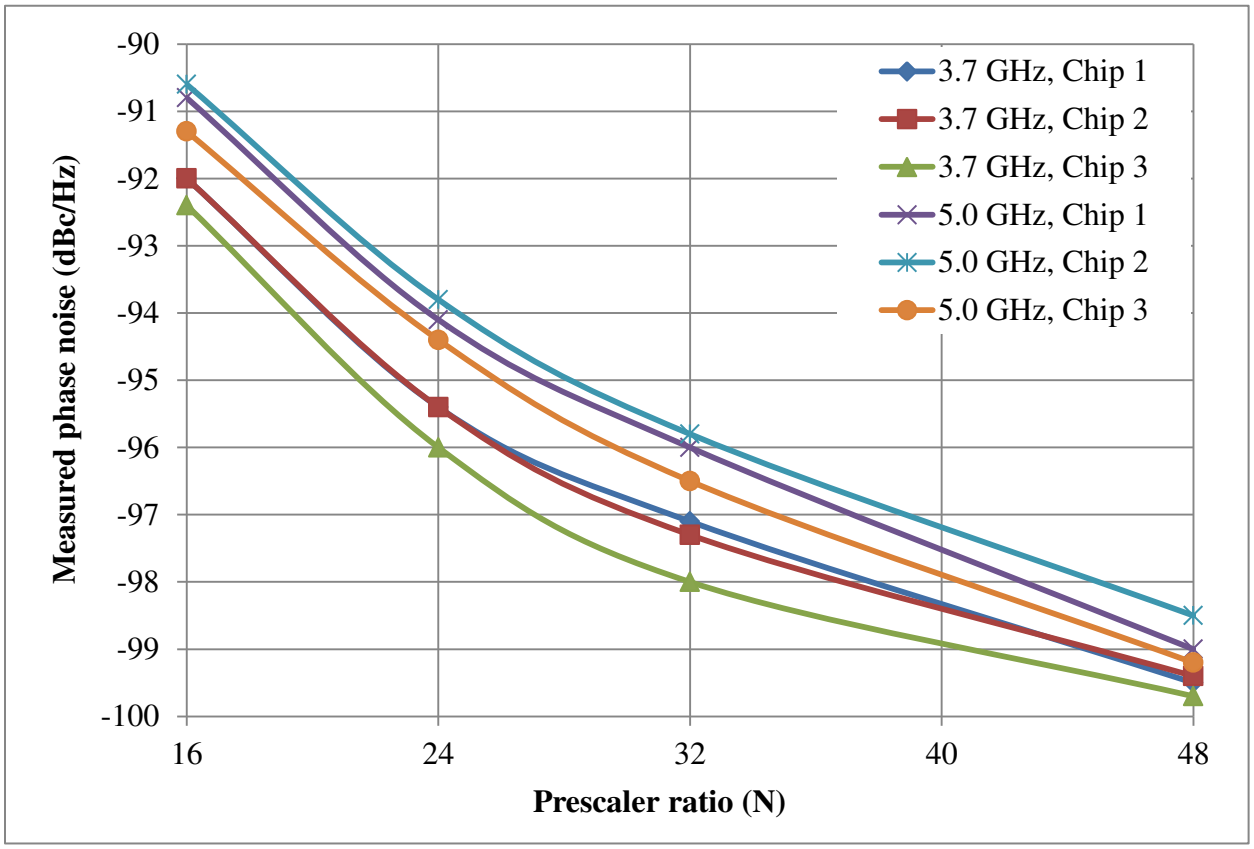

Figure 45. Measured phase noise of prescaler driven by VCO at 10 kHz offset

Adding this phase noise reduction back to the measured phase noise value yields an estimate for inferred VCO phase noise (assuming no noise contribution from the prescaler). The calculated, inferred VCO phase noise is shown in Figure 46. For all test chips and all prescaler division ratios, the inferred VCO phase Using this approximation, the phase noise reduction due to frequency division can be added to the measured output phase noise to recover an inferred VCO phase noise is actually less than measured directly from the VCO (~ −60 dBc/Hz). This result is not realistically possible as this implies the frequency divider reduces the phase noise of the VCO itself. This measurement artifact is caused by limitations in measurement accuracy as well as using a VCO from a separate test chip to infer the phase noise of the VCO on the prescaler test chip. In Figure 46, the visible increase in phase noise with prescaler division ratio illustrates an increased phase noise contribution from the prescaler as the prescaler division ratio is increased. This very slight increase in phase noise over the prescaler division range illustrates just how minimal the phase noise contribution of the prescaler itself is to the overall test structure.

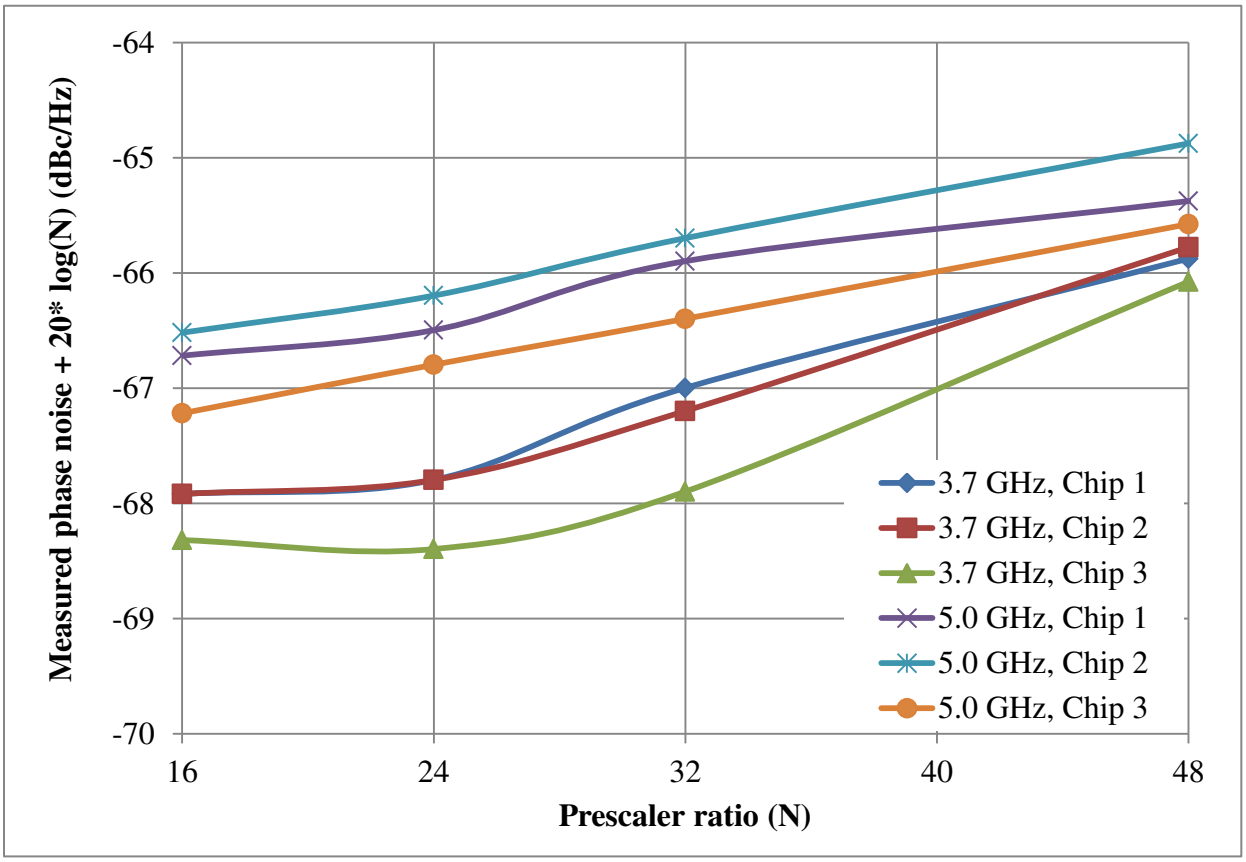

Figure 46. VCO-referred measured phase noise of at 10 kHz offset

5.5 Testing of frequency synthesizer ASIC with embedded prescaler

To verify the implementation of the prescaler within a phase-locked loop, the frequency synthesizer ASIC was tested for several device configurations. These various frequency synthesizer configurations resulted in a wide range of prescaler input frequencies and division ratios. Each of these tests showed proper operation of the prescaler as well as the frequency synthesizer as a whole. An example of such a frequency synthesizer test is shown in Figure 47. Phase noise and jitter measurements of the frequency synthesizer ASIC with embedded prescaler were also taken for several device configurations. Several measurements were taken for each frequency synthesizer configuration and demonstrated very consistent results. All of these configurations revealed low phase noise and jitter measurements as seen in the example test shown in Figure 48.

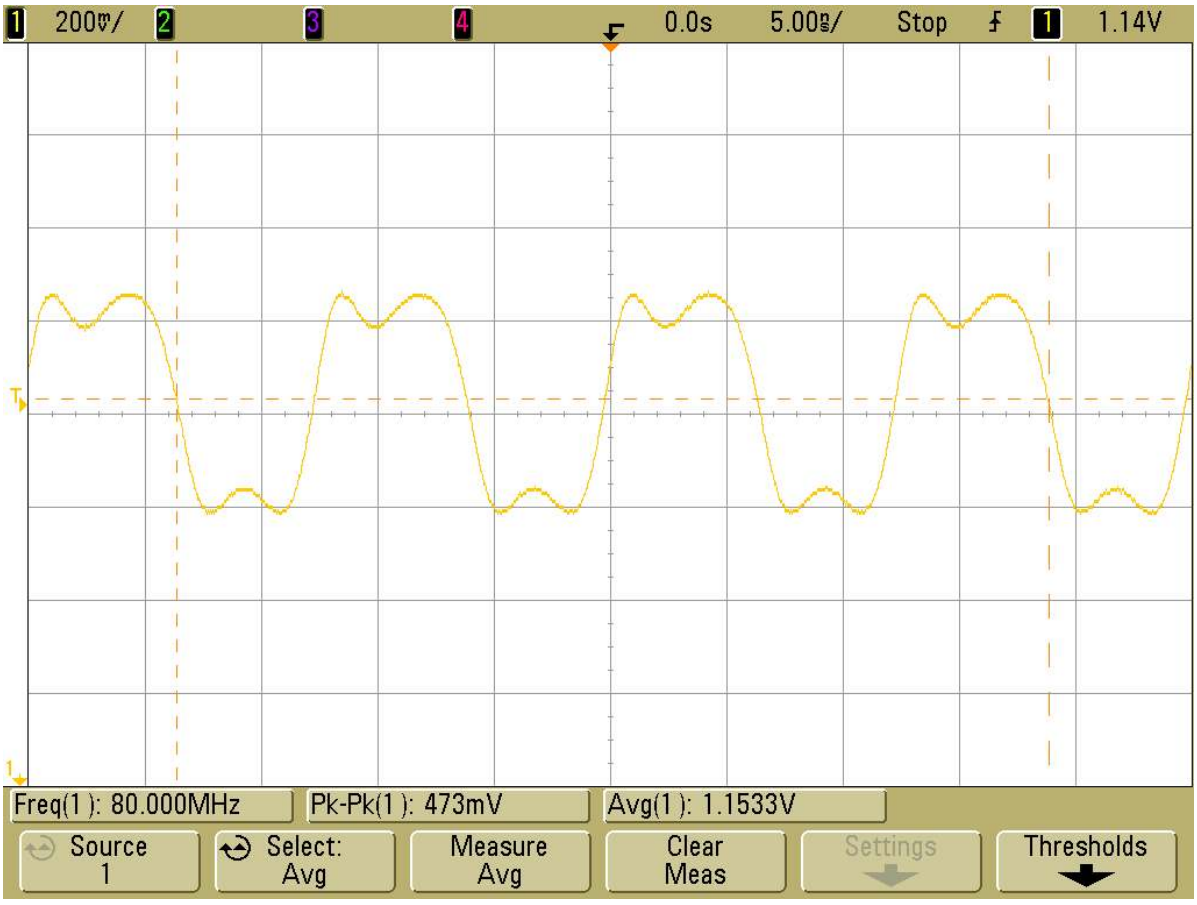

Figure 47. Frequency synthesizer ASIC functionality demonstration, room temperature, 3.3 V supply voltage, 20 MHz crystal reference frequency, 80 MHz LVDS output (single-ended), prescaler input (VCO) frequency of 3.84 GHz, prescaler division ratio – 48

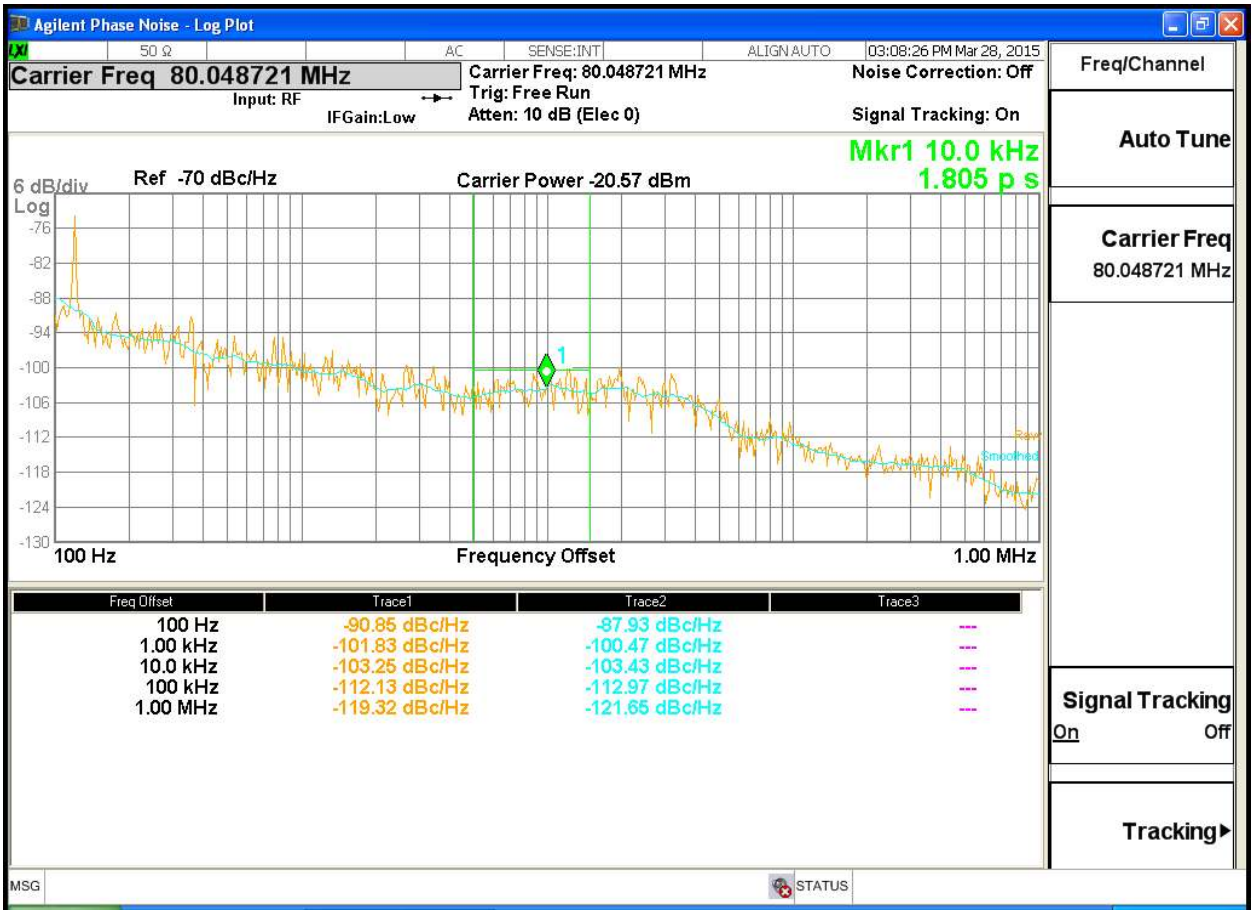

Figure 48. Frequency synthesizer ASIC phase noise measurement, room temperature, 3.3 V supply voltage, 20 MHz crystal reference frequency, 80 MHz output frequency, prescaler input (VCO) frequency of 3.84 GHz, prescaler division ratio – 48

5.6 Prescaler error-correction testing

The final test of the prescaler was to demonstrate the error correction scheme used in the prescaler design. The more complicated error correction of the 3.5-8 divider section of the prescaler was tested as opposed to the relatively simple 4/5/6 divider section. For this test, an external, 400 kHz clock signal was applied to the 4/5/6 divider in divide-by-4 configuration and the 100 kHz output of the 4/5/6 divider was used to clock the 3.5-8 divider being tested. To accomplish this error correction demonstration, the 3.5-8 divider must be induced into an erroneous operating condition. Observing the outputs of all DFFs of the 3.5-8 divider, it was determined than the 3.5-8 divider can be induced to a closed (not auto-correcting), erroneous operation condition simply by switching from divide-by-4 to divide-by-8 while the prescaler is

operating. In fact, all faulty state tables for the divide-by-8 configuration are closed, and therefore ensure that the error correction circuit is forced to reset the 3.5-8 divider. This simple test procedure allows the error correction scheme to be demonstrated by flipping a single prescaler control bit (***b3***) while the prescaler is operating. This test was repeated over 40 times and the induced, erroneous operation of the 3.5-8 divider was successfully corrected each time. One demonstration of this error correction test is shown in Figure 49. From Figure 49, the 3.5-8 divider can be seen operating in the correct divide-by-4 configuration before the switching event of the prescaler control bit (the top waveform of Figure 49). In the divide-by-4 configuration, only DFF outputs $D_3 - D_0$ are used by the 3.5-8 divider while $D_7 - D_4$ have no effect on divider operation. Just after the switching event, all DFF outputs are used by the 3.5-8 divider in divide-by-8 configuration and the divider is induced to an erroneous operating condition as shown in Figure 49.

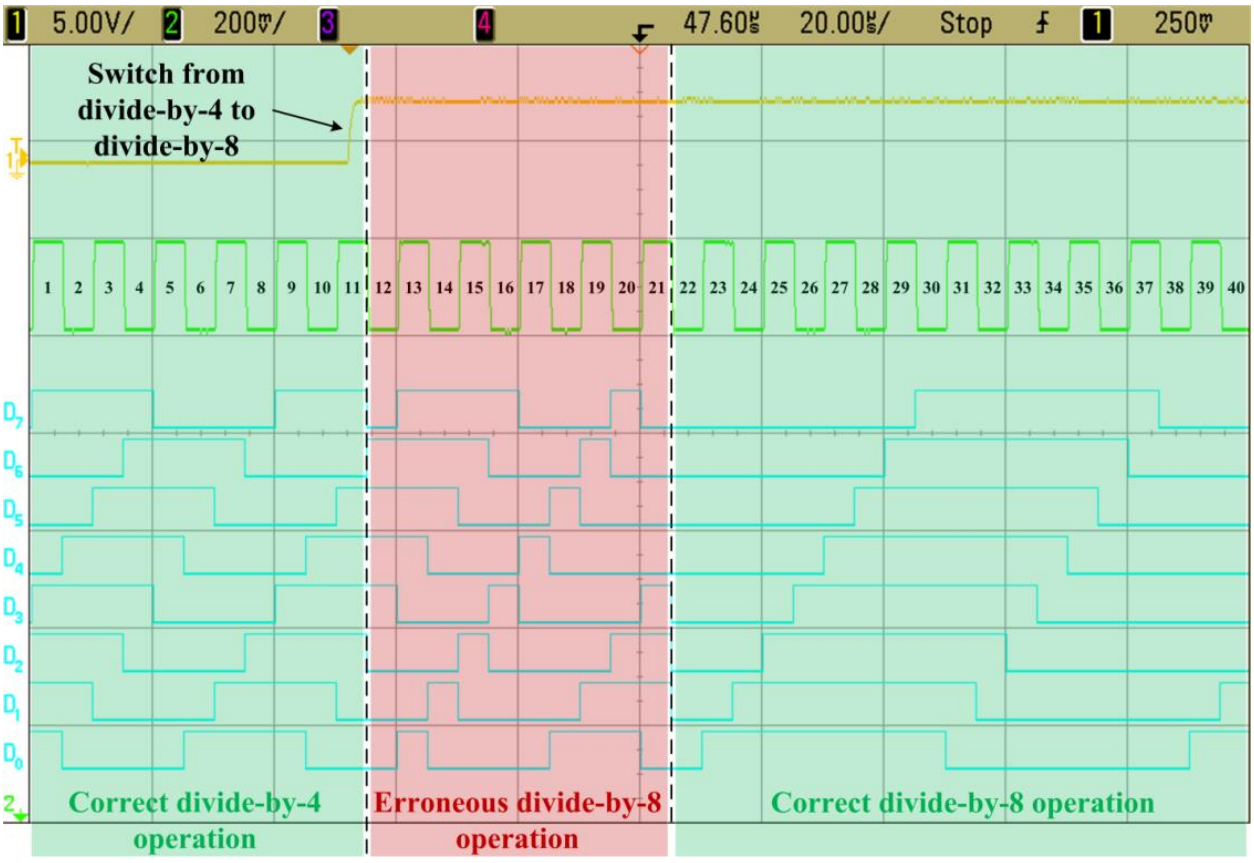

Figure 49. Demonstration of prescaler error-correction (3.5-8 divider), top – prescaler control bit (*b3*), middle –3.5-8 divider clock signal, bottom – 3.5-8 divider DFF digital outputs

This erroneous operating condition persists until one of the three monitored error codes (**0101**, **1001**, **1101**) of the 4 LSBs ($D_3 - D_0$) is detected, at which point, the error correction circuit resets all DFFs and the 3.5-8 divider enters the correct divide-by-8 operation. In the event that a monitored error code is detected, all DFFs of the divider are reset during the same clock pulse as when the error is detected. For this reason, the monitored error code does not appear at the output of error-correction testing prescaler. Therefore, the last erroneous state observable is the state just before the monitored error code. To summarize these findings, a state table diagram of the result shown in Figure 49 is provided in Table 7. In Table 7, the last observable, erroneous state is **00001110**. The subsequent state for **00001110** in the divide-by-8 configuration, although not observable, can be easily shown to be **00011101**. The 4 LSBs of this state are, in fact, one of the three monitored error codes. All DFFs can be observed to reset after the erroneous state **00001110**, thereby demonstrating successful operation of the error correction scheme. All error-correction tests performed showed similar results, in which the last observable erroneous state was the state just before the monitored error code. No event was observed in which the induced erroneous operation of the 3.5-8 divider failed to enter correct operation within 16 clock cycles (the length of any state table in divide-by-8 configuration).

Table 7. State table of the 3.5-8 divider from Figure 49

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
1	1	0	0	0	1	1	1	1	Correct Divide-by-4 Operation
2	1	0	0	1	1	1	1	0	
3	1	0	1	1	1	1	0	0	
4	1	1	1	1	1	0	0	0	
5	0	1	1	1	0	0	0	0	
6	0	1	1	0	0	0	0	1	
7	0	1	0	0	0	0	1	1	
8	0	0	0	0	0	1	1	1	
9	1	0	0	0	1	1	1	1	
10	1	0	0	1	1	1	1	1	
11	1	0	1	1	1	1	0	0	
** swtich from divide-by 4 to divide-by-8 operation **									
12	0	1	1	1	1	0	0	0	Erroneous Divide-by-8 Operation
13	1	1	1	1	0	0	0	1	
14	1	1	1	0	0	0	1	0	
15	1	1	0	0	0	1	0	0	
16	1	0	0	0	1	0	0	0	
17	0	0	0	1	0	0	0	0	
18	0	0	1	0	0	0	0	1	
19	0	1	0	0	0	0	1	1	
20	1	0	0	0	0	1	1	1	
21	0	0	0	0	1	1	1	0	
**	0	0	0	1	1	1	0	1	*** Non-observable state*
22	0	0	0	0	0	0	0	0	Correct Divide-by-8 Operation
23	0	0	0	0	0	0	0	1	
24	0	0	0	0	0	0	1	1	
25	0	0	0	0	0	1	1	1	
26	0	0	0	0	1	1	1	1	
27	0	0	0	1	1	1	1	1	
28	0	0	1	1	1	1	1	1	
29	0	1	1	1	1	1	1	1	
30	1	1	1	1	1	1	1	1	
31	1	1	1	1	1	1	1	0	
32	1	1	1	1	1	1	0	0	
33	1	1	1	1	1	0	0	0	
34	1	1	1	1	0	0	0	0	
35	1	1	1	0	0	0	0	0	
36	1	1	0	0	0	0	0	0	
37	1	0	0	0	0	0	0	0	
38	0	0	0	0	0	0	0	0	
39	0	0	0	0	0	0	0	1	
40	0	0	0	0	0	0	1	1	

CHAPTER 6: CONCLUSION

6.1 Original contributions of this research

This research work demonstrates a novel solution for multi-modulus prescaler design and error correction that advance the state of the art. The common dual-modulus approach that is used in most prescaler designs allows for fractional-N division, but requires the range of moduli to be relatively high. This dissertation describes a cascaded, multi-modulus structure that is not limited in this way. To achieve fractional-N division without using a dual-modulus approach, a divider capable of half-integer division is implemented using a double-edge triggered, CML DFF technique. This prescaler design required the development a novel error correction scheme that can be implemented with drastically lower penalties to chip area and power consumption as seen in other error correction schemes.

- Successful development of SiGe-based, high-resolution, low-range, multi-modulus prescaler
- Development of configurable, 8-bit, ½-integer divider using double-edge triggered, current-mode logic DFFs
- Design of high-speed, extreme environment capable, CML gates in SiGe
- Numerical analysis for determining minimal, comprehensive error correction solution for division-by-3.5 to 8
- First demonstration of configurable frequency divider with comprehensive error detection and correction with minimal increase in chip area (10%) and power consumption (22%).

6.2 Potential directions for future work

Future work for the multi-modulus prescaler could involve examining several avenues for reducing power consumption. The current multi-modulus prescaler design allows all DFFs to remain biased, even when the prescaler is configured in a manner in which some DFFs are not used. The power consumption of the multi-modulus prescaler could be reduced for lower division ratios by deactivating unused DFFs in both dividers, particularly the 3.5-8 divider. A simple logic circuit could be implemented that leverages the existing prescaler control bits that would turn off the bias currents supplied to unused DFFs for a given prescaler configuration. Such a logic circuit would use static signals and could be implemented with negligible chip area

increase. Implementing such a scheme could potentially reduce the current consumption of the prescaler by as much as 52% for the lowest configurable modulus.

Another avenue for reducing prescaler power consumption could be the implementation of an adaptive bias scheme. Due to the lack of device models below −55°C, the current version of the prescaler was implemented with a constant current bias to minimize risk associated with uncertainty in device behavior at low temperature. Successfully characterizing the HBT behavior in this low-temperature region would allow a more aggressive biasing scheme to be implemented without incurring excessive risk to prescaler functionality.

The minimum operating supply voltage of the multi-modulus prescaler is directly related to the base-emitter voltage of the HBT devices. The supply voltage must be high enough to maintain forward-active operation of the switching HBTs in each cell of the multi-modulus prescaler. To meet this requirement, the supply voltage must be greater than three base-emitter voltages plus the voltage drop of the CML resistor. Using a room temperature base-emitter voltage of ~720 mV and the 200 mV CML resistor drop, the minimum supply voltage for the current multi-modulus prescaler is approximately 2.36 V at room temperature. Simulations of the HBT device used throughout the prescaler design show a base-emitter temperature coefficient of approximately −1.15 mV/°C for constant current bias. Using this value, the approximate, minimum supply voltage of the multi-modulus prescaler as a function of temperature is shown in Figure 50. The temperature coefficient of the HBT, however, is not truly linear and minimum supply voltages at very low temperatures are actually lower than predicted in Figure 50. Future work for the prescaler could aim toward reducing the required supply voltage (and therefore power consumption) by designing CML (or other logic families) gates that require fewer than 3 base-emitter voltage drops to properly operate. This would also allow the prescaler design to be ported to a lower-supply voltage technology node.

Another avenue for future work could investigate expanding the error correction scheme to a wider/higher range of moduli. This investigation could involve determining the increase in minimal error correction complexity for higher division ratios as well as for a wider range. Determining the range of moduli for which a single error correction circuit solution is viable could greatly expand the potential applications of this error correction concept.

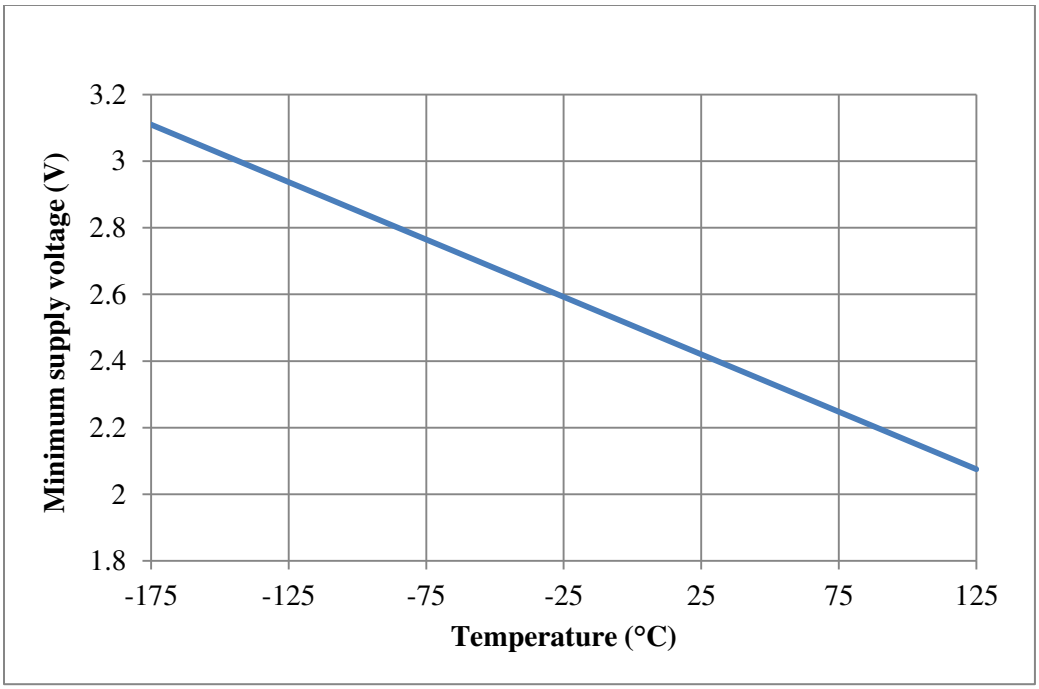

Figure 50. Minimum supply voltage of multi-modulus prescaler (constant current bias, −1.15 mV/°C base-emitter temperature coefficient)

6.3 Conclusion

This dissertation outlines the development of a novel GHz-range, high division resolution, multi-modulus prescaler capable of operating in extreme environments. A review of SiGe BiCMOS technology and high-speed logic design was performed for background information of this research work. An extensive literature review of existing prescaler technology applicable to this research was performed. This literature review highlighted the gap in the state-of-the-art that exists for prescalers meeting the demanding requirements outlined in Chapter 2 of this dissertation. A new design approach was used to develop a prescaler capable of high division resolution for a low range of divisors. This approach required the development of error correction circuits able to detect and correct any erroneous divider operation for any divider configuration. These error correction circuits induce minimal chip are and power overhead and were implemented such that they do not alter the normal operation of the prescaler. The designs for the building blocks of the 4/5/6 and 3.5-8 dividers were described, which include DFFs, AND gates, and multiplexers. Block-level simulation results for the 4/5/6 and 3.5-8 dividers were presented to verify the functionality of the multi-modulus prescaler solution. Measurements of

the fabricated prescaler were taken to verify functionality and measure current consumption over the full operating temperature range. Phase noise measurements were made to qualitatively examine the phase noise contribution of the prescaler. Finally, an error correction testing method was described, which allowed the prescaler to be forced into erroneous operation and demonstrate successful recovery and return to correct operation.

REFERENCES

[1] J. R. Vig, "Introduction to Quartz Frequency Standards," *Research and Development Technical Report*, U.S. Army Electronics Technology and Devices Laboratory, March 1992.
[2] T. H. Lee, "Phase-locked loops," in *The Design of CMOS Radio Frequency Integrated Circuits*, 2nd edition, New York, NY: Cambridge University Press, 2004, pp. 560-563.
[3] F. M. Gardner, *Phaselock Techniques*, 3rd edition, Hoboken, NJ: John Wiley and Sons Inc., 2005.
[4] R. L. Pease, A. H. Johnston, and J. L. Azarewicz, "Radiation Testing of Semiconductor Devices for Space Electronics," *Proceedings of the IEEE*, vol. 76, no. 11, pp. 1510-1526, 1988.
[5] A. Hammoud, R. L. Patterson, S. Gerber, and M. Elbuluk, "Electronic Components and Circuits for Extreme Temperature Environments," *10th IEEE International Conference on Electronics, Circuits, and Systems*, vol. 1, pp 44-47, 2003.
[6] E. A. Gutierrez-D, M. J. Deen, and C. L. Claeys, "," *Low Temperature Electronics: Physics, Devices, Circuits, and Applications*, 1st edition, Waltham, MA: Academic Press, 2000, pp. .
[7] T. R. Oldham, A. J. Lelis, H. E. Boesch, J. M. Benedetto, F. B. McLean, and J. M. McGarrity, "Post-irradiation effects in field-oxide isolation structures," *IEEE Transactions on Nuclear Science*, vol. 34, no. 6, pp. 1184-1189, Dec. 1987.
[8] H. J. Barnaby, "Total-ionizing-dose effects in modern CMOS technology," *IEEE Transactions on Nuclear Science*, vol. 53, no. 6, pp. 1184-1189, Dec. 2006.
[9] V. Gromov, A. J. Annema, R. Kluit, J. L. Visschers, and P. Timmer, "A radiation hard bandgap reference circuit in a standard 0.13 µm CMOS technology," *IEEE Transactions on Nuclear Science*, vol. 54, no. 6, pp. 2727-2733, Dec. 2007.
[10] B. M. McCue, B. J. Blalock, C. L. Britton, J. Potts, J. Kemerling, K. Isihara, and M. T. Leines, "A wide temperature, radiation tolerant, CMOS-compatible precision voltage reference for extreme radiation environment instrumentation systems," *IEEE Transactions on Nuclear Science*, vol. 60, no. 3, pp. 2272-2279, Dec. 2007.
[11] J. D. Cressler, "SiGe HBT technology: A new contender for Si-based RF and microwave circuit applications," *IEEE Transactions on Microwave Theory and Techniques*, vol. 46, no. 5, pp. 572-589, May 1998.
[12] E.F. Crabbe, G. L. Patton, J. M. Stork, J. H. Comfort, B. S. Meyerson, and J. Y.-C. Sun, "Low temperature operation of Si and SiGe bipolar transistors," *International Electron Devices Meeting*, pp. 17-20, Dec. 1990.
[13] D. L. Harame, J. M. Stork, B. S. Meyerson, et. al., "Optimization of SiGe HBT technology for high speed analog and mixed-signal applications," *International Electron Devices Meeting*, pp. 71-74, Dec. 1993.
[14] J. D. Cressler, "SiGe BiCMOS technology: An IC design platform for extreme environment electronic applications," *45th Annual IEEE International Reliability Physics Symposium*, pp. 141-149, April 2007.
[15] E. O. Johnson, "Physical limitations on frequency and power parameters of transistors," *International Convention Record*, vol. 13, pp. 27-34, Mar. 1966.
[16] J. D. Cressler, "Silicon-germanium as an enabling technology for extreme environment electronics," *IEEE Transactions on Device and Materials Reliability*, vol. 10, no. 4, pp. 437-448, Dec. 2010.
[17] S. Kang, Y. Leblebici, *CMOS Digital Integrated Circuits: Analysis and Design*, 3rd edition, New York, NY: The McGraw-Hill Companies Inc., 2003, pp. 203-211, 222-225.

[18] L. S. Garrett, "Integrated-circuit digital logic families: III-ECL and MOS devices," *IEEE Spectrum*, vol. 7, issue 12, pp. 30-42, Aug. 2009.
[19] H. Hoshino, R. Tachibana, T. Mitomo, et. al., "A 60-GHz phase-locked loop with inductor-less prescaler in 90-nm CMOS," *33rd European Solid State Circuits Conference*, pp. 472-475, Sept. 2007.
[20] T. Luo, S. Bai, et. al., "A 43 GHz 0.13µm CMOS prescaler," *2008 IEEE Radio and Wireless Symposium*, pp. 179-182, Jan. 2008.
[21] C. Lee, L. Cho, and S. Liu, "A 44 GHz dual-modulus divide-by-4/5 prescaler in 90nm CMOS technology," *IEEE 2006 Custom Integrated Circuits Conference*, pp. 397-400, Sept. 2006.
[22] Y. Ding and Kenneth K., "A 21-GHz 8-modulus prescaler and a 20-GHz phase-locked loop fabricated in 130-nm CMOS," *IEEE Journal of Solid State Circuits*, vol. 42, no. 6, pp. 1240-1249, May 2007.
[23] H. Wei, Y. Chang, et. al., "A high-speed HBT prescaler based on the divide-by-two topology," *Asia-Pacific Microwave Conference 2007*, pp. 1-4, Dec. 2007.
[24] V. Zackriya and H. Kittur, "90nm CMOS lop power multimodulus 32/33/39/40/47/48 prescaler with METSPC based logic," *Third International Conference on Advances in Computing and Communications*, pp. 243-247, Aug. 2013.
[25] X. Lei, Z. Wang, K. Wang, and X. Wang, "A high speed low power pulse swallow frequency divider for DRM/DAB frequency synthesizer," *International Conference on Wireless Communications and Signal Processing*, pp. 1-4, Nov. 2009.
[26] A. Wafa and A. Ahmed, "High-speed RF multi-modulus prescaler architecture for Σ-Δ fractional-N PLL frequency synthesizers," *2004 International Symposium on Circuits and Systems*, vol. 4, pp. IV – 241-244, May 2004.
[27] D. Martynenko, G. Fisher, and O. Klymenko, "A low power programmable frequency divider intended for frequency synthesizer designed in accordance with IEEE 802.15.4a standard," *IEEE International Conference on Circuits and Systems*, pp. 21-26, Oct. 2012.
[28] S. Tseng, H. Wei, et. al., "True 50% duty-cycle high speed divider with the modulus of odd numbers," *Asia Pacific Microwave Conference*, pp. 305-308, Dec. 2009.
[29] H. Huang, S. Ho, and H. Su, "A dual-modulus prescaler using double-edge-triggered D-flip-flops," *IEEE 46th Midwest Symposium on Circuits and Systems*, vol. 1, pp. 209-212, Dec. 2003.
[30] X. Yu, M. Do, et. al., "Low power high-speed CMOS dual-modulus prescaler design with imbalanced phase-switching technique," *IEEE Proceedings on Circuits, Devices and Systems*, vol. 152, iss. 2, pp. 127-132, Apr. 2005.
[31] Q. Yuan, H. Yang, et. al., "Time borrowing technique for design of low-power high-speed multi-modulus prescaler in frequency syntheszier," *IEEE International Symposium on Circuits and Systems*, pp. 1004-1007, May 2008.

[32] L. Wang, S. Yue, Y. Zhao, and L. Fan, "An SEU-tolerant programmable frequency divider,"*8th International Symposium on Quality Electronic Design*, pp. 899-904, Mar. 2007.

[33] X. She and N. Li, "Single event transient tolerant frequency divider," *IET Computers and Digital Techniques*, vol. 8, iss. 3, pp. 140-147, June 2014.
[34] Mo, William Y., "Radiation Hardened Programmable Phase Frequency Divider," International Business Machines Corporation, assignee. Patent 7474134 B2. 06 Jan. 2009.
[35] G. Lyons, "A high performance rad hard 2-3 GHz integer N CMOS phase lock loop," *Radiation Effects Data Workshop*, pp. 41-45, Jul. 1999.
[36] P. Zhu, P. Gui, et. al., "A 400MHz-2.4GHz radiation-tolerant self-biased phase locked loop," *6th IEEE Dallas Circuits and Systems Workshop on System-on-Chip*, pp. 1-4, Nov. 2007.
[37] G. Lyons, "1.1 Ghz integer N phase lock loop with superior single event upset and total dose properties suitable for commercial space applications," *IEEE International SOI Conference*, pp. 101-102, Oct. 1998.
[38] P. Ghosh, "A 2.5 GHz radiation hard fully self-biased PLL using 0.25 µm SOS-CMOS technology," *IEEE International Conference on IC Design and Technology*, pp. 121-124, May 2009.
[39] D. Pan, "A radiation-hard phase-locked loop," *IEEE International Symposium on Industrial Electronics*, vol. 2, pp. 901-906, June 2003.
[40] D. Matsuura, K. Hirose, et. al., "Radiation-hardened phase-locked loop fabricated in 200 nm SOI-CMOS," *12th European Conference on Radiation and Its Effects on Components and Systems*, pp. 150-155, Sept. 2011.
[41] T. Toifl and P. Moreira, "A radiation-hard 80 MHz phase locked loop for clock and data recovery," *IEEE International Symposium on Circuits and Systems*, vol. 2, pp. 524-527, Jul. 1999.
[42] J. McGregor, D. Roulston, et. al., "A simple expression for ECL propagation delay including non-quasi-static effects," *Solid-State Electronics*, vol. 36, no. 3, pp. 391-396, 1993.
[43] K. Sharaf and M. Elmasry, "An accurate analytical Propagation delay model for high-speed CML bipolar circuits," *IEEE Journal of Solid State Circuits*, vol. 29, no. 1, pp. 31-45, Jan. 1994.
[44] V. Kakani, F. Dai, and R. Jaeger, "Delay analysis and optimal biasing for high speed low power current mode logic circuits," *2004 International Symposium on Circuits and Systems*, vol. 2, pp. II – 869-872, May 2004.
[45] T. Hancock and G. Rebeiz, "Design and analysis of a 70-ps SiGe Differential RF switch," *IEEE Transactions on Microwave Theory and Techniques*, vol. 53, iss. 7, pp. 2403-2410, July 2005.
[46] P. Heydari and R. Mohavavelu, "Design of ultra high-speed CMOS CML buffers and latches," *IEEE Transactions on VLSI Systems*, vol. 12, iss. 10, pp. 1081-1093, Oct. 2004.

VITA

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