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A GSM/EDGE/WCDMA Modulator With On-Chip D/A Converter for Base Stations

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***Abstract*—A global system for mobile communication (GSM)/enhanced data rates for GSM evolution (EDGE)/wideband code division multiple access (WCDMA) modulator with a 14-bit on-chip digital-to-analog (D/A) converter is presented. The modulator consists of several digital signal processing building blocks, including a programmable pulse shaping filter, interpolation filters, resampler, cordinate rotation digital computer (CORDIC) rotator, programmable output power level controller and ramping unit, and x/sinx filter. The precompensation filter, which compensates the sinc droop above the Nyquist frequency, makes it possible to use WCDMA signal images for up-conversion. The new programmable up/down unit allows power ramping on a time-slot basis as specified for GSM, EDGE and time division duplex (TDD)-WCDMA. The multistandard modulator meets the spectral, phase and error vector magnitude (EVM) specifications. The die area of the chip is 22.09 mm^2 in 0.35-μm CMOS technology. Power consumption is 1.7 W at 3.3 V with 110 MHz.**

***Index Terms*—Cordinate rotation digital computer (CORDIC), current steering digital-to-analog (D/A) converter, multicarrier, multistandard modulator, power control, power ramping, resampler.**

I. Introduction

THE global system for mobile communication (GSM) is a second generation (2G) system that has rapidly gained acceptance and a worldwide market share. As the mobile communications market develops, interest is building up in data applications and higher data rate operations. Short message services (SMS) were first added to the GSM system followed by high-speed circuit switched data (HSCSD) and the general packet radio service (GPRS). All of these services use the same modulation format as the original GSM network [0.3 Gaussian minimum shift keying (GMSK)], and change the allocation of the bits and/or packets to improve the basic GSM data rate. As a step toward 3G, enhanced data rates for GSM evolution (EDGE) provides a higher data-rate enhancement of GSM. It uses the GSM infrastructure with upgraded radio equipment to deliver significantly higher data rates. The primary objective of the EDGE signal is to triple the on-air data rate while taking up essentially the same bandwidth as the original 0.3 GMSK signal. The wideband code division multiple access (WCDMA) was selected by the European Telecommunications Standards Institute (ETSI) for wideband wireless access to support 3G services because of its resistance to multipath fading, and other advantages such as increased capacity. This technology has a wider bandwidth and different modulation format from GSM or EDGE.

The first generation of the 3G base station modulator should include support for GSM, EDGE and WCDMA. The digital IF modulator is designed using specifications related to those standards [1]–[3]. The main requirements of the modulator are shown in Table I. By programming the GSM/EDGE/WCDMA modulator, different carrier spacings, modulation schemes, power ramping, frequency hopping and symbol rates can be achieved. By combining the outputs of multiple modulators, multicarrier signals can be formed, or the modulator chips can be used for steering a phased array antenna. The formation of multicarrier signals in the modulator increases the base station capacity. The major limiting factor of digital IF modulator performance at base station applications is the digital-to-analog (D/A) converter, because the development of D/A converters does not keep up with the capabilities of digital signal processing with faster technologies [4].

The paper is organized as follows. Section II provides a description of the multistandard modulator. The new ramp generator and output power level controller is described in Section III. The up-conversion by using the images of the D/A converter is described in Section IV. The on-chip D/A converter is described in Section V. Finally, experimental results obtained from the chip are presented in Section VI; these are followed by a few concluding comments.

II. GSM/EDGE/WCDMA Modulator

The block diagram of the modulator chip is shown in Fig. 1. The use of different modulation formats requires programmable pulse shaping filter coefficients. The reconfiguration of new modulation formats can be done between bursts (e.g., GSM/EDGE). The two half-band filters increase preoversampling ratios, which reduce the complexity of the resampler (the order of the polynomial interpolator). The resampler circuit allows the sampling rate of the on-chip D/A converter to have a variable noninteger relationship with the input symbol rates [5]. This block is needed, because the specified D/A converter sampling rates and input symbol rates shown in Table I do not have integer frequency relationship. The coordinate rotation digital computer (CORDIC) rotator translates the baseband-centered spectrum to a programmable carrier center frequency [6]. The IF signal is filtered by an x/sinx filter for compensating the sample and hold response of the on-chip 14 bit D/A converter [7]. The internal wordlengths

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TABLE I
GSM/EDGE/WCDMA MODULATOR SPECIFICATIONS

Symbol rates/Chip rate	270.833 ksym/s (GSM/EDGE) 3.84 Msym/s (WCDMA)
Modulations	GMSK with BT = 0.3 (GSM), linearized Gaussian 3π/8-8PSK (EDGE), M-QAM (WCDMA)
Carrier Spacing	200 kHz (GSM/EDGE), 5 MHz (WCDMA)
Frequency error	2 Hz
Spurious Free Dynamic Range	-80 dBc
D/A converter sampling frequency	65 – 110 MHz
Power ramp duration	5 - 15 μs
Power ramp curve type	Hanning, Hamming, Blackman
Power control range	0 - -32 dB
Power control fine tuning step	0.25 dB

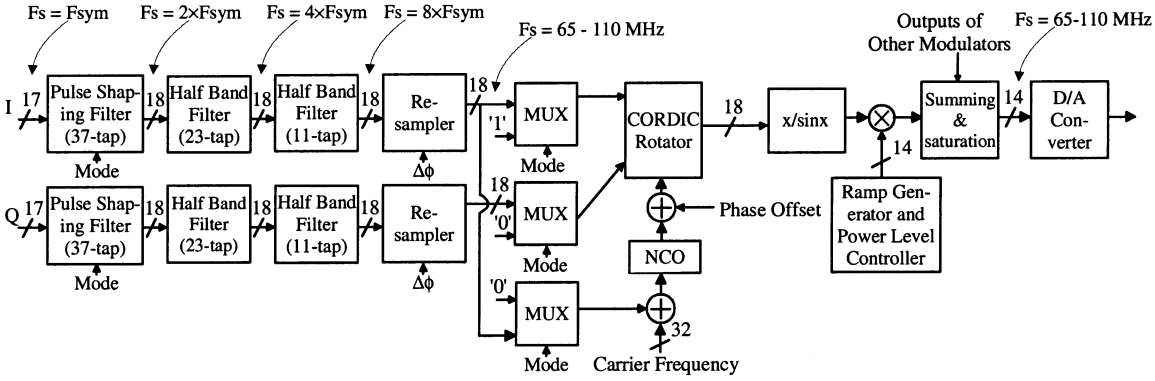

Fig. 1. GSM/EDGE/WCDMA modulator chip. The symbol rates (Fsym) are shown in Table I.

of the modulator are shown in Fig. 1. The wordlengths were chosen such that the 14-bit D/A converter quantization noise dominates the digital output noise.

A. Pulse Shaping and Half-Band Filters

The input symbols are filtered using Gaussian (BT = 0.3)/linearized Gaussian/square root raised cosine ($\alpha = 0.22$) pulse shaping filter in GSM/EDGE/WCDMA mode, respectively [8], [3]. The square root raised cosine filter (excess bandwidth ratio $\alpha = 0.22$) was designed to maximize the ratio of the main channel power to the adjacent channels' power under the constraint that the error vector magnitude (EVM) is below 2% [9]. In the GSM/EDGE systems a quarter of a guard bit is inserted after each burst, resulting a burst length of 156.25 symbols [10]. Therefore, the input symbols to the pulse shaping filter have to be oversampled by 4 in the GSM and EDGE modes. The pulse shaping filter is implemented using programmable canonic signed digit (CSD) coefficients [11].

The pulse shaping and the half-band filters are implemented using a polyphase structure [12]. Taking advantage of the fact that in the modulator data streams in the I and Q paths are processed with the same functional blocks, a further hardware reduction can be achieved by pipeline interleaving techniques [13]. The pulse shaping and the half-band filters are modified to handle two channels by doubling the sampling rate and delay elements between taps. This results in a more efficient layout with a penalty in terms of increased power dissipation. The fixed coefficients of the half-band filters are implemented using CSD numbers [14].

B. Resampler

The resampler consists of a resampling numerically controlled oscillator (NCO) and a cubic Lagrange polynomial interpolator shown in Fig. 2. The resampling NCO supplies sampling clocks for resampler (clk1), half-band and pulse shaping filters (clk1, clk1/2, clk1/4) as well as the trigger signal for the input data symbols (clk1/8). The frequency control word ($\Delta\phi$) is calculated from the ratio of the input sampling rate of the resampler (clk1) to output sampling rate (clk). The trigger signals for different input symbol rates could be achieved by altering the frequency control word. The output of the resampling NCO (μ_k) may be considered to represent the phase offset between the input sampling rate of the resampler (clk1) to the output sampling rate (clk). Since the phase offset changes on every output sample clock cycle, the interpolation filter coefficients are time-varying. The time-varying filter coefficients with long period can be easily implemented by polynomial-based interpolation filters using so called Farrow structure [15]. The cubic Lagrange polynomial interpolator was found suitable for our application, because it fulfills spectral and time domain (phase error and EVM) specifications [1]–[3]. The cubic Lagrange polynomial interpolator is implemented with Farrow structure [5], where the number of unit delay elements is minimized as in Fig. 2. Furthermore, the frequency

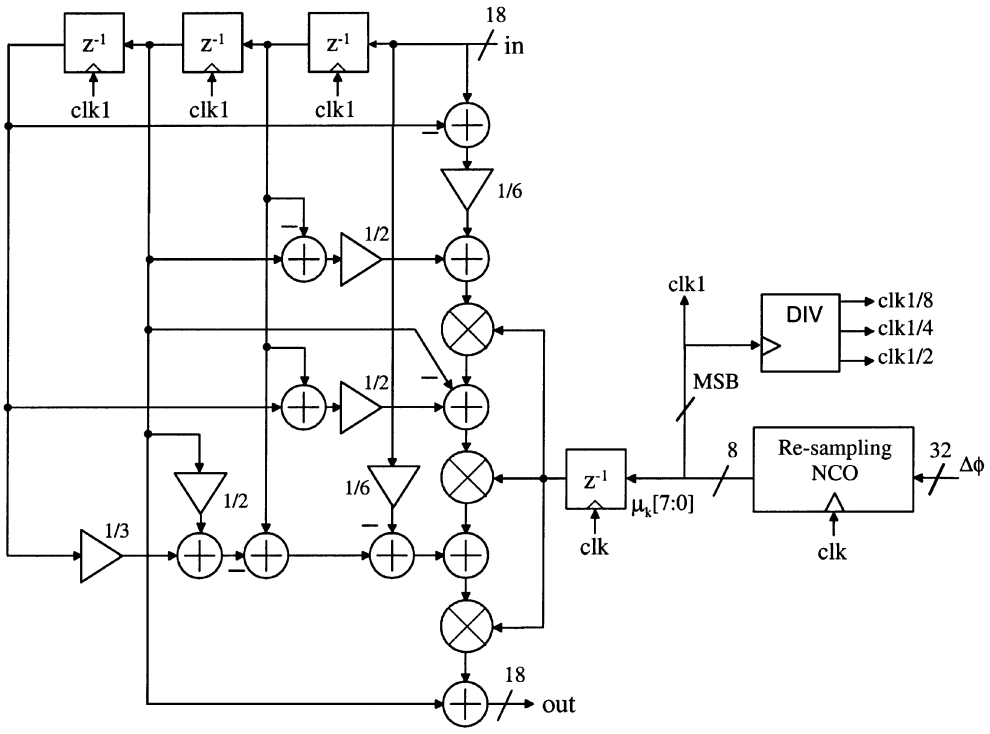

Fig. 2. Resampler.

error term generated by the external digital phase locked loop (DPLL) locking to an external symbol rate could be added to the frequency control word ($\Delta\phi$).

C. CORDIC Rotator

The in-phase output of the CORDIC rotator is

$$I_{\text{out}}(n) = I(n)\cos(\omega_{\text{NCO}}n) \pm Q(n)\sin(\omega_{\text{NCO}}n) \quad (1)$$

where $I(n)$, $Q(n)$ are pulse shaped and interpolated quadrature data symbols. The carrier frequency is

$$f_{\text{NCO}} = \frac{F_r F_s}{2^j}, -\frac{F_s}{2} \le f_{\text{NCO}} < \frac{F_s}{2} \quad (2)$$

where F_r is the j-bit carrier frequency control word which can range between $-2^{j-1} \le F_r < 2^{j-1}$, j is the NCO word length, and F_s is the sampling frequency. The carrier frequency resolution is found by setting $F_r = 1$

$$\Delta f_{\text{NCO}} = \frac{F_s}{2^j}. \quad (3)$$

The carrier frequency tuning resolution will be 0.0256 Hz by (3), when F_s is 110 MHz, and j is 32. The frequency resolution is better than the target frequency error specification in Table I. The sign in (1) is controlled by the frequency control word. The spectral inversion (modulation spectrum is reversed) in the other up-conversion stages could be compensated by changing the sign of the carrier frequency control word (the direction of the vector rotation) in (1).

In the frequency modulation mode (GMSK modulation in GSM [8]), the pulse shaped and interpolated I frequency samples are added to the carrier frequency control word, and the inputs of the CORDIC rotator are set constant [$I(n)$ is 1 and $Q(n)$ is 0] as in Fig. 1, then the output is from (1)

$$I_{\text{out}}(n) = \cos(\omega_{\text{NCO}}n + \theta(n)) \quad (4)$$

where θn is the information-bearing component of the phase. In the EDGE/WCDMA mode (quadrature amplitude modulation [8], [3]), the input to the adder before the NCO is set zero and I/Q samples are filtered by the pulse shaping filter and interpolated prior to the CORDIC rotator.

The phase offset adds an offset to the NCO. This allows multiple modulators to be synchronized in order to produce carriers with a known phase relationship. The phase offset allows intelligent management of the relative phase of independent carriers. This capability supports the requirements of phased array antenna architectures [16].

III. Ramp Generator and Output Power Level Controller

Summing the IF outputs from other devices allows the formation of a multicarrier signal in Fig. 1. This necessitates power control to be implemented in the digital domain. Otherwise, it would not be possible to adjust the relative power of a single carrier with respect to the others. Therefore, a digital ramp generator and output power level controller is used as in Fig. 1. The power control is realized by scaling the ramp curve [17].

The programmable up/down unit allows power ramping on a time-slot basis as specified for GSM, EDGE and time division duplex WCDMA (TDD-WCDMA) [1], [2]. The ramp generator is based on a recursive digital sine wave oscillator [17]. In previous work [17], the ramp duration was fixed and the ramp generator could only generate cosine windows that have only one

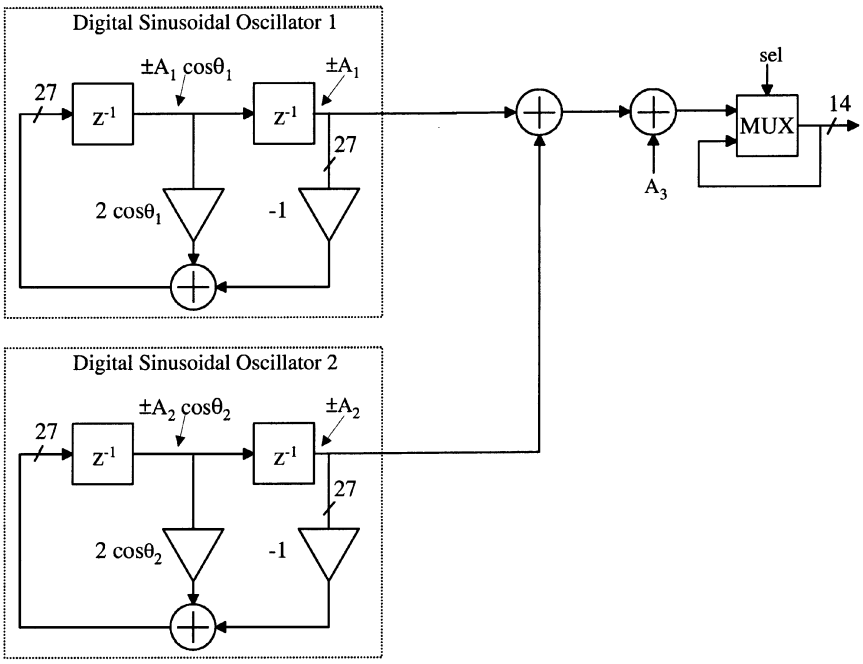

Fig. 3. Ramp generator and output power level controller.

cosine term (e.g., a Hanning window). In Fig. 3, two digital oscillators are used; these allow the Blackman window generation (two cosine terms). The Blackman window gives more attenuation to the switching transients than the Hanning window.

Another method for implementing the ramp generator is to use a look-up table LUT. Because the sampling frequency is high, the size of the LUT becomes large. The size of the LUT increases even more because of the high oversampling ratio required by the variable ramp duration (see Table I). Alternatively, interpolation between the samples in the LUT can be used at the expense of increased complexity. Furthermore, the multiplier is needed to set the output power level. Therefore, the choice was made in favor of the recursive digital oscillators.

A. Ramp Generator

The ramp generator shown in Fig. 3 has two recursive digital sine wave oscillators. Their difference equation comprises one multiplication operation and one subtraction

$$x(n+2) = \alpha x(n+1) - x(n) \tag{5}$$

where

$$\alpha = 2\cos(\theta_0). \tag{6}$$

The angle θ_0 represented by the oscillator coefficient is given by

$$\theta_0 = 2\pi f_0/F_s \tag{7}$$

where f_0 is the desired frequency. Solving the one-sided z transform of (5) leads to

$$X(z) = \frac{(z^2 - \alpha z)x(0) + zx(1)}{z^2 - \alpha z + 1} \tag{8}$$

where $x(0)$ and $x(1)$ are the initial values of state variables. Choosing the initial values of the state variables to be $x(1) = A\cos\theta_0$ and $x(0) = A$, we obtain from (8) a discrete-time sinusoidal function as the output signal

$$X(z) = \frac{A(z^2 - \cos\theta_0 z)}{z^2 - 2\cos\theta_0 z + 1}. \tag{9}$$

The equation has complex-conjugate poles at $p = \exp(\pm j\theta_0)$, and an impulse response

$$x(n) = A\cos(n\theta_0), \qquad n \geq 0. \tag{10}$$

The impulse response of the second-order system with complex-conjugate poles on the unit circle is a sinusoidal waveform. An initial phase offset φ_0 can be realized [18], namely

$$x(n) = A\cos(\theta_0 n + \varphi_0) \tag{11}$$

by choosing the initial values

$$x(1) = A\cos(\theta_0 + \varphi_0) \tag{12}$$

$$x(0) = A\cos(\varphi_0). \tag{13}$$

The amplitude and phase is determined by the initial values $x(0)$ and $x(1)$. The output frequency of the digital oscillator (θ_0) can be altered by changing the coefficient α in (5) and the initial value in (12). The details and finite wordlength effects of the digital ramp generator and output power level controller are described in [17].

B. Initial Values of the Ramp Generator

The rising ramp of the Blackman window is given by

$$0.42A + 0.5A\cos(\pi t/T_r + \pi) + 0.08A\cos(2\pi t/T_r) \tag{14}$$

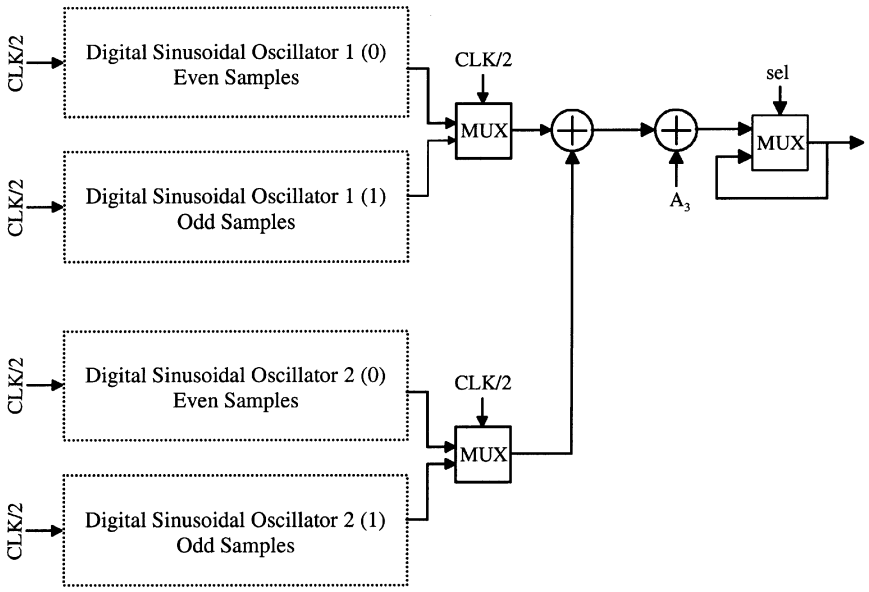

Fig. 4. Parallel structure.

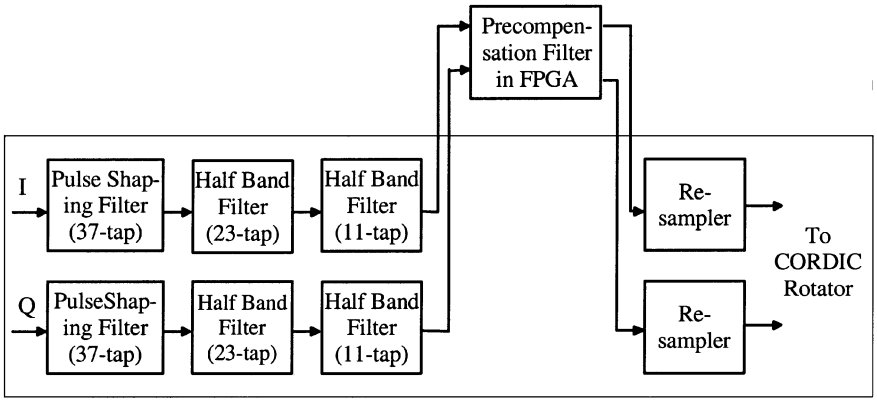

Fig. 5. Off-chip precompensation filter at baseband.

where T_r is the ramp duration, t is [0; T_r], and A is the amplitude of the ramp. The falling ramp of the Blackman ramp window is

$$0.42A + 0.5A\cos(\pi t/T_r) + 0.08A\cos(2\pi t/T_r). \quad (15)$$

The cosine terms are implemented with the digital sine wave oscillators and the term 0.42 A is added to their output. The initial values for the falling Blackman ramp are

$$x1(0) = 0.5A = A_1 \quad (16)$$

$$x1(1) = 0.5A\cos(\pi T_s/T_r) = A_1\cos(\theta_1) \quad (17)$$

for the first oscillator. The initial values of the second oscillator are

$$x2(0) = 0.08A = A_2 \quad (18)$$

$$x2(1) = 0.08A\cos(2\pi T_s/T_r) = A_2\cos(\theta_2). \quad (19)$$

The constant A_3 is $0.42A$. The initial values of the rising Blackman ramp for the first oscillator are the negatives of the falling ramp values. In the case of the Hanning window, the initial values are the same as in the Blackman case for the first oscillator, the values for the second oscillator are zero and the constant A_3 is $0.5A$. The ramp duration (T_r) can be altered by changing the output frequencies of the digital oscillators. The value (A) controls the amplitude of the ramp (output power level). During the ramp period the signal *sel* is low in Fig. 3 and the multiplexer conducts the ramp signal to the multiplier (Fig. 1). After the ramp duration (T_r) the signal *sel* becomes high; the output of the multiplexer is connected to the input of the multiplexer; and the output power level is constant.

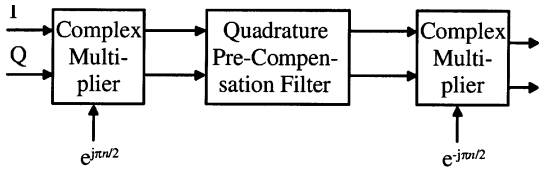

Fig. 6. Precompensation filter structure.

C. Parallel Structure

The recursive digital oscillator shown in Fig. 3 suffers from two major drawbacks: the quantization noise accumulates in the

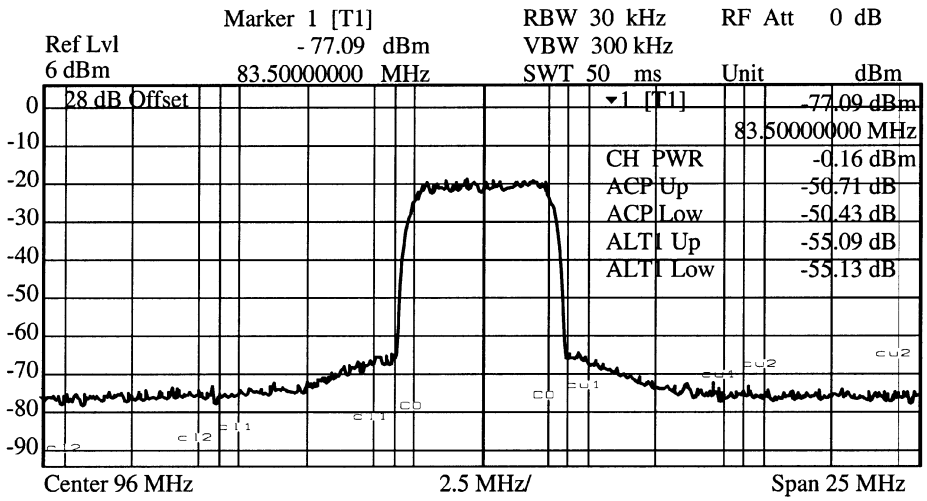

Fig. 7. Measured second image of the WCDMA signal.

recursive structure and the maximum sampling rate of the digital oscillator is determined by its recursive parts. The oscillator produces only one cycle of sine wave in the Blackman ramp and after that new initial values are updated, so the problem of the accumulated noise is alleviated. The parallel structure is used to reduce the sampling rate of the digital oscillators. Then the multipliers can be implemented with higher wordlengths but with a reasonable area, as the speed requirement is not so stringent. The idea of the implemented parallel structure is to generate the desired sinusoidal oscillating signal with two oscillators, one of which generates the odd samples, and the other the even samples. This means that four oscillators are needed to generate Blackman ramps. The parallel structure is presented in Fig. 4, where the sampling rate of the digital oscillator is halved. The odd and even oscillator outputs are alternately selected with a 2-to-1 multiplexer (MUX), the select signal of which is the divided clock. In order for the oscillators to generate correct samples to the multiplexer output, each oscillator must operate at a double output frequency (θ_0). A phase offset must be added to the odd oscillator so that the outputs are not duplicated. The initial values of the parallel ramp generator are calculated by choosing first the same initial values as in the normal case and calculating the next two values using the difference equation (5) and choosing the odd samples for the odd oscillators and the even samples for the even oscillators.

IV. Up-Conversion by Using Images of the D/A Converter

The output of the multistandard modulator can be heterodyned up to the desired frequency by employing a mixer/local oscillator/filter combination. An alternative method is to use images for up-conversion. To obtain frequencies above Nyquist frequencies, the output of the D/A converter is bandpass-filtered by an 'image-selecting' bandpass filter, rather than by the lowpass filter. The output spectrum of the ideal D/A converter is

$$|S(f)| = \left|\frac{\sin(\pi f/F_s)}{\pi f/F_s}\right| \sum_{n=-\infty}^{\infty} \sigma(f - nF_s \pm f_{\text{out}}) \qquad (20)$$

where F_s is the sampling rate of the D/A converter. The images exhibit significantly poorer signal to noise and distortion ratio (SNDR) than the fundamental signal does, because of the sinc attenuation. The amplitude of the image responses decreases according to $\text{sinc}(\pi f/F_s)$; spurious responses due to the D/A-converter clock feed-through noise and dynamic nonlinearities generally roll off much more slowly with the frequency. Nevertheless, the first and second image may still meet the system SNDR requirements. If an odd-numbered image is used, any modulation spectrum is inverted with respect to the fundamental output. The output spectrum in (1) can be inverted by changing the sign of the carrier frequency word.

The inverse sinc filter shown in Fig. 1 compensates for roll off in the first lobe of the $(\text{sinc}(x))$ frequency domain distortion function of the D/A converter. The sinc effect introduces a droop that is not acceptable when the bandwidth of the signal is wide (e.g., WCDMA signal [3]). If the distortions of the images are to be compensated, an additional precompensation filter is needed. The precompensation filter could be before the D/A converter. Locating the off-chip precompensation filter prior to the resampling operation allows the precompensation filter to run at a lower computational rate, as shown in Fig. 5.

In our case, the output signal of the D/A converter is precompensated so that the droop in the second image is canceled. The D/A converter sampling frequency is 76.8 MHz, the signal frequency is 19.2 MHz and the center frequency of the image is located at 96 MHz (76.8 MHz + 19.2 MHz). The peak error target specification is ± 0.045 dB over the frequency band from -2.5 MHz through 2.5 MHz (WCDMA channel spacing). The magnitude response of the precompensation filter is obtained from inverse of (20), where F_s is 76.8 MHz and f is 96 MHz $\pm$ 2.5 MHz. The precompensation of this frequency band is done at baseband (Fig. 5) and the inverse sinc filter in Fig. 1 is bypassed. The complex precompensation filter requires five taps with two CSD nonzero digits. These complex taps require a lot of hardware. An alternative method is to up-convert the baseband signal to $F_s/4$. Then the up-converted I and Q signals are filtered by the two real filters and after that, down-converted from $F_s/4$ to baseband. In this special case when the IF center frequency is equal to a quarter of the sample rate, considerable

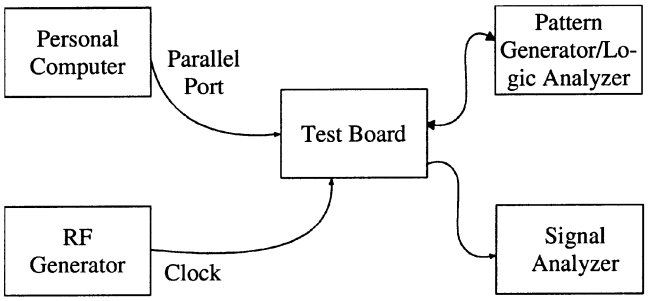

Fig. 8. Block diagram of test system.

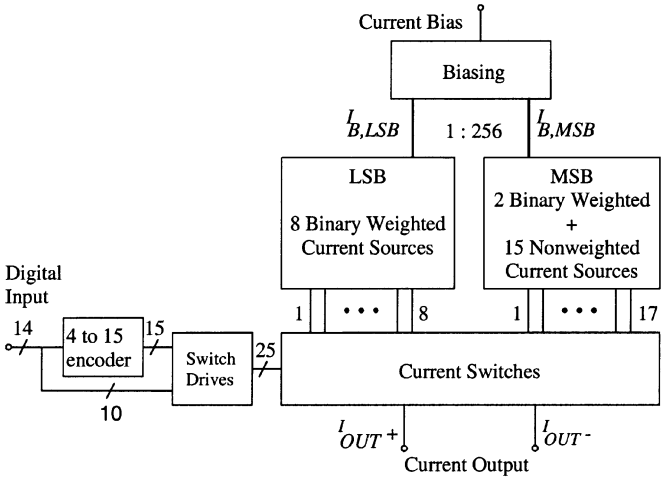

Fig. 9. Block diagram of the 14-b D/A converter.

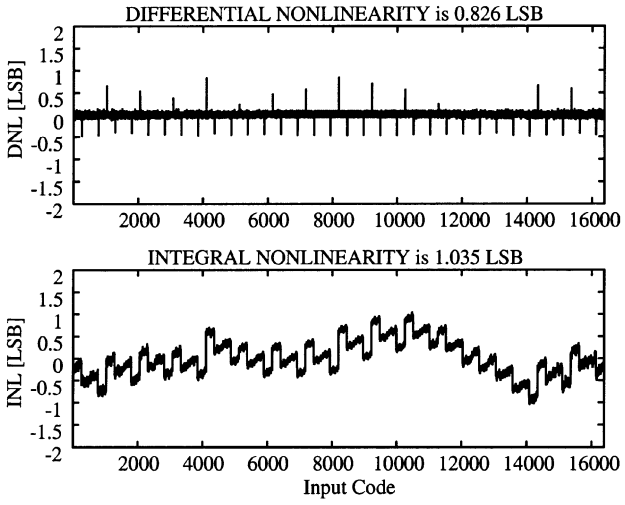

Fig. 10. Typical INL and DNL.

simplification is achieved since the sine and cosine signals representing the complex phasor degenerate into two simple sequences $[\cdots 0\ 1\ 0\ -1 \cdots]$ and $[\cdots 1\ 0\ -1\ 0 \cdots]$, thus eliminating the need for high-speed digital multipliers and adders to implement the mixing functions. The block diagram of this precompensation structure is shown in Fig. 6. The quadrature filter requires seven taps with two nonzero CSD digits.

The precompensation filters were implemented with an Altera FLEK 10KA-1 series device [19]. The complex filter requires 456 (26% of the total) logic elements (LEs) in the EPF10K30A device. The precompensation filter shown in Fig. 6 requires 416 (24% of the total) LEs in the EPF10K3A

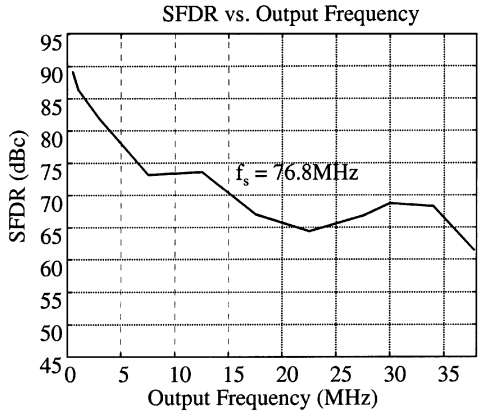

Fig. 11. SFDR as function of output frequency at full-scale (0 dBFS).

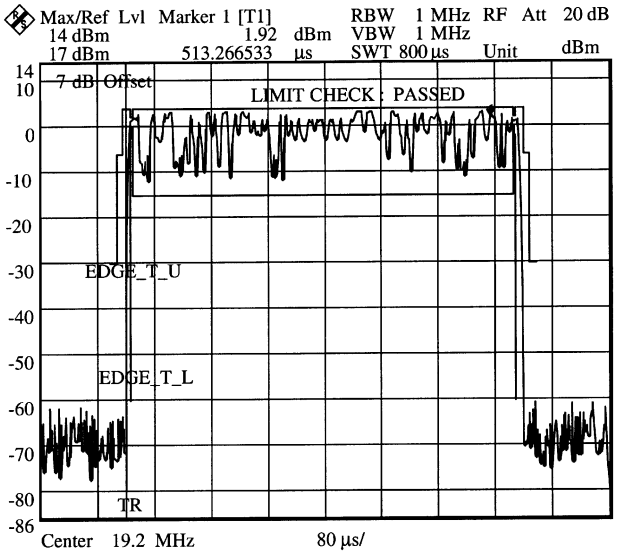

Fig. 12. Transmitted power level of the EDGE burst versus time. The carrier frequency is 19.2 MHz.

device. The precompensation filters were implemented by folded direct form structure [13]. Fig. 7 shows the second image of the precompensated WCDMA signal. The adjacent channel leakage power ratios are 50.43/55.09 dB, which meet specifications (45/50 dB) [3].

V. D/A Converter

As the multicarrier feature requires high dynamic range requirements for the D/A converter, the wordlength was chosen to be 14 bit. The 14-bit on-chip D/A converter is based on a segmented current steering architecture [20]. It consists of a 6b-MSB matrix (2-b binary and 4-b thermometer coded), and an 8-b binary coded LSB matrix (Fig. 9). The static linearity is achieved by sizing the current sources for intrinsic matching [20] and using layout techniques; this is a prerequisite for obtaining a good dynamic linearity. The cascode structure is used to increase the output impedance of the unit current source, which improves the linearity of the D/A-converter. The dynamic linearity is important in this IF modulator because of the strongly varying signal. Therefore, a well-designed and carefully laid out switch drivers and current switches are used. A major function of the switch driver in Fig. 9 is to adjust the

TABLE II
SPECTRUM DUE TO SWITCHING TRANSIENTS (PEAK–HOLD MEASUREMENT, 30 kHz FILTER BANDWIDTH, REFERENCE ≥300 kHz WITH ZERO OFFSET)

Offset (kHz)	Maximum Power Limit (dBc)		Measured Maximum Power (dBc) at Digital Output		Measured Maximum Power (dBc) at D/A converter Output	
	(GMSK)	(8-PSK)	(GMSK)	(8-PSK)	(GMSK)	(8-PSK)
400	- 60	-55	-77.3	-77.7	-65.64	-65.53
600	- 70	-65	-95.2	-94.2	-75.1	-75.36
1200	- 77	-77	-106.3	-106.8	-80.55	-78.57
1800	- 77	-77	-106.9	-107.7	-79.92	-79.23

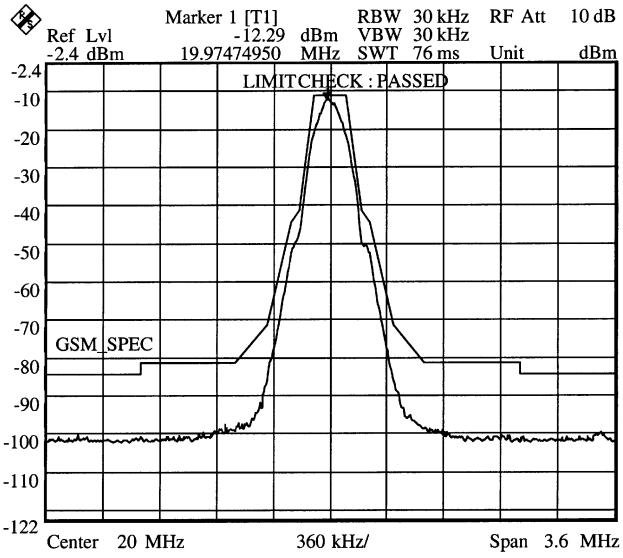

Fig. 13. Power spectrum of GSM signal.

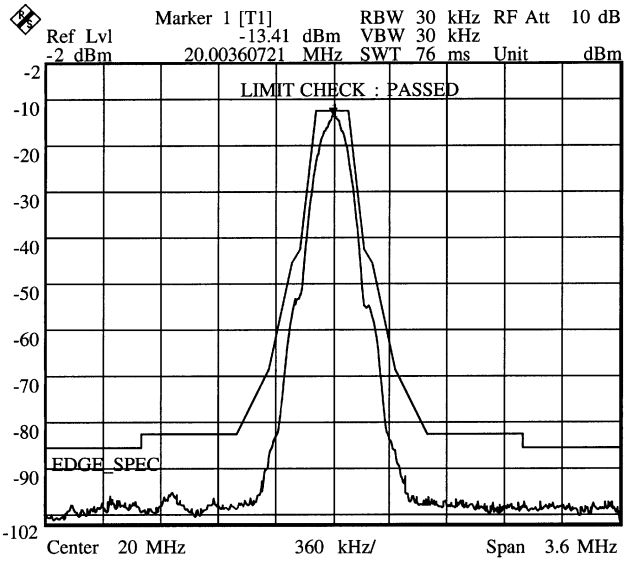

Fig. 14. Power spectrum of EDGE signal.

cross point of the control voltages, and to limit their amplitude at the gates of the current switches, in such a way that these transistors are never simultaneously in the off state and that the feedthrough is minimized. The crossing point of the control signals is set by delaying the falling edge of the signal [21]. Dummy switch transistors are used to improve the synchronization of the switch transistors control signals. Disturbances connected to the external bias current are filtered out on-chip with a simple one pole low-pass filter. The D/A-converter is implemented with a differential design, which results in reduced even-order distortions and provides a common-mode rejection to disturbances.

VI. MEASUREMENT RESULTS

To evaluate the multistandard modulator, a test board was built and a computer program was developed to control the measurements. Fig. 8 illustrates the block diagram of the multistandard modulator test system. The on-chip D/A converter was used in measurements. Measurements are performed with a 50 Ω doubly terminated cable. The sampling rate of the D/A converter was 76.8 MHz in the measurement. Fig. 10 shows that typical integral linearity (INL) and differential linearity (DNL) errors are 1.04/0.83 LSB, respectively. The spurious free dynamic range (SFDR) is shown as a function of the output frequency in Fig. 11. The SFDR to Nyquist frequency is better than

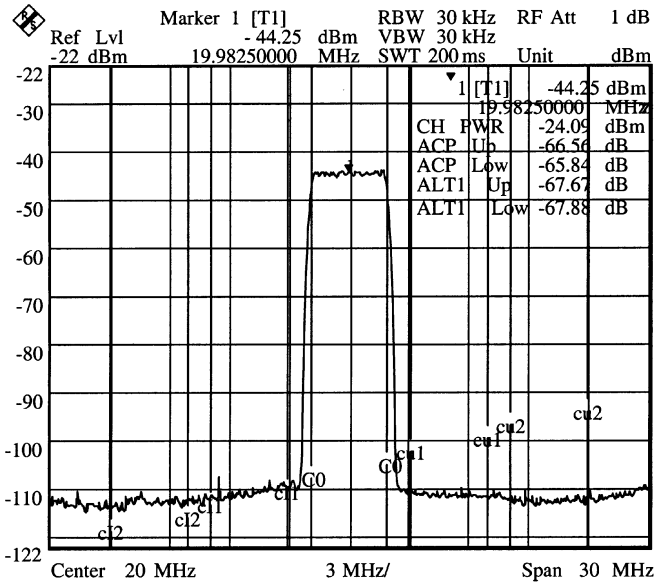

Fig. 15. Power spectrum of WCDMA signal.

80 dBc at low synthesized frequencies, decreasing to 62 dBc at high synthesized frequencies in the output frequency band (single tone).

Fig. 12 shows the measured ramp up and down profiles of the transmitted burst, which satisfy the EDGE base station masks.

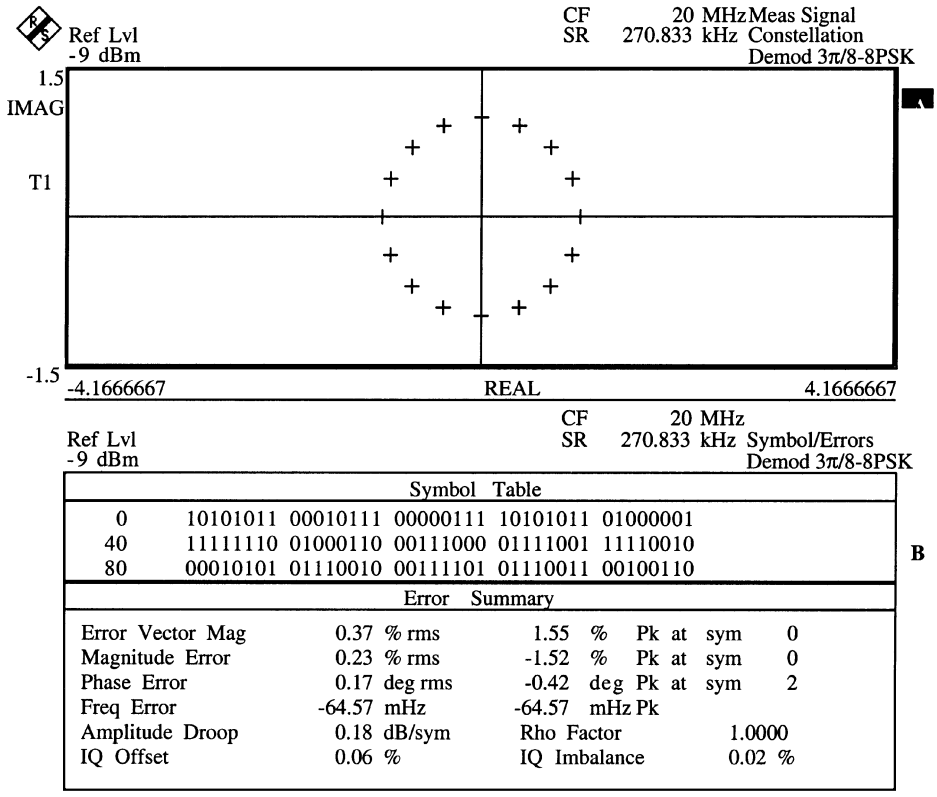

Fig. 16. Measured EVM errors in EDGE mode.

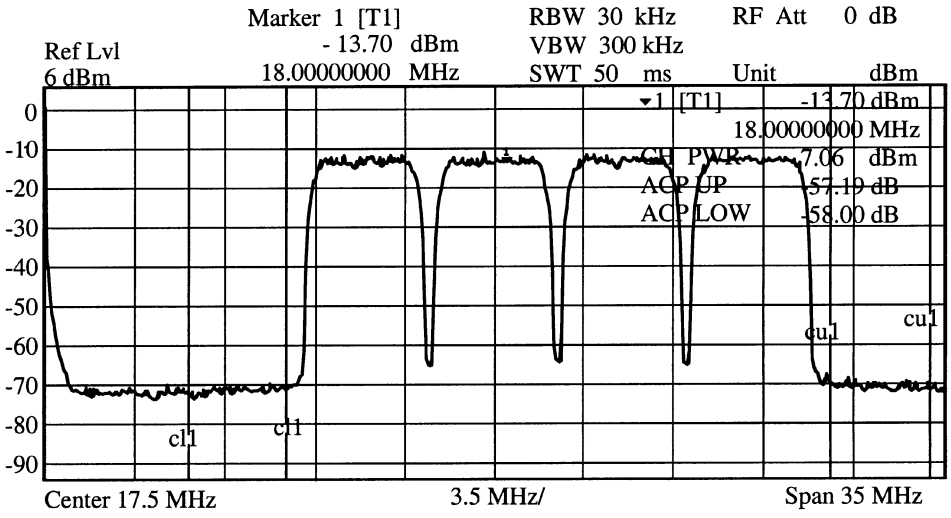

Fig. 17. Power spectrum of multicarrier WCDMA signal.

The allowed power of spurious responses originating from the power ramping before and after the bursts is specified by the switching transient limits. Some margin (3 dB) has been left between the values in [1] and the values specified for this implementation in Table II to take care of the other transmitter stages that might degrade the spectral purity of the signal. The power levels measured at the digital output and the D/A converter output meet the limits shown in Table II.

The output signal in Fig. 13 meets the GSM spectrum mask requirements [1]. The output signal in Fig. 14 meets the EDGE spectrum mask requirements [1]. Fig. 15 shows the WCDMA output with a crest factor of 11.43 dB, where the adjacent channel leakage powers (ACLR1/2) are 65.84 and 67.67, respectively. Fig. 16 shows the error vector magnitude (EVM) performance in EDGE mode, where the measured rms EVM is 0.37% with a maximum peak deviation of 1.55%. The signal performance is summarized in Table III. The phase error, EVM and spectral performance [3], measured at the digital output and the D/A converter output, meet the specifications shown in Table III. In the multistandard IF modulator, most of the errors are generated less by quantization errors in the digital domain and more by the D/A converter analog nonidealities, as shown in Table III. There is some margin in the D/A converter output for taking care of the other transmitter stages that might degrade the signal quality. Combining a number of parallel modulator outputs allows the formation of multicarrier signal

TABLE III
PERFORMANCE SUMMARY

Signal Quality					
Measured at	GSM Phase Error (°)		EDGE EVM (%)		WCDMA EVM (%)
	peak	rms	peak	rms	rms
Digital Data at D/A Converter Input	0.75	0.29	1.263	0.27	1.11
Analog Signal at D/A Converter Output	1.71	0.74	1.55	0.37	1.18
Specifications at the base station RF port	20	5	22	7.0	17.5

Spectral Properties				
	GSM	EDGE	WCDMA	
	600 kHz offset	600 kHz offset	ACLR1	ACLR2
Digital Data at D/A converter input	-100	-90	72.9	73.3
Analog Signal at D/A Converter Output	-87.34	-84.58	65.84 From Fig. 15	67.67 From Fig. 15
Specifications at the base station RF port	-70	-70	45	50

Fig. 18. Chip micrograph.

in Fig. 1. Fig. 17 shows the multicarrier signal at the D/A converter output. The first adjacent channel leakage power ratio is 57.19 dB, which meets the specification (45 dB) [3].

VII. CONCLUSION

A GSM/EDGE/WCDMA modulator with a 14-bit on-chip D/A converter was implemented. The precompensation filter, which compensates the sinc droop above the Nyquist frequency, makes it possible to use WCDMA signal images for up-conversion. The new programmable up/down unit allows power ramping on a time-slot basis as specified for GSM, EDGE and TDD-WCDMA. The multistandard modulator meets the spectral, phase, and EVM specifications. The die area of the chip is 22.09 mm^2 in 0.35-μm CMOS technology. Power consumption is 1.7 W at 3.3 V with 110 MHz (maximum clock frequency). The IC is in a 160-pin CQFP package. Fig. 18 displays the chip micrograph.

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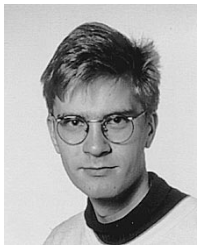

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