A High-Efficiency 100-W GaN Three-Way Doherty Amplifier for Base-Station Applications

Marco J. Pelk, *Student Member, IEEE*, W. C. Edmund Neo, *Student Member, IEEE*, John R. Gajadharsing, *Member, IEEE*, Raymond S. Pengelly, *Senior Member, IEEE*, and Leo C. N. de Vreede, *Senior Member, IEEE*

***Abstract*—A three-way Doherty 100-W GaN base-station power amplifier at 2.14 GHz is presented. Simple, but accurate design equations for the output power combiner of the amplifier are introduced. Mixed-signal techniques are utilized for uncompromised control of the amplifier stages to optimize efficiency, as well as linearity. The combination of the above techniques resulted in an unprecedented high efficiency over a 12-dB power backoff range, facilitating a record high power-added efficiency for a wideband code division multiple access test signal with high crest factor, while meeting all the spectral requirements for Universal Mobile Telecommunications System base stations.**

***Index Terms*—Base station, Doherty, high efficiency, mixed signal, power amplifier, predistortion, Universal Mobile Telecommunications System (UMTS), wideband code division multiple access (W-CDMA).**

I. Introduction

MORE THAN ever, there is increased interest from wireless industry in high-efficiency amplifier concepts to accommodate the third generation (3G) and upcoming fourth generation (4G) of communication standards. These new standards offer more and better data services, but to establish this within a restricted frequency band, they make use of signals with high peak-to-average power ratios. As a result, base-station amplifiers operating with these signals will function most of their time, at much lower levels than the peak powers they are designed for. Consequently, traditional class-AB amplifiers are less attractive candidates for these signals since their efficiency is seriously degraded when operating them below peak power. To avoid this efficiency degradation, various amplifier architectures with improved efficiency [1] have been proposed over time.

In spite of the large variety in amplifier concepts, only the envelope tracking [2], envelope elimination and restoration (EER)/polar modulation [3], [4] and Doherty amplifier [5]–[14] concepts seem to be actively being pursued by industry to become commercial products for the base-station market. In these approaches, the envelope tracking amplifier, in its most promising implementation, makes use of an efficient dc-to-dc converter in combination with a video amplifier to modulate the supply voltage. This increased complexity increases cost and gives rise to some additional power losses that slightly degrade the overall efficiency of the amplifier. A state-of-the-art envelope tracking amplifier is demonstrated in [2] offering a power-added efficiency (PAE) of 50.7% for a wideband code division multiple access (W-CDMA) signal, at an average output power of 37.2 W (in [2], the W-CDMA signal was clipped in order to reduce the crest factor to 7.67 dB). A comparable performance is very recently achieved with a two-way Doherty power amplifier (DPA) [15] where, for a W-CDMA signal (with 50-W average output power), a PAE of 53% has been achieved. Decresting is also used here to reduce the crest factor to 6.5 dB.

In theory, three-way Doherty amplifier implementations can offer even better efficiencies in power backoff operation. Something that is still highly desirable when dealing with single or multiple (unclipped) W-CDMA channels or modern 4G signals with even higher crest factors. Unfortunately, practical three-way DPA implementations rarely meet their expectations due their complicated implementation. To overcome these implementation issues and enable reproducible, as well as very efficient N-way Doherty amplifiers, the use of mixed-signal techniques was recently proposed to establish digital input control of the individual amplifier cells [8]. This approach facilitates the independent optimization of the amplifier-cell drive conditions for maximum efficiency. In [8], a prototype three-way Doherty amplifier was demonstrated using 4G NXP LDMOS devices. Up to this date, LDMOS is still the preferred technology for base-station power amplifiers due to its high reproducibility, good power handling, high linearity, and gain, but most importantly, due to its low cost. However, over time it is expected that wide-bandgap materials like GaN will challenge the position of silicon LDMOS technology since GaN can offer higher power densities and higher gain at microwave frequencies.

To investigate these prospects, this paper explores the potential of GaN technology for three-way DPAs with improved efficiency in far backoff operation to better serve signals with very high crest factors. For this purpose, we introduce a step-by-step procedure for the optimum design of a three-way Doherty power-combining network (Section II). By using mixed-signal techniques, the individual input-drive conditions of the amplifier cells can be optimized through software, avoiding limitations due to implementation imperfections. For this purpose, a dedicated test-bench and calibration technique was developed (Section IV). The measurement results of the GaN three-way DPA are given in Section V, representing

Manuscript received January 18, 2008; revised March 27, 2008. First published May 23, 2008; last published July 9, 2008 (projected). This work was supported by NXP Semiconductors and by CREE Inc.

M. J. Pelk, W. C. E. Neo, and L. C. N. de Vreede are with the Laboratory of High-Frequency Technology and Components (HiTeC), Delft Institute of Microsystems and Nanoelectronics (DIMES), Delft University of Technology, Delft 2628 CT, The Netherlands (e-mail: m.pelk@ewi.tudelft.nl).

J. R. Gajadharsing is with the RF Innovation Center, NXP Semiconductors, 6534 AE Nijmegen, The Netherlands.

R. S. Pengelly is with CREE Inc., Durham, NC 27703 USA.

Digital Object Identifier 10.1109/TMTT.2008.924364

to the authors' best knowledge, the highest efficiency ever reported for a W-CDMA signal when no decresting is used. In Section V-B, to compensate for memory effects, a dedicated digital predistortion (DPD) algorithm was applied that can handle the three-input one-output DPA topology, enabling the GaN three-way DPA to meet all the linearity specifications for Universal Mobile Telecommunications System (UMTS) base stations at a carrier frequency of 2.14 GHz. We conclude our study in Section VI.

II. Design Procedure

A. Selection of Output Matching Topology

Doherty amplifiers use load modulation to improve their efficiency in power backoff. By enforcing increased loading impedances to the output of the active stages in power backoff, their effective output voltage swings are increased, as well as their related efficiencies.

It is common knowledge, however, that device parasitics and matching losses will decrease amplifier efficiency more when high impedance loading conditions are present, than when loading it with the much lower impedance for maximum output power. Consequently, to realize truly highly efficient Doherty operation with practical devices, one should avoid the use of too large load modulation ratios for the transistor cells once they are activated by their input signal.

In view of this, when considering the design of the output-power combining network, it can be proven that for a given position of the high-efficiency power backoff points (e.g., -6 and -12 dB), the linear three-way DPA output combining network [8] requires higher load modulation ratios (a factor of 4 for the main and a factor of 3 for peak1 device), than when using the classical three-way DPA power-combining network (a factor of 2 for the main and 3 for the peak1 device). Based on this observation and the fact that we aim with our design for the highest efficiency possible, we have decided to use the classical three-way DPA concept as a starting point for our design. The related linearity limitations of the classical three-way DPA will be overcome by the use of the mixed-signal concept to control the input signals [8], as we will demonstrate later.

B. Design of the High-Efficiency Three-Way DPA

To support an optimum and systematic design flow for our high-efficiency GaN three-way DPA, a new set of compact design equations will be introduced. These equations enable the designer to select, based on the availability of devices, the optimum position for the high-efficiency power backoff points, the best intermediate loading conditions of the amplifier cells, and finally to find the most suitable characteristic impedances (Z_{01}, Z_{02} and Z_{03}) for the quarter-wave lines of the output-power combining network (see Fig. 1).

Note that current design methodologies found in the literature do not offer this flexibility [6] since, in these methods, the characteristic impedances of these lines follow directly from the chosen high-efficiency power backoff points. Successively, with these line impedances, the resulting loading conditions for the amplifier cells are found. The inflexible nature of this classical design approach often results in difficult to implement high-Q matching conditions, yielding high losses and bandwidth restrictions. In our modified design strategy we present below, we have developed design equations that provide more flexibility in determining the optimum matching network. As result, high-Q matching conditions can be avoided.

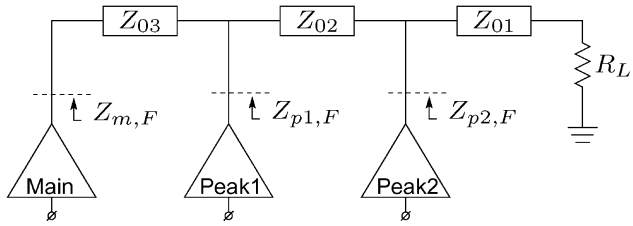

Fig. 1. Loading conditions for the amplifier cells at full output power.

The first step in this procedure is to obtain a good indication for the optimum size of the peak1 and peak2 devices (m_1 and m_2) relative to the main device, based on the desired high-efficiency power backoff points k_1 and k_2. This can be expressed as

$$m_1 = \frac{1-k_2}{k_2} \quad m_2 = \frac{1-k_1}{k_1 k_2}. \tag{1}$$

If the backoff points are chosen at -6 dB ($k_1 = 0.5$) and -12 dB ($k_2 = 0.25$), the required device size ratio will be $1 : m_1 : m_2 = 1 : 3 : 4$. Unfortunately, in practical situations, these device sizes are not always available. Also in our study, there were only two devices available, namely, 15 and 45 W. Consequently, the configuration that approximates the intended device ratios best is 1 : 3 : 3. Using these ratios and rewriting (1), the location of the efficiency peaks can be calculated as

$$k_1 = \frac{1+m_1}{1+m_1+m_2} \quad k_2 = \frac{1}{1+m_1}. \tag{2}$$

The resulting high-efficiency operation points are located at -4.9- and -1- dB power backoff, respectively. Note that, by this device size selection (see the Appendix), the load modulation ratios of the main (Υ_m) and peak1 device (Υ_{p1}) are also fixed as follows:

$$\Upsilon_m = \frac{(1+m_1)^2}{1+m_1+m_2} \tag{3}$$

$$\Upsilon_{p1} = \frac{m_1(1+m_1+m_2)}{m_1^2+m_1-m_2} \tag{4}$$

which yields $\Upsilon_m = 2.3$ and $\Upsilon_{p1} = 2.3$, which are very favorable numbers compared to the situation when using a linear DPA output combining network, as has been discussed above. Our next step is to find the proper tradeoffs between the characteristic impedance and the loading impedances required by the amplifier cells. For this purpose, we have derived the following equations (see the Appendix):

$$Z_{01} = \sqrt{\frac{Z_{p2,F} R_L m_2}{1+m_1+m_2}} \tag{5}$$

$$Z_{02} = \sqrt{\frac{Z_{p2,F} Z_{p1,F} m_1 m_2}{(1+m_1)^2}} \tag{6}$$

$$Z_{03} = \sqrt{Z_{m,F} Z_{p1,F} m_1}. \tag{7}$$

TABLE I
LOADING CONDITIONS FOR THE INDIVIDUAL AMPLIFIER CELLS

	Full*	Backoff 1	Backoff 2
Z_{main}	50 Ω	50 Ω	114.3 Ω
Z_{peak1}	25 Ω	58.3 Ω	—
Z_{peak2}	50 Ω	—	—
P_{main}	14.29 W	14.29 W	6.25 W
P_{peak1}	42.86 W	18.37 W	0 W
P_{peak2}	42.86 W	0 W	0 W

*These values are chosen by the designer

As can be observed from these equations, the characteristic impedance of the lines can be influenced by selecting convenient intermediate loading conditions of the amplifier cells at the full power point ($Z_{m,F}$, $Z_{p1,F}$, and $Z_{p2,F}$). Selecting too high impedance levels for the amplifier cells will complicate the output matching due to the large impedance transformation ratios required. Choosing too small values results in unpractical widths for the quarter-wave lines of the power-combining network. In our design, the loading conditions of Table I were used for the amplifier cells, providing the best tradeoff in amplifier cell matching and impedance levels of the quarter-wave lines, namely, $Z_{01} = 32.7\,\Omega$, $Z_{02} = 26.5\,\Omega$ and $Z_{03} = 61.2\,\Omega$. Note that these values can be easily implemented in the used substrate technology (Taconic, TLT 0.8 mm).

The remaining step is to design the matching network for the individual amplifier cells, which should provide matching for optimum efficiency at all the loading conditions specified for the different power backoff levels, something that has been already addressed in earlier studies [5], [6], [8].

III. SIMULATED PERFORMANCE

Upon completion of our design, we have to find the optimum input drive conditions for our DPA to achieve maximum efficiency for complex modulated signals like W-CDMA [16]. To address this problem, we will first optimize the single-tone DPA efficiency as function of power in the backoff region. Note that this is a very effective approach since once the probability distribution function (PDF) of a complex modulated signal is known, the average drain efficiency $\langle \eta_d \rangle$ can be calculated based on the PDF and the DPA single-tone efficiency versus power backoff [17] using

$$\langle \eta_d \rangle = \frac{\langle P_{\rm out} \rangle}{\langle P_{\rm DC} \rangle} = \frac{\int P_{\rm out} p(P_{\rm out})\,{\rm d}P_{\rm out}}{\int \dfrac{P_{\rm out} p(P_{\rm out})}{\eta_d(P_{\rm out})}\,{\rm d}P_{\rm out}} \tag{8}$$

where:

- $P_{\rm out}$ = RF output power;
- $P_{\rm dc}$ = dc input power;
- η_d =Drain efficiency;
- p =probability.

In order to optimize the input drive signals of the DPA, the phase relations ($\varphi_{\rm peak1}$ and $\varphi_{\rm peak2}$) between the amplifier cells also need to be determined. In practice, the following three phase dependencies are considered:

1) phases optimized at the full power condition;
2) phase optimization at the second backoff point;
3) phase optimization at all power levels.

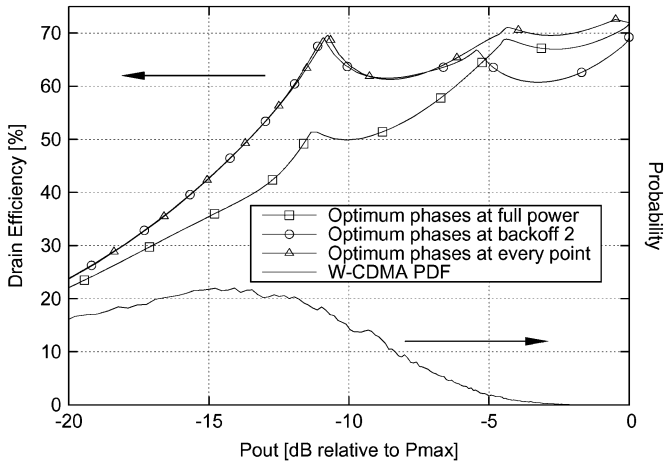

Fig. 2. Simulated drain efficiency using three different phase optimization methods. (1) The relative phases for the peak1 and peak2 amplifiers optimized at full output power. (2) The relative phases for the peak1 and peak2 amplifiers optimized at the second backoff point. (3) The relative phases for the peak1 and peak2 amplifiers optimized at each power level. Also shown is the PDF for a W-CDMA signal.

TABLE II
CALCULATED W-CDMA DRAIN EFFICIENCY BASED ON SINGLE TONE SIMULATION DATA FOR THREE DIFFERENT CASES

	Full Power	Backoff 2	Everywhere
η_d	54.4 %	60.2 %	61.2 %

Fig. 2 shows the related simulated drain efficiencies. Also shown is the power PDF for the W-CDMA signal without decresting, which will be used later in our efficiency considerations.

By comparing the results of Fig. 2 with DPA results found in the literature [15], [18], we can conclude that most conventional DPA implementations with a passive input power splitter use phase relations, which are optimized for high efficiency at the maximum output power condition.

In order to make a careful selection of the optimum phase relations for driving the DPA, we use (8) with the efficiency curves of Fig. 2 to calculate the W-CDMA efficiency performance for all three cases. The results of this calculation are presented in Table II.

Clearly, the situation where the phase angles are optimized at each power level will yield the highest efficiency. A 1% reduction in efficiency is found for the case where we have optimized the efficiency for backoff point 2. Worse performance is found for the situation where the phase DPA phase relations are entirely optimized for maximum output power operation.

It should be mentioned that for single-tone operation, phase optimization at each output power level is relatively easy to implement. However, when using complex modulated signals to-

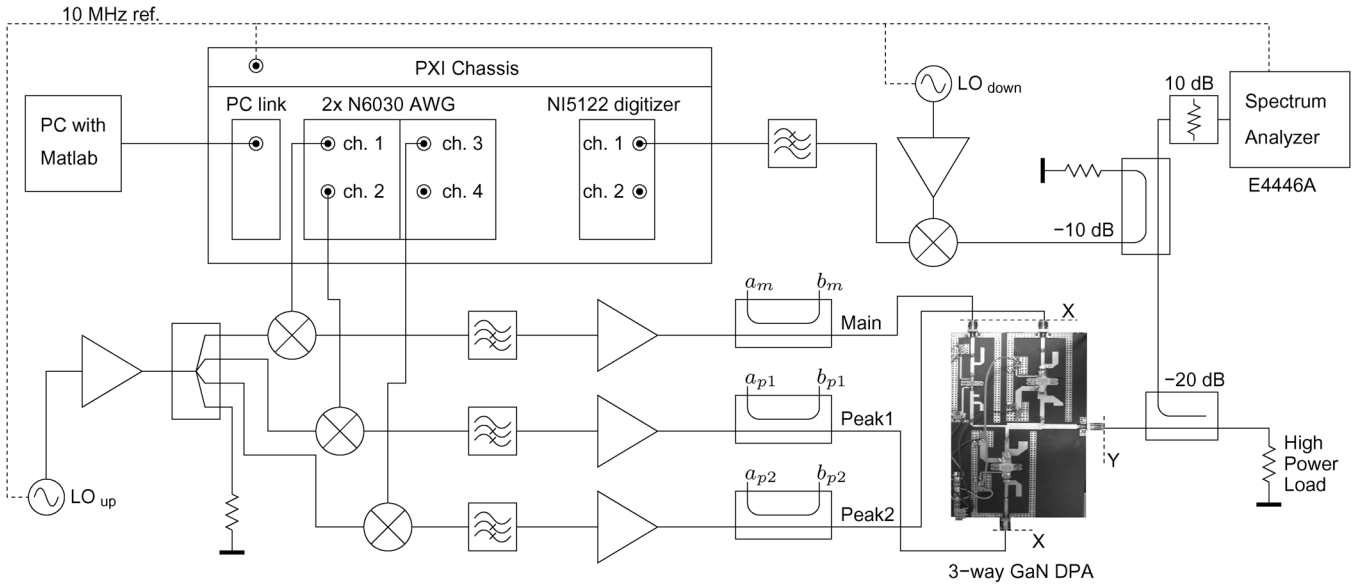

Fig. 3. System setup to verify the performance of the GaN three-way DPA.

gether with phase relations that change continuously as a function of instantaneous power, this concept proves to be very difficult to implement. For this fact, we decided to avoid too much computational overhead in signal processing for only 1% efficiency improvement. Consequently, we will restrict ourselves to the use of fixed, but optimized phase relations for signals fed to the amplifier cells.

IV. Testing of the Three-Way DPA

In order to verify the conclusions, we have constructed a custom test setup for our three-way DPA. This setup is an improved version of the one introduced in [8]. Its new features are described below.

A. Hardware Configuration

In Fig. 3, the schematic of the custom amplifier test bench is shown. Its structure is based on the heterodyne transceiver architecture in which the transmitter/up-conversion chain is duplicated three times to enable individually controlled inputs of the three-way DPA. The complex baseband signals are generated using MATLAB and uploaded as a digital 400-MHz IF signal to the synchronized Agilent N6030A arbitrary waveform generators (AWGs). By using a single oscillator to drive the mixers, three phase coherent RF channels are created at a center frequency of 2.14 GHz. A high-pass filter suppresses the lower sideband and leakage of the oscillator. After filtering, the drive signals are amplified to reach the required power levels. In order to facilitate measurement of actual input powers (needed for the PAE measurement), directional couplers are inserted after the drive amplifiers prior to the inputs of the three-way DPA.

At the output of the three-way DPA, the maximum power level is close to 50 dBm. To reduce this level to a suitable level for detection, a two couplers configuration is used to split off a fraction of the output power, while the remaining power is delivered to a 500-W dummy load. The detection signals are fed to a spectrum analyzer for the measurement of the (channel) powers and spectral purity, as well as to a down-converting mixer.

This high-linearity down-converting mixer is driven by a 2115-MHz local oscillator (LO) signal, which is frequency locked to the LO signal used for the up-conversion. Consequently, the output signal of the GaN three-way DPA is down-converted in a linear fashion to an IF signal of 25 MHz. By using high-speed digitizer cards from National Instruments (NI-PXI5122), this signal is acquired and through software operations converted to a complex baseband representation. This baseband signal representation is used as input for the DPD algorithm, which will be employed in conjunction with the GaN three-way DPA later in this paper.

B. System Calibration

To perform accurate characterization of the three-way DPA amplifier, several power and phase calibration steps have to be implemented. The input reference plane for the measurements is located at the three input connectors of the GaN three-way DPA (point $\times$ in Fig. 3). The RF phase for the main amplifier is set as a reference and is assumed to be 0°. The phases of the peak1 amplifier and peak2 amplifier are defined relatively to the main amplifier.

Step 1) *Output Calibration*: The first calibration step is to relate the spectrum analyzer readings with the actual output power of the amplifier under test. For this purpose, a signal generator with accurately known output power is connected at reference plane Y (Fig. 3). The difference between measured and actual power is used as correction in the spectrum analyzer.

Step 2) *Input Power Calibration*: The calibration for the available input power is done for each channel separately. To calibrate, the planes X and Y are directly connected together. By now performing a single-tone power sweep generated by the AWGs,

the powers are measured with the spectrum analyzer and stored in a lookup table.

Step 3) *Input Reflection Calibration*: For the PAE measurements, the actual input powers are required [as opposed to available power levels from calibration Step 2)]. For this purpose, a one-port calibration procedure similar to a conventional short-open-load network analyzer calibration is used. Three different loading conditions at plane X are applied, while the a and b coupler outputs, which represent the incident and reflected powers, respectively, are connected to plane Y. From this data, the incident and reflected power for any loading condition can be accurately determined.

Step 4) *Input Phase Calibration*: Calibration for the relative phase of the peak1 and peak 2 channels is done by connecting the main channel and one of the other channels to the inputs of an in-phase power combiner. The output of the combiner is connected to Y and the phase of the peak signal is swept until a dip in the output power is observed. At this point, the two channels are exactly out-of-phase (180°). With this final step, our system calibration is completed.

V. Experimental Verification

For our experimental verification, we use the measurement setup of Section IV, which is computer controlled through MATLAB. These MATLAB scripts handle all the required actions to perform the calibration, signal generation, and data acquisition. Before we start characterizing the three-way DPA, the measurement setup was calibrated using the procedure from Section IV.

A. Single-Tone Characterization of the Three-Way DPA

From the simulations in Section III, a good estimate is achieved for the power levels of the input signals for the main, peak1, and peak2 amplifiers, as well for the relative phases to reach maximum PAE at the 12-dB backoff point (38 dBm). Using these initial values as starting point in the MATLAB optimization, the optimum input powers and phase relations for maximum PAE are found. We have repeated the same procedure at 4.9-dB backoff (45.1 dBm) and at full power (50 dBm). At each point, the three input powers $P_{\rm main}, P_{\rm peak1}, P_{\rm peak2}$ and the two relative phases $\varphi_{\rm peak1}, \varphi_{\rm peak2}$ are optimized. Linear interpolation is used to obtain values between these points. Note that this approach is almost equivalent to the use of optimized drive conditions at each power level, as discussed in Section III. The resulting PAE as function of normalized output power is plotted in Fig. 4, indicating the upper bound for PAE we can achieve with our three-way DPA. Note the rather exceptional PAE performance as function of backoff power. As a second experiment, we have used the more simplistic drive condition with constant phase relations between the amplifier cells. Doing so we can avoid the complication of continuously varying phases in combination with complex modulated signals, as discussed in Section III. Consequently, we keep the phase relations constant, but optimize their relative angles for maximum PAE at the second power backoff point. The resulting PAE as function of backoff power is also plotted in Fig. 4. Table III gives the resulting phases of $\varphi_{\rm peak1}$ and $\varphi_{\rm peak2}$ at the three high-efficiency points for both drive profiles. It can be noted from Table III that the phases are relatively close to the theoretical values of $-90°$ and $-180°$ as one would expect for a three-way Doherty amplifier.

It is clear that the curve with continuously optimized phase relations (Fig. 4) indeed gives a better performance over the use

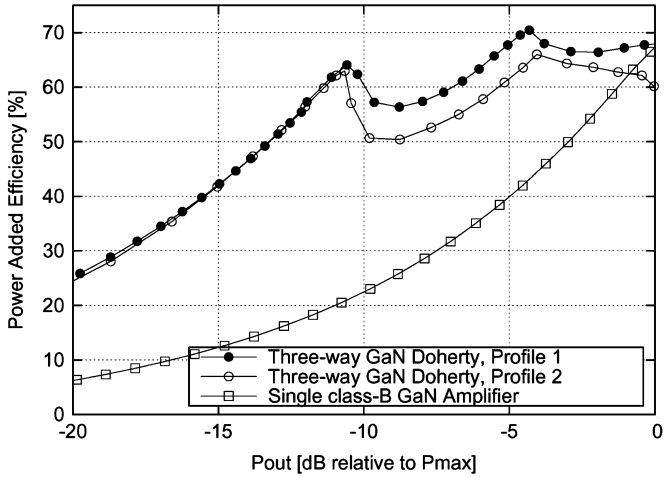

Fig. 4. Measured single-tone PAE versus output power backoff for different drive profiles. For the GaN three-way DPA, $P_{\rm max} = 50$ dBm, and for the single class-B amplifier, $P_{\rm max} = 44.5$ dBm.

TABLE III
RELATIVE PHASE FOR PEAK1 AND PEAK2

	Profile 1		Profile 2	
	φ_{peak1}	φ_{peak2}	φ_{peak1}	φ_{peak2}
Full Power	$-81.7°$	$-191.2°$	$-99.8°$	$-198.2°$
Backoff 1	$-97.1°$	$-198°$	$-99.8°$	$-198.2°$
Backoff 2	$-99.8°$	$-198.2°$	$-99.8°$	$-198.2°$

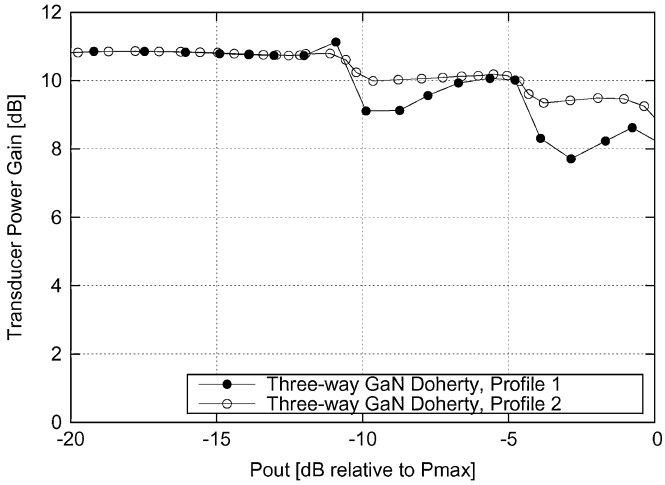

Fig. 5. Measured gain versus output power backoff for the two different drive profiles. Drive profile 1 is with continuously varying phase and drive profile 2 is with fixed phase relations. As can be seen, the gain flatness is much better for the second drive profile. Also here, $P_{\rm max} = 50$ dBm.

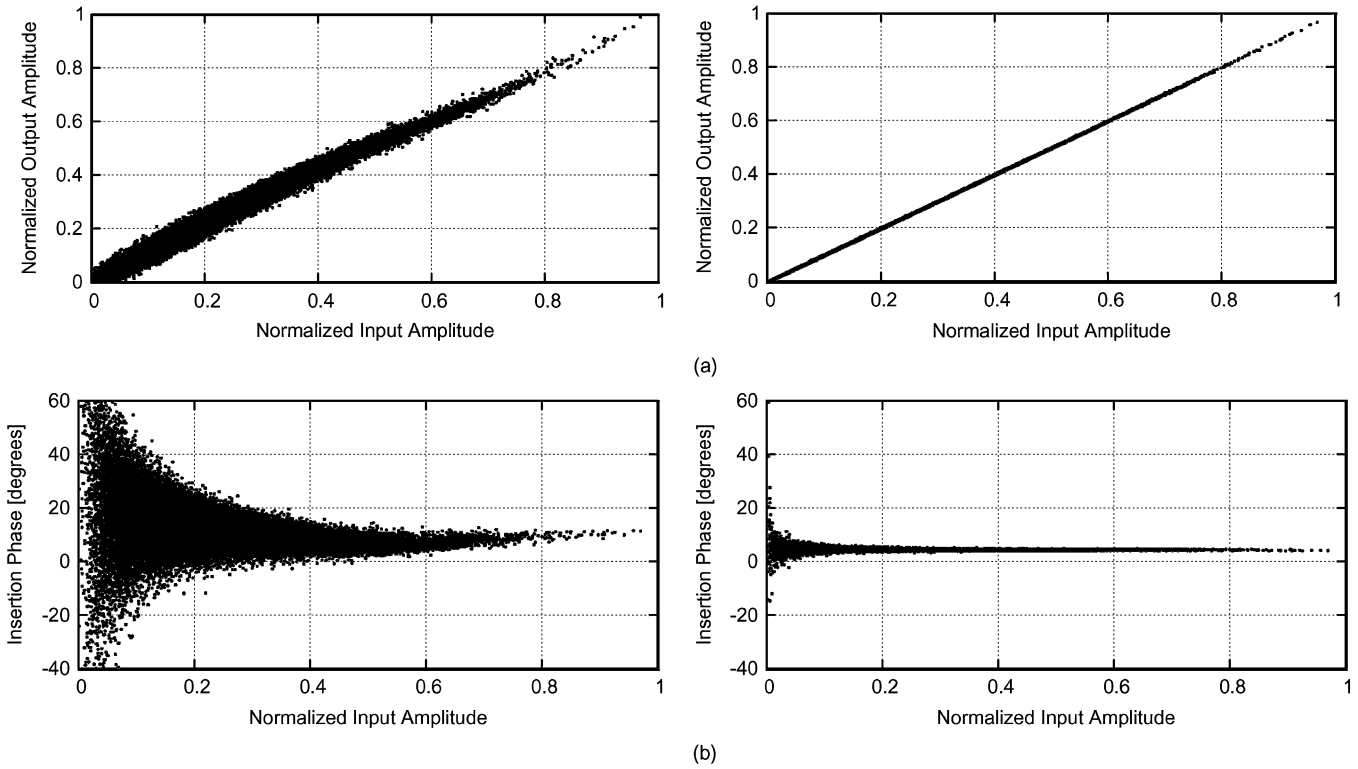

Fig. 6. (a) Measured AM–AM distortion and (b) AM–PM distortion for the GaN three-way DPA. At the left, the performance without predistortion can be seen, and the right plots show the performance after predistortion with memory effect compensation.

of fixed phase relations at higher power levels. However, as discussed in Section III, this difference is not significant enough to justify a much more complicated signal processing when the DPA is driven with a complex modulated signal. Another reason why the fixed-phase drive condition is preferred is its more well-behaved gain flatness (Fig. 5), yielding a less critical predistortion.

Fig. 4 also shows the normalized measured PAE of a 45-W class-B GaN amplifier, which utilizes an identical device as applied in the peak1 amplifier. It is interesting to see that at maximum output powers, both the DPA, as well as the class-B amplifier using the same device technology reach a maximum PAE of almost 70%, confirming the close to ideal operation of the DPA design at full power. Note that the PAE of class-B GaN amplifier decreases proportional with the square of the backoff power, whereas the GaN three-way DPA demonstrates very high efficiency throughout the entire backoff range of 12 dB. At the 12-dB backoff point, the GaN three-way DPA provides a three time higher PAE than the class-B amplifier for continuous wave (CW) signals, indicating the very high efficiency potential of the three-way DPA for complex modulated signals with a high peak-to-average power ratio.

B. Measured W-CDMA Performance

One of the most important specifications for UMTS base-station amplifiers is the adjacent channel leakage ratio (ACLR) since this gives a direct indication on the achieved spectral purity. To test amplifiers for this property, Test Model 1 [16] specifies a realistic W-CDMA traffic scenario with 16, 32, or 64 dedicated physical channels (DPCHs). Currently, to improve base-station efficiencies, people decrest W-CDMA signals [19] to reduce their peak-to-average power ratio, enabling amplifiers to operate at higher efficiencies. This decresting of the WCDMA signal typically results in a crest factor reduction of several decibels without any significant degradation of the error vector magnitude (EVM) and ACLR. In our three-way DPA amplifier, however, decresting is no longer needed since its PAE versus backoff power dependence is optimized to handle modulated signals with crest factors in the order of 10–12 dB.

For the characterization of our three-way DPA, a W-CDMA signal with 64 DPCHs was created using Agilent Technologies' Advanced Design System (ADS) having a crest factor of 11.5 dB. Next, we have used this signal as input in MATLAB to obtain the three input signals needed to drive the three-way DPA. For this purpose, we have made use of the optimum PAE single-tone drive conditions found in Section V-A. Fig. 6 gives the resulting AM–AM and AM–PM characteristics of the GaN three-way DPA when driven by the W-CDMA test signal. The left plots show the initial performance when no predistortion is applied. In these graphs, the "haze" found around the AM–AM and AM–PM characteristics indicate the presences of memory effects, which are caused by thermal effects, trapping in the devices and imperfect dc biasing of the devices. To suppress the influence of these effects, we have developed a dedicated predistortion algorithm, based on memory polynomials [20]–[22], which is applicable to our three-way DPA amplifier and compensates for the memory present in the circuit. The right plots of Fig. 6 show the resulting AM–AM and AM–PM distortion when this newly developed algorithm is applied. Comparing the later results with the nonpredistorted results, a clear reduction in

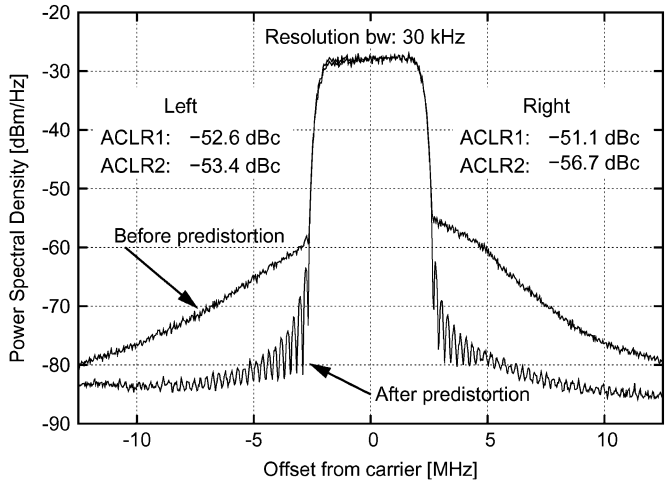

Fig. 7. Measured spectrum for a W-CDMA signal before and after predistortion. The ACLR values shown are after predistortion. The average channel output power is 38.5 dBm and the PAE is 53%.

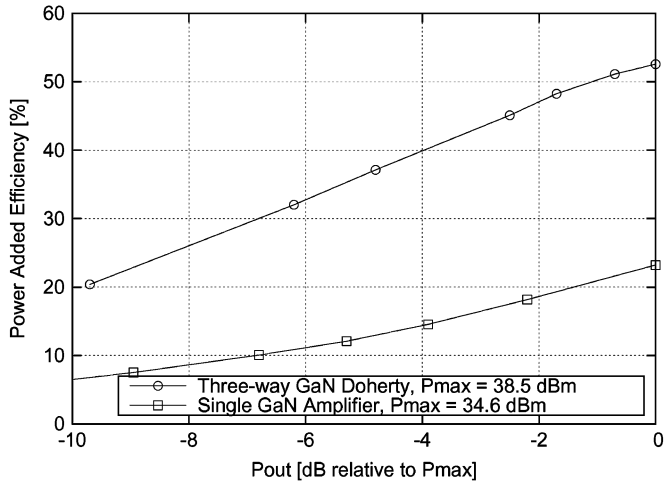

Fig. 8. Measured PAE versus output power backoff for W-CDMA operation. Note that $P_{\max}$ here refers to the average output power.

haze can be observed, while the resulting characteristic closely approaches the behavior of an ideal linear system, indicating the correct operation of the algorithm.

Consequently, Fig. 7 shows the spectrum of the signal before and after predistortion. The measured channel power over a bandwidth of 5 MHz is 38.5 dBm (approximately 7 W) and the measured peak power is 50 dBm (100 W). Note that with predistortion a very significant improvement in linearity is indeed achieved, resulting in a measured ACLR of better than −50 dBc for both ACLR 1 and ACLR 2. The related measured PAE for this power level is 53% with a crest factor of 11.5 dB. To the authors' best knowledge, this is the highest PAE reported in the literature for a base-station amplifier operating with a W-CDMA signal under these conditions.

In addition to the above, Fig. 8 shows the measured PAE of the GaN three-way DPA and class-B GaN amplifier driven with the W-CDMA signal as a function of backoff power. The backoff power level here is taken relative to the average W-CDMA output power. Note that although the class-B and three-way DPA have a similar peak efficiency for their single-tone operation (Fig. 4), W-CDMA operation results in a more than two times higher PAE for the three-way DPA, while still meeting all linearity specifications. The slow reduction of PAE for the three-way DPA versus increased power backoff indicates once more the enormous performance potential of GaN technology for base-station applications when signals with an even higher crest factor come into use.

VI. Conclusion

In this paper, the performance potential of GaN technology for Doherty base-station applications has been investigated. For this purpose, we have utilized the mixed-signal N-way Doherty amplifier concept introduced in [8] to establish optimum control of the main and peaking amplifier stages. This improved control allows us to avoid all design/linearity limitations that are inherently related to classical Doherty implementations.

To achieve the highest efficiency possible, in this study a systematic design method was introduced to select the size of the main and peaking devices in relation with the chosen power backoff levels where efficiency peaking occurs. In addition, the proposed method also facilitates optimum selection of the amplifier-cell loading in combination with the transmission line impedances of the output power-combining network. Using these techniques, the GaN devices can be operated at full performance, while losses due to the output combining network are minimized.

With the above in mind, a three-way Doherty amplifier using CREE Inc.'s GaN technology has been realized as a demonstrator of the proposed design techniques. To facilitate its calibrated testing, a custom three-way test-bench has been developed, which can provide the required input signals, as well as measure the resulting input/output port powers. Using this setup, the CW performance of the three-way GaN DPA has been characterized and optimized using software control, yielding a measured performance of: 68% PAE at 50 dBm (full power), 70.4% at 45 dBm (first backoff point), and 64% at 38 dBm (second backoff point), while the measured transducer power gain was greater than 10 dB at all times.

To demonstrate that this exceptional high-efficiency performance can be effectively utilized for practical base-station operation, our GaN three-way DPA was driven with a W-CDMA signal with a crest factor of 11.5 dB. Using a dedicated memory-effect compensating predistortion algorithm, the resulting measured PAE for this signal was 53% at an average power of 38.5 dBm, while meeting all linearity specifications. To the authors' best knowledge, this is the highest PAE performance ever reported for any power amplifier operating with a W-CDMA signal without using crest factor reduction techniques.

To support this conclusion, various recent amplifier designs were considered, which also provide excellent W-CDMA performance (Table IV, column A). Note that a straightforward comparison is troubled by the fact that W-CDMA signals with different crest factors have been used. However, to obtain a good estimate of the performance of these amplifiers for the unaltered W-CDMA signal (crest factor 11.5 dB), as used in our experiments, we have calculated their estimated efficiency for this signal as well. The computations are based on provided

TABLE IV
W-CDMA PERFORMANCE OF RECENT AMPLIFIER DESIGNS

Design	W-CDMA crest factor used in ref.	A Measured drain efficiency with crest factor used in ref.	B Estimated drain efficiency with crest factor of 11.5 dB
Steinbeiser et al. [15]	6.5 dB	57 %	45.2 %
Yamamoto et al. [23]	9 dB	50 %	44.9 %
Ui et al. [24]	7.8 dB	42 %	36.2 %
Kimball et al. [2]	7.67 dB	53.4 %	45.4 %*
This work	**11.5 dB**	**55 %**	**55 %**

*Assuming crest factor independent efficiency for the envelope amplifier.

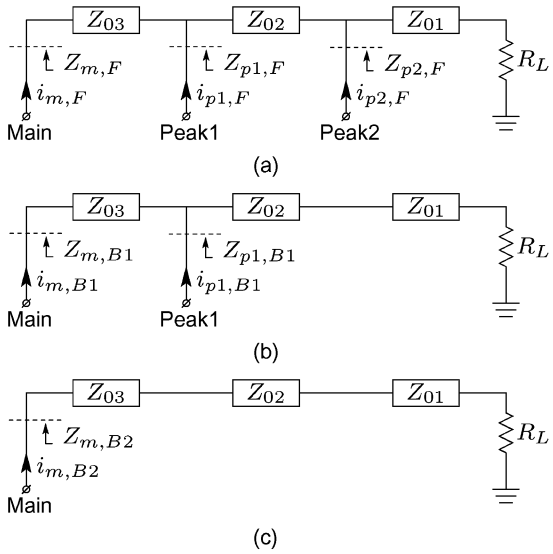

Fig. 9. Output power combiner consisting of three 90° transmission lines. (a) Full power condition. (b) Backoff 1. (c). Backoff 2.

data for their single-tone drain efficiency as function of backoff power using the procedure described in Section III. This estimate will be accurate within a few percent. The results are given in Table IV, column B.

The above demonstrates the performance potential of GaN technology for Doherty amplifiers, making the mixed-signal GaN three-way DPA an interesting candidate for future 3G and 4G base-station power amplifiers.

APPENDIX
CALCULATION OF THE OUTPUT POWER COMBINER

For the mixed-signal approach of designing three-way Doherty amplifiers, class-B operation for all amplifier cells is used. The following analysis assumes ideal devices and transmission lines. Ideal class-B operation has a maximum output power of

$$P_{\text{out,max}} = \frac{1}{2} V_{\text{DC}} i_{\text{out}}. \tag{9}$$

In the case of a three-way Doherty amplifier, i_{out} is the sum of the individual device output currents, which, at the full power condition, will be distributed across the devices according to the device size ratios m_1 and m_2. This will yield the following device output currents:

$$i_{m,F} = \frac{2P_{\text{out,max}}}{V_{\text{DC}}(1+m_1+m_2)} \tag{10}$$

$$i_{p1,F} = \frac{2m_1 P_{\text{out,max}}}{V_{\text{DC}}(1+m_1+m_2)} \tag{11}$$

$$i_{p2,F} = \frac{2m_2 P_{\text{out,max}}}{V_{\text{DC}}(1+m_1+m_2)}. \tag{12}$$

Fig. 9 shows the output power combiner consisting of three transmission lines with an electrical length of 90° and the corresponding device currents and loading conditions. Now taking the backoff ratios k_1 and k_2 into account, the device output currents for the backoff 1 and backoff 2 conditions can be derived.

Note that the main device current at backoff 1 is equal to the full power condition in a classical Doherty amplifier [8]

$$i_{m,B1} = i_{m,F} = \frac{2P_{\text{out,max}}}{V_{\text{DC}}(1+m_1+m_2)} \tag{13}$$

$$i_{p1,B1} = \frac{(k_1-k_2)2m_1 P_{\text{out,max}}}{(1-k_2)V_{\text{DC}}(1+m_1+m_2)} \tag{14}$$

$$i_{p2,B1} = 0 \tag{15}$$

$$i_{m,B2} = \frac{k_2 2P_{\text{out,max}}}{k_1 V_{\text{DC}}(1+m_1+m_2)} \tag{16}$$

$$i_{p1,B2} = 0 \tag{17}$$

$$i_{p2,B2} = 0. \tag{18}$$

In order to relate the backoff ratios to the device sizes, the total output power at both backoff conditions can be written as

$$P_{\text{out},B1} = 0.5 V_{\text{DC}} i_{m,B1} + 0.5 V_{\text{DC}} i_{p1,B1} = k_1^2 P_{\text{out,max}} \tag{19}$$

$$P_{\text{out},B2} = 0.5 V_{\text{DC}} i_{m,B2} = k_2^2 P_{\text{out,max}}. \tag{20}$$

Substituting (13), (14), and (16) and solving for k_1 and k_2 yields

$$k_1 = \frac{1+m_1}{1+m_1+m_2} \tag{21}$$

$$k_2 = \frac{1}{1+m_1}. \tag{22}$$

The amplifier load impedances from Fig. 9 at the various output power conditions can be obtained by applying the active load–pull principle [25]

$$Z_{m,F} = \frac{Z_{03}^2 Z_{01}^2 (1+m_1+m_2)}{Z_{02}^2 R_L (1+m_1)^2} \tag{23}$$

$$Z_{p1,F} = \frac{Z_{02}^2 R_L (1+m_1)^2}{Z_{01}^2 m_1 (1+m_1+m_2)} \tag{24}$$

$$Z_{p2,F} = \frac{Z_{01}^2 (1+m_1+m_2)}{R_L m_2} \tag{25}$$

$$Z_{m,B1} = \frac{Z_{03}^2 Z_{01}^2 (1+m_1+m_2)}{Z_{02}^2 R_L (1+m_1)^2} \tag{26}$$

$$Z_{p1,B1} = \frac{Z_{02}^2 R_L (1+m_1)^2}{Z_{01}^2[(1+m_1)^2 - (1+m_1+m_2)]} \tag{27}$$

$$Z_{m,B2} = \frac{Z_{03}^2 Z_{01}^2}{Z_{02}^2 R_L}. \tag{28}$$

Based on chosen values for the full power loading conditions, the characteristic impedance for the following three transmission lines can be calculated:

$$Z_{01} = \sqrt{\frac{Z_{p2,F} R_L m_2}{1+m_1+m_2}} \tag{29}$$

$$Z_{02} = \sqrt{\frac{Z_{p2,F} Z_{p1,F} m_1 m_2}{(1+m_1)^2}} \tag{30}$$

$$Z_{03} = \sqrt{Z_{m,F} Z_{p1,F} m_1}. \tag{31}$$

The load modulation ratios Υ_m and Υ_{p1} for the main and peak1 device, respectively, can also be written in terms of device size

$$\Upsilon_m = \frac{Z_{m,B2}}{Z_{m,F}} = \frac{(1+m_1)^2}{1+m_1+m_2} \tag{32}$$

$$\Upsilon_{p1} = \frac{Z_{p1,B1}}{Z_{p1,F}} = \frac{m_1(1+m_1+m_2)}{m_1^2+m_1-m_2}. \tag{33}$$

ACKNOWLEDGMENT

The authors would like to thank J. Qureshi, Delft University of Technology, Delft, The Netherlands, for the useful discussions. The authors would also like to thank T. Dekker and R. Baker, both with CREE Inc., Durham, NC, for promptly responding to questions and providing the GaN devices and related models. The authors would also like to acknowledge R. Jos, NXP Semiconductors, Nijmegen, The Netherlands, for supporting this study.

REFERENCES

[1] F. H. Raab, P. Asbeck, S. Cripps, P. B. Kenington, Z. B. Popovic, N. Pothecary, J. F. Sevic, and N. O. Sokal, "Power amplifiers and transmitters for RF and microwave," *IEEE Trans. Microw. Theory Tech.*, vol. 53, no. 3, pp. 814–826, Mar. 2002.

[2] D. F. Kimball, J. Jeong, C. Hsia, P. Draxler, S. Lanfranco, W. Nagy, K. Linthicum, L. E. Larson, and P. M. Asbeck, "High-efficiency envelope-tracking W-CDMA base-station amplifier using GaN HFETs," *IEEE Trans. Microw. Theory Tech.*, vol. 54, no. 11, pp. 3848–3856, Nov. 2006.

[3] J. Groe, "Polar transmitters for wireless communications," *IEEE Commun. Mag.*, vol. 45, no. 9, pp. 58–63, Sep. 2007.

[4] N. D. Lopez, X. Jiang, D. Maksimovic, and Z. Popovic, "A high-efficiency linear polar transmitter for EDGE," in *IEEE Radio Wireless Symp.*, Jan. 22–24, 2008, pp. 199–202.

[5] M. Iwamoto, A. Williams, P. Chen, A. G. Metzger, L. E. Larson, and P. M. Asbeck, "An extended Doherty amplifier with high efficiency over a wide power range," *IEEE Trans. Microw. Theory Tech.*, vol. 49, no. 12, pp. 2472–2479, Dec. 2001.

[6] N. Srirattana, A. Raghavan, D. Heo, P. Allen, and J. Laskar, "Analysis and design of a high-efficiency multistage Doherty power amplifier for wireless communications," *IEEE Trans. Microw. Theory Tech.*, vol. 53, no. 3, pp. 852–860, Mar. 2005.

[7] C. T. Burns, A. Chang, and D. W. Runton, "A 900 MHz, 500 W Doherty power amplifier using optimized output matched Si LDMOS power transistors," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Jun. 2007, pp. 1557–1580.

[8] W. C. E. Neo, J. Qureshi, M. J. Pelk, J. R. Gajadharsing, and L. C. N. de Vreede, "A mixed-signal approach towards linear and efficient N-way Doherty amplifiers," *IEEE Trans. Microw. Theory Tech.*, vol. 55, no. 5, pp. 866–879, May 2007.

[9] R. S. Pengelly, "N-way RF power amplifier with increased backoff power and power added efficiency," U.S. Patent 6 700 444, Mar. 2, 2004.

[10] R. S. Pengelly and S. M. Wood, "N-way RF power amplifier circuit with increased back-off capability and power-added efficiency using unequal input power division," U.S. Patent 6 737 922, May 18, 2004.

[11] R. S. Pengelly and S. M. Wood, "N-way RF power amplifier circuit with increased back-off capability and power-added efficiency using selected phase lengths and output impedances," U.S. Patent 6 791 417, Sep. 14, 2004.

[12] I. Blednov, "Integrated Doherty type amplifier arrangement with high power efficiency," Int. Patent WO 2006/003 608, Jan. 12, 2006.

[13] I. Blednov, "Integrated Doherty type amplifier arrangement with integrated feedback," Int. Patent WO 2006/006 119, Jan. 19, 2006.

[14] I. Blednov, "Integrated Doherty type amplifier arrangement with high power efficiency," Int. Patent WO 2006/123 289, Nov. 23, 2006.

[15] C. Steinbeiser, T. Landon, and C. Suckling, "250 W HVHBT Doherty with 57% WCDMA efficiency linearized to −55 dBc for 2c11 6.5 dB PAR," in *Proc. IEEE Compound Semiconduct. Integr. Circuit Symp.*, Oct. 2007, pp. 1–4.

[16] "3G TS 25.141 base station conformance testing (FDD)," Tech. Specification Group Radio Access Networks, 3rd Generation Partnership Project, Valbonne, France, Tech. Spec., Rev. V3.1.0, 2000.

[17] J. Deng, P. S. Gudem, L. E. Larson, D. F. Kimball, and P. M. Asbeck, "A SiGe PA with dual dynamic bias control and memoryless digital predistortion for WCDMA handset applications," *IEEE J. Solid-State Circuits*, vol. 41, no. 5, pp. 1210–1221, May 2006.

[18] J. Gajadharsing, O. Bosma, and P. van Westen, "Analysis and design of a 200 W LDMOS based Doherty amplifier for 3G base stations," in *IEEE MTT-S Int. Microw. Symp. Dig.*, 2004, pp. 529–532.

[19] L. Larson, P. Asbeck, and D. Kimball, "Challenges and opportunities for compound semiconductor devices in next generation wireless base station power amplifiers," in *Proc. IEEE Compound Semiconduct. Integrated Circuit Symp.*, Nov. 2005, 1 p.

[20] H. Ku and J. Kenney, "Behavioral modeling of RF power amplifiers considering IMD and spectral regrowth asymmetries," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Jun. 8–13, 2003, vol. 2, pp. 799–802, vol. 2.

[21] S. McBeath and D. Pinckley, "Digital memory-based predistortion," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Jun. 12–17, 2005, 4 pp.

[22] A. Zhu and T. Brazil, "Behavioral modeling of RF power amplifiers based on pruned Volterra series," *IEEE Microw. Wireless Compon. Lett.*, vol. 14, no. 12, pp. 563–565, Dec. 2004.

[23] T. Yamamoto, T. Kitahara, and S. Hiura, "50% drain efficiency Doherty amplifier with optimized power range for W-CDMA signal," in *IEEE MTT-S Int. Microw. Symp. Dig.*, 2007, pp. 1263–1266.

[24] N. Ui, H. Sano, and S. Sano, "A 80 W 2-stage GaN HEMT Doherty amplifier with 50 dBc ACLR, 42% efficiency 32 dB gain with DPD for W-CDMA base station," in *IEEE MTT-S Int. Microw. Symp. Dig.*, 2007, pp. 1259–1262.

[25] S. C. Cripps, *RF Power Amplifiers for Wireless Communications.*. Norwood, MA: Artech House, 1999.

Marco J. Pelk (S'06) was born in Rotterdam, The Netherlands, in 1976. He received the B.Sc. degree in electrical engineering from The Hague Polytechnic, The Hague, The Netherlands, in 2000, and is currently working toward the Ph.D. degree at the Delft Institute of Microsystems and Nanoelectronics (DIMES), Delft University of Technology, Delft, The Netherlands.

In 2000, he joined DIMES. From 2000 to 2002, he was involved in the implementation of compact and mixed-level device models for circuit simulation. Beginning in 2002, he was also involved with the development of a novel active harmonic load–pull system, as well as the design and practical realization of highly efficient amplifier concepts together with a custom-made measurement setup to characterize its performance. He has authored or coauthored over ten technical papers. He holds several patents. His current research interests are microwave circuit design, nonlinear device characterization, and radar systems.

W. C. Edmund Neo (S'05) received the B.Eng. degree in electrical engineering from the National University of Singapore, Singapore, in 2002, the M.Sc. degree in electrical engineering from the Delft University of Technology, Delft, The Netherlands, in 2004 and is currently working toward the Ph.D. degree in electrical engineering at the Delft University of Technology.

His research interest is in the area of novel circuit design techniques for high-efficiency power amplifiers and the design of digital predistorters for linearizing them.

John R. Gajadharsing (A'95–M'04) was born in Paramaribo, Surinam, in 1959. He received the B.Sc. degree in electronic engineering from the Polytechnical Institute, Arnhem, The Netherlands, in 1985.

Upon graduation, he joined the Semiconductors Division, Philips Semiconductors (now NXP Semiconductors), Nijmegen, The Netherlands, where he is currently the System Architect for wireless infrastructure in business-line cellular. His current technical interests include advanced linearization techniques, high-efficiency amplifier concepts, and system architectures for next-generation base stations.

Mr. Gajadharsing is a member of the IEEE Microwave Theory and Techniques Society (IEEE MTT-S).

Raymond S. Pengelly (M'87–SM'90) received the B.Sc. and M.Sc. degrees from Southampton University, Southampton, U.K., in 1969 and 1973, respectively.

From 1969 to 1986, he was with the Plessey Company, where he was involved in a variety of engineering roles with increasing seniority. From 1978 to 1986, he managed the GaAs Monolithic Microwave Integrated Circuit (MMIC) Department, Plessey Research, Caswell, U.K., during which time, following several years of development, the department produced one of the world's first phased-array radar transmit/receive modules to be put into a demonstration system. In 1986, he joined the Tachonics Corporation, Princeton, NJ, where he was Executive Director of Design for analog and microwave GaAs MMICs. In 1989, he joined Compact Software, Paterson, NJ, as Vice President of Marketing and Sales, where he was responsible for the development of state-of-the-art computer-aided design tools to the RF, microwave, and lightwave industries. In 1993, he joined Raytheon Commercial Electronics, Andover, MA, where he was MMIC Design and Product Development Manager and Director of Advanced Products and New Techniques. Under these capacities, he managed a growing team to develop new products for emerging markets including power amplifiers for wireless local loop applications using pseudomorphic HEMT (pHEMT) technology, Si–Ge mixed-signal products, and flip-chip and chip-scale packaging, as well as new subsystem techniques such as I/Q predistortion. Since August 1999, he has been with CREE Inc., Durham, NC, where he was initially the General Manager for CREE Microwave, responsible for bringing CREE Inc.'s wide-bandgap transistor technology to the commercial marketplace. Upon the acquisition of UltraRF, Sunnyvale, CA, in 2001, he became Chief Technical Officer, enabling his skills in microwave semiconductor technology, based on 30 years of experience, to be utilized. Since September 2005, he been responsible for new business development of wide-bandgap technologies for RF and microwave applications for Cree Inc., most recently has been involved with the release of GaN HEMT transistors and integrated circuits (ICs) for general-purpose and telecommunications applications. He has authored or coauthored over 90 technical papers and four technical books. He holds ten patents.

Dr. Pengelly is a Fellow of the Institution of Engineering and Technology (IET).

Leo C. N. de Vreede (M'01–SM'04) was born in Delft, The Netherlands, in 1965. He received the B.S. degree in electrical engineering from the Hague Polytechnic, The Hague, The Netherlands, in 1988, and the Ph.D. degree from the Delft University of Technology, Delft, The Netherlands, in 1996.

In 1988, he joined the Laboratory of Telecommunication and Remote Sensing Technology, Department of Electrical Engineering, Delft University of Technology. From 1988 to 1990, he was involved in the characterization and physical modeling of ceramic multilayer capacitor (CMC) capacitors. From 1990 to 1996, he was involved with modeling and design aspects of HF silicon ICs for wideband communication systems. In 1996, he became an Assistant Professor with the Delft University of Technology, where he was involved with the nonlinear distortion behavior of bipolar transistors at the device physics, compact model, as well as circuit level with the Delft Institute of Microsystems and Nanoelectronics (DIMES). In Winter 1998–1999, he was a guest of the High Speed Device Group, University of San Diego, La Jolla, CA. In 1999, he became an Associate Professor with the Delft University of Technology, responsible for the Microwave Components Group . He has coauthored over 50 IEEE refereed conference and journal papers. He holds several patents. His current interest is technology optimization and circuit design for improved linearity and RF performance.