A HIGH EFFICIENCY CLASS A AMPLIFIER ACCOMPANIED BY CLASS D SWITCHING AMPLIFIER

Jae Hoon Jeong*, Gue Hong Kim*, Byeong Rok Min*, Che Hong Ahn* and Gyu Hyeong Cho**
*Korea Telecom
** Korea Advanced Institute of Science and Technology

Abstract - A high power class A amplifier has excellent fidelity but dissipates too much power. A class D amplifier has high efficiency but shows poor fidelity. This paper proposes a combination of a high fidelity class A power amplifier with class D power amplifier as variable power supply. This amplifier named as class I has the merits of both class A amplifier and class D. The efficiency is seventy-seven percent at full power rating. The distortion of the proposed amplifier is about the same as that of class A amplifier. The measured 3dB bandwidth is from 10Hz to 100kHz.

I. INTRODUCTION

Recently the dynamic range of the sound source has been expanded by the improvements of digital and other recording techniques. The trend of the efficiency of loudspeaker becomes low to reproduce low frequency well. These will need higher power and require better fidelity in the future, however, a high power amplifier is trending to be bulky and costly proportional to the fidelity by a big power supply and large heat sinks. These induce growing interests in increasing the efficiency and fidelity in the high power amplifiers.

There are class D, G and H in the high efficiency techniques[1-4]. Although the class D has the highest efficiency among all classes, the performances such as distortion and linearity are the poorest because of switching operation. The class G and H increase the efficiency by changing the power supply voltage discretely according to the input signal level [3,4], therefore, their efficiencies are merely improved around middle output power and are equal to that of class B at maximum output power.

Meanwhile the characteristics of class A are the lowest efficiency and the highest linearity in all classes. Although class A is sometimes applied to obtain superior quality in high end audio amplifier, it is difficult to obtain high power because of a large size and costly power components. If a high power amplifier has both high efficiency and high linearity, it would be the best amplifier.

Dissipating power of class A is calculated from the integrated product of the voltage between collector and emitter (V_{CE}) and the quiescent current (I_Q). Reducing either I_Q and/or V_{CE} can decrease dissipating power. There are some products announced to increase the efficiency by controlling I_Q according to input signal level[5]. This paper proposes a new class A plus D amplifier that has high linearity and high efficiency by changing the voltage of the class A power supply continuously adaptive to the input signal level. We named this method class I because the last class name is class H.

II. VARIABLE POWER SUPPLY

If the V_{CE} is maintained constant, small and independent of output voltage in the class A amplifier, it is possible to decrease the power dissipation drastically comparing with the conventional class A amplifier. The constant and small V_{CE} can be provided by the variable power supply voltage to be linearly changed with the input voltage.

Figure 1 shows the configuration of the proposed class I amplifier. The output is taken at the output node of class A amplifier and the variable power supply is made of a class D power amplifier and two floating DC supplies. The class D amplifier is a switching power supply having high efficiency, rapid dynamic response and good linearity about the input signal.

If the power transistors operate in the active region and yet the voltage between collector and emitter is small, the power dissipation of class A amplifier becomes small. If the efficiency of a class D amplifier has higher than 90%, the efficiency of the proposed class I amplifier also approached nearly 90%. However, the voltage V_{CE} cannot be too small because of the saturation voltage plus some margin for the output transistors of class A to be separated in the active region. Two floating power supplies of which the DC levels are small are attached to satisfy this condition in series with the output of class D amplifier.

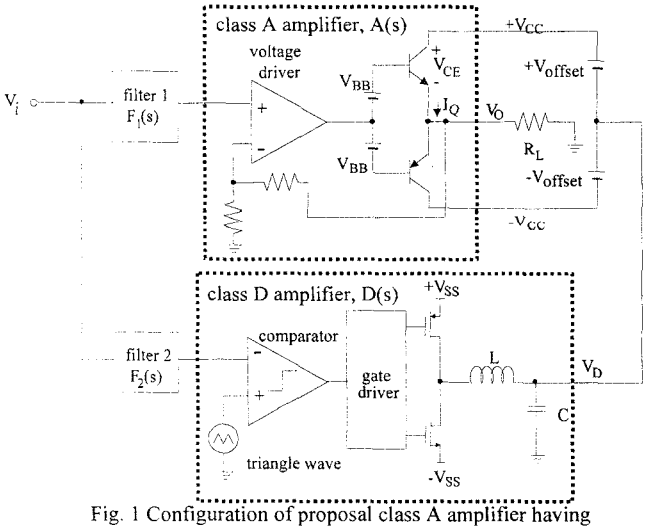

Fig. 1 Configuration of proposal class A amplifier having the variable power supply.

0-7803-3840-5/97/$10.00 © 1997 IEEE

III. CLASS A PART

The output transistors of conventional class A generate too much heat by high power consumption. As the output power rating of the amplifier increases, many transistors and large heat sinks are needed for stable operation. The temperature rise of semiconductor junction relative to the surrounding ambiance can be expressed as

$$T_J - T_A = (\theta_{JC} + \theta_{CS} + \theta_{SA})\, P_{diss} \quad (1)$$

where T_J : junction temperature,
T_A : ambiance temperature,
θ_{JC}: thermal resistance between junction and case,
θ_{CS}: thermal resistance between case and heat sink,
θ_{SA}: thermal resistance between heat sink and ambiance,
P_{diss}: dissipating power.

As the dissipating power increases, the thermal resistance should be low under the given temperature difference. Even if the heat sink is infinity, transistors are not safe from thermal problem because of the thermal resistance between junction and heat sink. As a result the temperature difference has a limit by the recommended junction temperature and ambiance. These limit the dissipating power per transistor. The output transistors of a high power class A amplifier is connected in parallel to solve the thermal problem. The number of transistors in parallel, n, is given by

$$n = \frac{P_{diss}(\theta_{JC} + \theta_{CS} + \theta_{SA})}{T_J - T_A} \quad (2)$$

The dissipating power at the class A is $2V_{CC}I_Q$ that is two times the output power. Meanwhile that of the class A part of the proposed class I amplifier, P_I, is given by

$$P_I = 2V_{offset} I_Q = \frac{\sqrt{2} V_{offset} V_O}{R_L} \quad (3)$$

where V_{offset} : floating power supply voltage,
I_Q : quiescent current,
R_L : load resistance,
V_O : RMS output voltage at full power.

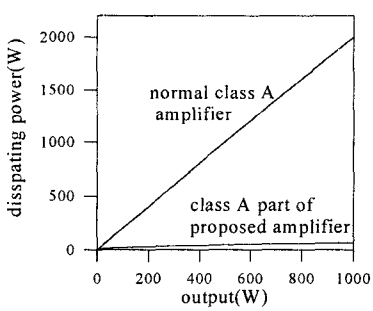

Fig. 2. Dissipating powers

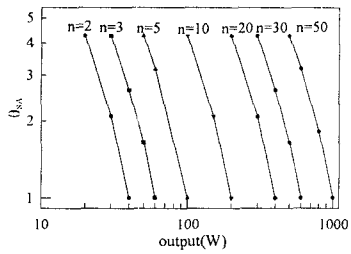

Fig. 3(a). Output power vs. thermal resistance at class A where n is the number of power transistors in parallel.

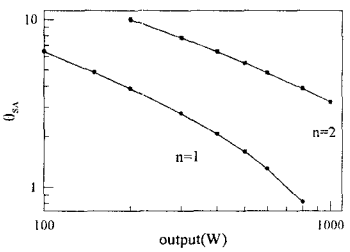

Fig. 3(b). Output power vs. thermal resistance at the class A part of proposed amplifier where n is the number of power transistors in parallel.

Figure 2 shows the dissipating power of conventional class A only and the class A part of the proposed class I amplifier where the V_{offset} is 3V at 8Ω load. Figure 3 is the graph of the output power versus the thermal resistance between heat sink and ambiance per transistor at changing the number of transistors under the same condition where dissipating power = 2 x output power, T_J = 80°C, T_C = 25°C, θ_{JC} = 1.25°C/W, θ_{CS} = 1.0°C/W, R_L = 8Ω and V_{offset} = 3V, respectively. The required number of transistors in the output driver of the actual amplifier is twice that of transistors in Fig. 3 because the output driver circuit is the push-pull. Figure 3(a) shows that a conventional class A needs many transistors and large heat sink as output power increases. A conventional class A amplifier at rating 100W needs 10 transistors by push-pull and the heat sink of which the volume is 6.8 liter and 200W transformer theoretically. If 1KW class A power amplifier is aimed, 100 transistors with 68 liter volume of heat sink and 2KW transformer are needed theoretically. These power components generate large parasitic components that may make the system in trouble. On the other hand, only four transistors with the heat sink of which the volume is smaller than 1 liter and 1.1KW transformer are needed in the class A amplifier part of the proposed class I amplifier at rating 1KW as shown in Fig. 3(b). Undoubtedly, much less transistors and small heat sink are needed at rating 100W.

The power conversion efficiency, κ, between a conventional class A and the proposed class I amplifier is expressed as

$$\kappa = \frac{P_O/(P_P + P_O)}{P_O/P_A} \approx \frac{2V_O}{\sqrt{2}V_{offset} + V_O} \quad (4)$$

where κ : power conversion efficiency between two type power amplifiers,

P_A : supplied power in a general class A amplifier,

R_L : load,

P_O : output power.

The power conversion efficiency of the proposed class I is close to two times that of a conventional class A amplifier as the output power rating increases.

IV. Class D Part

To get good performances in the class A part of the proposed class amplifier, the output of class D amplifier should be close to that of class A as shown in Fig. 4. If the output amplitude of class D amplifier is inferior to that of class A, the output can not be gotten sufficiently. The bandwidth of the class D amplifier should also be as wide as possible to get wide bandwidth from the output node of the proposed amplifier. The bandwidth of a conventional class D amplifier, however, is narrow and changing by the output load. The switching frequency needs to be higher to widen the bandwidth, however, the output swing range becomes narrower in this case because the ratio of transient time versus steady-state time becomes larger per switching period. Dual negative feedback can also be applied to improve the performances as shown in Fig. 5. Inner loop is the current feedback loop from the output inductor current, and outer loop is the voltage feedback loop from the output load voltage in Fig. 5[6].

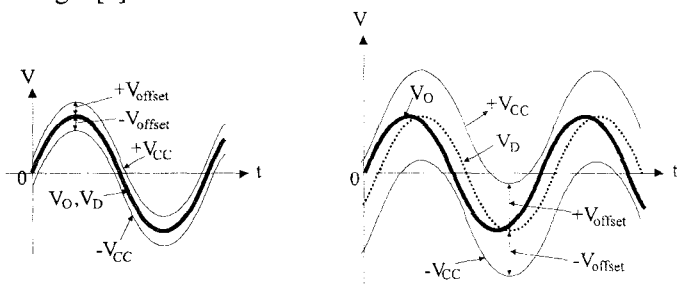

Fig. 4. Waveforms of amplifier supply voltage

$\pm V_{CC}$: supply voltage of class A amplifier

V_O : output of class A amplifier

V_D : output of class D amplifier.

The consideration points at the design are as follows.

a) Wide bandwidth : The bandwidth of class D should be as wide as possible. The cutoff frequency of an LC output filter that makes dominant double or complex poles is chosen higher than 20KHz.

b) Low phase delay : The LC output filter rejects the switching noise, however, it produces complicated phase distortions near the cutoff frequency range. The filters in front of the amplifiers as shown in Fig. 1 are designed to compensate amplitude and phase difference between the class A amplifier and the class D.

c) Switching frequency : The lower the switching frequency, the lower the switching loss. Thus the switching frequency should be chosen as low as possible to gain high efficiency. On the other hand, the switching frequency should be higher than two times the cutoff frequency of class D amplifier by sampling theorem. However, it is known that a class D amplifier bandwidth is less than one-third of the switching frequency[6,7]. Thus the switching frequency should be chosen higher than three times that of the cutoff frequency.

Considering the above points, the cutoff frequency of LC output filter is chosen to be thirty kilo hertz. The overall bandwidth of the class D amplifier with the dual negative feedback is set to about fifty kilo hertz by moving poles. The second order LC filter is selected for less phase delay at the output. The switching frequency is six times higher than the bandwidth. Additional LC notch filter of which the pole frequency is three hundred kilo hertz is inserted to reject the switching noise sufficiently.

V. Matching Filter

The performances of the class A part are excellent. The bandwidth is wide and flat from DC to several hundred kilo hertz. The phase delay is nearly zero in the audio frequency range. The class D part, however, has poor performances although the dual negative feedback is applied. The bandwidth is not wide and only flat from several hertz to several tens of kilo hertz. The phase delay is generated by the switching delays of the comparator, gate driver, output switching power devices and LC filter. One component of the phase delay is the group delay by the switching operation, and another is the delay by the poles of output filter and op-amps. These make phase shift as well as amplitude degradation in the audio frequency range. Filters need to match the frequency response difference between the class A and the class D.

The transfer function from V_i to V_O in Fig. 1 is $F_1(s)A(s)$, and that from V_i to V_D is $F_2(s)D(s)$. Two transfer functions should be same in the audio frequency range minimally. The conditions to get the output are successfully as follows :

$$F_1(s)A(s) = F_2(s)D(s) \quad (5)$$

$$|D_s\cos(\omega_s t)| + V_{sat} < V_{offset}. \quad (6)$$

The first condition to satisfy Eq. (5) is to match the amplitude of the class A amplifier, $|A(s)|$, with that of the class D, $|D(s)|$. This is tuned by equalizing the gains of two amplifiers at 1KHz. The two filter gains are also made unity at 1KHz. The amplitude of D(s), however, becomes lower than that of A(s) in the low and high frequency ranges. The low frequency range of class D amplifier is wide sufficiently to several hertz. To simplify the filter 1, a pole and a zero that make low cutoff frequency are inserted to fit the bandwidth of class A

amplifier to that of class D. Equation (5) ignoring poles and zeros of low frequency can be written approximately as

$$F_1(s)\cdot\frac{A_1}{\left(\frac{s}{\alpha}+1\right)} = F_2(s)\cdot\frac{D_1 e^{-st_d}}{\left(\frac{s}{\beta}+1\right)\left(\frac{s}{\beta^*}+1\right)} \quad (7)$$

where A_1 and D_1 are the same, the frequency of α is several hundred kilo hertz, those of β and β^* are several tens of kilo hertz, t_d is a switching delay. From this equation a zero, β, should be inserted to enhance the gain of the high frequency range of class D amplifier in $F_2(s)$. $F_2(s)$ should have one more pole, α, by causal system. $F_1(s)$ is set to compensate the other pole, β^*, and switching delay time, that is,

$$F_1(s) = \frac{e^{-st_d}}{\left(\frac{s}{\beta_{RE}}+1\right)} \quad (8)$$

where β_{RE} = real part of complex β.

According to this, the amplitude between class A amplifier and class D is matched, phase does not. The difference between two amplifiers outputs without the filter 1 and 2 is given by

$$A_o \sin(\omega t) - D_o \sin(\omega t+\theta) = 2A_o \sin\left(\frac{-\theta}{2}\right)\cos\left(\omega t+\frac{\theta}{2}\right) \quad (9)$$

where $A_O = D_O$ = output voltage,
$\theta = 2\pi f t_d$,
t_d = sum of delay time of switching devices.

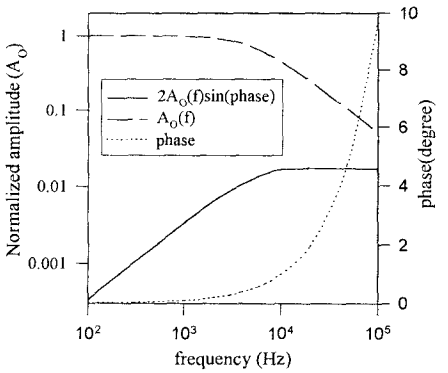

Fig. 6. Amplitude between class A amplifier and class D.

The sum of the delay time of switching devices including a comparator, a gate driver and MOSFETs is 270ns according to databooks[8,9]. The difference between two amplifier outputs without the filter 1 and 2 is $2A_O \sin(-2.7\times10^{-7}\pi f)\cos(\omega t+2.7\times10^{-7}\pi f)$. It is known that the power bandwidth of audio signal is 5KHz. Namely, the equation is rewritten as $2A_O(f)\sin(-2.7\times10^{-7}\pi f)$, where $A_O(f)$ is $A_O/\sqrt{1+(f/5000)^2}$. The maximum magnitude of $2A_O(f)\sin(-2.7\times10^{-7}\pi f)$ is $0.0137A_O$ as shown Fig. 6. As the magnitude is too small, switching delay does not affect the performance. The phase delay by a complex pole of the class D is also not important, because the amplitude of audio signal is too small around this frequency. The filter 1 can be simplified as follows :

$$F_1(s) = \frac{1}{\left(\frac{s}{\beta}+1\right)} . \quad (10)$$

To set stable bias voltage of class A output, Eq. (6) is rewritten as follows :

$$2A_O \sin(-\theta/2) + 0.5\,|\,D_s\cos(\omega_s t)| + V_{sat} < V_{offset} . \quad (11)$$

The offset voltage must be larger than the sum of the difference between amplifier outputs, the ripple voltage of class D output and the saturation voltage of power transistors of class A part. Assuming each term to be about one volt, the offset voltage should be higher than three volt.

IV. Efficiency

A. Dissipation power of class A circuit

The class A part consists of an input stage, a voltage gain stage and an output stage. The dissipation power of the input stage and the voltage gain stage is less than one tenth that of the output stage. The dissipation power of the output stage is shown in Eq. (3).

B. Losses of class D circuit

Figure 7 shows the turn-on and turn-off waveform plots of MOSFET. The power loss of class D comes from the conduction loss, switching loss and gate drive loss. The switching loss varies depending upon the operation mode of output circuit. The operation mode is determined by the amplitude difference between the peak output current of audio signal and ripple current of output circuit. The ripple current is given by

$$I_{ripple} = \frac{V_{CC}}{2f_S L} \quad (12)$$

where V_{CC} = supply voltage of class D amplifier,
f_S = switching frequency,
L = inductance of the inductor of the output filter.

The peak output current of audio signal is $\sqrt{2P_O/R_L}$ where P is output power and R_L is output load. If the peak output current is less than the ripple current, the switching operation of the output MOSFET occurs at the zero voltage condition, otherwise it becomes hard switching.

1) Conduction loss

The conduction time is from t_3 to t_6 in Fig. 7. For the purpose of brevity, the loss of antiparallel diode is assumed to be ignored, as the conduction time of antiparallel diode is short. Then the conduction loss can be simplified as follows :

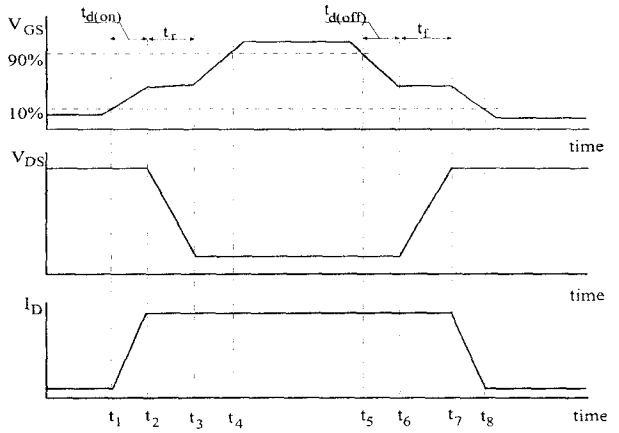

Fig. 7. turn-on and turn-off waveform of MOSFET.

$$P_{oond} = \frac{t_{cond}\hat{I}_O^{\,2} R_{on}}{T} \quad (13)$$

where t_{cond} = conduction time of MOSFET,
T = switching period,
$\hat{I}_O$ = RMS output current,
R_{on} = on resistance of MOSFET.

2) Turn-on switching loss

The MOSFET device has a high voltage across its output terminals and no current at the turn-on instant. The current starts to rise toward its final value and the voltage starts to fall from its initial value. The turn-on time is from t_1 to t_3 in Fig. 7. If these slopes are linear during this time and the reverse recovery time of diode is short and the operation mode is hard switching, the turn on switching loss is given by

$$P_{t\text{-}on} = \frac{1}{T}\left[V_{CC} I_D (t_{d(on)} + t_r) + V_{CC} Q_{rr} t_{rr} \right] + \frac{1}{2} f_S C_{OSS} V_{CC}^{\,2} \quad (14)$$

where $t_{d(on)}$ = turn on delay time,
t_r = rise time,
t_{rr}=reverse recovery current,
V_{CC}=supply voltage,
I_D = drain current,
Q_{rr}=reverse recovery charge.
C_{OSS} : stray capacitance of MOSFET.

3) Turn-off switching loss

Comparing with turn-on state, the state of MOSFET is opposite at the turn-off instant. The turn-off switching loss is generated by the integrated product of the current and the voltage during this transient time that is the sum of the turn off delay time and the fall time. This loss always generates no matter what operation mode. The turn-off time is from t_6 to t_8 in Fig. 7. Supposing this time is about the same as turn-on delay time because of the reverse operation of turn-on, the turn-off switching loss is approximately

$$P_{t\text{-}off} = \frac{1}{2T}\left[2V_{CC} I_D (t_{d(on)} + t_f) \right] \quad (15)$$

where t_f = fall time.

4) gate driver loss

Charging and discharging the gate capacitance cause this loss. The total gate charge, Q_g , that is gate-to-source charge and gate-to-drain("Miller") charge required by the gate and the peak voltage across the gate determines the amount of energy stored in the gate capacitance. As the gate is being charged through a gate resistor, the same amount of energy is dissipated in that resistor. When the gate is discharged, the stored energy is also dissipated. Therefore, the loss of the gate associated with turning the devices on and off per cycle is

$$P_g = V_{gs} Q_g f_s \quad (16)$$

where V_{gs} : gate voltage for turning on a device
Q_g : total gate charge required to raise the gate voltage to V_{gs}.

5) total loss of class D

The total loss of a class D is the sum of the above losses. As an example, lte us consider a class D amplifier of which the electrical specifications are that supply voltage is ±40V and load is 8Ω for 100W. The selected power MOSFETs are IRF540 and IRF9540, and gate driver is TC427. The calculated conduction loss, turn-on loss, turn-off loss and gate driver loss are 1.53W, 5.74W, 0.94W, and 0.53W at full power rating of 100W by databooks, respectively[8,9]. The calculated total power loss of the class D is 8.74W. The power conversion efficiency of class D is $P_{out}/(P_{out} + P_{D\text{-}loss})$ where $P_{D\text{-}loss}$ is total loss of class D. It is about ninety-two percent at 100W rating of the class D amplifier.

C. Efficiency of the proposed amplifier

The power supplied to class D part is the sum of output power and dissipating power. The power supplied to class A part is the sum of the power from the output of class D part and offset voltage. The power conversion efficiency of the proposed amplifier is described as follows :

$$\eta = \frac{P_{out}}{P_{D\text{-}out} + P_{D\text{-}loss} + P_{A\text{-}avg}} = \frac{1}{\eta_{class\text{-}D} + \frac{\sqrt{2}V_{offset} V_O}{\hat{V}_O^{\,2}}} \quad (17)$$

where $P_{out} = P_{D\text{-}out}$: output power
$\eta_{class\text{-}D}$: efficiency of class D
$\hat{V}_O$: output voltage.

Since $\hat{V}_O \le V_O$, $V_{offset} << V_O$, the maximum efficiency is obtained when $\hat{V}_O = V_O$, and depends upon the ratio between the offset voltage and the peak output voltage. Being assumed that class D has ninety-two percent throughout the output power, the efficiency of the proposed amplifier is shown Fig.

8 together with the other ones. It shows that the lower the offset voltage, the higher the power conversion efficiency. The efficiency is better than that of class B as well as class A throughout the whole range of output power.

VII. Simulation and Experimental Results

To show the performances of the proposed amplifier, the variable power supply is designed with the class D amplifier having an output power rating of 100W at 8Ω load with 300kHz switching frequency. Compensation filters are designed considering the frequency responses of the class A and the class D is gotten. The quiescent current of class A part

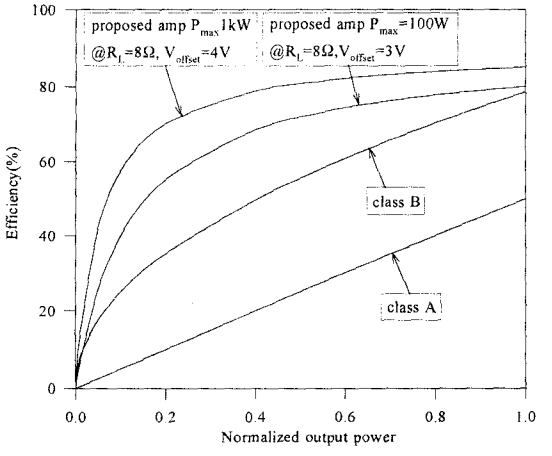

Fig.8. Efficiency of class A and class B and proposed amplifier.

is set somewhat higher than the conventional class A to minimize the nonlinearity. Simulations are done by setting the quiescent current of class A to be 3A, and the offset voltage to be.

To verify the performances of proposed class I amplifier, one prototype amplifier is constructed and tested. The -3dB bandwidth is measured from 3Hz to 100kHz as shown Fig. 9. This shows that the frequency response of the proposed amplifier is made mostly flat by the well-designed filters in spite of the poor frequency response of class D amplifier. The upper frequency higher than one hundred kilo hertz is not measured because the maximum bandwidth of the class D amplifier is nearly one third of switching frequency. The output power of the class D part is 112W, and the offset voltage power is 18W. The loss of class D amplifier is larger than the calculated losses, because of ignoring the losses of body diode and parasitic components, so on. Figure 10 is the efficiency comparison of four kinds of classes. The distortion of the proposed amplifier is seventy-seven percent at 100W.

Meanwhile the efficiency of class A amplifier for the same rating is thirty-seven percent. This figure shows that the efficiency of the proposed amplifier is superior to that of class B as well as that of class A amplifier. Figure 11 shows each node voltage at 25W. The distortion is mainly composed of the second harmonic distortion and some switching noise of class D amplifier. Figure 12 is a distortion graph. Although the measured distortion of class D is 0.051 percent at the rating of 10W at 1KHz, that of the proposed amplifier is 0.018 percent. The experimental results, however, are influenced somewhat the switching noise of class D amplifier through ground wire and EMI.

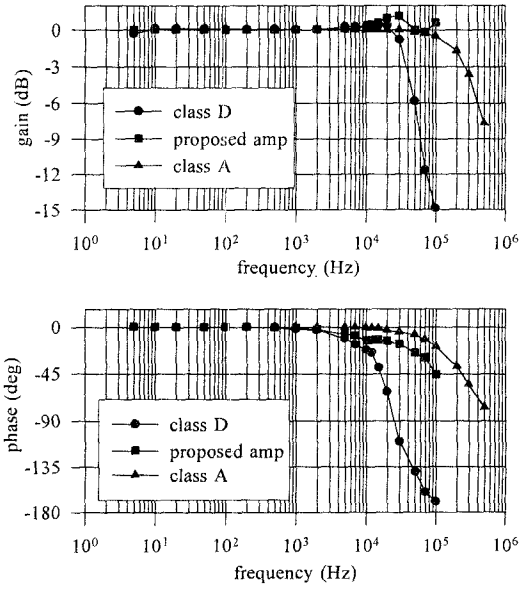

Fig. 9. Frequency responses of class A and class D and proposed amplifier.

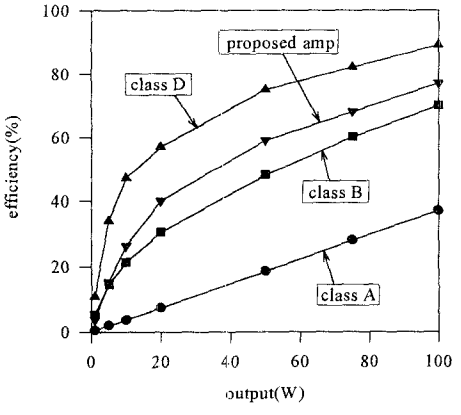

Fig. 10. Efficencies of class A,B,D and proposed amplifier.

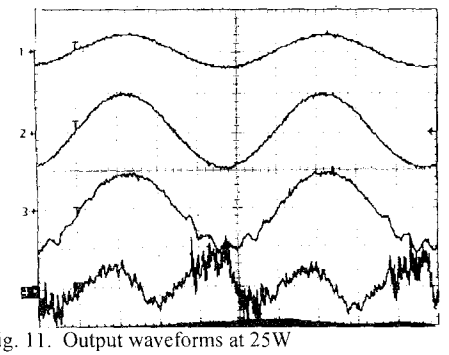

Fig. 11. Output waveforms at 25W
1 : input (1V/div) 2 : proposed amp output (10V/div)
3 : output of class D amp (10V/div)
4 : noise of proposed amp output, time : (200μs/div).

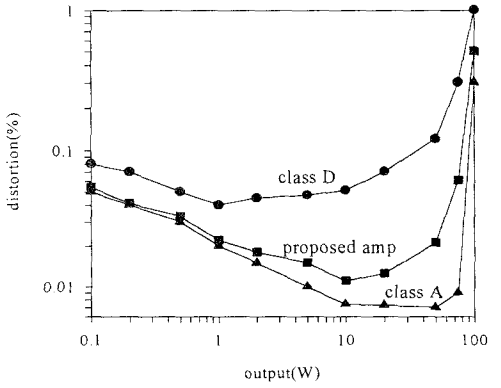

Fig. 12. Distortion of class A, D, and proposed amplifier.

VIII. Conclusions

There are a number of papers announced to increase the efficiency of output power amplifier. Especially they use class G and H in the audio frequency range, which increase the efficiency of an output driver by changing power supply voltage discretely. This paper proposes a method to increase the efficiency by changing the supply voltage continuously according to input signal level, which is named class I. To implement the class I, a high efficiency class A power amplifier accompanied by a class D switching power amplifier and floating power supplies is constructed. Because the bandwidth of the proposed amplifier depends on that of class D amplifier, the performances of class D amplifier is improved by applying dual negative feedback. To match the frequency responses between class A and class D, filters are inserted considering the condition of the offset voltage.

As the power requirement of a conventional class A amplifier is too high, a lot of power transistors and large heat sink are needed. It is hard to make a class A power amplifier higher than 100W. In the proposed amplifier, it is easy to make a high power amplifier, because it has less heat problem and fewer power components. This amplifier needs more careful wiring and shielding because of the switching noise.

The proposed amplifier has better efficiency than class A amplifier and less distortion than class D amplifier. The efficiency of the proposed amplifier increases as the output power rating does. This class I amplifier is thought to be a new candidate that can satisfy both the high-fidelity and high efficiency with high power rating.

References

[1] J. A. Jensen, "A New Principle for a High-Efficiency Power Audio Amplifier for Use with a Digital Preamplifier," J. Audio Eng. Soc. vol.35. No.12 1987 Dec. pp984-993

[2] S. El-Hamamsy, "Design of High-Efficiency RF Class-D Power Amplifier," IEEE Transactions on Power Electronics, Vol. 9, No. 3 May 1994 pp297-308

[3] T. Sanpei, S. Ohashi, Y. Ohta, S. Inosue, "Highest Efficiency and Super Quality Audio Amplifiers Using MOS Power FETs in Class G Operation, " IEEE Tran. Consumer Electron, vol. CE-24, 1978. Aug. pp300-307

[4] Frederick, "Average Efficiency of Class G Power Amplifiers," IEEE Transactions on Consumer Electronics, Vol. CE-32, No.2 May 1986

[5] Bill Roehr, "A Simple Direct-Coupled Power MOSFET Audio Amplifier Topology Featuring Bias Stabilization," IEEE Transactions on Consumer Electronics, Vol. CE-28, No.4 Nov. 1982

[6] J. H. Jeong, H. H. Seong, J. H. Yi, G. H. Cho, "A Class D Switching Power Amplifier with High Efficiency and Wide Bandwidth", 1995 IEEE Conference on Consumer Electronics 1995 Jun. 7-9 pp.428-429

[7] Hsu, A. Brown, L. Rensink, R.D. Middlebrook, "Modeling and Analysis of Switching DC-to-DC Converters in Constant Frequency Current Programmed Mode," IEEE PESC Proceeding 1979

[8] "HEXFET Power MOSFET Designers Manual" 1987 INTERNATIONAL RECTIFIER

[9] "Teledyne components", Teledyne databook 1992