A High Efficiency, Soft Switching DC–DC Converter with Adaptive Current-Ripple Control for Portable Applications

Siyuan Zhou, *Student Member, IEEE*, and Gabriel A. Rincón-Mora, *Senior Member, IEEE*
Georgia Tech Analog & Power IC Design Lab

***Abstract*— A novel control scheme for improving the power efficiency of low-voltage DC-DC converters for battery-powered, portable applications is presented. In such applications, light-load efficiency is crucial for extending battery life, since mobile devices operate in stand-by mode for most of the time. The proposed technique adaptively reduces the inductor current ripple with decreasing load current while soft-switching the converter to also reduce switching losses, thereby significantly improving light-load efficiency and therefore extending the operation life of battery-powered devices. A load-dependent, mode-hopping strategy is employed to maintain high efficiency over a wide load range. Hysteretic (sliding-mode) control with user programmable hysteresis is implemented to adaptively regulate the current ripple and therefore optimize conduction and switching losses. Experimental results show that for a 1 A, 5 to 1.8 V buck regulator, the proposed technique achieved 5% power efficiency improvement (from 72% to 77%) at 100 mA of load current and a 1.5% improvement (from 84% to 85.5%) at 300mA, which constitute light-load efficiency improvements, when compared to the best reported, state-of-the-art techniques. As a result, the battery life in a typical DSP microprocessor application is improved by 7%, which demonstrates the effectiveness of the proposed solution.**

***Index Terms*— Efficiency, Battery life, DC-DC converter, switching regulator, buck converter, soft switching, hysteretic control, sliding-mode control**

I. Introduction

BATTERY-POWERED, portable electronic devices like cellular phones, pagers, laptop computers, PDAs, etc. have become increasingly popular. In such systems, low-voltage circuits are necessary to satisfy the demands of single battery operation and the ever decreasing breakdown voltages of state-of-the-art technologies [1]. Furthermore, to maximize battery life, highly power efficient DC-DC converters are strongly desired [2]. In a battery-supplied environment, load conditions change drastically from high to low power levels. A full loading condition is not present for prolonged periods; rather, these devices run at light loads (stand-by mode) for most of the time [3]. Therefore, improving light-load efficiency of DC-DC converters is crucial for extending battery life.

A complete characterization of power losses in DC-DC converters is offered in [4]. A typical efficiency curve of a DC-DC converter can be generally partitioned into three regions, as shown in Fig. 1. In region I (high loads), the dominant power losses are the conduction losses induced by the load current (DC component of the inductor current, i.e., I_{load} as shown in Fig. 2), which is high. In region II (light loads), the major power losses result from the V-I overlap losses and current ripple induced conduction losses (i.e., rms losses). The V-I overlap losses are switching losses associated with the voltage-current (V-I) overlap of the power train (S_P and S_N in Fig. 2), which are proportional to load current, input voltage, and switching frequency. The conduction losses caused by the current ripple (systematic AC component of the inductor current, i.e., ΔI_{Lf} as shown in Fig. 2) become dominant because the overlap loss scales down with the load current while the power dissipated by current ripple normally remains constant. Thus, soft switching [5-10], which eliminates overlap losses, is the best existing power-saving technique in this load range. In region III (very light loads), the gate-drive losses consumed when charging and discharging the gate capacitances of the power transistors (S_P and S_N in Fig. 2) during switching transitions dominate, so decreasing the switching frequency is the best way to reduce the total loss. Although the exact rank of power losses depends on specific converter design parameters, like the current ripple magnitude, input voltage, and size of the power transistors, Fig. 1 is a conceptual guideline to choose the best power-saving technique for a variety of load ranges, extending to both extreme ends of the load-current range.

Many efficiency improvement techniques have been proposed over the years [4]. Among those techniques, soft switching is attractive since it eliminates the V-I overlap losses by switching the power transistor when either its voltage or its current is zero (zero-voltage/current switching or ZVS/ZCS).

Manuscript received February 3, 2005; revised July 8, 2005. This work was supported by Texas Instruments through the Texas Instruments Analog Fellow program at the Georgia Institute of Technology. This paper was recommended by Associate Editor Soumitro Banerjee.

The authors are with the Georgia Tech Analog & Power IC Design Lab, School of Electrical and Computer Engineering, Georgia Institute of Technology, Atlanta, GA 30332 USA (e-mail: syzhou@ece.gatech.edu; rincon-mora@ece.gatech.edu).

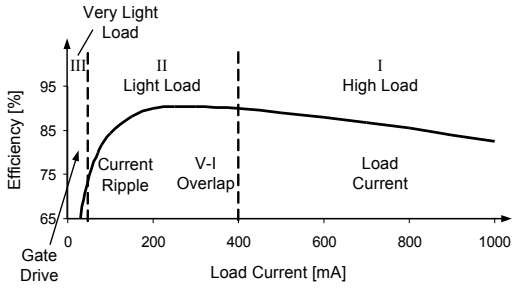


Fig. 1. General partition of the efficiency curve of a DC-DC converter.

Various soft switching topologies have been reported such as quasi-resonant (QR) [5] and multi-resonant (MR) [6] converters, quasi-square-wave converters (QSW) [7], ZVS/ ZCS-PWM converters [8], and zero-voltage/ current-transition (ZVT/ZCT) PWM converters [9-10]. A comparative evaluation of those topologies is offered in [11]. For portable applications, where volume, weight, and cost are particularly important, the QSW is the most suitable, since the fewest additional components (only one resonant capacitor) are used, when compared to other soft switching topologies. As shown in Fig. 2, it achieves ZVS in synchronous discontinuous-conduction mode (DCM) by utilizing the reverse inductor current to charge the resonant capacitor during "dead time." Since the inductor current ripple is larger than twice the maximum load current, this topology suffers from high conduction losses, high current stresses, and degraded accuracy at high loads. At light loads, nevertheless, a hard-switched converter naturally enters synchronous DCM, when the load current drops below half of the current ripple, thus QSW is feasible at light loads. However, in a conventional QSW ZVS converter, the current ripple does not change when the load current decreases, therefore the constant conduction losses associated with the current ripple severely degrade overall efficiency. On the other hand, if the current ripple is adaptively reduced while ensuring ZVS operation, the light-load efficiency can be significantly improved, which is the essence of the strategy proposed in this paper.

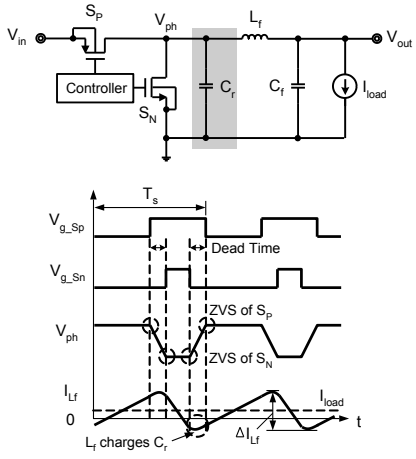


Fig. 2. Circuit schematic and waveforms of the conventional QSW ZVS buck converter (in synchronous DCM).

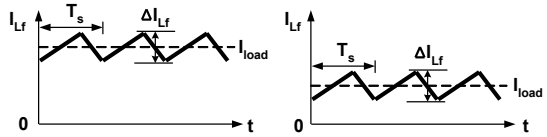
The organization of the rest of the paper is as follows. The proposed control strategy and a circuit implementation using hysteretic control are described in Sections II and III, respectively. Experimental results, which verify the proposed strategy, are shown and discussed in Section IV, and finally conclusions are offered in Section V.

II. Proposed Control Strategy

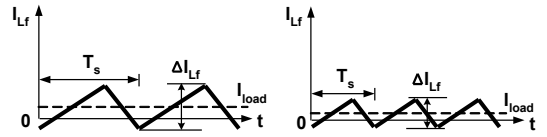
As shown in Fig. 1, at light loads (region II), the dominant and therefore targeted power losses are V-I overlap and current ripple induced conduction losses. As a result, to optimize power efficiency, soft switching should be implemented with minimum required current ripple. Since the filter inductor current ripple (ΔI_{Lf}) and switching frequency (f_s) are related by

$$f_s = \left(\frac{V_{out}}{V_{in}} \times \frac{V_{in} - V_{out}}{L_f}\right)\frac{1}{\Delta I_{Lf}}, \qquad (1)$$

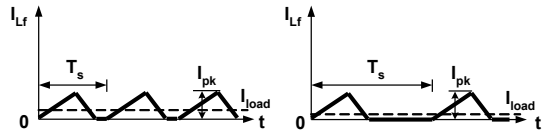
smaller current ripple implies higher switching frequency, if other parameters are fixed. The waveforms of the inductor current ripple in the proposed three operational modes are shown in Fig. 3. At high loads (region I), the load current itself determines the majority of the total power losses, therefore the proposed control strategy is the conventional synchronous continuous-conduction mode (CCM) with constant current ripple and hard switching, as shown in Fig. 3(a).



(a) Mode 1 (CCM with constant current ripple)



(b) Mode 2 (synchronous DCM with adaptive current ripple)



(c) Mode 3 (asynchronous DCM with constant peak current)

Fig. 3. Waveforms of the filter inductor current ripple in the proposed three operation modes: (a) Mode 1, (b) Mode 2, and (c) Mode 3.

At light loads (region II), the proposed converter hops from CCM to synchronous DCM by first increasing the current ripple until enough reverse inductor current is available to achieve QSW ZVS. The increased conduction losses induced by the higher current ripple are balanced by the reduced V-I overlap losses, so the efficiency is not degraded. Moreover, instead of maintaining the current ripple constant, it is reduced as the load current decreases, as shown in Fig. 3(b), thereby adaptively reducing conduction losses and significantly improving light-load efficiency. On the other hand, a larger current and output voltage ripple is tolerable since the accuracy requirements at light loads (stand-by mode) are

relaxed.

At very light loads (region III), the frequency increases to the point where gate-drive losses start to degrade the efficiency. Thus, the frequency is reduced at very light loads, hopping back to hard switching, asynchronous DCM, since the V-I overlap loss is now negligible. Moreover, with constant peak current control [12] (Skip Mode), the frequency decreases proportionally with load current, as shown in Fig. 3(c), which keeps the efficiency approximately constant. Therefore, a load-dependent mode hopping strategy [13], based on the trade-offs between conduction and switching losses, is proposed to maintain high efficiency over a wide load-current range.

III. Proposed Circuit Implementation

In this implementation, it is assumed that the output voltage ripple (ΔV_{out}), like in many practical commercial solutions [14], is dominated by the equivalent series resistance (ESR) of the filter capacitor, as is the case for low-cost tantalum capacitors. Therefore, a hysteretic (sliding-mode), voltage-controlled scheme using a comparator with programmable hysteresis [15] can be utilized to adaptively control the current ripple, which is simple and inherently stable. As shown in Fig. 4, the comparator output (V_{comp}) is triggered when V_{fb} exceeds the controllable upper and lower hysteretic window limits ($V_{hyst(U)}$ and $V_{hyst(L)}$), which lie above and below V_{ref}. Thus, the current ripple can be expressed by

$$\Delta I_{Lf} = \frac{\Delta V_{out}}{R_{Cf\_ESR}} = \frac{V_{hyst(U)} + V_{hyst(L)}}{R_{Cf\_ESR}}, \quad (2)$$

and adaptively controlled by changing the hysteresis.

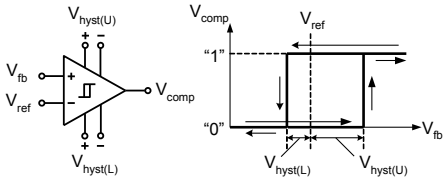


Fig. 4. Characteristics of the user programmable hysteretic comparator.

The detailed schematic of the proposed converter is shown in Fig. 5. Compared to a conventional hard-switched buck converter, an auxiliary NMOS switch (S_1), a resonant capacitor (C_r), and the corresponding control circuits are added. The user programmable hysteretic comparator is used for the main loop control. For proof of concept, both hysteresis setting and mode hopping are realized manually. The *Mode* signal is used to enable the soft switching operation (Mode 2). The detailed control of the proposed three operational modes is described below.

In Mode 1 (high loads), *Mode* is low, so S_1 is disabled and C_r is disconnected from ground. The converter operates in conventional CCM with constant current ripple and hard switching, i.e. $V_{hyst(U)}$ equals $V_{hyst(L)}$, which is constant.

In Mode 2 (light loads), *Mode* is high, so C_r is connected to ground via S_1. The converter transforms to the QSW topology, and ZVS for S_P and S_N in synchronous DCM is realized, as shown in Fig. 2. Moreover, $V_{hyst(U)}$ and $V_{hyst(L)}$ are both set to $(I_{load}+I_{neg})\times R_{Cf\_ESR}$, thus, ΔI_{Lf} equals $2\times(I_{load}+I_{neg})$ (I_{neg} is the minimum negative inductor current needed to achieve QSW ZVS) and is thus adaptive to I_{load}.

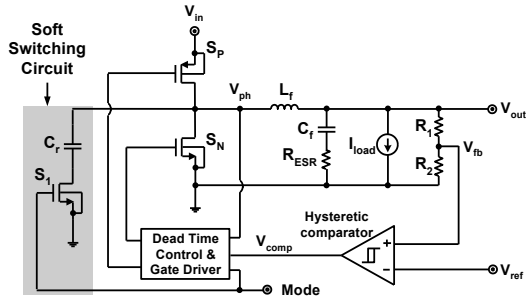


Fig. 5. Detailed schematic of the proposed buck converter.

In Mode 3 (very light loads), *Mode* is low, so C_r is again disconnected. The proposed converter operates with hard switching in asynchronous DCM, where $V_{hyst(U)}$ and $V_{hyst(L)}$ are different and approximately determined by

$$V_{hyst(U)} = I_{pk} R_{Cf\_ESR} + \frac{I_{pk}^2 \times L_f}{2C_f (V_{in} - V_{out})}, \quad (3)$$

and

$$V_{hyst(L)} = \frac{I_{pk}^2 \times L_f}{2C_f (V_{in} - V_{out})} \left(\frac{V_{in}}{V_{out}} \right), \quad (4)$$

where I_{pk} is the preset constant peak current in L_f and is significantly higher than I_{load}. Although S_1 is hard-switched, it only happens during mode transition depending on the loading conditions; thus, after averaging over time, its hard-switching losses will not significantly degrade overall efficiency performance.

IV. Experimental Results

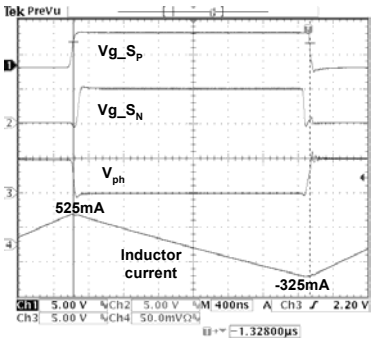
The proposed converter shown in Fig. 5 is implemented on a PCB prototype. The component parameters are summarized in Table 1. The gate-drive signals for S_P and S_N, the node voltage V_{ph}, and the inductor current waveform shown in Fig. 6 verify the functionality of the proposed control scheme. As shown in Fig. 6(a), the buck converter operates in synchronous CCM and hard switching with 850mA of current ripple. With the same current ripple and thus 325mA negative inductor current, QSW ZVS for S_P and S_N can be realized, as shown in Fig. 6(b). However, the current ripple can be decreased while ensuring QSW ZVS. As shown in Fig. 6(c), the current ripple is reduced to 500mA, and ZVS for S_P turning on is still achieved with 150mA negative inductor current. Therefore, the proposed scheme of reducing the current ripple, while ensuring QSW ZVS at light loads, is indeed feasible.

The efficiency of the proposed buck converter shown in Fig. 5 is compared with the best combination of the previously reported techniques, as applied to the same converter, including the conventional synchronous CCM (constant ripple, hard switching with positive inductor current) [16], PWM in synchronous DCM (constant ripple, hard switching with negative inductor current) [17], the conventional QSW ZVS (constant ripple, soft switching with negative inductor current) [7], and the conventional PFM in asynchronous DCM (skip

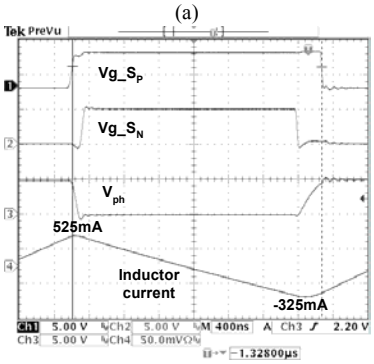
mode, constant peak current, hard switching with no negative inductor current) [12].

TABLE 1
THE COMPONENT PRAMATERS OF THE PROTOTYPE CONVERTER.

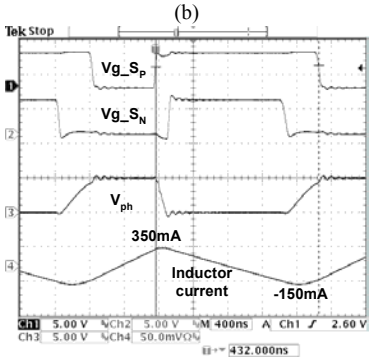
Component	Parameters
Input voltage	5V
Output voltage	1.8V
Load current	1mA to 1A
S_P	IRF7105, Rds(on)=300mΩ, Cin=290pF
S_N	IRF7105, Rds(on)=150mΩ, Cin=330pF
S_1	IRF7311, Rds(on)=25mΩ, Cin=900pF
L_f	8.2uH, ESR=20mΩ
C_f	47uF, tantalum cap, ESR=75mΩ
C_r	12nF, ceramic cap, ESR<1mΩ
Hysteretic comparator	TPS56100 from Texas Instruments



(a)



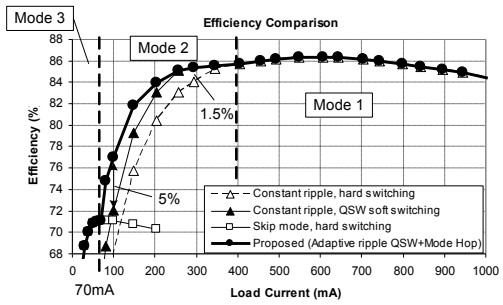
(b)



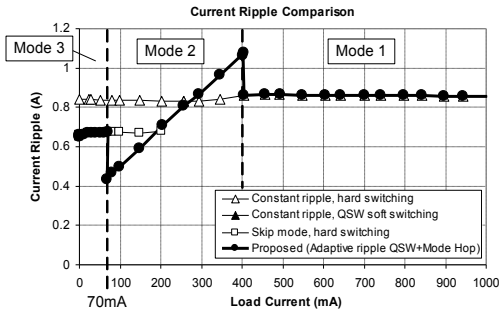
(c)

Fig. 6. Experimental waveforms of the buck converter at 100mA load current: (a) hard switching, current ripple=850mA, (b) soft switching, current ripple=850mA, (c) soft switching, current ripple=500mA.

The efficiency and current ripple performance of the converter in different techniques are compared in Fig. 7, with a load-current range from 1 mA to 1 A. The current ripple at light loads (70 to 400 mA) is adaptively controlled to $2\times(I_{load}+150mA)$. Mode-hopping thresholds are determined from the intersections of the efficiency curves for the various modes.



(a)



(b)

Fig. 7. Experimental performance comparison of the converter using different control schemes: (a) efficiency and (b) current ripple.

In Mode 1 (I_{load} > 400 mA), the proposed converter operates in conventional CCM with constant 850mA current ripple and hard switching. In Mode 2 (70 < I_{load} < 400 mA), the efficiency from 250 to 400 mA is improved over its hard switching, synchronous CCM counterpart from 84% to 85.5% at 300 mA. The increase of current ripple enables QSW ZVS by introducing enough negative inductor current (150mA) to charge V_{ph} during dead time. The V-I overlap loss may not be completely eliminated due to the speed limit (bandwidth) of the control circuit. Also, additional power losses occur due to charge and discharge of resonant capacitor C_r. However, as shown in Fig. 8(a) which compares all the power losses at 300mA from measurement and calculation using the equations in [4], the reduced V-I overlap loss (14mW) is larger than the increased current ripple conduction loss (4mW), which results in a net total power reduction (10mW) and therefore an overall improvement in efficiency by 1.5% at 300mA. For load currents from 70 to 250 mA, light load efficiency is significantly improved over the conventional QSW ZVS with constant current ripple, from 72% to 77% at 100mA. As shown in Fig. 8(b), the conventional QSW ZVS improves the efficiency by reducing 47% of the total V-I overlap loss (18mW) at 100mA; however, the constant current ripple conduction loss (20mW) limits the extent of the improvement (from 68% to 72%). With the proposed adaptive current ripple control in QSW ZVS, the further 60% reduction in current-ripple-induced conduction loss (12mW) achieves another 5% overall efficiency improvement (from 72% to 77%) at 100mA, which demonstrates the benefit of the proposed control

scheme. In Mode 3 (I_{load} < 70 mA), the efficiency is maintained above 60% by adopting the skip mode control in [12]. With the mode-hopping strategy, a high efficiency can therefore be maintained over a wide load current range.

The battery life (runtime or operational life) improvement is measured by powering the buck converter with a four-cell NiMH battery stack in a typical DSP microprocessor application. The batteries are fully discharged before reuse to minimize the memory effect. The proposed control scheme and the combination of the best reported techniques are applied to the same converter. Experimental results show that the battery life is improved by 7%, from 195 minutes using the existing control techniques to 210 minutes using the proposed control strategy.

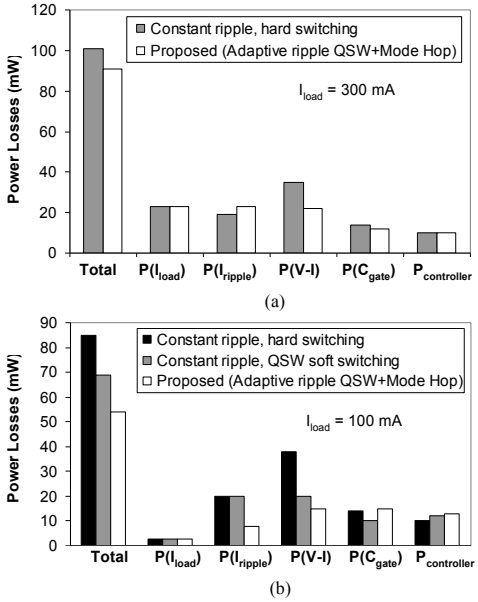


Fig. 8. Experimental comparison of power losses under various control algorithms: (a) I_{load} = 300 mA and (b) I_{load} = 100 mA.

V. Conclusion

An experimental prototype of the proposed scheme has verified improvements in light-load efficiency of a 1A, 5 to 1.8 V buck converter from 72% to 77% at 100mA and from 84% to 85.5% at 300mA over the best reported, state-of-the-art alternatives. The light-load efficiency performance is significantly improved by adaptively reducing the current ripple with decreasing load currents, while allowing high enough reverse inductor current to assure QSW ZVS, thereby minimizing both conduction and switching losses simultaneously. The battery life (runtime or operational life) in a typical DSP microprocessor application is thereby improved by 7% as a result of the enhanced light-load efficiency. The control scheme is simply implemented by adaptively changing the hysteresis window of a sliding-mode, hysteretic buck converter.

In conclusion, the essence of the proposed power-saving technique is to adaptively control the current ripple in a soft switching environment, optimally balancing conduction and switching losses in a battery-powered application. A load-dependent, mode-hopping strategy maintains high efficiency over a wide load-current range, which is critical in the exploding portable, battery-powered market.

Acknowledgment

The authors thank Texas Instruments for its sponsorship of the research project.

References

[1] A.J. Stratakos, S.R. Sanders, and R. Brodersen, "A Low-Voltage CMOS DC-DC Converter for a Portable Battery-Operated System," 25th Annual IEEE Power Electronics Specialists Conference, Vol. 1, pp. 619–626, 1994.

[2] T. Ogawa, S. Hatanaka, and K. Taniguchi, "An On-Chip High-Efficiency DC-DC Converter with a Compact Timing Edge Control Circuit," Symposium on VLSI Circuits, Digest of Technical Papers, pp. 278–279, 2002.

[3] "The Art of Analog Design," National Semiconductor analog seminar series 2003/04, pp. 4-52.

[4] M. Gildersleeve, H. P. Forghani-zadeb, and G.A. Rincón-Mora, "A Comprehensive Power Analysis and a Highly Efficient, Mode-Hopping DC-DC Converter," IEEE Asia-Pacific Conference on ASIC, pp. 153–156, 2002.

[5] K.H. Liu, R. Oruganti, and F.C. Lee, "Quasiresonant Converters – Topologies and Characteristics," IEEE Transactions on Power Electronics, Vol. PE-2, pp. 62–74, 1987.

[6] W.A. Tabisz and F.C. Lee, "Zero-Voltage-Switching Multi-Resonant Technique – A Novel Approach to Improve Performance of High-Frequency Quasiresonant Converters," 19th Annual IEEE Power Electronics Specialists Conference Records, pp. 9–17, 1988.

[7] V. Vorperian, "Quasi-Square Wave Converters: Topologies and Analysis," IEEE Transactions on Power Electronics, Vol. 3, No. 2, pp. 183–191, April 1988.

[8] G. Hua and F.C. Lee, "A New Class of ZVS-PWM Converters," High Frequency Power Conversion Conference, pp. 244–251, 1991.

[9] G. Hua, C. Leu, Y. Jiang and F.C. Lee, "Novel Zero-Voltage-Transition PWM Converters," 23rd Annual IEEE Power Electronics Specialists Conference Records, pp. 55–61, 1992.

[10] R.N. Prado, "A New ZVT PWM Converter Family: Analysis, Simulation and Experimental Results," 9th Annual Applied Power Electronics Conference and Exposition, Vol. 2, pp. 978–983, 1994.

[11] G. Hua and F.C. Lee, "Soft-Switching Techniques in PWM Converters," IEEE Transactions on Industrial Electronics, Vol. 42, No. 6, pp. 595–603, December 1995.

[12] B. Arbetter, R. Erickson and D. Maksimovic, "DC-DC Converter Design for Battery-Operated Systems," 26th Annual IEEE Power Electronics Specialists Conference, Vol. 1, pp. 103–109, 1995.

[13] A. Prodic and D. Maksimovic, "Digital PWM Controller and Current Estimator for A Low-Power Switching Converter," 7th Annual Workshop on Computers in Power Electronics, pp. 123–128, 2000.

[14] "Designing Fast Response Synchronous Buck Regulators Using the TPS5210," Texas Instruments Application Report, SLVA044, pp. 16, March 1999.

[15] G.A. Rincón-Mora, "Accurate, fast, and user programmable hysteretic comparator," US Patent 6,229,350 B1, May, 2001.

[16] O. Djekic and M. Brkovic, "Synchronous Rectifiers vs. Schottky Diodes in a Buck Topology for Low Voltage Applications," 28th Annual IEEE Power Electronics Specialists Conference, Vol. 2, pp. 1974–1980, 1997.

[17] S.H. Jung, N.S. Jung, J.T. Hwang, and G.H. Cho, "An Integrated CMOS DC-DC Converter for Battery-Operated Systems," 30th Annual IEEE Power Electronics Specialists Conference, Vol. 1, pp. 43–47, 1999.