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Wu, Yu, Jiang, Dai, Bardill, Andy ORCID logoORCID: <https://orcid.org/0000-0002-2451-3260>,
de Gelidi, Serena ORCID logoORCID: <https://orcid.org/0000-0001-6141-2736>, Bayford,
Richard ORCID logoORCID: <https://orcid.org/0000-0001-8863-6385> and Demosthenous,
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A High Frame Rate Wearable EIT System Using Active Electrode ASICs for Lung Respiration and Heart Rate Monitoring

Yu Wu, *Student Member, IEEE*, Dai Jiang, *Member, IEEE*, Andy Bardill, Serena de Gelidi, Richard Bayford, *Member, IEEE* and Andreas Demosthenous, *Fellow, IEEE*

Abstract—A high specification, wearable, electrical impedance tomography (EIT) system with 32 active electrodes is presented. Each electrode has an application specific integrated circuit (ASIC) mounted on a flexible printed circuit board, which is then wrapped inside a disposable fabric cover containing silver-coated electrodes to form the wearable belt. It is connected to a central hub that operates all the 32 ASICs. Each ASIC comprises a high performance current driver capable of up to 6 mA_{p-p} output, a voltage buffer for EIT and heart rate signal recording as well as contact impedance monitoring, and a sensor buffer that provides multi-parameter sensing. The ASIC was designed in a CMOS 0.35- μm high-voltage process technology. It operates from ± 9 V power supplies and occupies a total die area of 3.9 mm². The EIT system has a bandwidth of 500 kHz and employs two parallel data acquisition channels to achieve a frame rate of 107 frame/s, the fastest wearable EIT system reported to date. Measured results show that the system has a measurement accuracy of 98.88% and a minimum EIT detectability of 0.86 Ω /frame. Its successful operation in capturing EIT lung respiration and heart rate biosignals from a volunteer is demonstrated.

Index Terms—Active electrode, electrical impedance tomography (EIT), heart rate, integrated circuits, lung respiration monitoring, multi-parameter sensing, wearable EIT belt.

I. INTRODUCTION

EACH year 15 million babies are born prematurely, many with respiratory morbidity requiring respiratory support to improve their survival. Exposing their vulnerable lungs to mechanical ventilation is, however, a risk factor for lung injury and likely to cause long-term respiratory sequelae lasting to adulthood [1], [2]. Available monitoring tools, such as X-rays or computerized tomography scan, only provide intermittent diagnosis that may cause delay in treatment of atelectasis. Lack of regional ventilation information, and exposure of infants to radiation also makes these methods far from ideal [3].

Electrical impedance tomography (EIT) is a non-invasive, radiation-free medical imaging technique that can provide continuous real-time lung aeration monitoring. It can image the

relative interior alteration of any conductive object by injecting small ac currents through electrodes placed on the subject under test (SUT). The resulting current paths through the SUT, induce potentials on its boundary surface. Due to interior conductivity re-distribution, for example, from lung respiration, inner-impedance variation occurs which is reflected on the amplitude and the phase of the electrode voltages. Using this voltage data, an image that reflects the relative interior alteration of the SUT can be constructed.

In the last 30 years many EIT systems have been developed [4]-[6] for general or targeted medical applications. Although some of the more recognizable systems have gone through several updates [7], [8] EIT is still far from ready for daily clinical practice due to image qualities affected by errors in the hardware as well as stray capacitance influence [9] caused by the impractical patient electrode interfaces [10], [11]. Methods investigated to improve system performance include: 1) current drivers with high output impedance [12]; 2) fully-parallel read-out channels to reduce delays in EIT scans and improve image frame rate (this is not only more suitable for monitoring neonates whose breathing is twice as fast as adults, but also can capture rapid physiological changes such as epilepsy [13], [14]); 3) stray capacitance cancellation circuits aiming to calibrate out the stray capacitance [15], [16]; which finally evolves to the most practical, 4) active electrode approach that reduces the effect of parasitic capacitance in the cables and switch networks by placing the electronics in direct contact with the electrodes [17].

To minimize noise and improve hardware performance while keeping the size small, some of today's EIT systems use application specific integrated circuits (ASICs) as active electrodes [18]-[20]. Also, two commercial systems for adult respiration support have been developed [21], [22] and clinical studies monitoring aeration in preterm babies using these adult systems have been reported with positive results [23], [24]. However, especially for infants born extremely preterm, a successful wearable bedside EIT system for lung function monitoring in daily clinical practice is still hampered by their limited functionality (e.g. low frame rate). To address this, a high specification wearable EIT system is described in this paper. Although it is demonstrated in an adult system in the form of an active 'wearable belt' its specification technology conforms to the requirements of neonatal applications. The main features of this 32 electrode EIT system (CRADLvision 1.0) are: 1) a high performance ASIC for active electrodes; 2) a

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Y. Wu, D. Jiang, and A. Demosthenous are with the Department of Electronic and Electrical Engineering, University College London, Torrington Place, London WC1E 7JE, U.K. (e-mail: a.demosthenous@ucl.ac.uk).

A. Bardill, S. de Gelidi, and R. Bayford are with the Department of Natural Sciences, Middlesex University, The Burroughs, London NW4 6BT, UK.

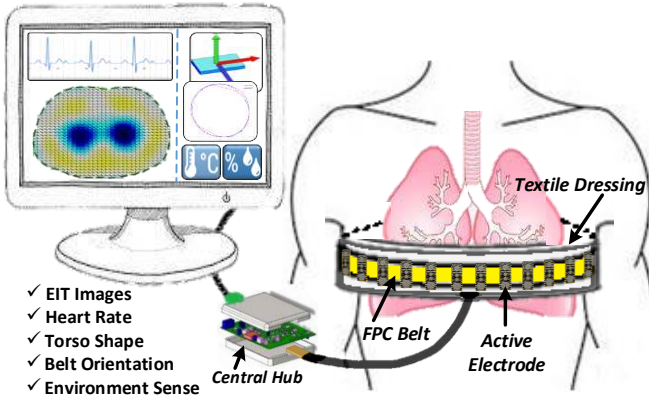


Fig. 1. Wearable EIT lung respiration monitoring system with heart rate monitoring and other functions using active electrode ASICs.

high frame rate (107 fps); 3) disposable textile electrode dressing [25]; and 4) multi-sensing functionality (heart rate monitoring, incubator temperature and humidity, and belt orientation and patient torso detection aiding EIT model selection for enhanced image reconstruction).

The rest of the paper is organized as follows. Section II describes the overall system design architecture, the digital control and signal processing blocks. Section III describes the ASIC for active electrodes comprising a linear feedback current driver and two analog buffer amplifiers. Section IV presents the measured electrical performance of the ASIC as well as measurements with the 32-electrode wearable EIT system constructed using these ASICs. The system is compared with other work showing its superiority in terms of high specification performance. Concluding remarks are presented in Section V.

II. SYSTEM DESIGN AND IMPLEMENTATION

The overview of the CRADLvision 1.0 EIT system is shown in Fig. 1. It comprises a wearable flexible printed circuit board (FPC) belt covered by a textile dressing, a central hub which controls the 32 active electrodes on the belt, and a computer display to visualize the captured clinical parameters (e.g. EIT images, heart rate etc). The first prototype belt has been designed to fit an average adult for test and validation purposes and can then be miniaturized for neonate applications.

A. System Architecture and Design

Fig. 2 shows the detailed system architecture. Each of the 32 ASICs [26] comprises a current driver (CD), a main buffer (B1) for measuring EIT and heart rate signals, and a multi-sensor buffer (B2). The ASIC is mounted on an active electrode printed circuit board (PCB) together with two analog switches (S1: ADG1211; S2: ADG1213) and a digital CPLD (XC2C64A) to provide signal routing. The 32 active electrode PCBs are identical and share all the colored analog paths shown in Fig. 2 (e.g. VDC, VO4, VO3 etc). The CPLD receives two daisy chains from the central hub. Sequentially, the first chain configures the desired active electrode to current drive mode while the other puts the selected electrode into voltage sense mode. The CPLD shifts the digital control signal in daisy chain

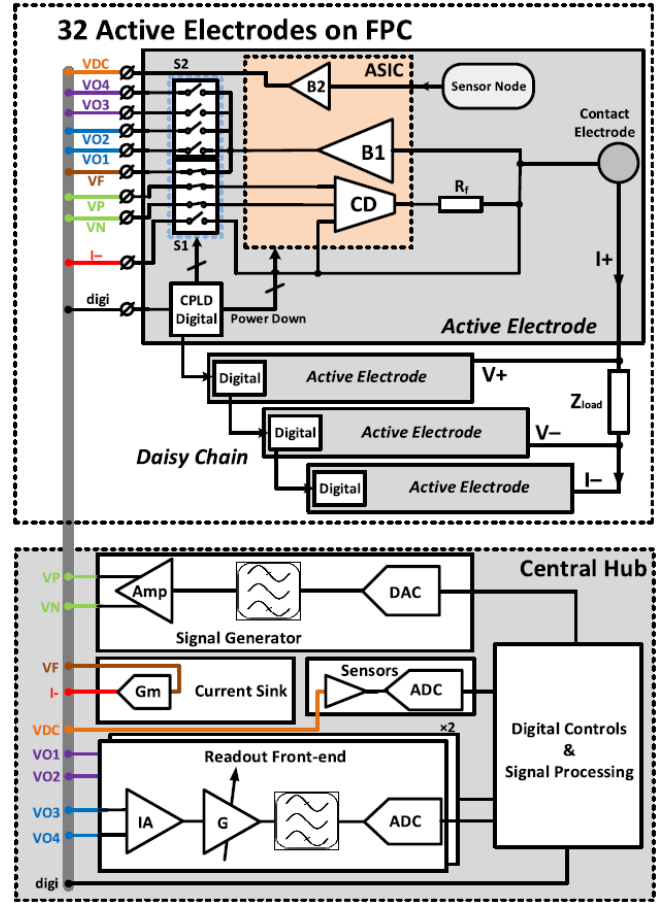


Fig. 2. Active electrode belt system architecture. B1 is the main buffer, B2 is the sensor buffer and CD is the current driver on the ASIC. All electrodes share colored analog paths, and are controlled by the digital CPLD.

according to a user-defined scan pattern. This method allows the user to define injection or measurement EIT scan patterns independently.

In the example of Fig. 2, the four active electrodes are configured into a typical tetrapolar bio-impedance measurement scheme. The top electrode is configured into current drive master-mode; CD in the ASIC is powered-on and the differential excitation signals VP and VN are connected to CD to generate current I_+ . Buffer B1 is connected to the VF path to send back the injecting electrode voltage for current sink feedback. The bottom active electrode is configured into current drive slave-mode. In this mode, the electrode turns on the appropriate analog switch to provide a current return path for I_- to flow back to the central hub. The two middle active electrodes are configured to voltage sense mode where only B1 is functioning. The CPLD selectively connects the output of B1 to one of the four VO paths (VO1, VO2, VO3, VO4) to send the voltage signal back to the instrumentation amplifiers (IAs) in the central hub. There are two parallel recording channels in the central hub; each channel concurrently converts 16 of the 32 measured voltages into the digital domain for I-Q demodulation.

Sensors with a voltage output can be connected to buffer B2 that can be selectively powered by the CPLD. The powered-on B2 sends its sensor measurement back to the central hub

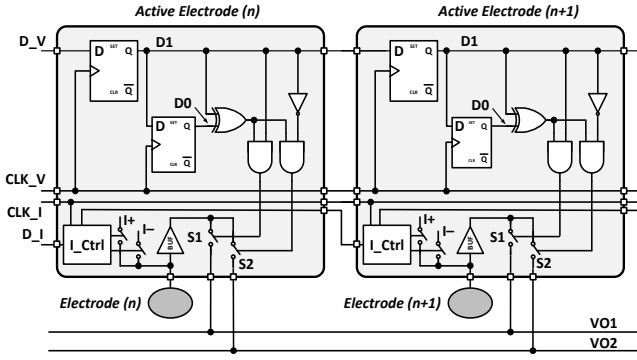


Fig. 3. Control logic for electrode selection.

through the VDC line. All modes of operation are explained in Section III.

B. Digital Controls and Signal Processing

1) Active electrode control:

One of the design challenges in the active electrode arrangement is how to address the electrodes for current drive and voltage scan. In order to construct one frame of image, the electrode voltage needs to be scanned 1024 times from different electrode positions. Using two parallel readout front-ends for voltage scan (see Fig. 2) and for a frame rate higher than 100 fps, data acquisition on each pair of electrodes must be completed within 19.5 μ s before the IAs are switched to the next pair of electrodes. Therefore, the digital control of electrode switching must be as fast as possible to allow sufficient time for the amplifiers to settle and for acquiring sufficient samples for signal processing. Independently activating each electrode for current drive or voltage scan would provide the maximum flexibility and fastest control, but would require two dedicated tracks on the belt for each electrode, which significantly increases the risk of device failure. Another option is to assign each electrode an address and broadcast the addresses of the selected electrodes via a shared bus on the belt. Although this solution could reduce the number of tracks on the belt, it requires a high data rate (>5 Mbits/s) to broadcast the addresses for fast electrode switching. A third option is to activate the electrodes in a pre-stored sequence. This avoids the shortcoming of the previous two solutions but limits the flexibility in electrode selection.

This design uses a shifting daisy chain control arrangement. This allows the electrode selection to be conducted from shared clock and data buses, where electrode switching is completed at a single clock edge and individual electrode addressing is not required. There are two 2-line control buses on the belt to activate the electrodes for current drive and voltage scan. Each bus consists of a clock line and a data line. The clock line is shared by all the active electrodes, and the data line is arranged in a daisy chain fashion. Fig. 3 illustrates the control arrangement for voltage scan. The data line D_V is cascaded in a daisy chain, which is clocked by CLK_V on the clock line. There are two latches in each electrode, where $D1$ is connected to the next electrode as part of the D_V daisy chain, and its output also feeds into the second latch, $D0$. During operation, a 32-bit stream shifts through the electrodes along D_V at one bit per rising edge of CLK_V . The bit stream has two identical

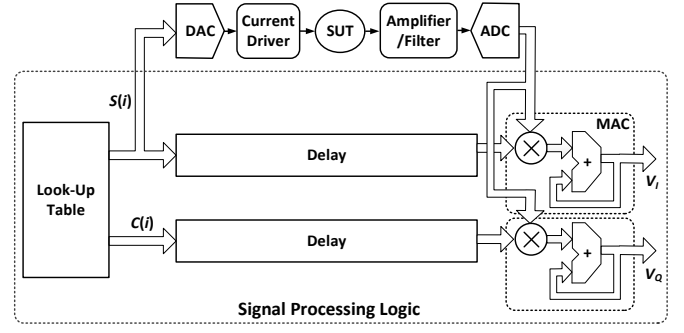


Fig. 4. Control flow of calculating vectors V_I and V_Q .

16-bit segments with either segment consisting of m consecutive logic “1” bits and $(16 - m)$ logic “0” bits. At every rising edge on CLK_V , each electrode latches the incoming bit to $D1$ and compares it with the previous bit on D_V , now latched on $D0$, to decide whether and how to activate this electrode for voltage scan. For example, as shown in Fig. 3, if $D1$ is “1” and $D0$ is “0” on *Active Electrode (n)* on the left, $S1$ will turn on to connect the buffered electrode voltage to $VO1$, which is connected to the positive voltage input of the IA in the readout front-end in the central hub (see Fig. 2). Concurrently, $D1$ will be “0” and $D0$ “1” on *Active Electrode (n+m)*, which will turn on $S2$ to buffer the electrode voltage to the negative input of the IA through $VO2$ (similarly for $VO3$ and $VO4$ from *Active Electrode (n+16)* and $(n+16+m)$, respectively). A full voltage scan cycle is completed by shifting the bit stream through the daisy chain, where the scan pattern can be programmed by changing the value of m .

The electrode activation for current drive is similar and is operated from the other 2-line bus on the belt consisting of D_I and CLK_I . The selected electrode connects to either $I+$ or $I-$. The scan pattern for current drive can also be programmed in the same fashion. For every bit shifting on D_I , a full voltage scan cycle is conducted. Once the bit stream on D_I has shifted through all the 32 active electrodes, the image acquisition of one frame is completed. CLK_I , CLK_V , D_I and D_V are all generated by the control and signal processing module in the central hub.

2) Control and Signal Processing in the Central Hub:

The control and signal processing module in the central hub operates at a 45 MHz master clock frequency. Besides controlling the electrode selection among the active electrodes, this module also manages a DDS-based signal generator for generating a frequency programmable sinusoidal signal for the current drivers, the operation of data acquisition from the readout front-end, and the extraction of the real and imaginary values of the impedance from the acquired data using digital lock-in demodulation.

Fig. 4 shows the control flow of impedance measurement during the voltage scan on a chosen pair of electrodes. The operation of data demodulation synchronizes to the signal generator. In operation, two 16-bit sequences, $S(i)$ and $C(i)$, are read out from a look-up table at a sampling rate of 3 MHz, where $S(i) = \sin 2\pi(n/N)$ and $C(i) = \cos 2\pi(n/N)$, and $N = 16$. $S(i)$ goes to the digital-to-analog converter (DAC) to generate a sinusoidal signal for the current drivers. Concurrently, both $S(i)$ and $C(i)$ values are first delayed to align with the time required

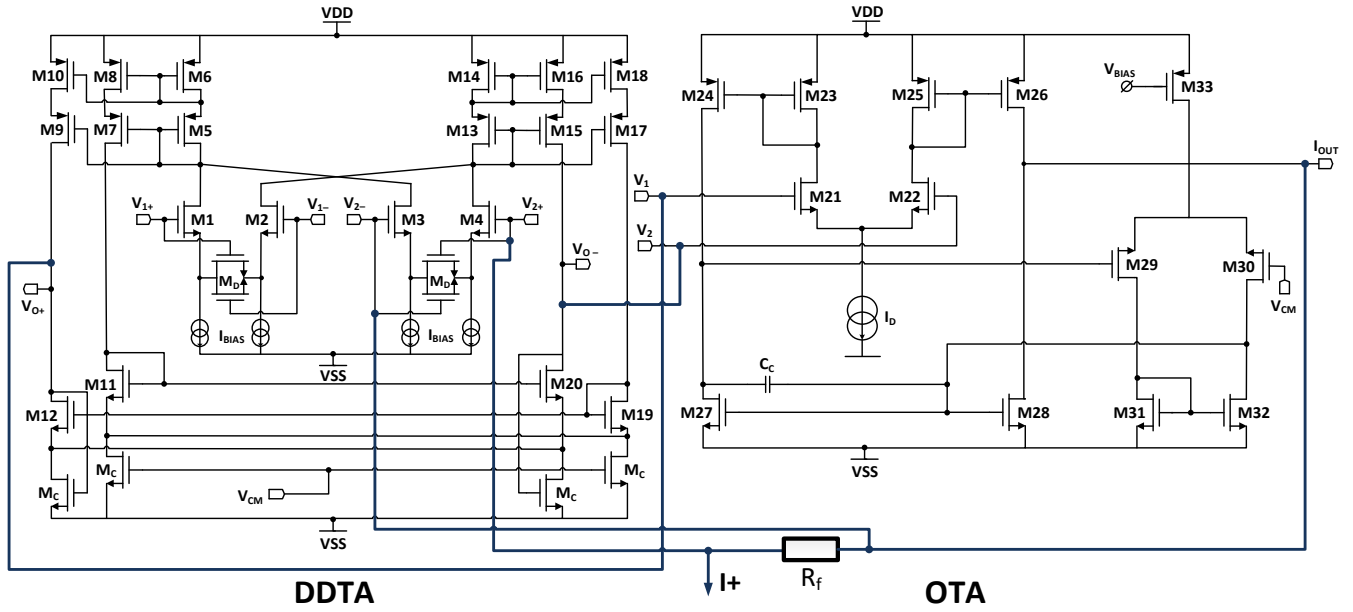


Fig. 5. Detailed transistor level schematic of the current driver (CD).

for the data conversion and analog readout circuits, and then are fed to a pair of multiplier accumulators (MACs) to multiply the analog-to-digital converter (ADC) samples of the voltage readout, $sample(n)$. The real and imaginary vectors, V_I and V_Q , can be respectively derived using

$$V_I = \sum_{n=0}^{N-1} sample(n) \cdot \sin 2\pi(n/N) \quad (1)$$

$$V_Q = \sum_{n=0}^{N-1} sample(n) \cdot \cos 2\pi(n/N). \quad (2)$$

The gains of the amplifiers in the readout front-end (Fig. 2) are set with respect to the relative position between the electrode pairs for voltage scan and current drive, in order to utilize the full dynamic range of the ADC input.

III. ACTIVE ELECTRODE ASIC

For active electrode EIT, a dedicated current driver and voltage buffer are intimately connected to each electrode and any signal routing is done afterward where the parasitic capacitance effect is less critical. This approach has several advantages over the passive or multiplexing EIT systems. For current drive, the parasitic capacitance due to the cables and switch network ranging up to hundreds of pF is reduced to only a few pF. This allows the current driver to maintain a high output impedance even at high frequencies [12], [16]. This not only increases the measurement accuracy but also increases the system operating bandwidth. For voltage measurement, a high and stable input impedance is seen from the SUT, and signals are buffered and carried to the central hub on a low-impedance path that is less sensitive to electromagnetic interference and crosstalk [15], [17].

The design of active electrodes in an EIT system remains challenging. Recently, an active buffer topology has been reported [17], where active voltage buffers are used together with passive current sources. In recent publications, integrated circuits have been developed and placed very close to the

electrodes [20]. However, a switch network still exists and this degrades the performance of the overall system. The system described in this paper employs an active electrode ASIC [26] that has both a wideband, high power current driver and low noise buffers directly connected to the skin-contact electrode, offering good performance and small size.

A. Current Stimulation and Contact Impedance Monitoring

The textile skin-contact electrode used has a measured noise of $236 \mu V_{rms}$ from 50 kHz to 1 MHz, suggesting that the minimum detectable voltage should be close to $1 mV_{p-p}$ to ensure an adequate SNR. For a 32-electrode system, the voltage potential developed on the furthest electrode could be 60-70 dB smaller than the potential at the current drive electrode. The textile electrodes used have a skin-electrode contact impedance $\sim 500 \Omega$ [25]. When injecting a current of $6 mA_{p-p}$ (which is within the international medical safety standard IEC-60601) it produces $\sim 3 V_{p-p}$ at the current drive electrode, and hence a voltage signal at the furthest electrode that is above the fabric-electrode noise level.

Fig. 5 shows the transistor level schematic of the current driver. It comprises a differential difference transconductance amplifier (DDTA) and an operational transconductance amplifier (OTA). The DDTA transfer function is

$$V_{O+} \approx \frac{\beta \cdot g_{m1}}{g_{out}} [(V_{1+} - V_{1-}) - (V_{2+} - V_{2-})] \quad (3)$$

where g_{out} is the admittance at node V_{O+} , β is the transistor current gain factor between transistors M6 and M8, and g_{m1} is the transconductance of the input transistors M1 to M4. To achieve a high output current amplitude with low distortion, four source-degenerated transistors M_D are added to the cross-coupled input pairs of the DDTA. The output branch is mirrored to provide a fully differential output. Using the four triode-transistors M_C for common-mode feedback, a bias voltage V_{CM} can set the common mode voltage at the circuit's

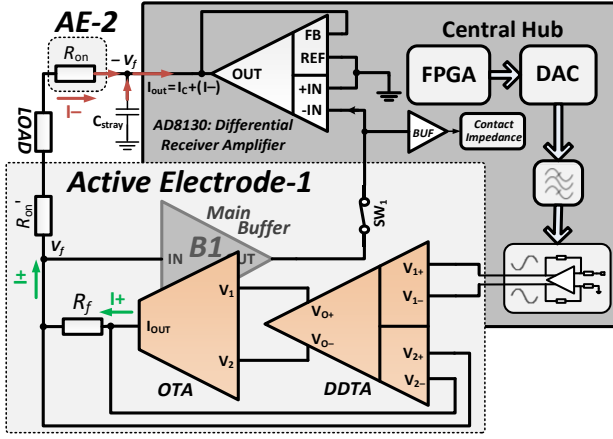


Fig. 6. Complete current driver topology in the EIT system.

output.

The transistor level circuit for the OTA is shown on the right-hand side of Fig. 5. It is based on a symmetrical topology and has a dc biasing stage M29 to M32 configured into a feedback loop with M24 and M27 to provide a biasing voltage for transistor M27 and M28 and set the dc level at I_{OUT} . The compensation capacitor C_C improves the phase margin of this dc biasing feedback loop. The OTA enhances the current output ability of the current driver.

In feedback, the DDTA measures the current in the off-chip feedback resistor R_f , and compares it with the input signal between V_{1+} and V_{1-} to provide the desired current. The transfer function of the current driver is

$$Gm_{CD} = \frac{I_{OUT}}{V_{1+} - V_{1-}} = \frac{Gm_{loop}}{1 + Gm_{loop} \cdot R_f} \approx \frac{1}{R_f} \quad (4)$$

where $Gm_{loop} = Gm_{ota} \cdot A_{ol_ddta}$; A_{ol_ddta} is the open loop gain of the DDTA and Gm_{ota} is the transconductance of OTA in Fig. 5. As the current is independent of the load, this feedback results in a high output impedance:

$$Z_{out} = [ro_{ota} + R_f(Gm_{loop} \cdot ro_{ota} + 1)] \quad (5)$$

where ro_{ota} is the small-signal high impedance at node I_{OUT} of the OTA. For $R_f = 500 \Omega$, $Gm_{loop} \geq 1.5 \text{ A/V}$ and $ro_{ota} \geq 1.5 \text{ k}\Omega$, Z_{out} is above $1 \text{ M}\Omega$. In practice, the output impedance seen by the load is defined by Z_{out} in parallel with any parasitic capacitances seen at the output. An active electrode provides an intimate connection between the current driver output and the electrode. This arrangement avoids the large parasitic capacitance from the cables and switches used to make the electrode connections in a conventional EIT system without active electrodes, and thus allows the high output impedance to be maintained at high frequency.

The transconductance of the current driver is frequency dependent:

$$Gm_{CD}(\omega) \approx \frac{1/R_f}{1 + \frac{j\omega R_f}{2\pi(f_p Gm_{loop} R_f)}} \quad (6)$$

The dominant pole is $f_p \cdot Gm_{loop} \cdot R_f$, where f_p is the dominant pole of the current driver in open loop. The OTA is designed to

have a wide bandwidth to enhance the Gm_{loop} and provide a large output current, thus f_p originates from the DDTA stage. For the current driver to have a bandwidth of 500 kHz and a phase delay $< 5^\circ$ at 500 kHz , the dominant pole of the DDTA is designed to be around 8 kHz . This results in a closed-loop dominant pole at 6 MHz , and a phase delay of 4.8° at 500 kHz .

The current driver implemented on the ASIC shown in Fig. 5 provides a single-ended excitation drive I_+ . As the SUT must be driven differentially, a current sink circuit is required to provide I_- (see Fig. 2). Any transconductance mismatch between the current source and current sink would force the unmatched current to flow through the output impedance node of the current drivers. This would produce a large common-mode signal that could produce measurement errors or even saturate the driver output [27]. The active electrode current drive method in [26] is not ideal, and an alternative sink current must be provided from the central hub.

A fully differential current source is proposed as shown in Fig. 6. When the selected *Active Electrode-1* is configured into master current excitation mode, a fully differential voltage signal is generated from the central hub as inputs to the current driver. This minimizes the input difference between the 32 current drivers on the wearable belt. The current driver on the ASIC sources a current of I_+ and the main buffer B1 senses the voltage V_f directly on the load and feeds it back to the central hub. The differential receiver amplifier (AD8130) receives V_f and generates a sink current I_- . When the source current I_+ is equal to sink current I_- , the voltage across the load is fully differential with zero common-mode voltage. This can be achieved by monitoring the common-mode voltage and actively offsetting the unmatched current [27], or generating a differential voltage with respect to V_f through feedback as shown in Fig. 6. With this circuit configuration, the transfer function of the differential receiver amplifier can be written as:

$$V_{out_AD8130} = V_f \left(\frac{1 - A_{open-loop}}{A_{open-loop}} \right) = -V_f \quad (7)$$

where $A_{open-loop}$ is the open loop gain of the AD8130. AE-2 is another active electrode that is configured in current drive slave-mode in Fig. 6. In this mode, an analog switch is turned-on to connect the differential receiver amplifier to the load. As this switch has an on-resistance R_{on} , a dummy R_{on}' is placed in series with R_f for load matching.

Despite the current sink circuit is located in the hub, its input signal V_f is actively buffered using B1, therefore the cable stray capacitance on the signal path is isolated from the output of the current driver on the active electrode, and the high output impedance of the current driver can be maintained. At the output of the differential receiver amplifier, to achieve $-V_f$, the receiver sinks not only a current I_- equal to I_+ , but also a current I_C to compensate for the cable stray capacitance in the current return path. As this current sink topology responds to the linear current feedback loop in the ASIC current driver, and compensates for the stray capacitance at its output, it also has a high output impedance.

The voltage V_f fed back by B1 can also be used to monitor the contact impedance. For a good contact, the contact impedance is around 500Ω , and a bad contact can be detected

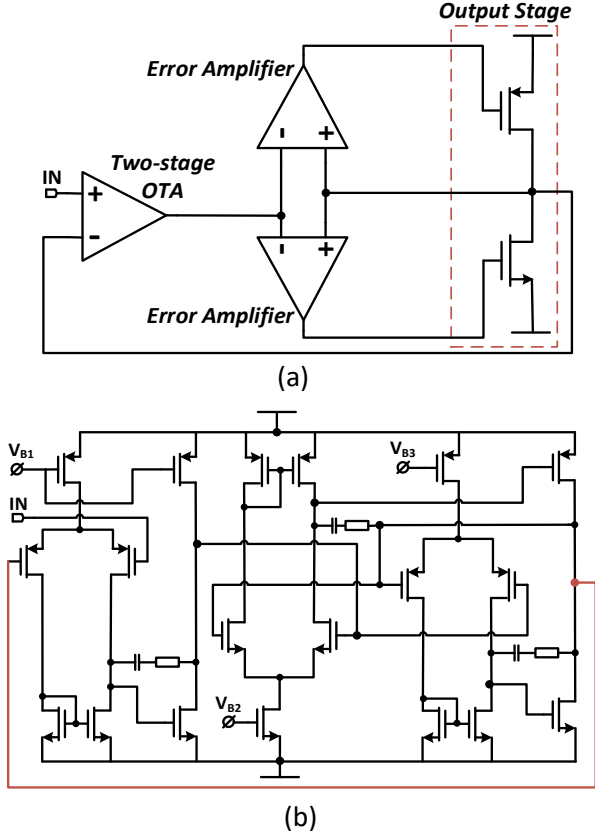


Fig. 7. Main buffer B1: (a) working principle and (b) transistor level circuit.

when the amplitude of $V_f > (I+) \times 500 \Omega$. By checking the voltage level on the buffer, the electrode contact can be continuously monitored while making EIT measurements in real-time.

B. EIT and Heart Rate Recording

The schematic of main buffer B1 is shown in Fig. 7. It comprises a two-stage Miller OTA, two error amplifiers, and a common-source push-pull output stage (necessary to drive the large capacitive load on the FPC). The two error amplifiers regulate the quiescent current in the push-pull transistors, and ensure the voltage at its output stage is equal to the voltage at the output of the OTA. The error amplifiers and the OTA are compensated for loop stability. With this configuration, the amplifier is designed to have a high slew-rate, and can drive a capacitive load on the FPC of up to 20 pF. During EIT recording, a pair of active electrodes is selected to be in the voltage sense mode. The main buffer B1 sends the signal back to an IA in the central hub (see Fig. 8) according to the user defined EIT scan pattern to measure the voltage difference between two electrodes. The current driver on the ASIC whose active electrodes are in voltage sense mode is powered-down as shown in Fig. 8.

The heart rate is also monitored between EIT scans. It is measured using a selected pair of active electrodes in voltage sense mode to detect the electrocardiogram (ECG) and send it via a separate analog path in the hub as shown in Fig. 8. After filtering which comprises a bandpass filter and 50 Hz notch filter, the ECG is digitalized and the heart rate can be plotted on a PC. This provides an efficient way of measuring heart rate as

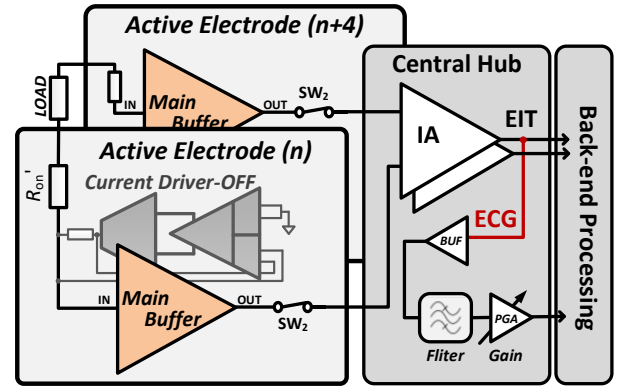


Fig. 8. Proposed EIT voltage signal recording with active electrodes.

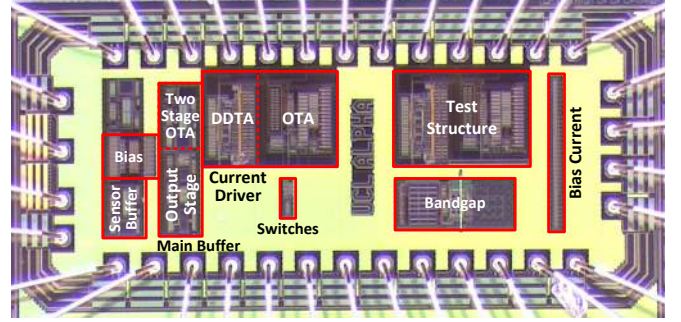


Fig. 9. Active electrode ASIC micrograph.

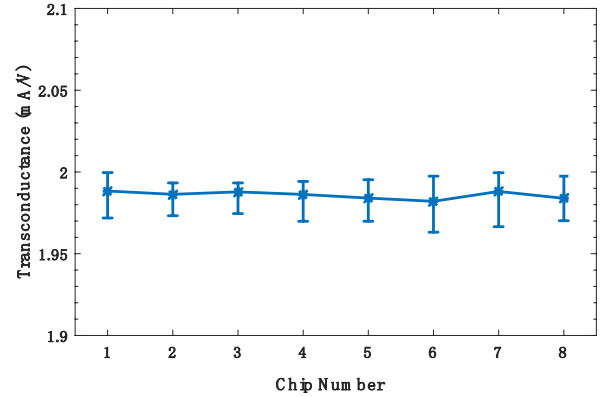


Fig. 10. Measured transconductance of the current driver across eight chip samples. The average value is 1.99 mA/V with a standard deviation of 10.3 μ A/V.

well as EIT without the need for dedicated electrodes or an ECG device.

C. Multi-Parameter Sensor Buffer

In addition to EIT and heart rate monitoring, the sensor buffer B2 on the ASIC allows measurement of dc signals from any connected sensor (e.g. shape sensor). This buffer uses a two-stage amplifier connected in unity feedback with a power-down. By controlling the power-down, the output of all sensor buffers can share a single bus line to the central hub for processing; this significantly simplifies the FPC design (see Fig. 2).

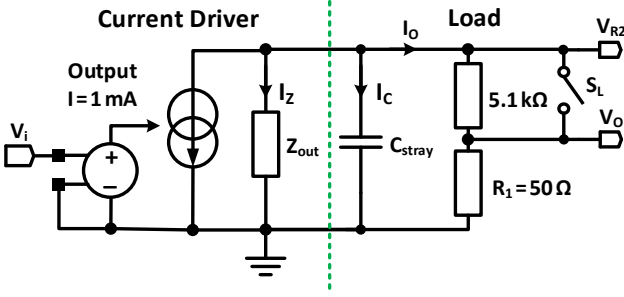


Fig. 11. Current driver output impedance measurement circuit equivalent model.

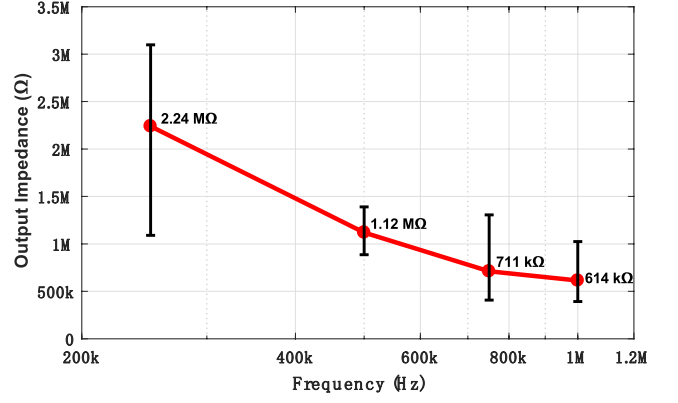


Fig. 12. Measured mean output impedance of the current driver.

TABLE I. ASIC MEASURED PERFORMANCE

	Transconductance (mA/V)	Bandwidth (Hz)	Phase (at 500 kHz)	Z_{out} (at 500 kHz)	Maximum I_{OUT}	THD	Voltage Compliance
Current Driver	1.99	500k	4°	1.12 M Ω	6 mA _{p-p}	55 dB	10 V _{p-p}
	Gain (V/V)	Bandwidth (Hz)	Phase (at 500 kHz)	Output Swing	THD	Input-Referred Noise (0.02-1 MHz)	
Main Buffer B1	0.98	750 kHz	2°	14 V _{p-p}	59 dB	22 μ V _{rms}	
Sensor Buffer B2	0.99	dc buffer	-	16 V at dc	-	-	

IV. MEASURED RESULTS

A. Active Electrode ASIC

The ASIC was designed in 0.35- μ m CMOS HV process technology and operates from ± 9 V power supplies. The chip micrograph is shown in Fig. 9 with the various blocks labeled. The total area is 3.1 mm \times 1.25 mm. For electrical performance evaluation, eight chip samples were tested.

The average gain of the sensor buffer B2 is 0.99 V/V at dc and the average gain of the main buffer B1 is 0.98 V/V up to 750 kHz. At 500 kHz it has a phase delay of 2°. Its output swing reaches 14 V_{p-p} at 500 kHz with an average total harmonic distortion (THD) of 59 dB. It has an input-referred noise voltage of 22 μ V_{rms} measured from 20 kHz to 1 MHz. The transconductance of the current driver (Gm_{CD}) was measured at 500 kHz with a load of 50 Ω to eliminate the effect of parasitic capacitance. The output current was measured from 200 μ A to 6 mA and the transconductance was calculated by $Gm_{CD} = V_{load}/(V_{in} \times 50 \Omega)$ where V_{load} is the voltage across the load. As shown in Fig. 10, the average transconductance is 1.99 mA/V with a standard deviation of 10.3 μ A/V. The current driver has a THD of 55 dB at the maximum output current of 6 mA_{p-p} and a phase delay of 4° at 500 kHz.

When measuring the output impedance Z_{out} , any parasitic capacitance in parallel with Z_{out} should be excluded. The measurement method used to obtain Z_{out} is shown in Fig. 11. The current driver is driving two different loads which can be toggled using a switch S_L . Initially, it drives $R_1 = 50 \Omega$ to minimize the effect of the parasitic capacitance C_{stray} so the output current can be accurately set to $I = 1$ mA_{p-p} and the initial phase delay θ_{R1} due to the current driver can be measured between V_i and V_o . Then S_L opens and the current driver connects to $R_2 = 5.1k + 50 \Omega$. As R_2 is significantly

larger, the output current I splits into I_Z , I_C and I_o that flow into Z_{out} , C_{stray} and R_2 , respectively. As a result, a new phase delay θ_{R2} and voltage V_{R2} can be recorded and the output impedance of the current driver can be calculated using the following equations:

$$Z = \frac{V_{R2}}{1 \text{ mA}} \text{ and } \theta_C = \theta_{R2} - \theta_{R1} \quad (8a)$$

$$R_X = \sqrt{Z^2 + Z^2 \times \tan^2(\theta_C)} \quad (8b)$$

$$Z_{out} = \frac{(R_X \cdot R_2)}{R_2 - R_X} \quad (8c)$$

where Z combines R_2 , Z_{out} and C_{stray} in parallel, and θ_C is the phase delay due to C_{stray} only. Using (8b) the capacitance C_{stray} can be excluded giving R_X (which is simply R_2 and Z_{out} in parallel) and using (8c) finally Z_{out} is calculated.

Fig. 12 shows Z_{out} measured from 250 kHz to 1 MHz; it is on average >1 M Ω at the targeted 500 kHz bandwidth. The error bars in Fig. 12 indicate the spread at a specific frequency. This spread occurs because the measurement has a very sensitive accuracy.

Table I summarizes the measured performance of the ASIC.

B. Multi-Parameter Sensors

As proof of concept, four different types of sensor were integrated onto the belt with small FPCs to provide additional parameters while EIT is taking place. A NTC based temperature sensor and a Honeywell HIH4000-001 humidity sensor were embedded to monitor the environmental temperature and humidity (useful when an infant is lying in an incubator cot in the intensive care unit of a hospital). Accelerometer sensors were included for belt orientation monitoring and patient boundary shape tracking. These two parameters can provide additional information to aid the

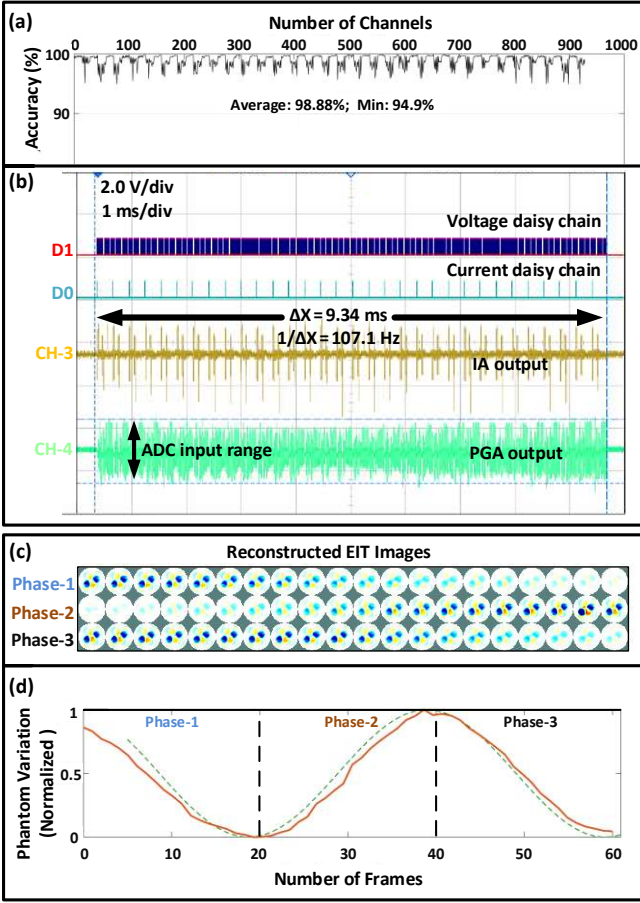


Fig. 13. (a) System calibration results; (b) image frame rate capture on the oscilloscope; (c) resistive-mesh phantom test results in form of EIT images; (d) impedance variation plotted using data from resistive-mesh phantom test compared to the idea variation.

selection of EIT models for enhanced image reconstruction [28], [29].

C. System in-Vitro Test

For EIT operation, the system was first calibrated by connecting the odd and even number electrodes to each end of a single load, providing 928 voltages (excluding the injecting pair) after a typical EIT scan. After calibration, the system gave a measurement accuracy of 98.88% between all 928 EIT reading combinations as shown in Fig. 13(a). It was then connected to a resistive-mesh phantom for EIT imaging. This phantom modified from the First Gottingen phantom [30], has two diagonal inner resistive elements that are made variable from 36.5Ω to 53.6Ω . Shown in Fig. 13(b) is the oscilloscope signal waveform captured in one EIT frame. The D0 signal is the current drive daisy chain trigger signal CLK_I, and there are 32 signals indicating 32 current drive positions in one complete EIT frame. Between two current daisy chain signals, as shown by D1, 16 voltage-sense daisy chain triggers CLK_V are captured so that 16 differential voltages are measured per channel within one current drive position. Also in Fig. 13(b),

oscilloscope channel 3 shows the differential voltage signal at the output of the IA in the first data acquisition channel, and oscilloscope channel 4 shows the dynamic gain feature in the same data acquisition channels. The PGA equalizes all the voltage signals after the IA to a level close to the maximum ADC input range before digitization to improve the SNR. The wideband active electrode ASIC and the two parallel data acquisition channels in the central hub, allow one EIT frame to be completed in 9.32 ms or 107 fps.

As shown in the waveforms in Fig. 13(d), the variable resistive element changes its impedance in a sinewave fashion shown in dotted green. The system captures 20 frames of data in a single phase. In Fig. 13(c) the EIT image was reconstructed using EIDORS [31]. The two dark blue circle areas indicate the location of the variable element. As the two elements change their resistive values from maximum to minimum, for example, in phase-1, the images tend towards all-white and vice-versa. Visually some sequential images seem identical but the average impedance value indicator which is plotted in solid-red in Fig. 13(d) shows that changes in impedance value within the SUT are detected in each image frame. Overall, the system can detect 0.86Ω change per frame.

D. Wearable Belt Design

In the reported active EIT belts [20], [22] the electronics are permanently connected; autoclaving will damage the electronic components and the whole belt must be disposed of after use. The proposed belt is a combination of a FPC electronic core and a separate textile belt dressing. Only the low-cost textile dressing is disposed of after use. This significantly reduces the cost per patient from hundreds of dollars to a few dollars. Fig. 14 shows the detailed belt layer-stacking diagram in 3D. Each FPC unit contains eight active electrode PCBs and an active belt consists of four units, joined by FPC-to-FPC connectors. This provides a 32-electrode EIT system. The $8 \text{ mm} \times 30 \text{ mm}$ electrode-pads are on the bottom layer of the FPC to facilitate connection between the active electrode ASIC and the skin-contact electrode via the textile dressing. As only bus-lines are running on the FPC, this design allows easy adjustment of the overall length of the belt for future neonate applications. The disposable textile dressing consists of a white textile substrate with silver-coated (dry) fabric-electrode stripes evenly distributed across it. Each stripe wraps all the way around the substrate and when the FPC is placed on the top of the dressing, the electrode-pad on the bottom layer of the FPC contacts the fabric-electrode, which will then contact the skin. This arrangement results in skin contact only a few millimeters away from the electronics with an electrode impedance of less than 1Ω from 50 kHz to 1 MHz. With the help of Velcro folding strips, the FPC electronic-core is held firmly inside the fabric dressing. The device is secured on the sternum by means of an elastic fastening.

E. System in-Vivo Test

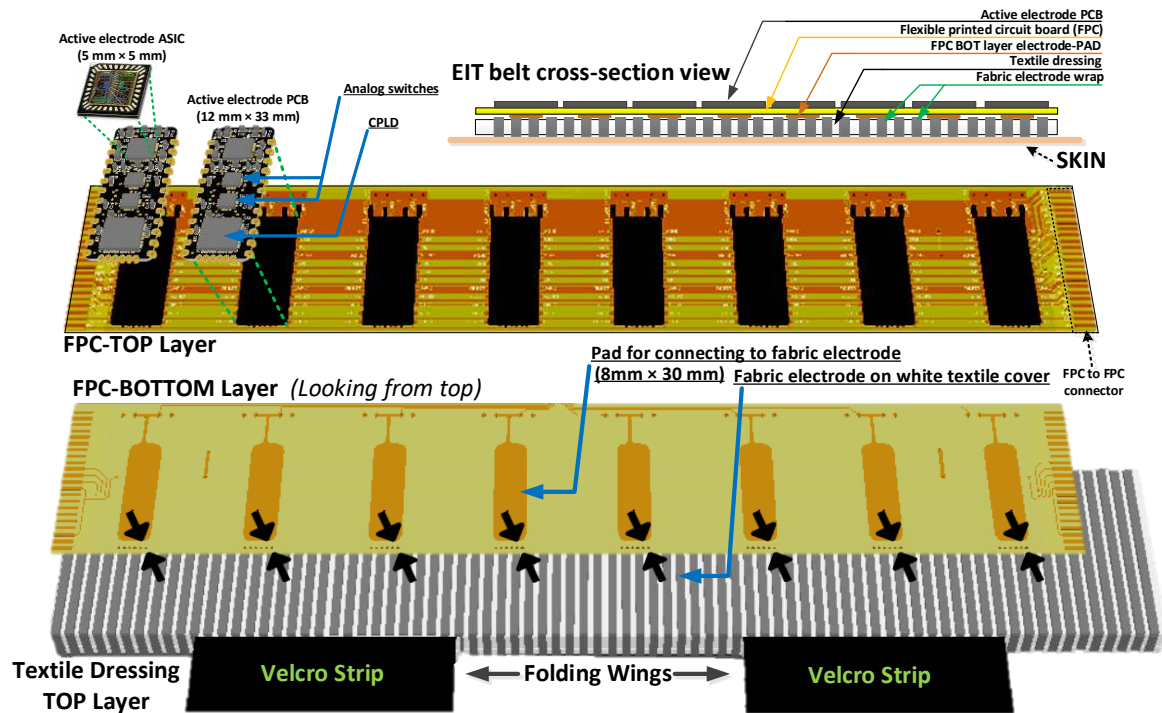


Fig. 14. Detailed active EIT belt layer-stacking and cross-section view.

The belt was covered with the textile dressing and worn by a volunteer. The volunteer's lung respiration cycle was captured; see Fig. 15(a). Fig. 15(b) shows the ECG signal recorded for 30 s, switching between three different locations by selecting different pairs of active electrodes.

F. Comparison

Table II compares wearable EIT systems for lung function monitoring. The system reported in this paper has advantages, not only in terms of electronic design specification, but also in providing more functions for clinical applications.

V. CONCLUSION

A multi-functional adult wearable EIT system based on high performance active electrode ASICs has been developed, the functions of which will form the basis of a neonatal design. The 32-electrode system features an innovative belt dressing. It can provide EIT images at 107 fps with the ability to configure EIT in any scan pattern. Tested on a custom-made resistive phantom, the system has an accuracy of 98.8% and a detectability of at least $0.86 \Omega/\text{frame}$. With the replaceable textile dressing, it has been tested on a human volunteer and the lung respiration has been successfully imaged. The system is also capable of recording heart rate signals as well as providing other measurement parameters such as environmental temperature and humidity. The accelerometer sensors integrated on the belt [32] offer the possibility of tracking the individual patient's thorax shape and laying position to aid in EIT model selection.

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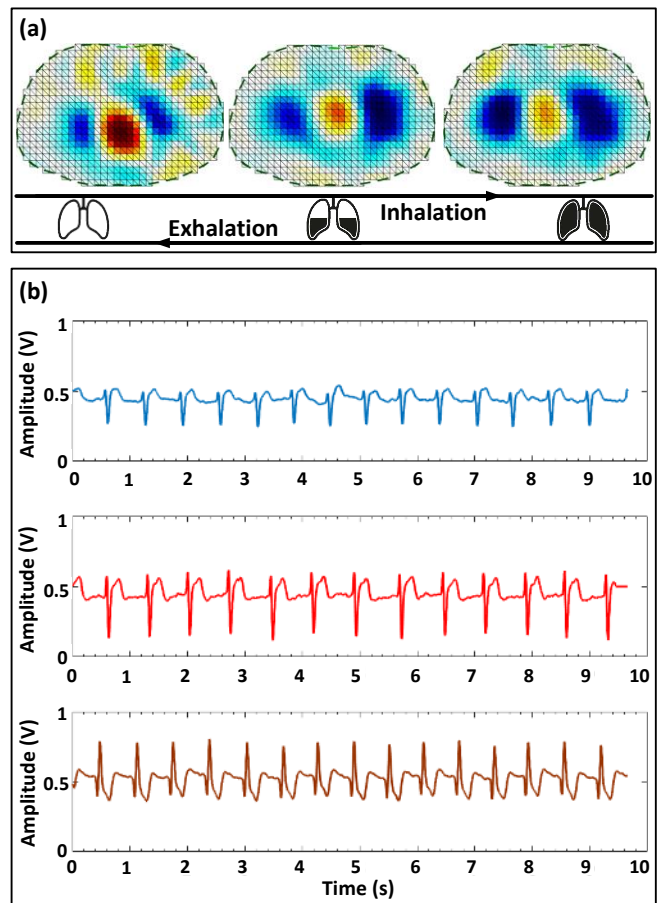



Fig. 15. EIT in-vivo test with the belt worn by a volunteer. (a) The exhalation and inhalation lung images. (b) ECG signals captured in 30 s switching between three different locations using the EIT system.

TABLE II. COMPARISON WITH OTHER WORK

Wearable EIT system for lung function monitoring	Dräger [21]	Swisstom [22]	KAIST [20]	This Work
				
Number of electrodes	16 electrodes + 1 reference	32 electrodes	32 electrodes	32 electrodes
Active electrodes	No	Yes	No (Electronics on belt)	Yes
Active electrode configuration	N/A	Voltage sense	N/A	Voltage sense and current drive
EIT scan pattern	Adjacent	N/A	Adjacent	Fully programmable
Frequency	80 – 130 kHz	150 kHz	10 – 200 kHz	50 – 500 kHz
Current amplitude	90% of I_{max}^1	50% of I_{max}^1	0.1 – 1 mA _{p-p}	≤ 6 mA _{p-p}
Frame rate	≤ 30 fps	50 fps	≤ 20 fps	107 fps
Heart rate	No	No	No	Yes
Belt orientation	No	Yes	No	Yes
Torso shape	No	No	No	Yes
Environmental sensors	No	No	No	Yes

¹ Maximum patient auxiliary current conforming to IEC 60601-1.

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