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A High-Gain and Low-Noise 0.9 µW Operational Amplifier

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Abstract A low-voltage, low-power, high-gain and low-noise operational transconductance amplifier (OTA) by modifying conventional one is presented and analyzed. Design strategies are discussed for minimizing noise and increasing gain. The simulation results show that the open loop gain is improved from 68 dB to 74 dB and the input referred noise is also reduced from 926 $nV/\sqrt{Hz}$ to 475 $nV/\sqrt{Hz}$. This amplifier operates at 0.8 V power supply voltage with a power consumption of 0.9 µW. All the simulations are obtained by using Hspice tool with 0.18 µm CMOS TSMC parameters.

Keywords Transdonductance Amplifier, High Gain Op-Amp, Low Noise, Low Voltage, Low Power

1. Introduction

In recent years, much effort has been put into the reduction of supply voltage and the supply power of mixed signal CMOS systems [1]. Three main reasons can be given for the advent of low-voltage circuits [2]. As a first reason, since the channel length is scaled down into submicron and gate-oxide thickness is decreased dramatically, in order to ensure the device reliability, the supply voltage has to be reduced. As a second reason, because of increasing number of components implanted on a single chip, the power per electronic function is increased. Since a silicon chip can only dissipate a limited power per unit area, the power consumption has to be lowered. The third reason is dictated by portable and battery-powered equipment. The supply power and the supply voltage have to be reduced to have an acceptable operation period from a battery.

The low noise operational amplifier is one of the most essential parts of analog circuits. In MOSFET devices, there are two important noise sources, which are flicker noise (below 1MHz) and thermal noise [3], [4]. Designing a high dc gain and low noise CMOS OTA with a low supply voltage is very complicated. In this paper by using a simple modification the gain and noise of conventional OTA are improved with the constant power consumption.

The proposed OTA is described in section 2. In section 3 a design procedure is presented. In section 4 proposed circuit has been simulated using the models of the TSMC 0.18 µm technology and a comparison of proposed OTA with conventional one and other configurations is summarized. The paper is concluded in section 5.

2. Proposed OTA

Circuit schematic of proposed OTA is shown in Fig. 1A, which is indeed a modified version of a conventional OTA shown in Fig. 1B. In this circuit the input signal is applied to transistors M1 to M4. Thus transistors M3 and M4 are not used as an active load anymore. Transistors M7 to M10 are used to improve gain and output signal swing.

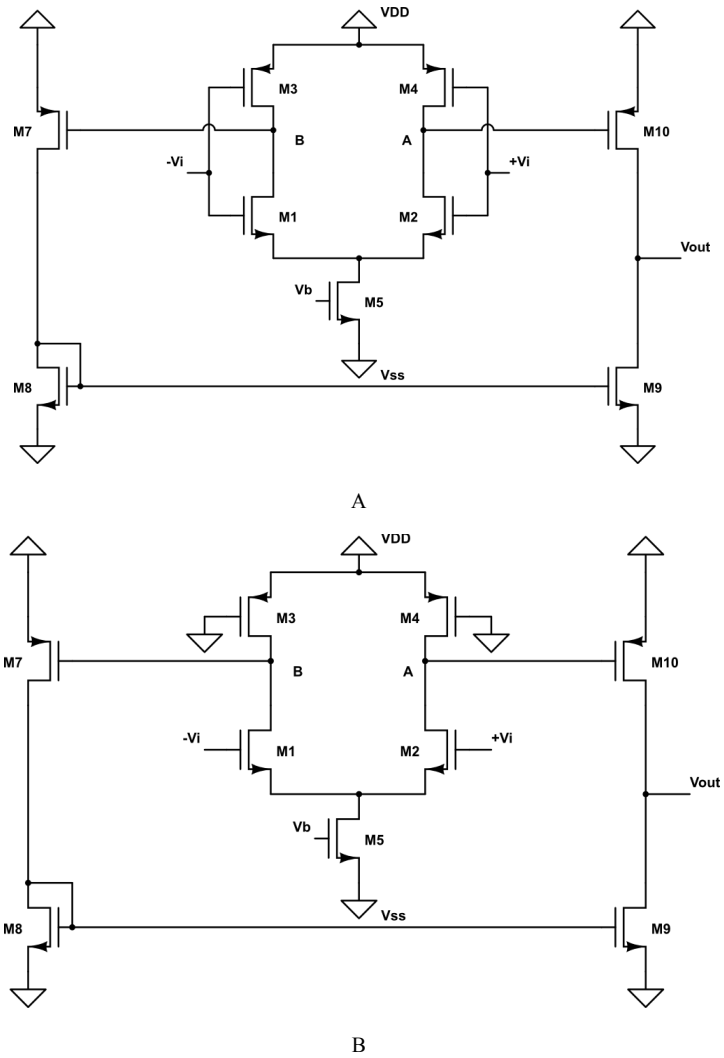


Figure 1. (A) Proposed OTA. (B) Conventional OTA.

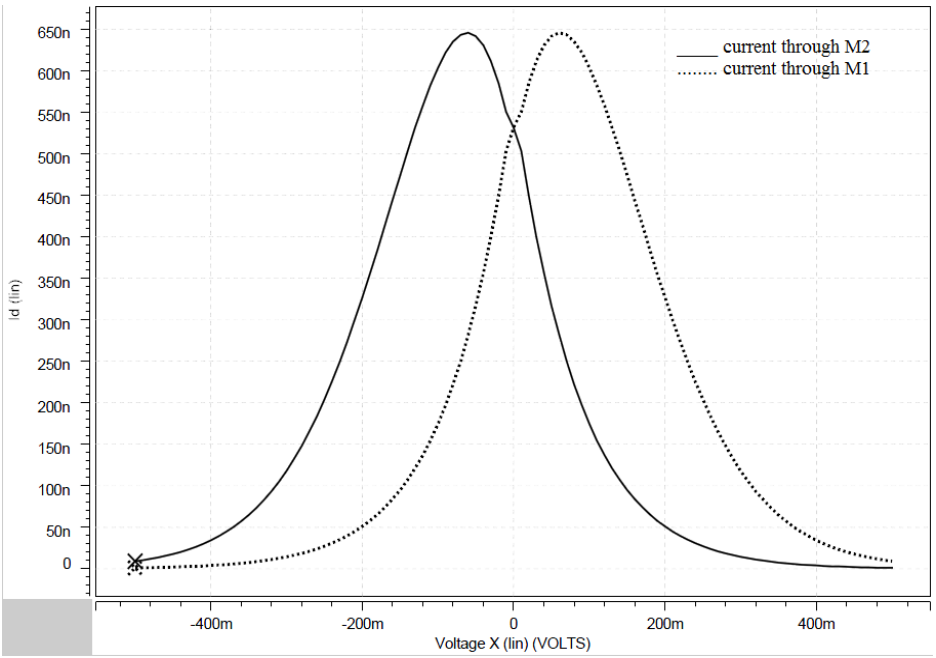


Figure 2. Current variations vs. input differential voltage v_{i2}-v_{i1}.

Fig. 2 shows the current variations versus input differential voltage v_{i2}-v_{i1}. It can be observed that the circuit works as a differential amplifier in part of the input signal.

Voltage gain of the proposed OTA is given by:

$$A_{Vd} = g_{m10}(g_{m2} + g_{m4})(r_{o2} \| r_{o4})(r_{o10} \| r_{o9}) \quad (1)$$

It is almost two times larger than the open-loop gain of conventional OTA with the same power consumption which is equal to:

$$A_{Vd} = g_{m10} g_{m2}(r_{o2} \| r_{o4})(r_{o10} \| r_{o9}) \quad (2)$$

The noise contribution of the second stage of the opamp is negligible, because it is divided by the gain of the previous stage when referred to the input [5]. Also noise contribution of current source is negligible. Thus thermal noise per unit bandwidth [6] produced by transistors is almost given by:

$$\overline{V_n^2}\,|_{M1-4} = 2 \times 4kT\gamma \times \frac{1}{g_{m1} + g_{m3}} \quad (3)$$

$$\overline{V_n^2}\,|_{M7-8} = 4kT\gamma \times \frac{g_{m7} + g_{m8}}{(g_{m1} + g_{m3})^2 g_{m7}^2 (r_{o1} \| r_{o3})^2} \quad (4)$$

$$\overline{V_n^2}\,|_{M9-10} = 4kT\gamma \times \frac{g_{m9} + g_{m10}}{(g_{m1} + g_{m3})^2 g_{m10}^2 (r_{o1} \| r_{o3})^2} \quad (5)$$

Thus input-referred thermal noise Power Spectral Density (PSD) of the proposed OTA and conventional OTA can be written as:

$$\overline{V_{thermal}^2} = \frac{8kT\gamma}{(g_{m1} + g_{m3})}\left(1 + \frac{g_{m9} + g_{m10}}{(g_{m1} + g_{m3})\, g_{m10}^2 (r_{o1} \| r_{o3})^2}\right)$$

Proposed OTA (6)

$$\overline{V_{thermal}^2} = 8kT\gamma\left(\frac{1}{g_{m1}} + \frac{g_{m3}}{g_{m1}^2} + \frac{g_{m9} + g_{m10}}{g_{m1}^2 g_{m10}^2 (r_{o1} \| r_{o3})^2}\right)$$

Conventional OTA (7)

Where k is the Boltzmann's constant, T is the temperature in kelvin. The coefficient γ is equal to 2/3 for long channel transistors and it needs to be replaced by a larger value for submicron MOSFETs. It also varies to some extent with the drain- source voltage [3].

Input-referred flicker noise PSD of the proposed OTA and conventional OTA can be shown as (8) and (9) respectively, where C_{OX} is capacitance per unit area of the gate oxide, K_{fN} is NMOS flicker noise coefficient and K_{fP} is PMOS flicker noise coefficient. It can be observed that total input-referred noise in proposed OTA is much smaller than conventional one.

In this work all transistors are biased in weak inversion to have large g_m in addition of low power consumption. Since opamps are usually designed to be operated with negative-feedback connection, frequency compensation is necessary for closed-loop stability. The frequency compensation of proposed OTA is easily achieved like the conventional one [7].

The main drawback of this OTA is its limited input signal caused by transistors M3 and M4, which is equal to:

$$V_{SS} + V_{DS_{sat}} + V_{GS_2} \le V_i \le V_{DD} - V_{SG_4} \quad (10)$$

Input signal swing is one threshold voltage smaller than conventional OTA, that is because of transistors M3 and M4.

Note that if the output signal is taken from nodes A or B, for ideal current source M5, CMRR is given by:

$$\overline{V_{flicker}^2} = \frac{2}{C_{OX} f (g_{m1} + g_{m3})^2}\left[\frac{\frac{K_{fN}}{(WL)_9} g_{m9}^2 + \frac{K_{fP}}{(WL)_{10}} g_{m10}^2}{g_{m10}^2 (r_{o2} \| r_{o4})^2} + \frac{K_{fP}}{(WL)_3} g_{m3}^2 + \frac{K_{fN}}{(WL)_1} g_{m1}^2\right]$$

Proposed OTA (8)

$$\overline{V_{flicker}^2} = \frac{2}{C_{OX} f}\left[\frac{\frac{K_{fN}}{(WL)_9} g_{m9}^2 + \frac{K_{fP}}{(WL)_{10}} g_{m10}^2}{g_{m1}^2 g_{m10}^2 (r_{o2} \| r_{o4})^2} + \frac{K_{fP}}{(WL)_3}\frac{g_{m3}^2}{g_{m1}^2} + \frac{K_{fN}}{(WL)_1}\right]$$

Conventional OTA (9)

$$CMRR = \frac{(g_{m2} + g_{m4}) r_{o2}}{2 g_{m4}(r_{o4} + r_{o2})} \quad (11)$$

For $r_{o2} = r_{o4}$ it is approximated by:

$$CMRR = \frac{g_{m2} + g_{m4}}{4 g_{m4}} \quad (12)$$

It is lower than CMRR of conventional OTA.

3. Design Procedure

For $g_{m9}=g_{m10}$ and $g_{m1}=g_{m2}=g_{m3}=g_{m4}$ noise spectral density can be written as:

$$S_n(f) = \frac{8KT}{3g_{m1}^2 g_{m10}(r_{o1} \| r_{o3})2} \tag{13}$$

Gain-Bandwidth product is almost equal to:

$$GB = \frac{4g_{m1}g_{m10}(r_{o1} \| r_{o3})}{C_L} \tag{14}$$

DC gain is also given by:

$$A_0 = 4g_{m1}g_{m10}(r_{o1} \| r_{o3})^2 \tag{15}$$

From (13) and (14) we obtain

$$r_{o1} \| r_{o3} = \frac{A_0}{GB \times C_L} \tag{16}$$

Substitute g_{m10} from (14) and the above equation into (13) yields:

$$g_{m1} = \frac{32KT}{3S_n(f)A_0} \tag{17}$$

$$g_{m10} = \frac{3(GB \times C_L)^2 S_n(f)}{128KT} \tag{18}$$

Since transistors are operating in subthreshold region, we have:

$$g_m = \frac{I_D}{NV_T} \tag{19}$$

$$I_C = \frac{I_D}{I_0(W/L)} \tag{20}$$

Where N is subthreshold coefficient, V_T, thermal voltage, I_C, inversion coefficient (which shows the operation region of transistor, for $I_C>1$ in strong inversion, for $0.1< I_C<1$ in moderate inversion, for $I_C<1$ in weak inversion), I_0, normalized current in subthreshold region (which is equal to $2N\mu C_{ox}V_T^2$).

From (17), (18), (19) and (20) we obtain:

$$(\frac{W}{L})_{1-4} = \frac{NV_T}{I_C I_0} g_{m1} \tag{21}$$

$$(\frac{W}{L})_{7,10} = \frac{NV_T}{I_C I_0} g_{10} \tag{22}$$

4. Simulation Results

The proposed OTA was simulated with the supply voltage of V_{DD} = 0.35 V and V_{SS} = - 0.45 V. For the simulations, 0.18 µm CMOS technology parameters were used. The biasing current source was 1 µA. All the devices used have 0.5 µm length (three times the lowest value for the employed topology). The inversion coefficient of transistors is $I_{C1,2}$ = 0.103 and $I_{C3,4}$ = 0.256, thus these transistors are in moderate inversion. Table 1 summarizes widths of the transistors used in the proposed circuit. Table 2 summarizes specifications of the circuit resulted from simulations and compares them with the conventional OTA and other configurations.

Table 1. Width for the transistors used in the proposed OTA

MOS	W(µm)
M1,M2	15
M3,M4	28
M5	1
M7,M10	2
M8,M9	0.3

Bode plot of the OTA is shown in Fig. 3. It can be observed that, since the DC gain is increased and bandwidth is constant, the unity gain-bandwidth product is larger than conventional OTA, however, phase margin is decreased.

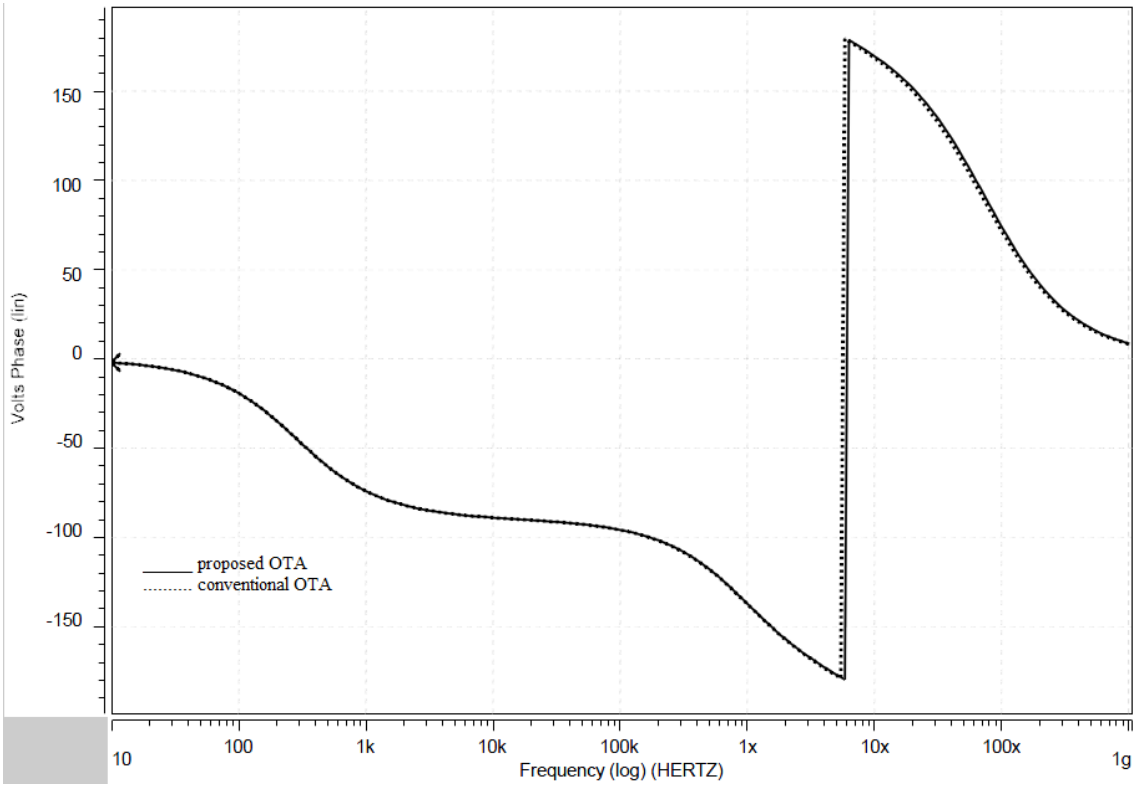
Fig. 4 shows the transient characteristic of the proposed structure with a capacitor load of 10 pF when a square signal of 0.6 V_{PP} at 2 MHz is applied at the input of unity-gain configuration of OTA. The slew rate is 0.8 V/µs which is equal to slew rate of conventional OTA.

Fig. 5 shows the equivalent input referred noise, it can be observed that the input referred noise is significantly lower than conventional OTA. Fig. 6 shows the total output noise voltage which is obvious that the proposed OTA has better performance than conventional one. Fig. 7 shows the measured response for a 100 Hz, 20 µV peak-to-peak sinusoidal input voltage. The measured THD was -44 dB.

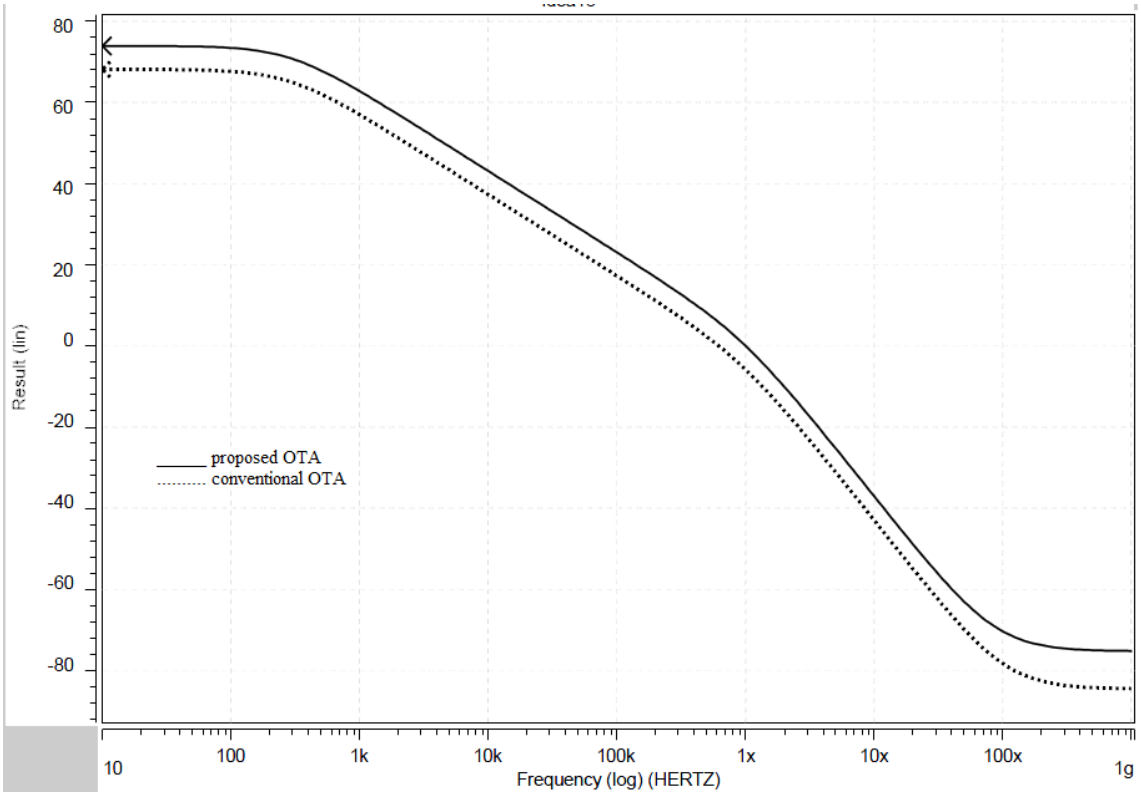
Fig. 8 shows the voltage of nodes A and B for proposed and conventional OTA. It can be observed that the slope of the curve (i.e., the voltage gain) in the proposed OTA is larger than conventional OTA.

Table 2. Simulation results summary

	Proposed OTA	Conventional OTA	[8]	[9]	[10]	[11]
Voltage Supply	0.8V	0.8V	0.8V	0.5V	0.8V	0.8V
Technology (CMOS)	0.18 µm	0.18 µm	0.18 µm	0.18 µm	0.18 µm	0.35 µm
DC Gain	74dB	68dB	51dB	55dB	68dB	66dB
UGBW	1MHz C_L=10pF	0.61MHz C_L=10pF	40 kHz C_L=10pF	8.72 MHz C_L=10pF	8.12 MHz C_L=1 pF	3.4 MHz C_L=5 pF
Phase Margin	42º	56º	65º	89º	89º	80º
Slew Rate C_L=10pF f=2MHz	0.8 V/µs	0.9 V/µs	0.12 V/µs	1.35 V/µs	2.89 V/µs	4.7 V/µs
FOM= (C_L*Slew Rate) /Power	8.3 pF.V/µs.µW	10 pF.V/µs.µW	2.34 pF.V/µs.µW	0.18 pF.V/µs.µW	0.03 pF.V/µs.µW	0.12 pF.V/µs.µW
Power Consumption	0.9µW	0.9µW	1 µW	77 µW	94 µW	194 µW
Gain/Power Consumption	82.2 dB/µW	75.5 dB/µW	50.8 dB/µW	0.71 dB/µW	0.72 dB/µW	0.34 dB/µW
Input referred noise @215Hz	$475\ nV/\sqrt{Hz}$	$926\ nV/\sqrt{Hz}$	-	-	-	-
BW	285Hz	285Hz	-	-	-	-
CMRR	33dB	50dB	-	-	-	-



A



B

Figure 3. Frequency response of proposed OTA (continuous line) and conventional OTA (dotted line) (A) Phase. (B) Gain.

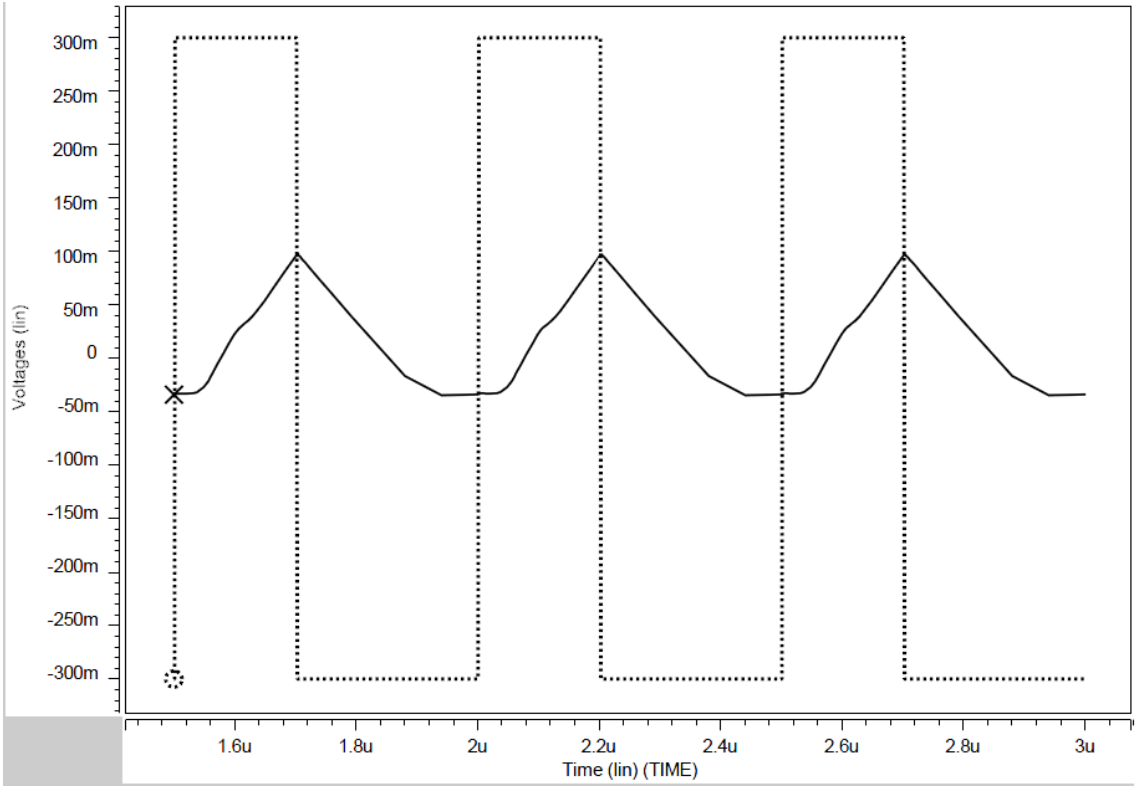


Figure 4. Output voltage of proposed OTA when performing a transient analysis using a $0.6V_{PP}$ square input signal 2MHz.

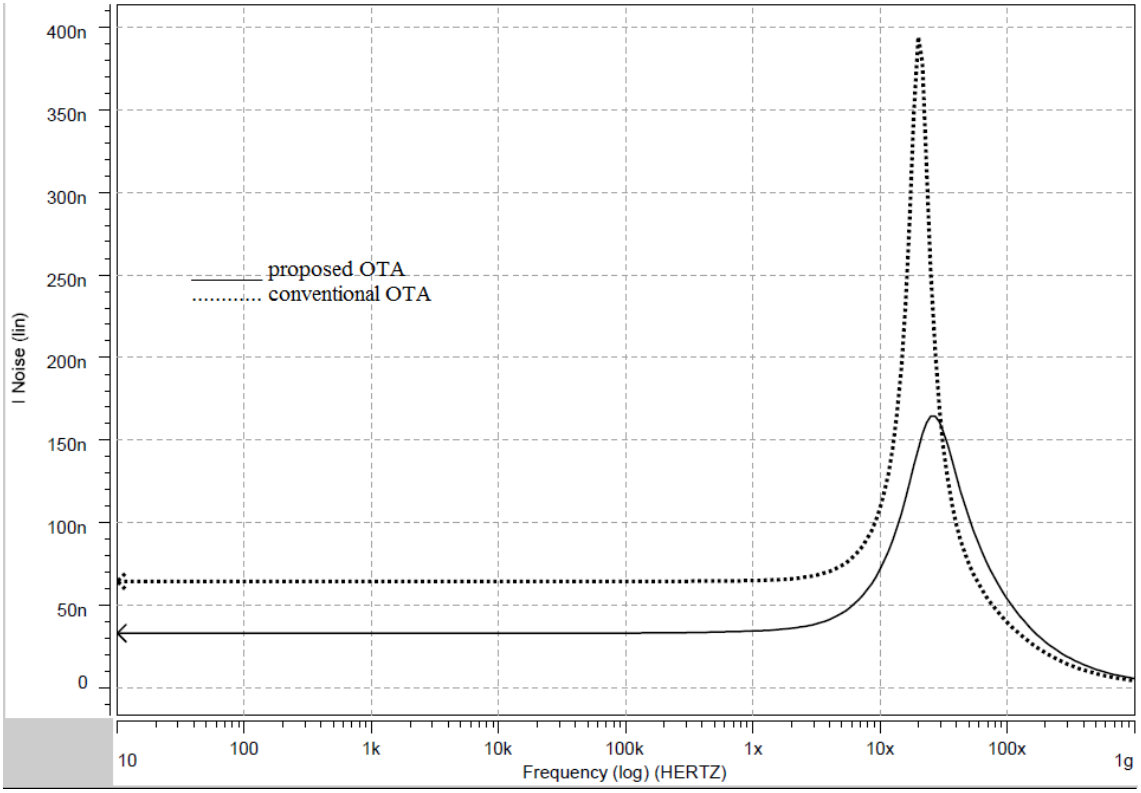


Figure 5. Equivalent input noise at V_{i2}.

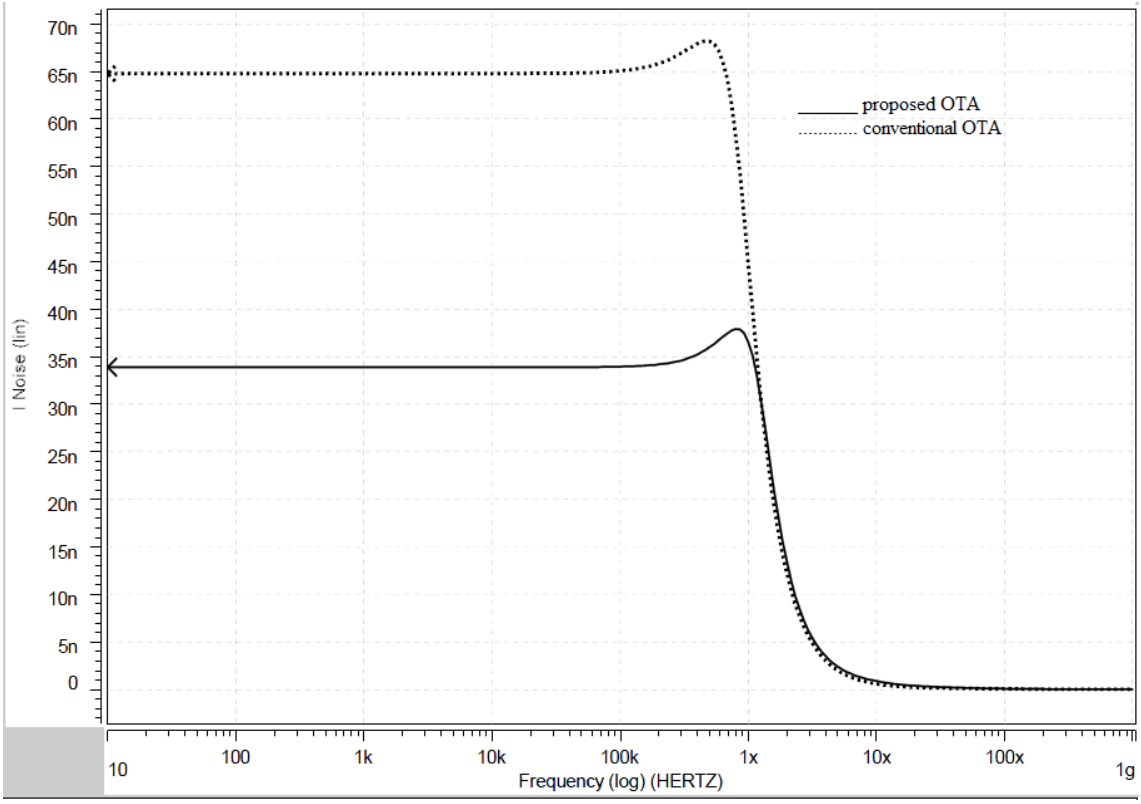


Figure 6. Total output noise voltage.

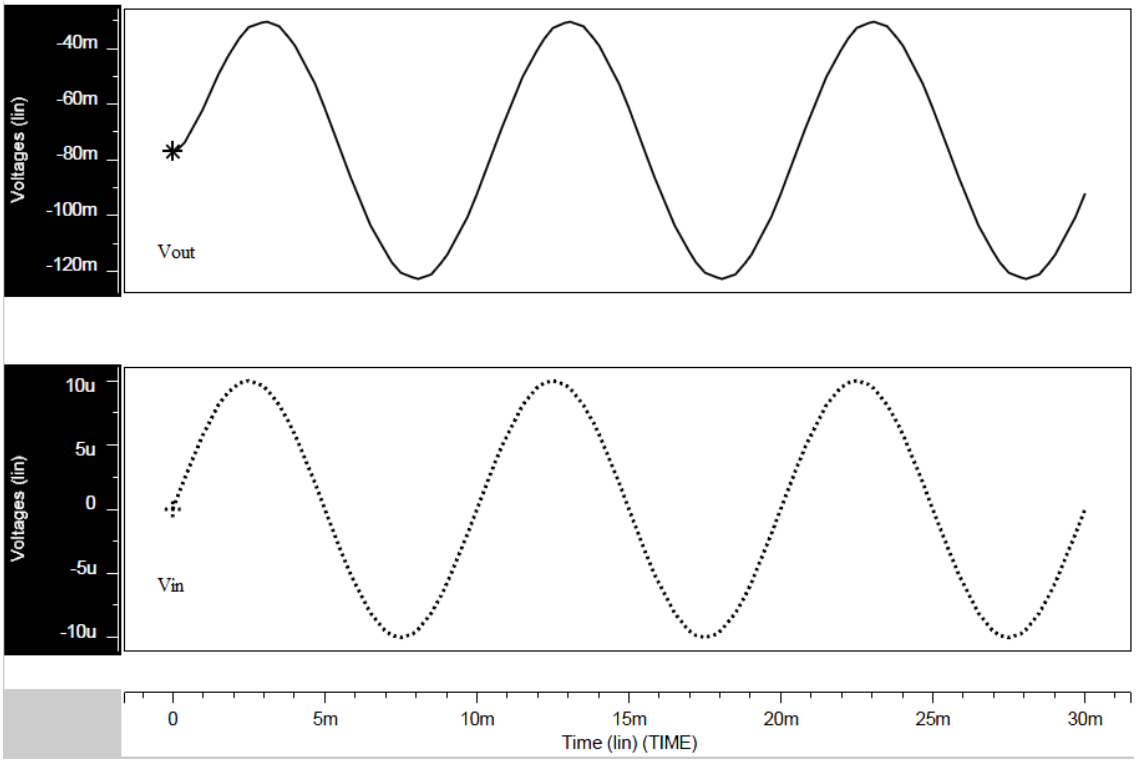
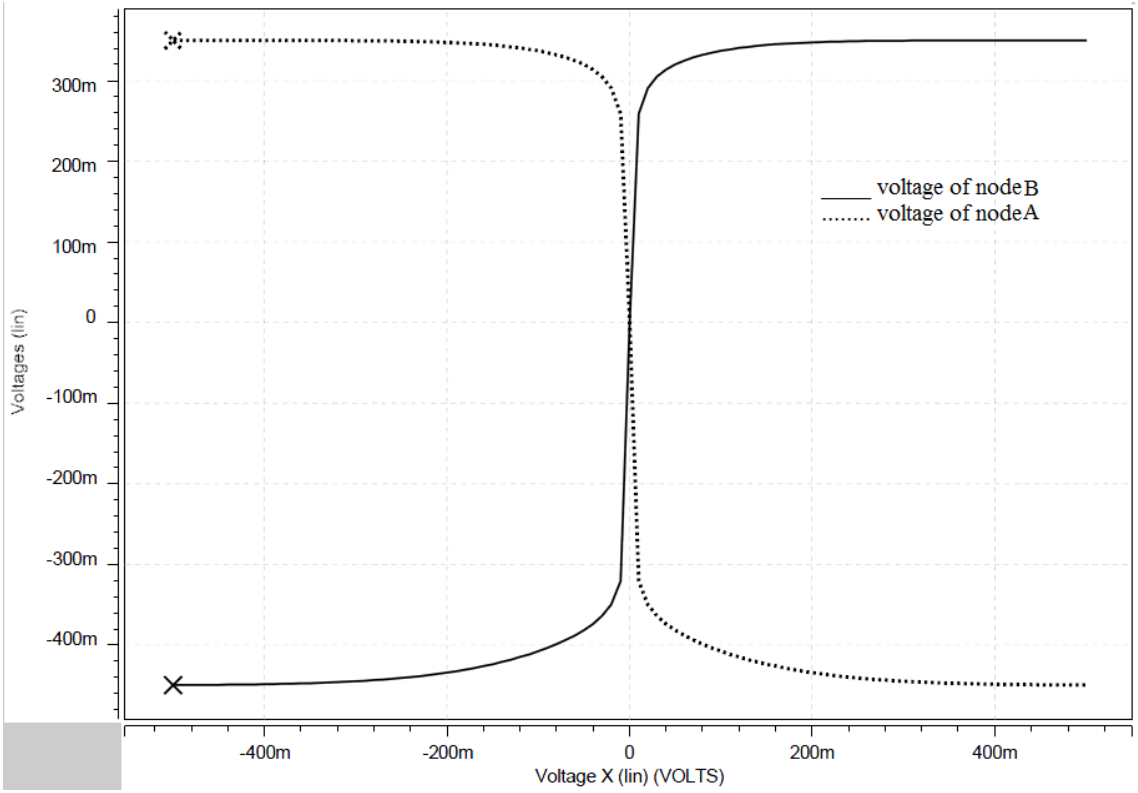
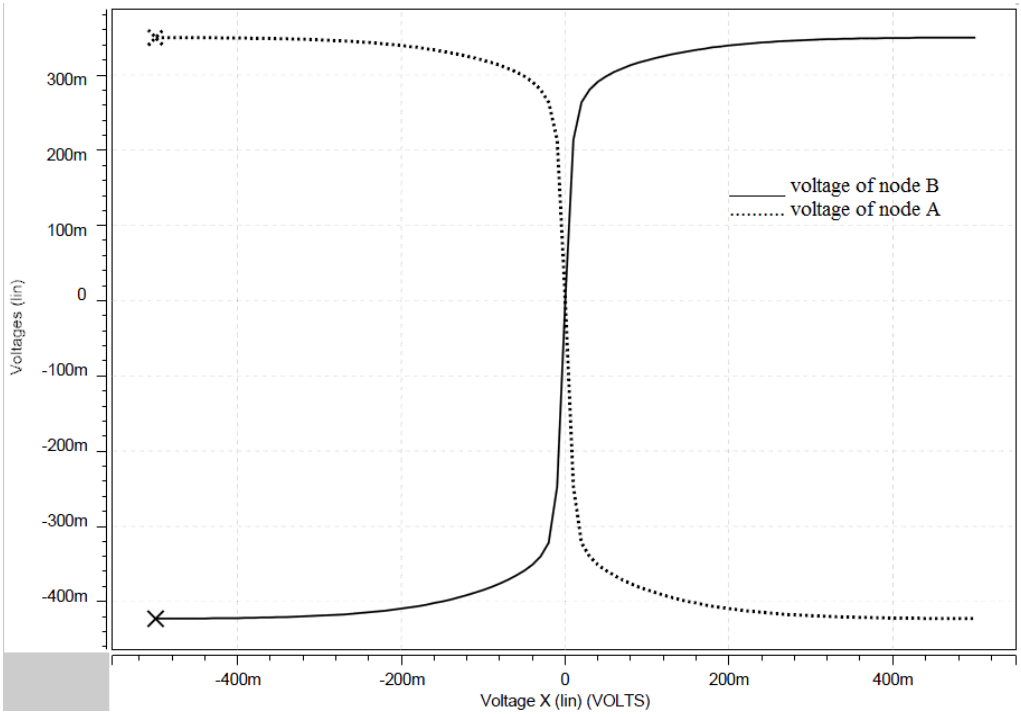


Figure 7. Output of the proposed OTA with 20µVPP sinusoidal input voltage.



A



B

Figure 8. Voltage of nodes A and B vs. differential input voltage V_{i2}-V_{i1}: (A) Proposed OTA. (B) Conventional OTA

5. Conclusion

A low-voltage and low-power OTA was proposed in this paper, which was modified version of conventional OTA. By using a simple modification, the voltage gain and noise performance were significantly improved, however the CMRR and input signal swing range in comparison to conventional OTA decreased. The simulation results showed that the DC gain is two times larger than conventional OTA and input referred noise is two times lower than conventional one.

To demonstrate the feasibility and scalability of the design a standard 0.18 µm CMOS process with very restrictive supply voltage of 0.8V has been used.

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