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# A High-Linearity and Low-EMI Multilevel Class-D Amplifier

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***Abstract*— This article presents a Class-D audio amplifier for automotive applications. Low electromagnetic interference (EMI) and, hence, smaller *LC* filter size are obtained by employing a fully differential multilevel output stage switching at 4.2 MHz. A modulation scheme with minimal switching activity at zero input reduces idle power, which is further assisted by a gate-charge reuse scheme. It also achieves high linearity due to the high loop gain realized by a third-order feedback loop with a bandwidth of 800 kHz. The prototype, fabricated in a 180-nm high-voltage BCD process, achieves a minimum THD+N of −107.8 dB/−102 dB and a peak efficiency of 91%/87% with 8- and 4-Ω loads, respectively, while drawing 7-mA quiescent current from a 14.4-V supply. The prototype meets the CISPR 25 Class 5 EMI standard with a 5.7-dB margin using an *LC* filter with a cutoff frequency of 580 kHz.**

***Index Terms*— Class-D amplifiers, electromagnetic interference (EMI), idle power, multilevel, pulsewidth modulation (PWM).**

## I. Introduction

THE development of automotive infotainment systems has driven the demand for high-performance and high-efficiency audio amplifiers. Class-D amplifiers are well suited for this application because their high power efficiency significantly simplifies their cooling requirements, thereby reducing system cost and size [1]–[4]. However, Class-D amplifiers generate electromagnetic interference (EMI), which originates from the high-frequency switching activities in the output stage, as shown in Fig. 1(a). This is then radiated by the long cable harness connecting the power supply, audio amplifiers, and speakers and, thus, can be problematic in automotive applications, which must comply with a strict EMI standard (e.g., CISPR 25 Class 5 [5]). To meet the stringent automotive EMI requirement, fully differential switching is preferred since it produces much less common-mode (CM) EMI, which can be a significant contributor to radiated emission [6], [7]. The residual EMI must then be suppressed by an *LC* filter at the output of the Class-D amplifier. Unfortunately, this significantly increases system cost and bulk.

Multiphase [6] and multilevel output stages [8]–[17] have been proposed to mitigate EMI. In multiphase output stages [see Fig. 1(b)] [6], several output stages drive separate inductors and switch at different moments. Therefore, the total high-frequency ripple current delivered to the load is reduced, which also reduces EMI. However, this increases the number of inductors required, as well as the idle power dissipation caused by the ripple currents circulating in the various output stages. As the number of audio channels increases, the total system cost and idle power dissipation increase proportionally. Multilevel output stages [see Fig. 1(c)] reduce EMI by reducing the switching step size. In [8]–[13], this is achieved by using multiple supply voltages, which often increases system cost. Alternatively, this can be done by using (relatively low-cost) external flying capacitors to generate an intermediate output level equal to a fraction (usually 1/2) of the supply [14], [15]. However, the extra control circuitry is required to fix the voltage across these capacitors at half of the supply, thus increasing design complexity. In [16], an extra output level is created by simply shorting the load, but it requires zero dead time for proper operation, resulting in a complicated gate-driving configuration. In [17], independent control of the back-to-back transistors shorting the load is proposed, which obviates zero dead time. However, in both cases, extra circuitry and, thus, idle power are required to robustly define the output CM.

Another way to meet the EMI challenge is by tailoring it to the requirements of the CISPR 25 EMI mask. Class-D amplifiers employing fixed-frequency pulsewidth modulation (PWM) [1] or a hybrid of PWM and $\Delta\Sigma$ modulation [2] can effectively reduce the *LC* filter size by switching at frequencies above 1.8 MHz where the EMI requirements are relaxed. However, this results in increased switching loss and, hence, higher idle power. On the other hand, Class-D amplifiers employing $\Delta\Sigma$ modulation [also known as pulse density modulation (PDM)] [13], [17]–[19] can reduce EMI peaks by spreading the switching energy, which is useful in consumer applications. However, even with sampling frequencies of several MHz, their out-of-band quantization noise still falls within the AM band, thus requiring a bulky *LC* filter to satisfy CISPR 25.

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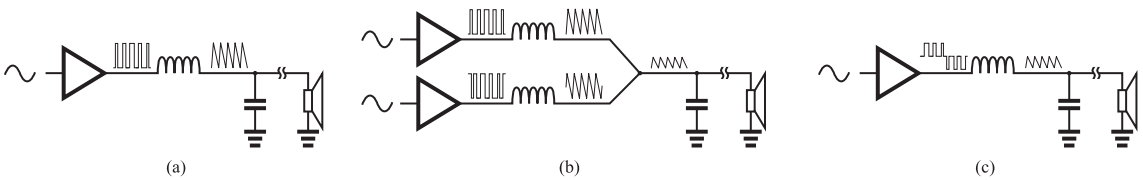


Fig. 1. Switching activity in (a) conventional, (b) multiphase, and (c) multilevel Class-D amplifiers.

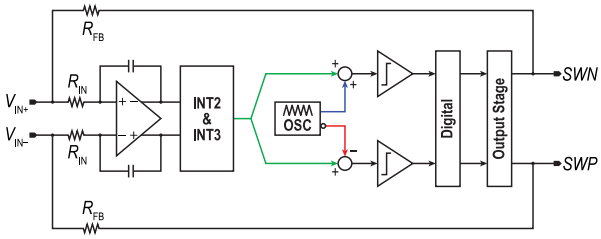


Fig. 2. System-level block diagram of the presented Class-D amplifier.

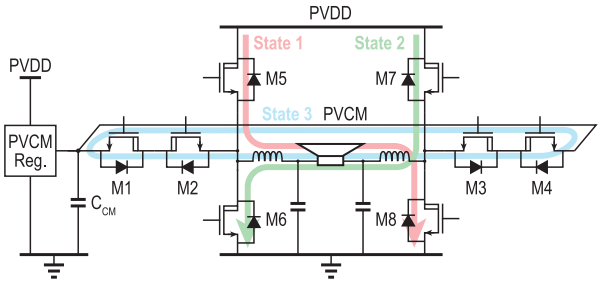


Fig. 3. Circuit topology of the proposed multilevel output stage.

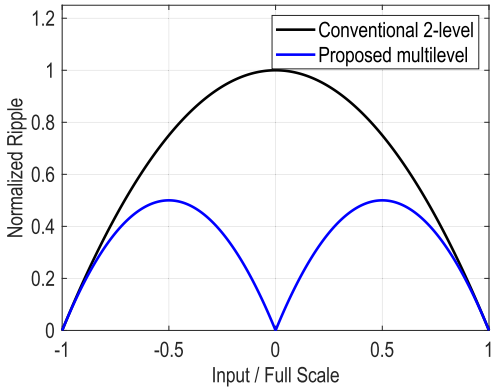


Fig. 4. Normalized peak-to-peak output ripple as a function of average output voltage for the proposed multilevel and conventional two-level output stages.

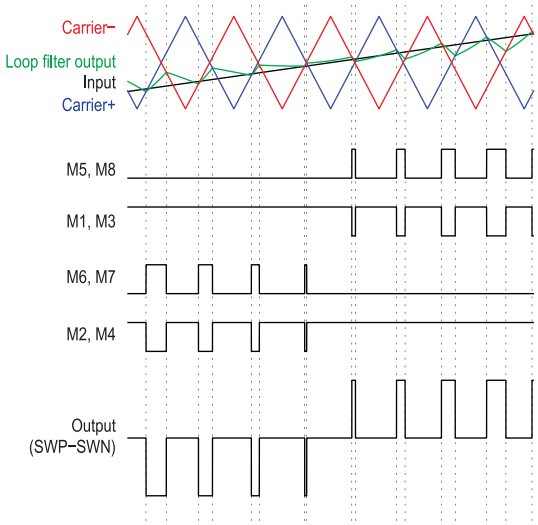


Fig. 5. Proposed modulation scheme, the resulting ON/OFF states of the output transistors, and differential output voltage.

This article extends on [20] and presents a multilevel Class-D amplifier that employs fixed-frequency PWM. Its system-level block diagram is shown in Fig. 2. It features a low-EMI fully differential multilevel output stage with lower cost and complexity compared with [14] and [16]. Compared with [17], the use of a closed-loop fixed-frequency PWM architecture significantly reduces EMI in the AM band and improves linearity in the presence of supply noise, timing errors, and near full-scale input signals. It also offers a well-defined constant output CM at the expense of two extra common-mode output transistors and an on-chip low-power linear regulator. Combined with a high switching frequency (4.2 MHz), the required *LC* filter cutoff frequency is significantly increased. The increased idle power due to the high switching frequency is mitigated by a modulation scheme that has minimal switching activity during idling and a gate-charge reuse technique. The output stage is placed in a third-order feedback loop, which provides a sufficient loop gain to achieve high linearity.

This article is organized as follows. Section II explains the proposed output stage architecture and modulation scheme. Section III describes the output stage's circuit implementation. Section IV details the design of the signal processing circuitry, including the loop filter and the pulsewidth modulator. Section V presents the measurement results, and Section VI summarizes and concludes this article.

## II. Proposed Multilevel Output Stage

### A. Topology

Fig. 3 shows the proposed fully differential multilevel output stage for a bridge-tied-load (BTL). Four CM output transistors (M1–M4) are added to the conventional H-bridge (M5–M8). A low-power linear regulator generates a voltage PVCM equal to half of PVDD. The output stage produces three differential output levels ($V_{OUTP} - V_{OUTN}$): +PVDD, −PVDD, and 0 in States 1, 2, and 3, respectively.

In State 1, M5, M8, M2, and M4 are turned on; in State 2, M6, M7, M1, and M3 conduct; and in State 3, M1–M4 are switched ON. The output CM in all states is maintained at 1/2 PVDD, effectively reducing CM EMI. The output stage switches between either States 1 and 3 or States 2 and 3. During the brief transition between States 1 and 3, only M2 and M4 are ON, and the body diodes of M1 and M3

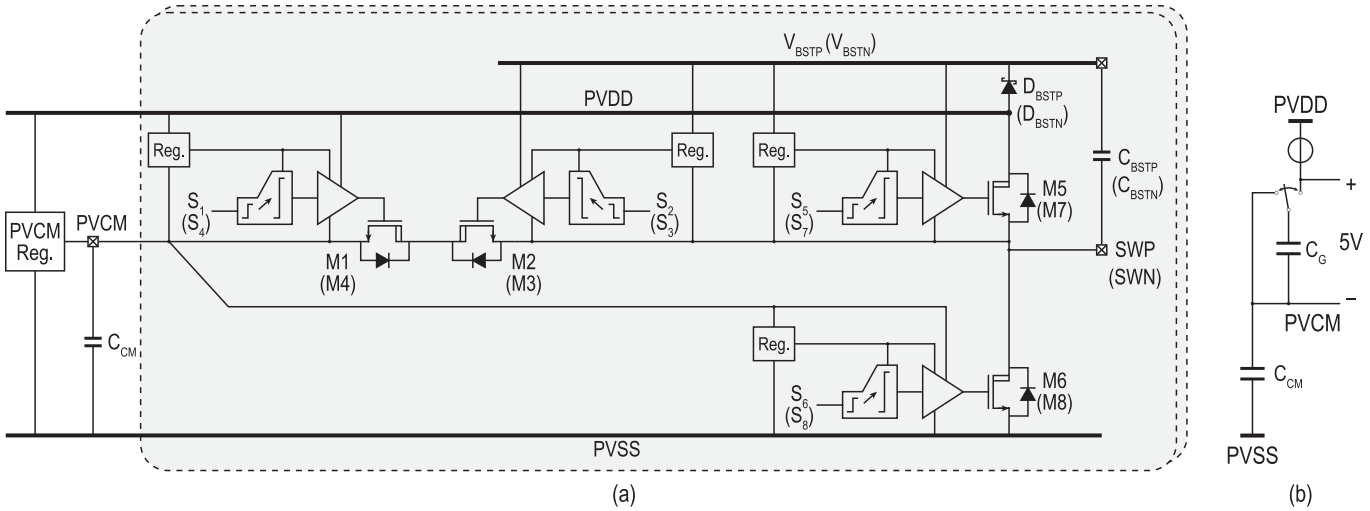


Fig. 6. (a) Simplified schematic of the output stage half circuit with floating regulators, level shifters, and gate drivers for the output transistors. (b) Equivalent circuit illustrating the charging of $C_{\mathrm{CM}}$ by M1 and M4 switchings.

provide a path for the inductor current to continue flowing. Similarly, the body diodes of M2 and M4 provide a path for the inductor current during the transition between States 2 and 3. Compared with [16], the proposed multilevel output stage does not require complex circuitry to avoid both dead time and cross-conduction. In contrast to [14], no complicated capacitor charge balancing circuitry is needed since, in State 3, the signal current only circulates within M1–M4. Thus, no signal current is drawn from PVCM, which can be maintained by a low-power linear regulator. Note that while idling, the output stage is mostly in State 3, which significantly reduces idle power.

Introducing the extra output level reduces the output step size by half, leading to significant EMI reduction. Although it is rather difficult to predict EMI by simulations, the ripple current injected into the load provides a relevant indication. Fig. 4 compares the peak-to-peak output ripple current of a conventional two-level AD mode output stage and the proposed multilevel output stage using the same inductor. The conventional output stage generates the most ripple when there is no audio signal, while the proposed output stage produces the least in this situation, with a 2× lower peak amplitude, which is reached at half full-scale. As a result, the proposed output stage should have significantly better EMI performance since most audio signals have a high crest factor.

### B. Modulation Scheme

As mentioned in Section I, fixed frequency PWM creates tones at well-defined frequencies in the EMI spectrum, which can be placed above the AM band. Hence, this work employs fixed-frequency PWM switching at 4.2 MHz. For the same amount of attenuation, this allows the *LC* filter cutoff frequency to be 2× higher than those in [1] and [2].

The proposed output stage generates three differential output voltages. To derive them, two triangular-wave carriers are employed, which are equal in amplitude but opposite in phase (see Fig. 5). The loop filter output is then compared with the two triangular waves. When the input signal is above both carriers, the output stage switches to State 1, bringing the differential output to +PVDD; when the signal is between the two carriers, the output stage switches to State 3, creating a zero differential output; and when the signal is below both carriers, the output stage switches to State 2 to provide −PVDD. Since PWM pulses appear twice in one carrier cycle, a 2.1-MHz carrier frequency is used to operate the output stage at 4.2 MHz.

## III. Circuit Implementation of the Output Stage

The proposed Class-D amplifier is implemented in a high-voltage BCD process, and its output stage is powered by a 14.4-V supply. To account for extra stress from supply ringing due to off-chip parasitic inductances, the power transistors are all implemented with n-channel LDMOS transistors with a 5-V gate oxide and 20-V $V_{\mathrm{DS}}$ rating. This section first describes the circuitry driving the output transistors and then gives the design details about the gate-charge reuse technique, the power transistor driving circuits, the sizing of the power transistors, and the implementation of the PVCM regulator.

### A. Architecture

As shown in Fig. 6(a), the output stage consists of eight power transistors (M1–M8) and their respective driving circuits, an external capacitor $C_{\mathrm{CM}}$ to hold the mid-rail level, and a PVCM regulator to maintain the voltage on $C_{\mathrm{CM}}$. Each output transistor is driven by a PWM signal generated by a 1.8-V PWM modulator (see Section IV-B). This signal is then used to drive the transistor via a level shifter and a gate driver. The level shifter and the gate driver of each output transistor are powered by a floating regulator that provides a 5-V local supply with respect to the source of each output transistor. M2, M3, M5, and M7 require local supplies above PVDD, which are obtained using external bootstrap capacitors $C_{\mathrm{BSTP}}$ and $C_{\mathrm{BSTN}}$ charged, respectively, through internal Schottky diodes $D_{\mathrm{BSTP}}$ and $D_{\mathrm{BSTN}}$, as in [2] and [21]–[23]. M2 and M5 (also M3 and M7) employ separate regulators to avoid crosstalk-induced timing errors due to

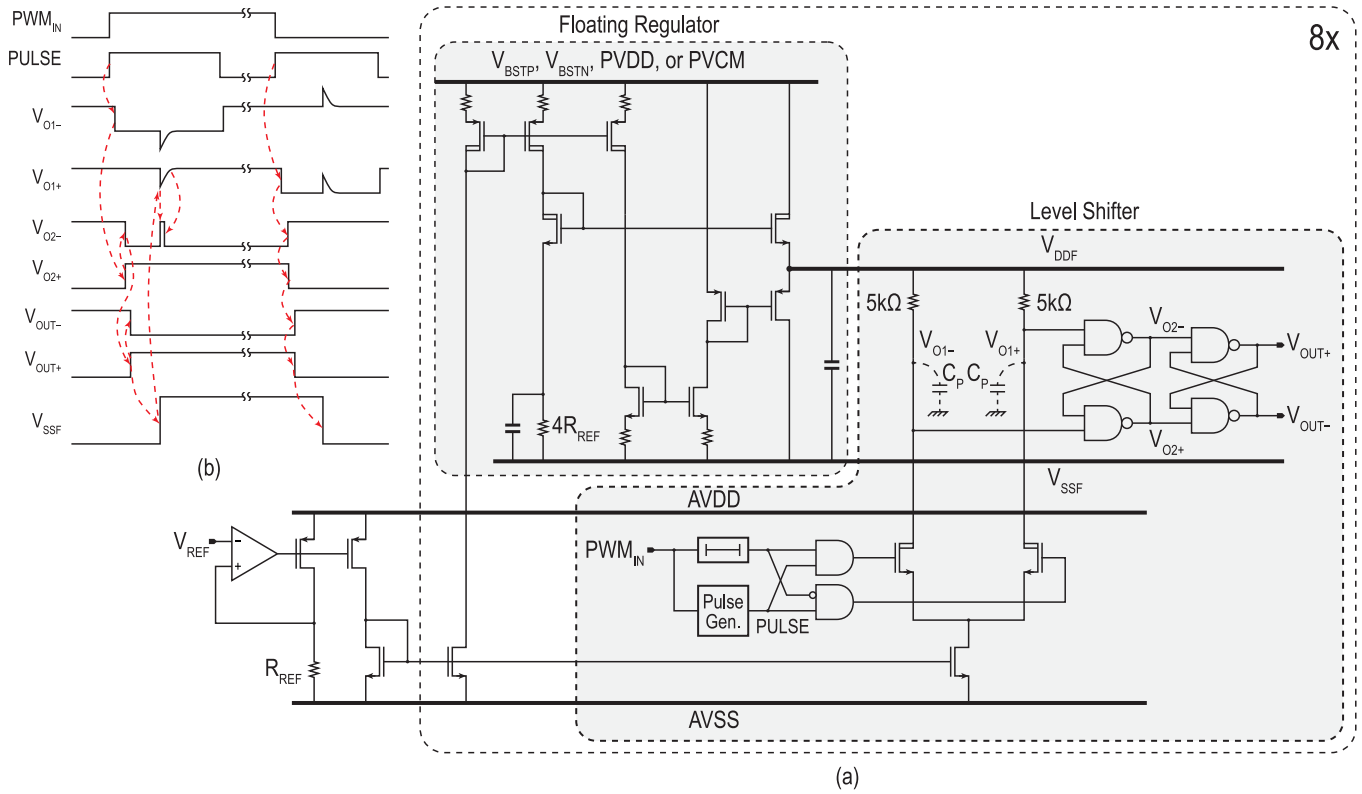


Fig. 7. (a) Design of floating voltage regulators and level shifters in the output stage. (b) Transient waveform on internal nodes of the level shifter.

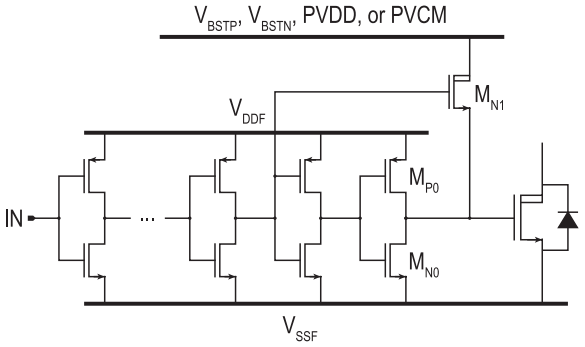


Fig. 8. Implementation of the gate driver.

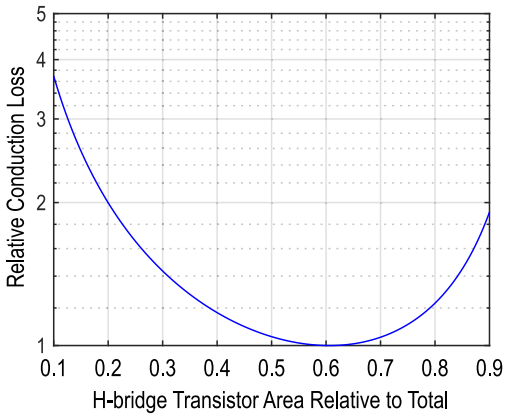


Fig. 9. Conduction loss as a function of the area allocated for H-bridge transistors M5–M8 in the output stage.

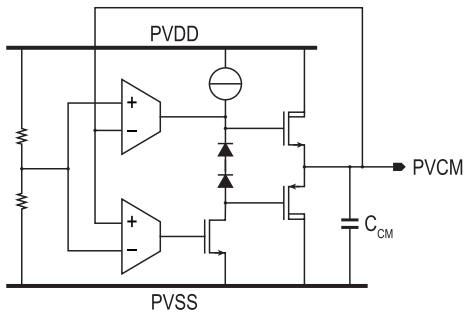


Fig. 10. Implementation of the PVCM regulator.

voltage droop at the regulator outputs during gate charging. The gate drive for M1 and M4 is regulated from PVDD, while that for M6 and M8 is derived from PVCM. This configuration allows M6 and M8 to recycle the gate charge from M1 and M4 along with the bias current of their respective floating regulators, which will be explained further in Section III-B. The PVCM regulator is a low-power linear regulator, which pre-charges $C_{CM}$ during startup and maintains it at mid-rail during normal operation.

### *B. Gate Charge Reuse*

When M1 and M4 are switched ON, $C_{CM}$ collects the current charging their gate–source capacitance. Effectively, the periodic charging and discharging of the gate–source capacitance of M1 and M4 create switched-capacitor resistors between PVDD and PVCM, charging $C_{CM}$. Fig. 6(b) shows the equivalent circuit. This charge is then reused for the gates of M6 and M8. The proposed gate-charge reuse scheme not only reduces the gate charging loss but also alleviates the loading on the PVCM regulator, which now only needs to

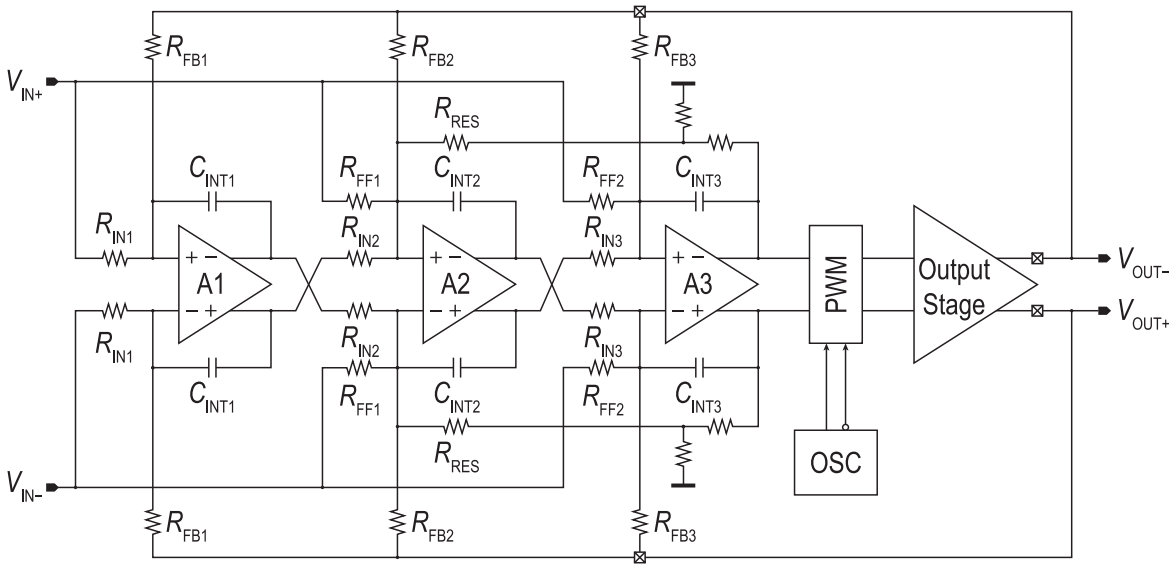


Fig. 11. Block diagram of the closed-loop Class-D amplifier.

supply the difference between the gate-charge currents of M6, M8 and M1, M4. According to simulations, the idle power would increase by 14 mW if the low-side gate driver's power was simply derived from PVDD.

### C. Floating Regulator

Fig. 7(a) shows the schematic of the floating regulator, similar to that in [2]. A current reference $I_{REF}$ is derived by imposing a reference voltage (1.25 V) across a resistor $R_{REF}$, whose copies are routed to each floating regulator. $I_{REF}$ flows through a 4× larger resistor of the same type in each regulator to create a scaled reference voltage of 5 V with respect to $V_{SSF}$ in the floating domain, which is then buffered by a class-AB source follower that supplies the level shifter and gate driver. Matching of resistors and current source devices guarantees sufficient accuracy of the output voltage [2], [24].

### D. Level Shifter

Fig. 7(a) also shows the level shifter translating the PWM signal from the 1.8-V domain to the floating voltage domains. It consists of a resistor-loaded differential amplifier and a CM-immune two-stage NAND latch. During an output transition, one of the differential pair inputs is pulled high, creating a 5-V voltage drop at the respective input of the floating-domain NAND latch, updating its output. A delay line before the AND gates at the input ensures that PULSE goes high before the input transition arrives at the differential pair, avoiding pulsewidth errors due to the pulse generator. In the level shifters for M2, M3, M5, and M7, $V_{SSF}$ switches to the new output level with a slew rate of several V/ns after a transition propagates to the output transistor. As shown in Fig. 7(b), displacement current through the parasitic capacitance at nodes $V_{O1+}$ and $V_{O1-}$ can pull them down and lead to glitches on $V_{O2+}$ or $V_{O2-}$. They are blocked by a second NAND latch, and thus, the level shifter output remains constant and correct during the slewing of $V_{SSF}$. The input pulse is designed to extend beyond the $V_{SSF}$ transition so that the first latch's output is restored after the transition. The pulse generators in all eight level shifters trigger during each output transition to guarantee that the outputs of the four level shifters not switching (see Fig. 5) also remain correct.

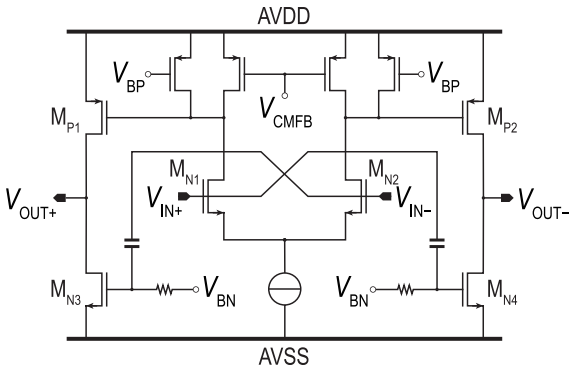


Fig. 12. Two-stage feedforward compensated OTA used in the loop filter.

### E. Gate Driver

Fig. 8 shows the gate driver design, which buffers the level shifter output and drives the output transistors. To reduce loading on the floating regulator, most of the gate charge is drawn from the floating regulator's input directly using a source follower $M_{N1}$ [2], [23]. In the last stage, the pull-down strength is chosen to be larger than the pull-up strength to avoid cross conduction and allow minimal dead time, which reduces the output stage distortion [22].

### F. Output Transistor Sizing

Multilevel output stages require additional output transistors that can drastically increase the overall area [8], [10], [14], [16]. At the first sight, the ON-resistance of M1–M4 should be 2× lower than that of M5–M8 such that the resistance between the output and any of the supply rails (PVDD, PVCM, and PVSS) would be the same. With the

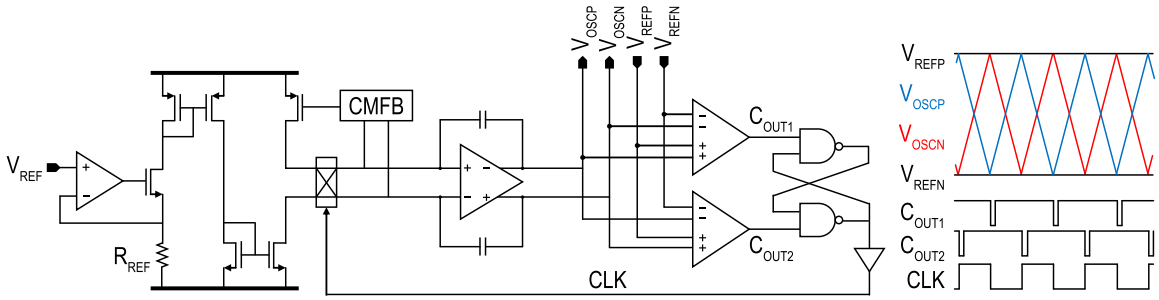


Fig. 13. Fully differential oscillator for carrier generation.

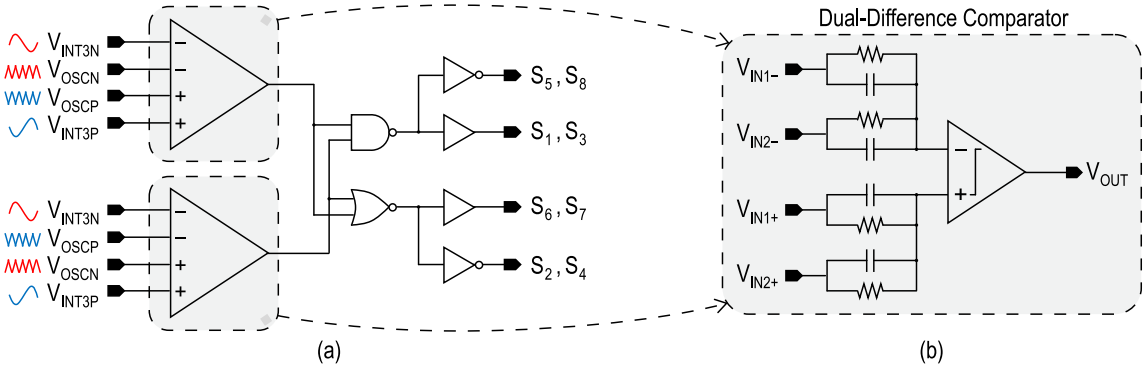


Fig. 14. (a) Fully differential multilevel pulsewidth modulator. (b) Dual-difference comparator in an oscillator and a pulsewidth modulator.

same type of transistor used, M1–M4 will occupy a 2× larger area compared with M5–M8. This is mitigated in the proposed output stage architecture. The ON-duty cycle of the CM switches (M1–M4) is given by $(1 - |V_{IN}|/V_{IN,FS})$, where $V_{IN,FS}$ is the input full scale and $V_{IN}$ is the differential input voltage between $\pm V_{IN,FS}$. Therefore, at high output power, as $|V_{IN}|$ approaches $V_{IN,FS}$, the ON-time of M1–M4 approaches zero. Fig. 9 shows the conduction loss as a function of relative sizing of M1–M4 and M5–M8 when the amplifier delivers a 10% THD clipped sine wave, representing the worst case for conduction loss and thermal dissipation. For a certain area budget, the conduction loss is minimized when M5–M8 occupy 60% of the total output transistor area. In this article, $R_{DS(on)}$ of M1–M4 is 210 mΩ, and that of M5–M8 is 140 mΩ.

### G. PVCM Regulator

As mentioned in Section II, the PVCM regulator does not supply the load current. However, since M1 and M4 are sized differently from M6 and M8, the regulator must compensate for the difference between their gate charges, which is also signal-dependent. When the duty cycle of M1 and M4 is almost 100%, and the ON-time of M6 and M8 is smaller than their gate voltages' rise time, a net current flows into PVCM. On the other hand, when the signal is large and since M1 and M4 have a smaller gate area, their gate charge is not enough to fully charge the gates of M6 and M8, and a net current flowing out of PVCM is required. To stabilize PVCM, the regulator uses a class-AB follower output stage to both source and sink currents. Fig. 10 shows its implementation, where a resistor divider creates a mid-rail reference voltage, which drives PVCM through a unity-gain buffer. It only draws 0.5 mA of quiescent current from PVDD.

## IV. Analog Signal Path

In closed-loop Class-D amplifiers, distortion in the output stage is suppressed by the loop gain while noise and distortion introduced in the loop filter directly impact the overall performance. Therefore, the performance of the loop filter and the pulsewidth modulator is of critical importance. This section presents the design considerations and implementation details of the loop filter and the multilevel pulsewidth modulator.

### A. Loop Filter

For Class-D amplifiers using fixed-frequency PWM, the maximum allowable bandwidth for stable operation is given by $f_{SW}/\pi$ [25]. A loop bandwidth of 800 kHz is chosen to allow for a sufficient stability margin, while a third-order loop filter guarantees sufficient loop gain in the audio band. Fig. 11 shows a simplified schematic of the loop filter, where active-*RC* integrators employing polysilicon resistors and metal–insulator–metal (MIM) capacitors are used for their superior linearity. The integration capacitors are built with switchable banks to compensate for the process variation of the *RC* time constant. A resonance at around 15 kHz is realized by local feedback through $R_{RES}$ around the second and third integrators to boost the loop gain in the audio band to above 82 dB [26]. Extra input feed-ins into the second and third integrators via $R_{IN2}$ and $R_{IN3}$ guarantee low swing at the output of the first two integrators and improve their linearity. In particular, the first integrator processes the difference between the input and feedback signals. The feedback signal contains significant high-frequency components, including the PWM tones, sidebands, and their harmonics. Nonlinearity in the amplifier A1 results in intermodulation among these

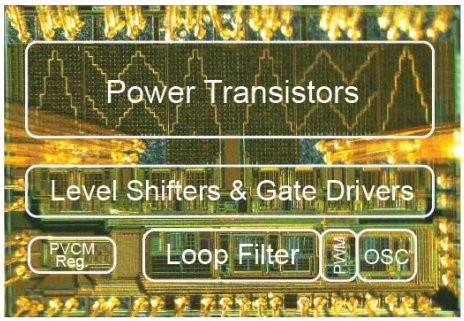


Fig. 15. Die micrograph.

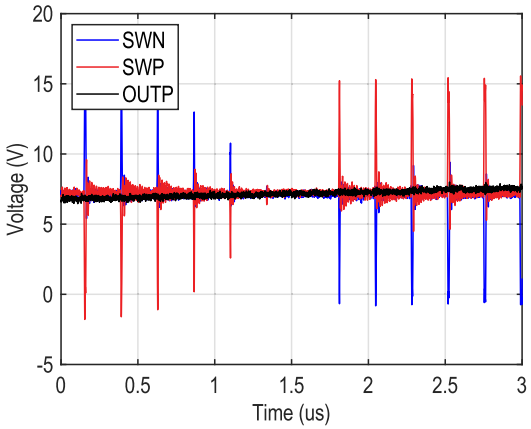


Fig. 16. Measured output voltage of the Class-D amplifier before the *LC* filter (SWP and SWN) and after the *LC* filter (OUTP).

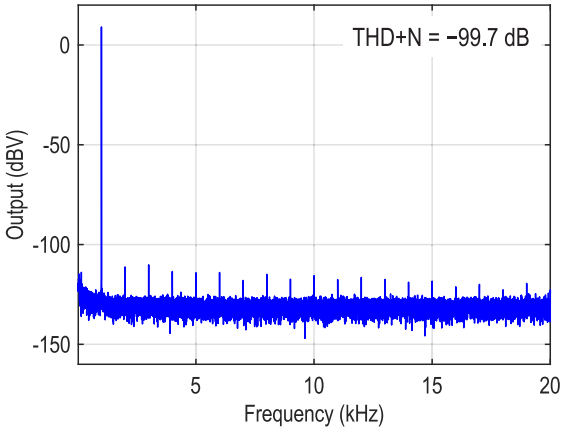


Fig. 17. Measured audio band spectrum when the prototype drives a 1-W sine wave into an 8-Ω load.

components, which is directly added to the input and leads to in-band distortion.

To mitigate this effect, a two-stage feedforward-compensated OTA instead of a conventional two-stage Miller compensated OTA is employed, as shown in Fig. 12. Feedforward compensation is implemented by ac-coupling the inputs to $M_{N3}$ and $M_{N4}$ in the second stage [2]. This allows for 14 dB of extra gain at the switching frequency to suppress the intermodulation distortion compared with a conventional Miller-compensated OTA without increasing the power consumption.

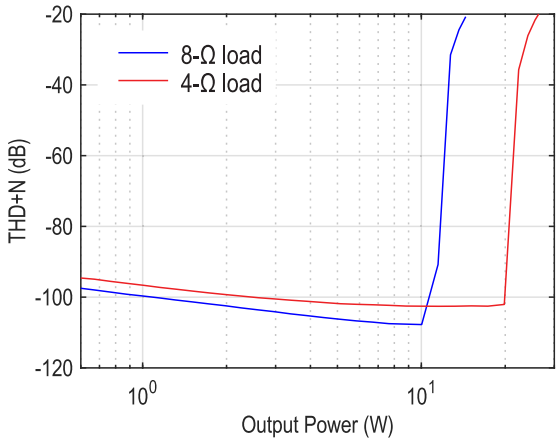


Fig. 18. Measured THD+N of the prototype across output power.

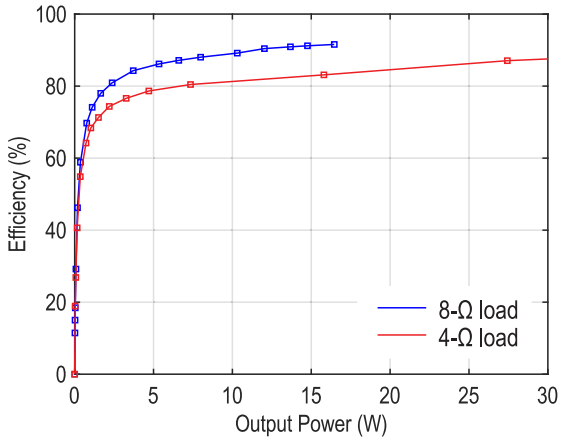


Fig. 19. Measured power efficiency at different output powers.

### *B. Pulsewidth Modulator*

As described in Section II, multilevel PWM is realized by comparing the loop filter output with two equal but opposite triangle waves. They are generated by the fully differential oscillator shown in Fig. 13, built around a fully differential OTA. When the absolute value of its differential output exceeds ($V_{REFP} - V_{REFN}$), one of the comparators toggles, reversing the polarity of integration using a chopper. The resulting triangle carrier frequency is proportional to $1/(R_{REF}C_{INT})$. $C_{INT}$ is made of trimmable banks to compensate for the process variation of the *RC* time constant so that the oscillator operates near 2.1 MHz. The same trim codes are then applied to the loop filter to center its transfer function. In the prototype, $V_{REF}$ is provided externally to fine-tune the oscillator to 2.1 MHz. The loop filter output ($V_{INT3P} - V_{INT3N}$) is compared with the two triangle waves ($V_{OSCP} - V_{OSCN}$) and ($V_{OSCN} - V_{OSCP}$) using two dual-difference comparators, as shown in Fig. 14, where the two differential inputs are combined using an all-pass passive network. The fully differential operation offers robustness against CM noise and mismatch (e.g., substrate noise) between the carrier and input compared with single-ended implementations [8], [27], [28]. Here, as in other time-interleaved systems, the mismatch between two comparators and imbalances in the differential triangle wave results in a residual spur at the carrier frequency

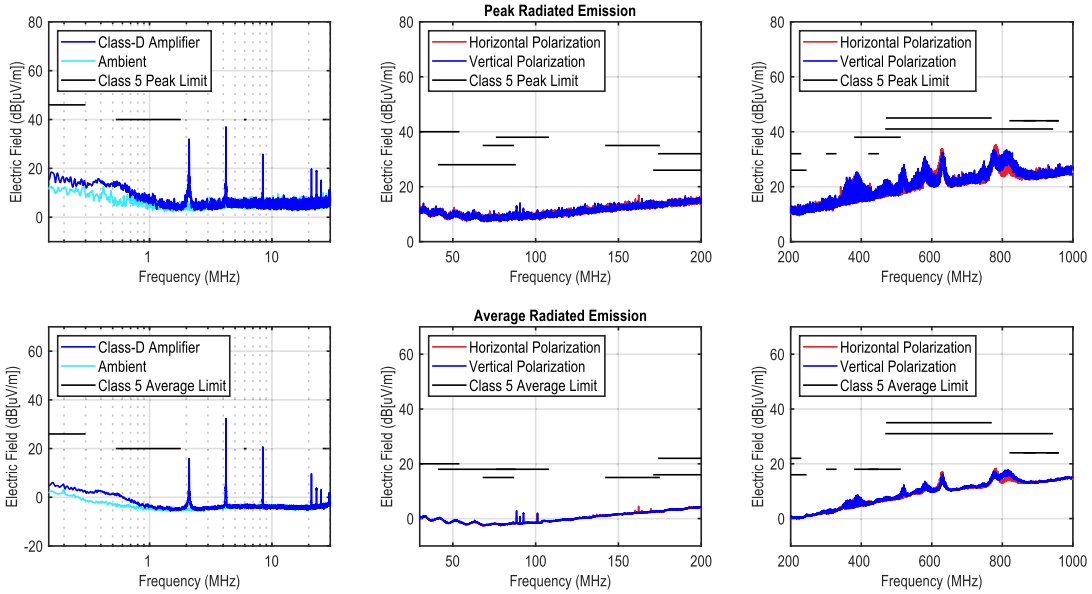


Fig. 20. Measured peak and average radiated EMI according to CISPR 25 standard from 150 to 1 GHz.

TABLE I
PERFORMANCE SUMMARY AND COMPARISON

| | This Work | | [1] | [2] ISSCC'20 | [4] ISSCC'18 | [6] JSSC'17 | [8] ISSCC'17 | [14] JSSC'16 | [16] JSSC'09 |
|---|---|---|---|---|---|---|---|---|---|
| **Architecture** | PWM 3 Level | | PWM 2 Level | DSPWM 2 Level | PWM 2 Level | PWM 2/4 phase | PWM 7 Level | PWM 5 Level | PWM 3 Level |
| **EMI standard** | CISPR 25 Class 5 | | CISPR 25 Class 5 | CISPR 25 Class 5* | - | - | - | - | FCC Class B |
| **$f_{SW}$ (kHz)** | 4200 | | 2100 | 2000 | 400 | 500 | 700 | 165~330 | 250 |
| **$f_{LC}$ (kHz)** | 580 | | 88 | 100 | - | - | - | - | - |
| **Load (Ω)** | 8 | 4 | 4 | 8 | 4 | 4 | 8 | 4 | 4 |
| **Output Power (W)** | 14 | 28 | 75 | 28 | 20 | 80 | 10 | 70 | 20 |
| **Efficiency** | 91% | 87% | 86% | 91% | 90% | > 90% | 91% | 90% | 90% |
| **Quiescent Current (mA)** | 7 | | 180 | 17 | 20.5 | - | 3.5 | 2.9 | - |
| **Idle Power (mW)** | 94 | | - | 245 | - | - | - | 70 | - |
| **Peak THD+N @ 1kHz** | 0.0004% | 0.0007% | 0.02% | 0.0008% | 0.0013% | 0.004% | 0.0023% | 0.003% | 0.1 |
| **SNR (A-weighted)** | 109.7 dB | | - | 108.6 dB | 116 dB | - | 106 dB | - | - |
| **DR (A-weighted)** | 111.2 dB | | - | - | 115.5 dB | 115 dB | - | 110 dB | - |

*Only 150 kHz to 30 MHz reported

(2.1 MHz), which is still above the AM band where the EMI limit is relaxed. The comparator outputs are processed by combinational logic to derive the gate control for each output transistor.

## V. MEASUREMENT RESULTS

A test chip of the proposed design is fabricated in a 180-nm BCD process and occupies an area of 5 $mm^2$. Fig. 15 shows the die micrograph. The test die is directly mounted and wire-bonded on a test PCB with output stage decoupling capacitors nearby to reduce the loop area of the high-frequency current in the output stage, reducing the ringing and EMI associated with parasitic inductance. Fig. 16 shows the measured output waveform during a zero crossing of the differential input signal. When the input crosses zero, there is almost no switching. This feature is beneficial for achieving a low idle power of 94 mW, in which about half is consumed as quiescent current in the floating regulators while the other half is due to occasional switching of the output stage driven by noise present at the loop filter output.

Audio performance is measured by an Audio Precision APx555 signal source and analyzer at the output of the *LC* filter, which has a cutoff frequency of 580 kHz ($L = 470$ nH and

$C = 160$ nF). The measured audio band spectrum when the chip delivers 1 W into an 8-Ω load is shown in Fig. 17. The measured THD+N is −99.7 dB. Fig. 18 shows the THD+N performance as a function of output power, where the lowest levels are achieved when the signal is near full scale. For an 8-/4-Ω load, the lowest levels achieved are −107.8 and −102.6 dB, respectively.

The measured peak efficiency is 91% for an 8-Ω load and 87% for a 4-Ω load, as shown in Fig. 19. Fig. 20 shows the measured level of radiated EMI according to the CISPR 25 standard from 150 kHz to 1 GHz when the prototype drives 12 W into a 4-Ω load. The prototype meets the Class 5 limit for both peak and average radiated emissions with a 5.7-dB margin.

Table I presents a performance summary of the proposed multilevel Class-D amplifier and compares it with other state-of-the-art designs. Due to the multilevel operation and high switching frequency, it satisfies the CISPR 25 Class 5 EMI limit while employing a much higher *LC* filter cutoff frequency compared with other works. Also, the proposed modulation and gate charge reuse scheme result in competitive idle power compared with other Class-D amplifiers that switch above 1 MHz. The high loop gain around the output stage and the OTA in the loop filter lead to state-of-the-art THD+N performance.

## VI. Conclusion

A low-EMI high-linearity Class-D amplifier employing a multilevel output stage is presented. The fully differential multilevel operation in this work significantly reduces EMI. With a 4.2-MHz switching frequency, the CISPR 25 Class 5 EMI standard is met with an *LC* filter cutoff frequency of 580 kHz. At idle, the fully differential multilevel operation results in minimal switching activity, leading to an idle power of only 94 mW. The high switching frequency also enables an 800-kHz loop bandwidth and 82 dB of audio band loop gain, suppressing the output stage nonlinearity to below the noise floor and helping the prototype achieve a THD+N of −107.8 dB.

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## References

[1] Texas Instruments. *TAS6424-Q1 75-W, 2-MHz Digital Input 4-Channel Automotive Class-D Audio Amplifier With Load-Dump Protection and I2C Diagnostics*. Accessed: Jul. 15, 2020. [Online]. Available: https://www.ti.com/lit/gpn/tas6424-q1

[2] S. Karmakar *et al.*, "A 28W −108.9dB/-102.2dB THD/THD+N hybrid ΔΣ-PWM class-D audio amplifier with 91% peak efficiency and reduced EMI emission," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2020, pp. 350–352.

[3] Maxim Integrated. *4-Channel, Automotive Class D Audio Amplifier*. Accessed: Jul. 31, 2020. [Online]. Available: https://www.maximintegrated.com/en/products/analog/audio/MAX13301.html

[4] E. Cope *et al.*, "A 2×20W 0.0013% THD+ N class-D audio amplifier with consistent performance up to maximum power level," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2018, pp. 56–58.

[5] *Vehicles, Boats and Internal Combustion Engines—Radio Disturbance Characteristics—Limits and Methods of Measurement for the Protection of on-Board Receivers*, CISPR, Geneva, Switzerland, Oct. 2016.

[6] D. Schinkel *et al.*, "A multiphase class-D automotive audio amplifier with integrated low-latency ADCs for digitized feedback after the output filter," *IEEE J. Solid-State Circuits*, vol. 52, no. 12, pp. 3181–3193, Dec. 2017.

[7] T. Karaca and B. Deutschmann, "Electromagnetic evaluation of class-D switching schemes," in *Proc. 11th Conf. Ph.D. Res. Microelectron. Electron. (PRIME)*, Jun. 2015, pp. 113–116.

[8] J.-H. Lee *et al.*, "An 8Ω 10W 91%-power-efficiency 0.0023%-THD+N multi-level class-D audio amplifier with folded PWM," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2017, pp. 88–89.

[9] S.-H. Yu and M.-H. Tseng, "Optimal control of a nine-level class-D audio amplifier using sliding-mode quantization," *IEEE Trans. Ind. Electron.*, vol. 58, no. 7, pp. 3069–3076, Jul. 2011.

[10] S.-H. Yang *et al.*, "A low-THD class-D audio amplifier with dual-level dual-phase carrier pulsewidth modulation," *IEEE Trans. Ind. Electron.*, vol. 62, no. 11, pp. 7181–7190, Nov. 2015.

[11] V. M. E. Antunes, V. F. Pires, and J. F. A. Silva, "Narrow pulse elimination PWM for multilevel digital audio power amplifiers using two cascaded H-bridges as a nine-level converter," *IEEE Trans. Power Electron.*, vol. 22, no. 2, pp. 425–434, Mar. 2007.

[12] C. Cerutti, "Multilevel class-D amplifier," U.S. Patent 8 330 541, Apr. 25, 2013.

[13] Analog Devices. *Digital 2.5 W, 5.1 V, Boost Class-D Audio Amplifier With Output Sensing*. Aug. 7, 2020. [Online]. Available: https://www.analog.com/media/en/technical-documentation/data-sheets/SSM4567.pdf

[14] M. Hoyerby, J. K. Jakobsen, J. Midtgaard, and T. H. Hansen, "A 2×70 W monolithic five-level class-D audio power amplifier in 180 nm BCD," *IEEE J. Solid-State Circuits*, vol. 51, no. 12, pp. 2819–2829, Dec. 2016.

[15] D. Nielsen, A. Knott, and M. A. E. Andersen, "Multilevel inverter based class d audio amplifier for capacitive transducers," in *Proc. 16th Eur. Conf. Power Electron. Appl.*, Aug. 2014, pp. 1–7.

[16] P. Siniscalchi and R. K. Hester, "A 20 W/Channel class-D amplifier with near-zero common-mode radiated emissions," *IEEE J. Solid-State Circuits*, vol. 44, no. 12, pp. 3264–3271, Dec. 2009.

[17] S.-H. Chien *et al.*, "An open-loop class-D audio amplifier with increased low-distortion output power and PVT-insensitive EMI reduction," in *Proc. IEEE Custom Integr. Circuits Conf.*, Sep. 2014, pp. 1–4.

[18] E. Gaalaas, B. Y. Liu, N. Nishimura, R. Adams, and K. Sweetland, "Integrated stereo ΔΣ/ class D amplifier," *IEEE J. Solid-State Circuits*, vol. 40, no. 12, pp. 2388–2397, Dec. 2005.

[19] A. Matamura, N. Nishimura, and B. Y. Liu, "Filterless multi-level delta-sigma class-D amplifier for portable applications," in *Proc. IEEE Int. Symp. Circuits Syst.*, May 2009, pp. 1177–1180.

[20] H. Zhang *et al.*, "A −107.8 dB THD+N low-EMI multi-level class-D audio amplifier," in *Proc. IEEE Symp. VLSI Circuits*, Jun. 2020, pp. 1–2.

[21] M. Berkhout, "An integrated 200-W class-D audio amplifier," *IEEE J. Solid-State Circuits*, vol. 38, no. 7, pp. 1198–1206, Jul. 2003.

[22] M. Berkhout, "A class d output stage with zero dead time," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Jul. 2003, pp. 134–135.

[23] H. Ma, R. van der Zee, and B. Nauta, "A high-voltage class-D power amplifier with switching frequency regulation for improved high-efficiency output power range," *IEEE J. Solid-State Circuits*, vol. 50, no. 6, pp. 1451–1462, Jun. 2015.

[24] S. Karmakar *et al.*, "A 28-W, −102.2-dB THD+N class-D amplifier using a hybrid ΔΣ M-PWM scheme," *IEEE J. Solid-State Circuits*, vol. 55, no. 12, pp. 3146–3156, Dec. 2020, doi: 10.1109/JSSC.2020.3023874.

[25] M. Berkhout, L. Breems, and E. V. Tuijl, "Audio at low and high power," in *Proc. 34th Eur. Solid-State Circuits Conf.*, Sep. 2008, pp. 40–49.

[26] S. Pavan, R. Schreier, and G. C. Temes, "High-order delta-sigma modulators," in *Understanding Delta-Sigma Data Converters*. Piscataway, NJ, USA: IEEE Press, 2017, pp. 83–116.

[27] S.-H. Chien, Y.-W. Chen, and T.-H. Kuo, "A 0.96 mA quiescent current, 0.0032% THD+N, 1.45W class-D audio amplifier with area-efficient PWM-residual-aliasing reduction," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2018, pp. 60–62.

[28] W. Wang and Y. Lin, "A 0.0004% (-108dB) THD+N, 112dB-SNR, 3.15W fully differential class-D audio amplifier with Gm noise cancellation and negative output-common-mode injection techniques," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2018, pp. 58–60.

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