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A High-Loop-Gain Low-Dropout Regulator with Adaptive Positive Feedback Compensation Handling 1-A Load Current

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Abstract: Low-dropout regulators, which have the capabilities of handling large output current and obtaining a superior transient response, are receiving increasing attention. This paper presents a high-output-current low-dropout regulator with high loop gain. An adaptive positive feedback compensation method is presented. It guarantees stability under full load conditions and achieves high loop gain. Without relying on an external zero, a ceramic capacitor with low equivalent series resistance can be employed, resulting in the minimized output voltage variation during the load transient response. In addition, the load regulation and line regulation are both small. An impedance adapting stage is inserted between the error amplifier and power transistor. It is suitable for low-supply voltage applications and drives the power transistor quickly. The simulation results indicate that the proposed LDO can supply a 1000 mA load current with a 200 mV dropout voltage. The load regulation and line regulations are 0.089 μV/mA and 0.562 m V/V, respectively. The power supply rejection is above 75 dB at 1 kHz under the full range of the output current.

Keywords: low-dropout regulator (LDO); adaptive positive feedback compensation; transient response; power supply rejection (PSR)

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1. Introduction

Power management is a necessary block for all electronic systems. Linear regulators have simpler circuit complexity, faster response, and lower noise content, compared with their switching counterparts [1–3]. The increasing growth in portable point-of-sale systems, Wi-Fi access points, and communication modules has fueled the growth of the low-dropout voltage regulators to handle large output current (about 1 A) [4]. Due to the dropout requirements, stability, and related inefficiency, designing a separate LDO for high-current applications is still a challenge.

The N-type LDO, in which an NMOS or NPN power transistor is adopted, has a faster transient response and less silicon real estate than the P-type LDO because of the inherent low impedance and high carrier mobility. The main disadvantage of the N-type LDO is the high-dropout voltage [5–8]. An extra internal charge pump or a second low-power input rail is needed to achieve a low-dropout voltage for N-type LDO [9,10]. For the P-type LDO, there are at least two low-frequency poles in the negative feedback loop: p_1 at the gate of the power transistor, and p_2 at the output of the LDO [11,12]. Many advanced structures aiming for high stability have been reported [13–16]. In [17,18], a dynamically biased buffer with shunt feedback has been adopted to drive the power transistor. When a larger load current (e.g., 1 A) is required, the buffer will dissipate a much larger quiescent current to push the parasitic pole to higher frequencies. However, this circuit is not suitable for low-V_{DD} applications due to the PMOS buffer and power stage [19]. A low-voltage LDO with damping-factor-control frequency compensation has

been presented in [20], and a feedforward capacitor is employed to generate a left-half-plane (LHP) zero. The stability, output noise, and power-supply rejection ratio (PSRR) can be improved by using the feedforward capacitor [21], but the required reference voltage should be much smaller than the LDO output voltage, which limits the output range. Q-reduction frequency compensation has been proposed in [22], while the ESR of the off-chip capacitor is needed to introduce an LHP zero. Consequently, variations in the zero's location across process and temperature may lead to instability. The ESR is also detrimental to the load transient performance. Active frequency compensation techniques, such as impedance adapting compensation [23], adaptive miller compensation [24], and pole-tracking compensation [25,26], may suffer from tracking accuracy under the wide range of the load current. The loop response determines the performance of an LDO greatly, such as loop gain and unity-gain frequency (UGF). Wider UGF improves the transient response, usually resulting in larger quiescent current and worse regulation accuracy [27,28]. Digital LDOs can achieve fast transient responses, but the maximum load current is usually small [29,30].

In this paper, a large-output-current LDO employing adaptive positive feedback compensation is proposed. A non-inverting driver stage with adaptive impedance is introduced for low-voltage applications. This paper is organized as follows: Section 2 presents the LDO structure with the proposed driver stage. In addition, loop stability analysis and details of the LDO circuit design considerations are illustrated. Section 3 provides simulation results and a comparison with previous studies. Finally, a conclusion is drawn.

2. Proposed Structure

Figure 1 shows the structure of the proposed LDO with adaptive positive feedback frequency compensation, which consists of a voltage reference V_{REF}, an error amplifier EA1, a non-inverting driver, and a pass transistor. The small-signal output resistor of the buffer is inversely proportional to the output current, which will lead to a load-dependent LHP zero. As the phase from V_1 to V_g is non-inverting, the buffer and the capacitor C_c form the adaptive positive feedback compensation. A Miller capacitor C_f is used to create the dominant pole and realize the current buffer compensation. The bias current of the non-inverting driver is proportional to the load current so that the impedance at V_g can be decreased with the increase in the output current. It contributes to a better PSR performance without a complex circuit.

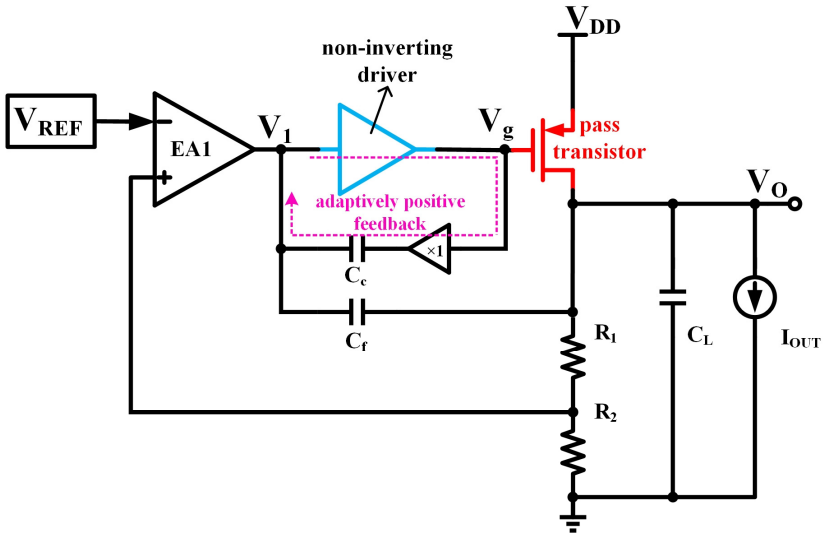

Figure 1. The proposed LDO structure with adaptive positive feedback compensation.

2.1. Non-Inverting Driver Stage

The proposed driver stage with adaptive impedance is shown in Figure 2. The first stage has a small signal gain and consists of transistors M_6, M_{7A} and the constant current source I_1. The second stage consists of transistors M_{7B}, M_{S1} and the constant current source I_2. The minimum supply voltage V_{DD} of this structure is about $|V_{thp}| + 2V_{dsat}$ to provide a large load current. Transistor M_{S1} realizes a dynamically biased load by sensing the output current in the pass transistor M_p. At light conditions, the current in M_{S1} is small, while M_{7B} is biased in the subthreshold region because the width of M_{7B} is large. As the load current increases, the bias current in M_{7B} increases, and the small output impedance to ground at node V_g decreases. Due to the diode-connected structure of M_{7A}, the parasitic pole frequency at node V_m is far beyond the UGF of the whole loop.

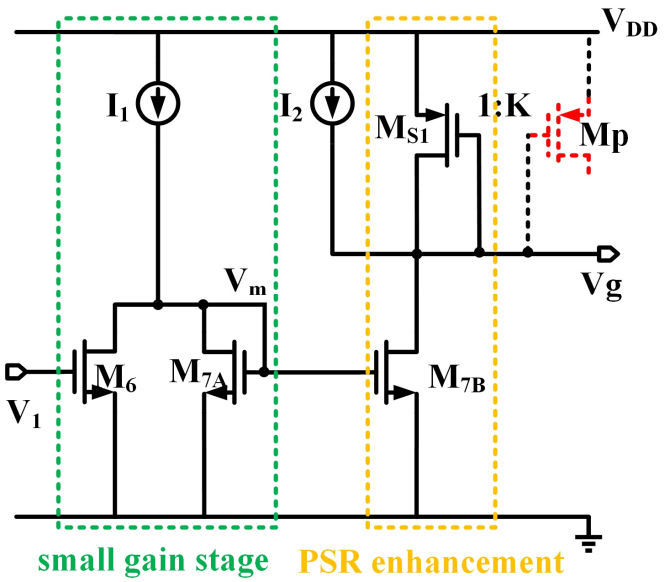

Figure 2. The non-inverting driver stage used in the proposed LDO.

In addition, the current mirror structure of the second driving stage allows the LDO to achieve better PSR performance without any complex circuitry. The driver stage is a non-inverting stage, thus forming the proposed adaptive positive feedback compensation with the compensate capacitor C_c.

2.2. Adaptive Positive Feedback Compensation

Figure 3 shows the transistor level schematic of the proposed LDO structure; the first stage of the error amplifier is realized by a single-stage folded-cascode structure, with transistors $M_{1A}/M_{1B} - M_{5A}/M_{5B}$. As discussed before, the driving stage can be viewed as a non-inverting, single stage. Accordingly, the LDO structure can be modeled as a three-stage amplifier in which the third stage is realized by the pass transistor M_p. A microfarad range off-chip capacitor C_L is used at the output of the LDO. The adaptive positive feedback compensation scheme creates a real LHP zero and allows the LDO to achieve higher stability with a lower quiescent current. M_8 and M_{s2} form the inverting buffer, in which the output is in series with capacitor C_c. The buffer has an adaptive output resistance, as the current in M_{s2} is proportional to the output current in M_p. C_f, C_c, M_{4B}, and the inverting buffer realize the compensation circuit of the proposed LDO. The loop stability and design considerations are discussed in what follows.

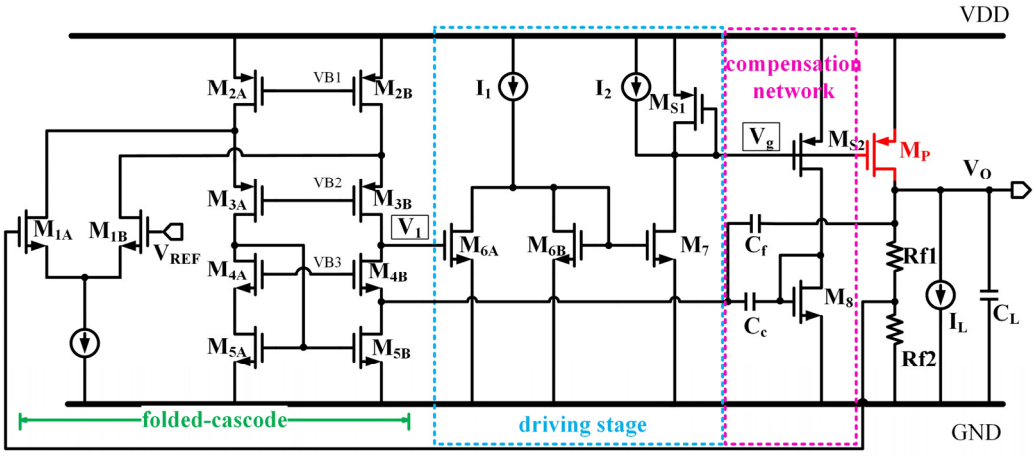

Figure 3. Transistor level schematic of the proposed LDO.

In order to study the stability of the LDO, the loop transfer function is derived. Figure 4 shows the small-signal block diagram representation of the structure in Figure 3. Hence, g_{m1}, g_{m2}, g_{mp}, and g_{mf} represent the transconductance of the input differential transistor pair M_{1A}/M_{1B}, the non-inverting driver stage, power transistor M_P, and transistor M_{4B}, respectively. The transconductance of M_{s2} is expressed as g_{mp}/k_1, and the small-signal output resistance of the buffer is inversely proportional to g_{m8}, which can be expressed as

$$g_{m8} = \frac{g_{mp}}{k_1}\sqrt{\frac{u_n}{u_p}\frac{(W/L)_{M8}}{(W/L)_{Ms2}}} = k_2 g_{mp} \tag{1}$$

$$k_1 k_2 = \sqrt{\frac{u_n}{u_p}\frac{(W/L)_{M5B}}{(W/L)_{M8}}} \tag{2}$$

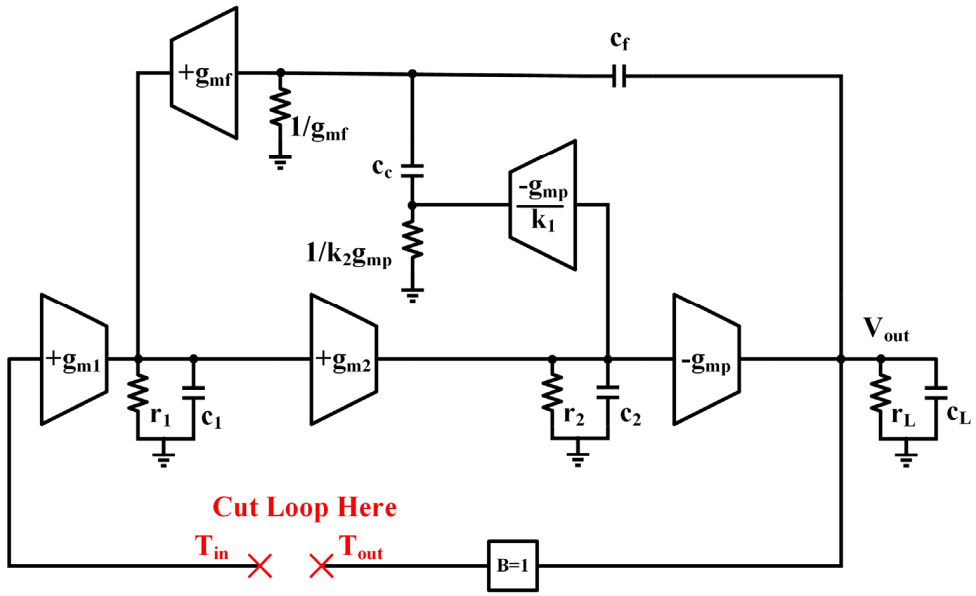

Figure 4. Small-signal block diagram of the proposed LDO.

In addition, the output impedance of each stage is denoted as r_i, $(i = 1, 2, L)$. The lumped parasitic capacitances at nodes V_1, V_g and V_o are modeled as c_1, c_2 and c_L, respectively. The feedback factor B = 1 is used to derive the loop gain function. The loop transfer function will be derived and simplified based on the following considerations:

- c_L is much larger than other capacitors;

- c_f, c_c, c_2 are much larger than c_1.

The loop-gain transfer function of the proposed LDO can be written as

$$T(s) = \frac{T_{out}}{T_{in}} = \frac{-T_0 \times \left(1 + a_1 s + a_2 s^2\right)}{(1 + b_1 s)\left(1 + \frac{b_2}{b_1} s\right)\left(1 + \frac{b_3}{b_2} s + \frac{b_4}{b_2} s^2\right)} \tag{3}$$

$$T_0 = g_{m1} g_{m2} g_{mp} r_1 r_2 r_L \tag{4}$$

$$a_1 = \frac{g_{mf} c_c + k_2 g_{mp}\left(c_c + c_f\right)}{k_2 g_{mp} g_{mf}} \tag{5}$$

$$a_2 = \frac{c_c c_f}{k_2 g_{mp} g_{mf}} \tag{6}$$

$$b_1 = g_{m2} g_{mp} r_1 r_2 r_L c_f \tag{7}$$

$$b_2 = \frac{g_{m2} r_1 r_2 r_L c_c\left(c_L + k_1 c_f\right)}{k_1 k_2} \tag{8}$$

$$b_3 = \frac{r_2 r_L c_2 c_L\left(g_{mf} c_c + k_2 g_{mp}\left(c_c + c_f\right)\right)}{k_2 g_{mp} g_{mf}} \tag{9}$$

$$b_4 = \frac{r_2 r_L c_2 c_L c_c c_f}{k_2 g_{mp} g_{mf}} \tag{10}$$

From (3), the transfer function is negative due to the negative feedback. The low-frequency loop gain can be expressed as T_0. Under a full range of the load current, the numerator of T(s) indicates that two real LHP zeros exit since $a_1^2 - 4a_2 > 0$. The denominator of T(s) implies that four poles exit. $p_1 = -1/b_1$ is the dominant pole, and $p_2 = -b_1/b_2$ is the second pole, with b_1, b_2, given in (8) and (9). The loop stability should be studied for different load conditions.

At light load conditions, g_{mp} is rather small, and $k_2 g_{mp} \ll g_{mf}$. Two LHP zeros are $z_1 = -g_{mf}/c_f$ and $z_2 = -k_2 g_{mp}/c_c$. Besides the dominant pole p_1 and the second pole p_2, the third pole is $p_3 = -b_2/b_3 \approx -g_{m2} g_{mp} r_1\left(c_L + k_1 c_f\right)/k_1 c_2 c_L$, and the fourth pole is $p_4 = -b_3/b_4 \approx -g_{mf}/c_f$. Hence, z_1 and p_4 cancel each other. The ratio of $z_2/p_2 = \left(c_L + k_1 c_f\right)/k_1 c_f$ indicates that z_2 is larger than $40 \times p_2$. The parasitic pole p_3 can be neglected due to the large $g_{m2} r_1$. In this case, the unity-gain frequency w_u and phase margin PM of the system are given by

$$w_u = \frac{g_{m1}}{c_f} \tag{11}$$

$$PM = 90^{\circ} - \arctan\frac{w_u}{p_2} \tag{12}$$

At medium-to-heavy load conditions, g_{mp} is much large and $k_2 g_{mp} \gg g_{mf}$. The third pole is $p_3 \approx -g_{m2} g_{mf} r_1 c_c\left(c_L + k_1 c_f\right)/\left[k_1 k_2 c_2 c_L\left(c_f + c_c\right)\right]$, and the fourth pole is $p_4 \approx -k_2 g_{mp}/\left(c_f \| c_c\right)$. Two LHP zeros are $z_1 = -g_{mf}/\left(c_f + c_c\right)$ and $z_2 = p_4$. Due to the large g_{mp}, p_2 is quite larger than z_1 and p_3. Thus, z_1 is fixed and extends the UGF. The LDO loop thus acts as a first-order system and the stability of the LDO can be guaranteed.

At certain load conditions, $k_2 g_{mp}$ is close to g_{mf}. The transfer function can be revised as

$$T(s) = \frac{T_{out}}{T_{in}} = \frac{-T_0 \times \left(1 + a_1 s + a_2 s^2\right)}{(1 + b_1 s)\left(1 + \frac{b_2}{b_1} s\right)\left(1 + m a_1 s + m a_2 s^2\right)} \tag{13}$$

$$m = \frac{k_1 k_2 c_2 c_L}{g_{m2} r_1 c_c\left(c_L + k_1 c_f\right)} \tag{14}$$

From (13), the parameter m is close to 0 due to the large $g_{m2}r_1$, resulting in conjugate poles p_3 and p_4. Consequently, p_3 and p_4 are far beyond the two LHP zeros z_1 and z_2. Large c_c is helpful to push the conjugate poles to higher frequencies while having a detrimental effect on the load transient response. In addition, large c_c may cause frequency peaks at light load conditions. By setting $c_f = 15pF = 3c_c$, the LDO can achieve a good compromise between stability and transient response.

Figure 5 depicts the simulated loop gain of the proposed LDO under different load currents. The DC loop gain is above 100 dB under full load conditions and the bandwidth increases with load current. The phase margin at no-load and full-load conditions are 52° and 94°, respectively. Process corner and temperature simulation are also implemented to prove the feasibility of the proposed compensation technique. As shown in Figure 6, for different process corners and temperatures, the phase margin of the proposed LDO is above 35° under the full range of load currents. Monte Carlo simulation of phase margin at worst stability, i.e., I_{load} = 1 mA is shown in Figure 7. Thus, stability is guaranteed over the full load current range.

2.3. Circuit Design Considerations

As discussed before, the main source of the operating supply current is derived from M_{S1} and M_{S2}. The ratio of M_P to M_{S1} is $k_1 = 5000$. The large k_1 indicates that a small dynamic current is required, which results in a high current efficiency under heavy load conditions. A 1.2 V internal voltage reference is integrated with the LDO to provide the reference voltage V_{REF} to the input of the error amplifier. In the proposed LDO, the gain of the error amplifier is always greater than 60 dB under the entire load current range. Under the no-load condition, the pass transistor M_P is in the subthreshold region, as it only provides current for the feedback resistors R_{f1} and R_{f2}. Adjustable output can be realized by changing the ratio of the feedback resistors R_{f1} and R_{f2}.The current is equal to $V_o/(R_{f1} + R_{f2})$, and the gate-source voltage V_{sg} required for M_P to minimize the amount of current can be around 400 mV. A ceramic capacitor, which has a low ESR value, is desired for low-output overshoot/undershoot during the load transient response. In this design, a few mΩ resistors are in series with the 4.7 µF capacitor, to emulate the effects of a practical ceramic capacitor.

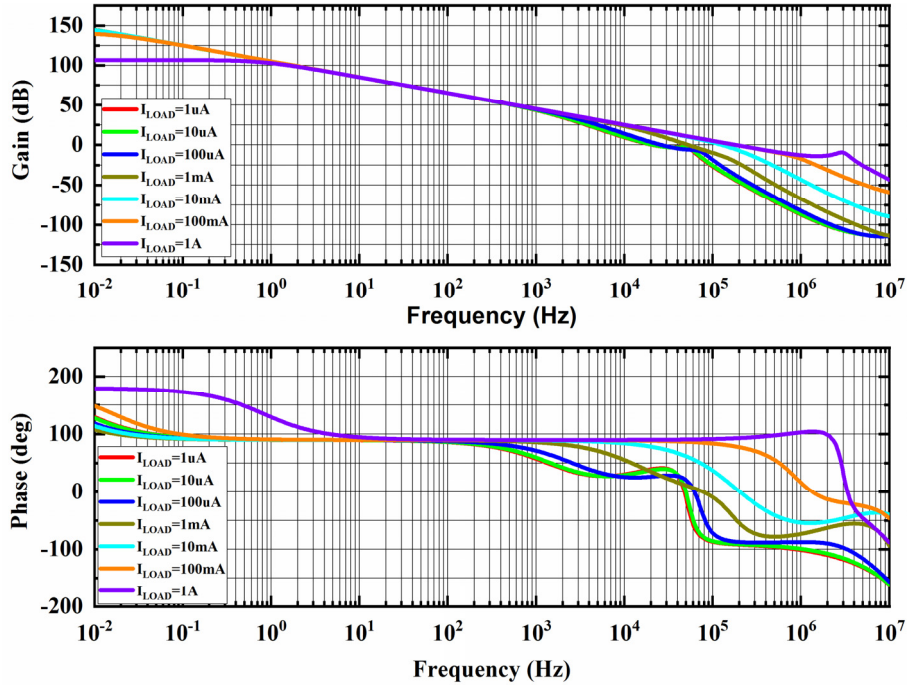

Figure 5. Simulated loop gain of the LDO under different load currents.

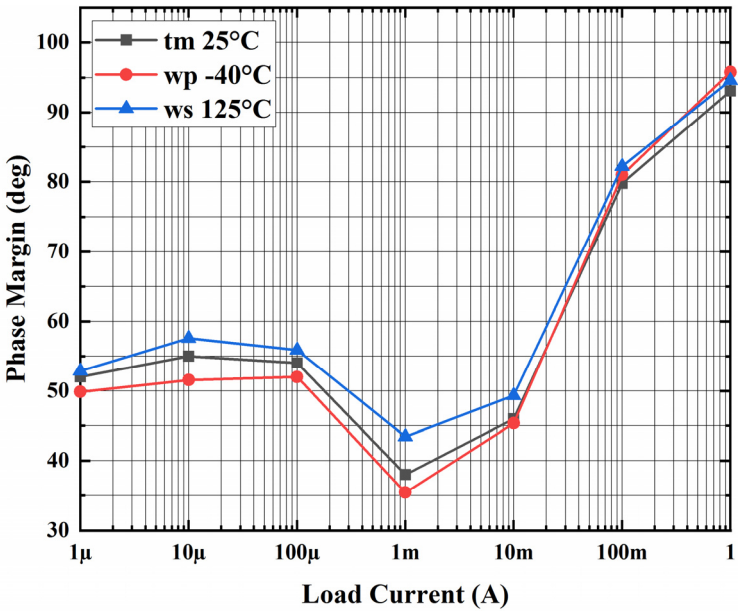

Figure 6. Phase margin of the proposed LDO under different load currents, process corners, and temperatures.

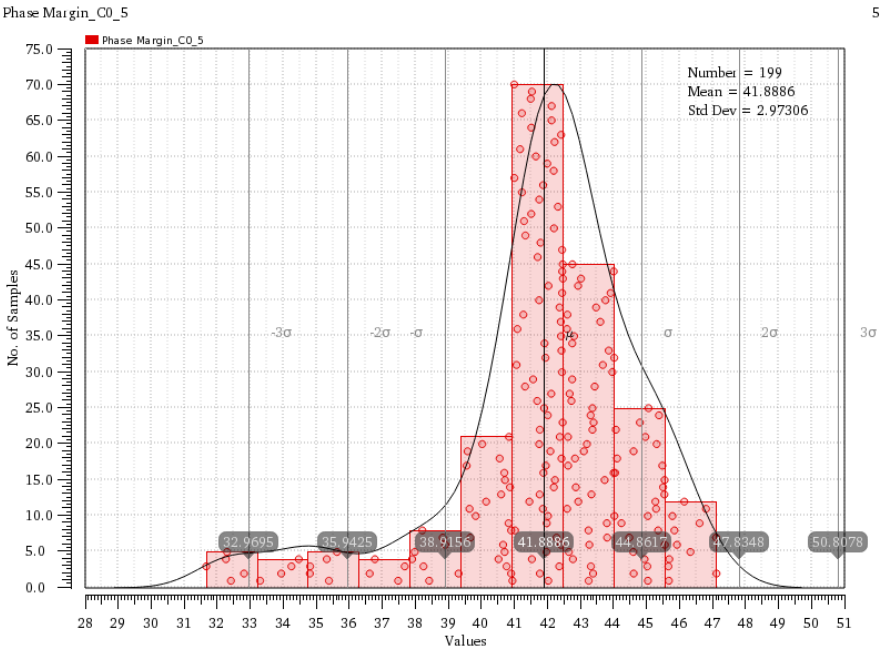

Figure 7. Monte Carlo simulation results of phase margin at 1 mA load current.

3. Simulation Results

The proposed LDO was designed and simulated in a 0.18 µm BCD process with 5 V NMOS and PMOS. Protect circuits and internal voltage reference circuits were integrated with the proposed LDO. The protect circuits consisted of overtemperature protect circuits, overcurrent protect circuits, and under-voltage locking circuits.t The total layout is shown in Figure 8; the whole chip area, including pads, is about 1184 µm × 1179 µm. The simulation results are presented below.

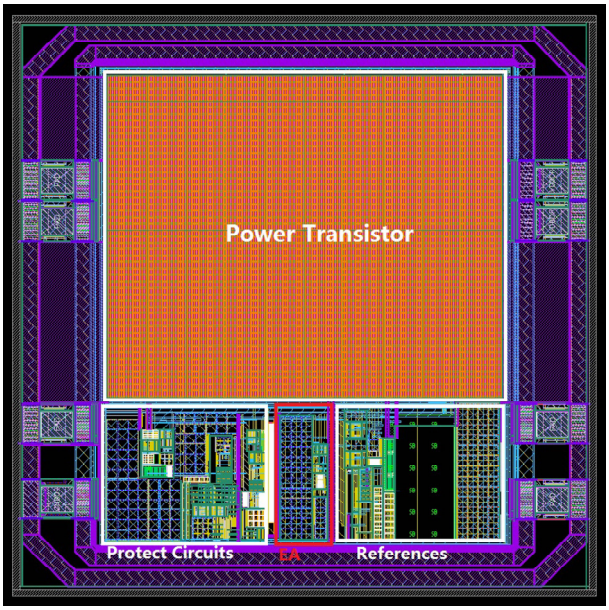

Figure 8. Layout of the proposed LDO.

The input voltage range of the LDO was designed from 1.6 V to 5.5 V for portable applications. The LDO can deliver up to 1 A with a dropout voltage of 0.2 V. Since the proposed LDO does not rely on the ESR zero, a ceramic 4.7 µF capacitor was used to minimize load transient dips caused by ESR. The LDO was also stable for output capacitor values of 4.7 µF to 22 µF. In addition, the LDO consumed a small quiescent current of 21 µA under the no-load condition, while the quiescent current of 424 µA was dissipated at full load condition. The current efficiency was 99.9% at full load condition.

High loop gain allows the LDO to achieve superior regulation. The load and line regulations were 0.089 µV/mA and 0.81 mV/V, respectively. Figure 9 depicts the PSR of the LDO under different load currents when V_{IN} = 1.6 V and V_o = 1.2 V. The PSR benefitted from the high loop gain and the current-mirror load structure used in the driving stage. In addition, the 4.7 µF output capacitor dampened the peaking effects in the PSR curves, resulting in the improved PSR performance at high frequency.

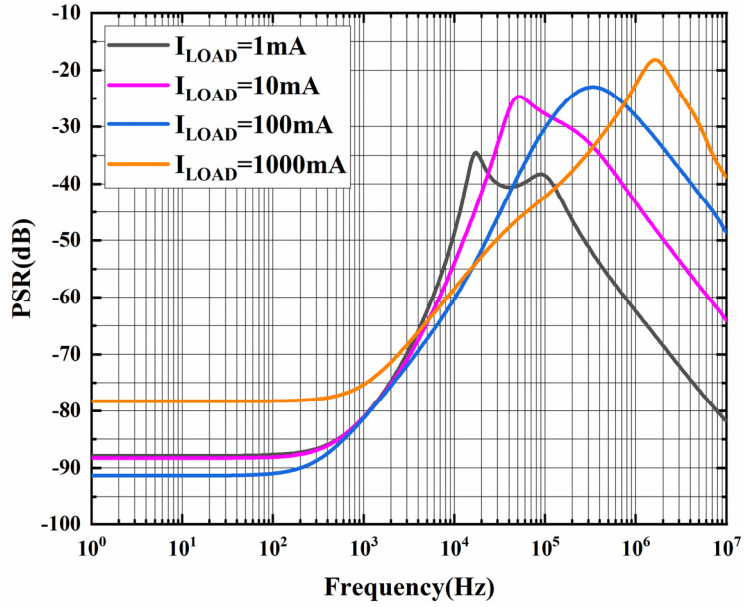

Figure 9. Simulated PSR of the LDO at different load conditions.

Figure 10 shows the simulated transient response when the load current switched between 0.1 A and 1 A with 1 µs rise/fall time. The maximum output voltage overshoot and undershoot were both less than 30 mV when V_o was at 1.2 V. Small transient variation under massive load-step change was obtained, which results from both the proposed adaptive impedance driving stage and positively adaptive feedback compensation. Otherwise, a large phase margin allowed the LDO to achieve a well-behaved settling characteristic.

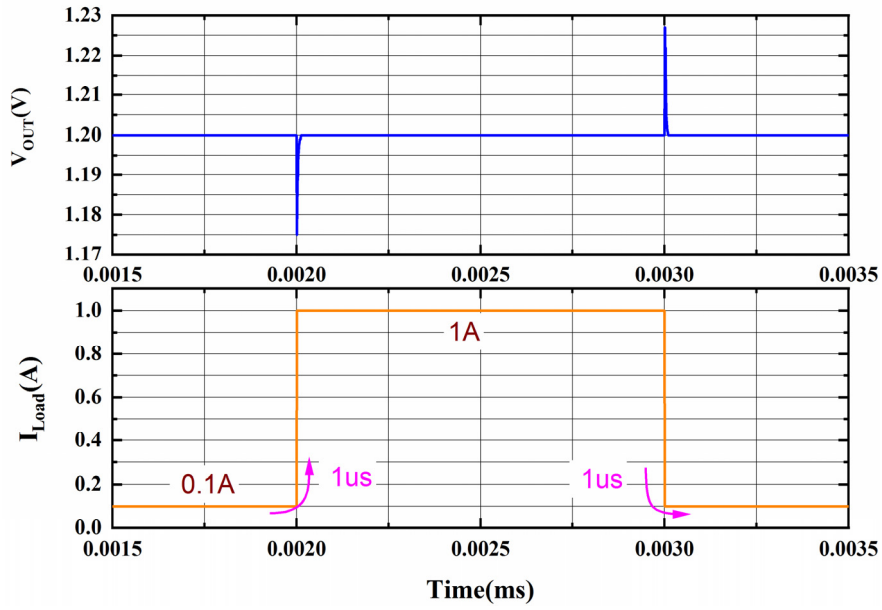

Figure 10. Simulated load transient response with 900 mA/µs.

The line transient response is given in Figure 11, according to which the implication of input voltage varied on the output voltage. When the change in the input voltage was from 1.6 V to 5.5 V with 10 µs rise and fall time, the output voltage changed by less than 100 mV at I_L = 0.2 A. When the change in the input voltage was from 1.6 V to 2.6 V with 10 µs rise and fall time, the output voltage changed by less than 5.5 mV at I_L = 0.2 A.

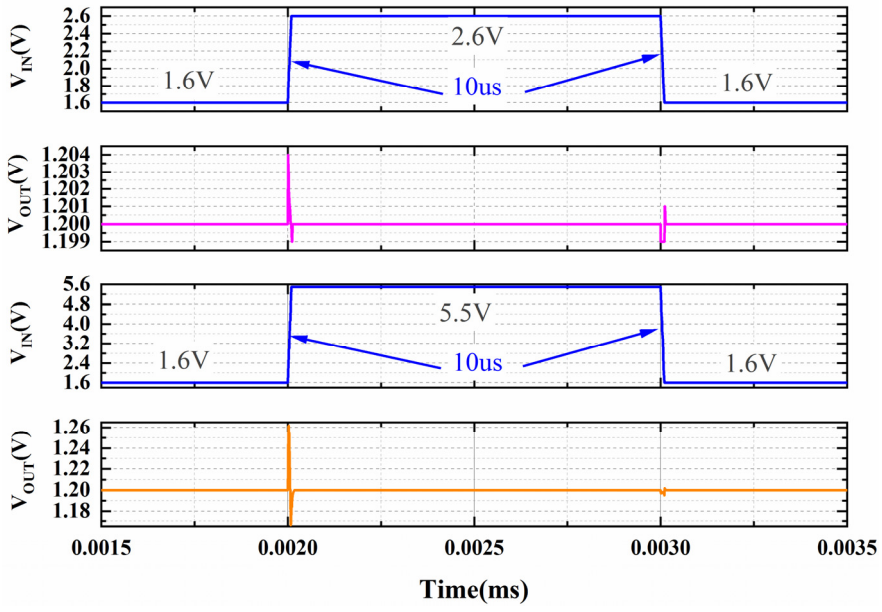

Figure 11. Simulated line transient response when input voltage change from 1.6 V to 5.5 V and 1.6 V to 5.5 V with a 10 µs transition-edge time.

In order to provide a clear picture of the performance improvement in the proposed LDO resulting from the adaptive impedance driving stage and adaptive positive feedback frequency compensation technique, a comparison with some reported LDOs in terms of performance is given in Table 1. A Figure of merit $FOM = C_L \times I_Q \times \Delta V_O / \Delta I_L^2$ [18] is introduced to compare the transient response of different LDOs, in which C_L, I_Q, ΔV_O, and ΔI_L represent the output capacitor, quiescent current, the output voltage variation due to the load switch, and the maximum load current step, respectively. Smaller FOM means a better level of transient performance of the LDO [31]. From Table 1, it is revealed that the proposed LDO achieved lower FOM and higher load regulation, compared with other reported LDOs.

Table 1. Performance comparison with reported LDOs.

	[5]	[8]	[32]	[33]	[34]	This Study
Technology (μm)	0.25	0.13	0.18	0.065	0.065	0.18
Power MOS type	NPN	PMOS	PMOS	PMOS	PMOS	PMOS
Input voltage (V)	3.9–10	1.05–2.0	1.2–1.8	1.2	0.7–1.1	1.6~5.5
Dropout voltage (mV)	>200	29.7	200	0.98	N/A	200
Max. Output current (mA)	500	300	100	20	120	1000
Quiescent current (μA)	350	14–120	135.1	385	495	21–424
Current Efficiency (%)	99.93	99.96	99.87	98.11	99.58	99.96
Load Regulation (μV/mA)	32.8	6	75	2300	600	0.089
Line Regulation (mV/V)	0.2	0.44	22.7	80	15	0.562 *
FOM (ps)	3388	12.44	439	N/A	20.46	6.031

*: Internal bandgap reference voltage is included.

4. Conclusions

In this paper, a high-output current (1 A) LDO with adaptive positive feedback compensation was proposed. The proposed compensation technique ensures loop stability under the full range of load currents. In addition, high loop gain was achieved, resulting in low load regulation. A driver stage that is suitable for low-supply voltage applications was also applied. It improved the driving ability of the power transistor so that enhances the transient response. The simulation results show that the overshoot and undershoot voltage of the output were both less than 30 mV when the load current varied from 0.1 to 1 A. Compared with other studies in the literature, the proposed LDO had lower FOM.

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Conflicts of Interest: The authors declare no conflict of interest.

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