

A High Performance Co-design of 26 nm 64 Gb MLC NAND Flash Memory using the Dedicated NAND Flash Controller

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Abstract—It is progressing as new advents and remarkable developments of mobile device every year. On the upper line reason, NAND FLASH large density memory demands which can be stored into portable devices have been dramatically increasing. Therefore, the cell size of the NAND Flash memory has been scaled down by merely 50% and has been doubling density each per year. [1] However, side effects have arisen the cell distribution and reliability characteristics related to coupling interference, channel disturbance, floating gate electron retention, write-erase cycling owing to shrinking around 20nm technology. Also, FLASH controller to manage shrink effect leads to speed and current issues. In this paper, It will be introduced to solve cycling, retention and fail bit problems of sub-deep micron shrink such as Virtual negative read used in moving read, randomization. The characteristics of retention, cycling and program performance have 3 K per 1 year and 12.7 MB/s respectively. And device size is 179.32 mm² (16.79 mm × 10.68 mm) in 3 metal 26 nm CMOS.

Index Terms—NAND FLASH memory, controller, Moving read, Virtual negative read, randomization, cycling, retention, interference, disturbance, SoC, SiP, ONFI.

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I. INTRODUCTION

As the mobile and portable device usage of NAND Flash memory have drastically been increased by such as smart phones, tablet personal computer, digital cameras, digital audio players, USB memories, hand-held game console and lots of portable devices, it is necessary to get large density and high performance. However, there exit two drawbacks of a scaling issue and a communicated speed, current issues. In case of sub deep 20 nm scaling in Fig. 1, [3] we have to concern about abnormal sensing cells, inherent coupling issues. There are lots of issues related to interference caused by adjacent programmed cells and fringing field, disturbance caused by excessive channel boosting, floating node charge loss tolerance, charge trapping caused by floating shrink and write performance degradation following more the number of program pulses around sub-20 nm node. [3] Providing

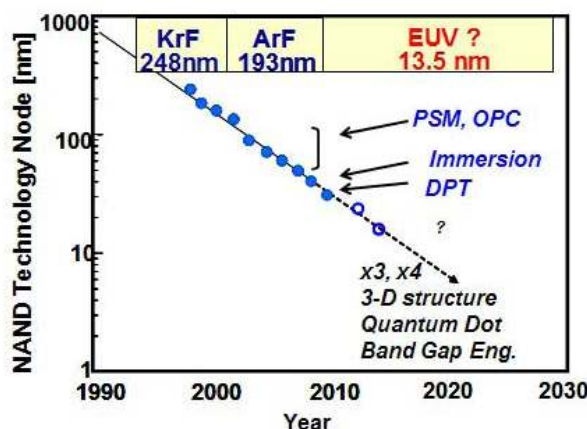


Fig. 1. A technology trend of a NAND Flash memory.

that both a NAND Flash memory and the dedicated NAND controller are packaged into one-chip to overcome scaling issue and high performance, and then there exist the large consumption of operating current and the bottle neck data path between interfaces using the embedded algorithm which is applied with SoC architecture.

II. CHIP ARCHITECTURE

As the block diagram in Fig. 2, both the NAND Flash memory and the dedicated NAND Flash controller are packaged into the one-chip that can implement high reliability and performance. As explaining operation simply, a host and the dedicated NAND Flash controller communicated with command, address and data input, output through an external interface and a data path can be stored into cache buffer bank0 and bank1 through the external interface because of dual channel. A control path related to command, address is directly communicated with control unit using FSM, Glue logic in the control unit. There exist the sequences of power-up and initial boot. In the case of power-up, the dedicated NAND controller is provided that synchronous clock is forced into μ -controller. The composition of the control unit is separated in μ -Controller, FSM, Glue logic and data encoder, decoder respectively. On the condition of executing command, each function blocks make it complete the sequential ECC algorithm which is driven by μ -Controller simultaneously. Initially, a subordinate

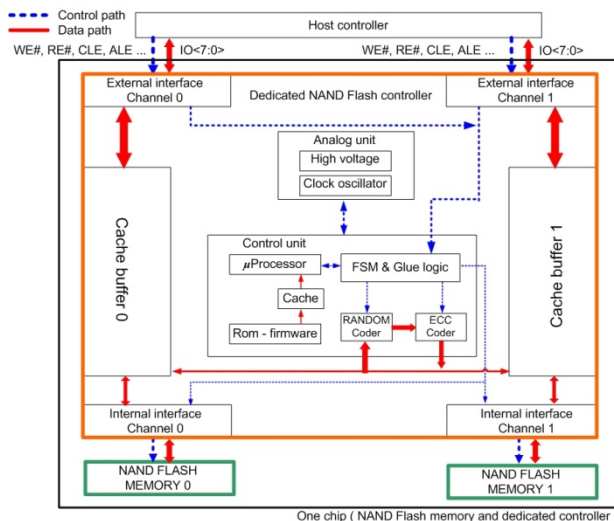


Fig. 2. One chip block diagram of NAND Flash memory and dedicated controller.

firmware related to algorithm is stored into a EEPROM. The NAND Flash memory is communicated by dual channel through the dedicated controller internal interface. It can be enhanced the performance with the methodology of interleave or concurrent in the multi-chip package and NAND Flash memory provides the ONFI compatible function of Set, Get parameter which can modify the internal parameter of sensing level, ISPP, Program start bias and unselected word line bias level to improve reliability using Moving read, Interference cancelling read and randomized process through the dedicated controller.

III. OVERCOME SCALING PROBLEMS

1. Moving Read using Virtual Negative Read

In case that Erase and Program sequence make steady progress gradually, Fowler–Nordheim tunneling comes from making degradation an interface field oxide and an internal floating gate, dramatically. As growing the number of cycling, these unit characteristics of retention is sharply degraded because interposing electron oxidation sites and floating gate electron trap number make the path of un-trapped electron, physical and electrical damages in Fig. 3(a) and (b).

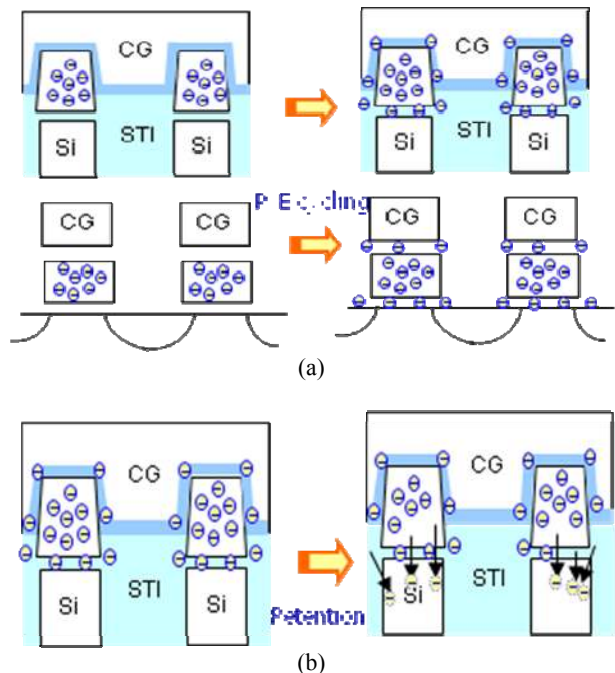


Fig. 3. (a) Cycling degradation effect, (b) Retention degradation effect.

There exists a problem of initial program cell distribution shifting left side because a charge get out of a floating gate in accordance with data retention characteristics. As well-known with moving read scheme, this method is wide usage of initial program cell state to adjust and compensate read-bias judging from the amount of left shifted cell distribution.[2]. It's possible to compensate a retention drawback within small V_{th} window using adjusting read 2 or read 3 sensing level. However, in the case of read 1, it is impossible to shift the word line sensing level under 0 V or more minus voltage out of accordance with adjusting read 2 and read 3. As it can be seen in Fig. 4, If data retention loss is occurred from the initial program cell status, moving read using virtual negative read at read 1 should be used to compensate a cell distribution with minus sensing read1 bias.

As the VCORE bias forces into all core signals except for a select word line to implement this method in the Fig. 5, it can be get an effect equal to forcing minus voltage which is a negative sensing level into the select word line. the VCORE bias forces into a bit line, PWELL, and source line (SL) and keeping read 1 bias into the select word line can be implemented by forcing VCORE bias level the same as shifting the left oriented cell distribution.

As it's mentioned in Fig. 4 and 5, in case that the sensing level of READ1 (RD1) is 0 V, the Virtual negative read is proposed to solve this data retention problem because of lowering moving read sensing level of READ 1 into a minus level.

As the moving read method using the virtual negative

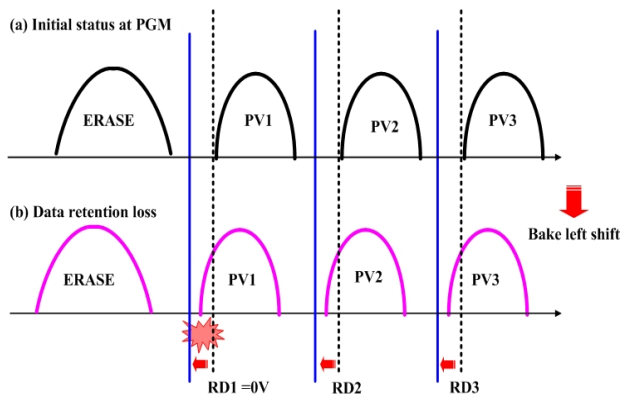


Fig. 4. Threshold voltage distribution of (a) Initial status at PGM and (b) Data retention loss adapted with virtual negative read.

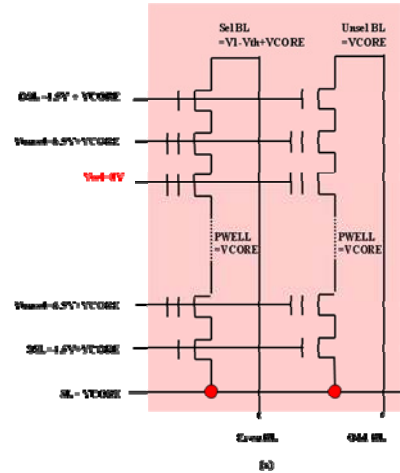


Fig. 5. An implemented Virtual negative read schematic diagram of NAND Flash memory array.

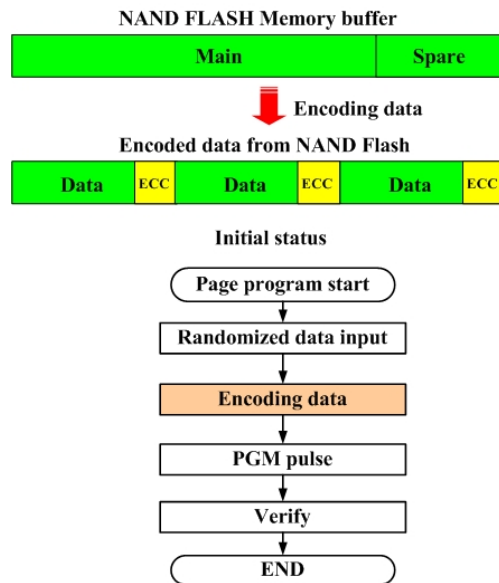


Fig. 6. NAND Flash memory encoding sequence.

read in Fig. 6, the randomized data of page buffer main and spare per each unit chunk make it program into the NAND cell array. If data retention is occurred, cell data will be shift cell distribution into left oriented direction.

The following sequence for the compensation, it is to read from NAND Flash memory page buffer to the dedicated controller cache buffer after NAND cell array page read in Fig. 7 in the meantime the dedicated controller have encoded ECC data of cache buffer bank0 and bank1 respectively. This data carry out checking equivalent between original page buffer data and ECC code. In case of equality to both either or maximum loop related to read re-try number, Fig. 7 sequence will be exited. In the opposite case, it will be read the

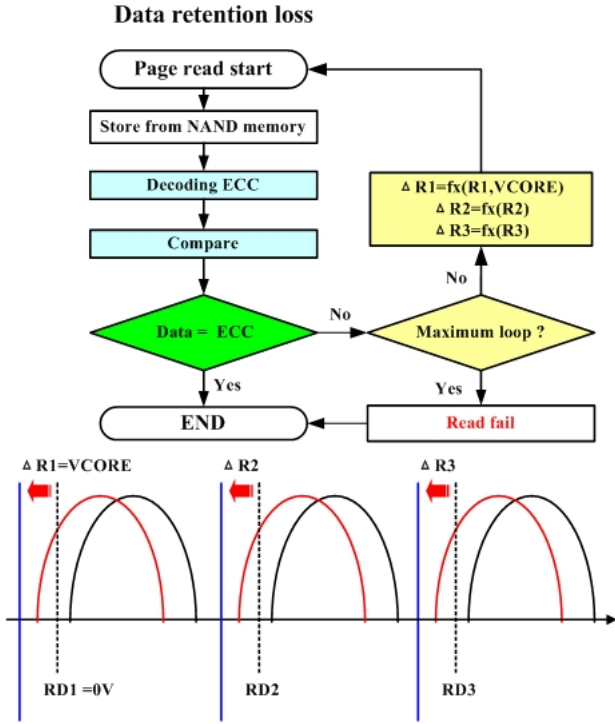


Fig. 7. Moving read concept and algorithm based on controller interface with virtual negative read.

compensated data using shifting $\Delta R1$, $\Delta R2$ and $\Delta R3$. The VCORE bias with the virtual negative read is determined by data retention loss level. And the dedicated NAND Flash controller calculates the shifting level and the number of read count. It's also implemented by the function of set, get parameter which supports NAND Flash memory internally. In the case of using moving read algorithm with virtual negative, user correctable error bit ratio can be considerably improved more than ~70% in Fig. 8. However, there exist increasing random access time about 5 μs and read operation current called

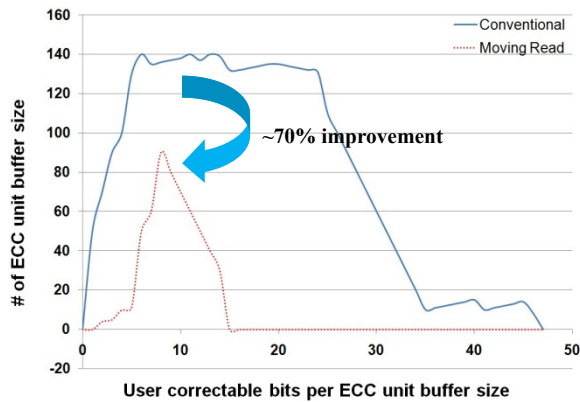


Fig. 8. Reliability margin comparison according to erase-write 3 K cycles and Bake 2h at 150 °C.

ICC1 about 2 mA because of charging and discharging into bit line, word line and PWELL during page read. This value can endure performance degradation and power consumption within the range of NAND Flash memory specification.

2. Randomized Data Input and Output based on Controller Interface

The randomized data encoding and decoding method in Fig. 9 explains reducing an interference gap related to both bit line to bit line and word line to word line, an erase 1 cell margin and a pattern dependency. Both the NAND Flash memory and the dedicated controller are shown in Fig. 9.

First of all, the external host controls the dedicated NAND Flash controller of the external I/F through two channels. In the case of data input, a random vector is generated from a seed generator. After data input of Seed<7:0>, the seed data which is synchronized with WE# generates RV<7:0>. That data which is encoded by XOR passes through the cache buffer and then the internal NAND I/F. On the contrary to stating above, data output is implemented by synchronizing with RE# toggle. There exists a seed of N cases in each page as dividing from page buffer size.

$$\left[\frac{(\text{page buffer size})}{N} \right] = N \times K + C \text{ (Seed mapping data)} \quad (1)$$

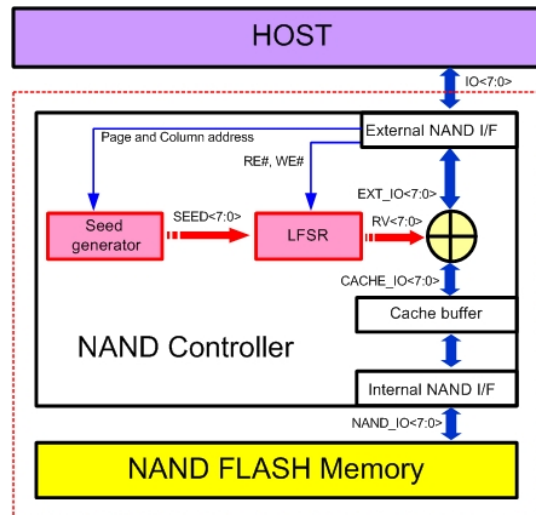


Fig. 9. Randomized behavior block.

Assuming that there exist the register number of N with LFSR(linear feedback shift register), the feedback polynomial data operated exclusive-OR is stored into 1st register bit and that sequence is circulated until the end of page address in Fig. 10.

This data is mapped from the seed coder in Fig. 11. In case of data input and output, this method allocates data with the identical column and page.

There exists a pattern dependency as mentioned above. All inhibit pattern has the zero fail bit. On the contrary that the worst pattern is in Fig. 12(d) and the best pattern is in Fig. 12(b). The randomized pattern data avoids the worst pattern and that fail bit count improves from 700

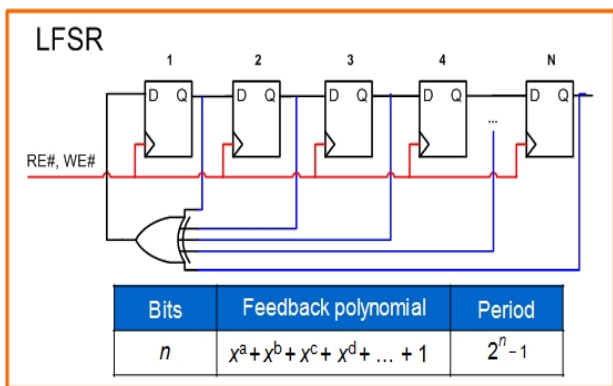


Fig. 10. Linear feedback shift register.

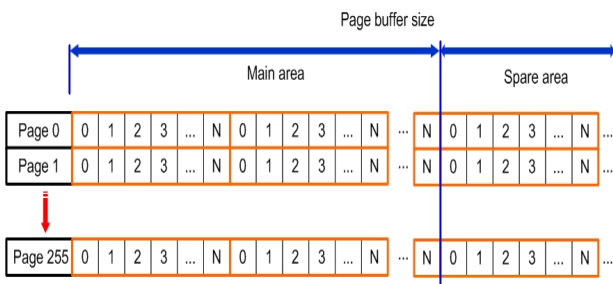


Fig. 11. Seed generator mapping code.

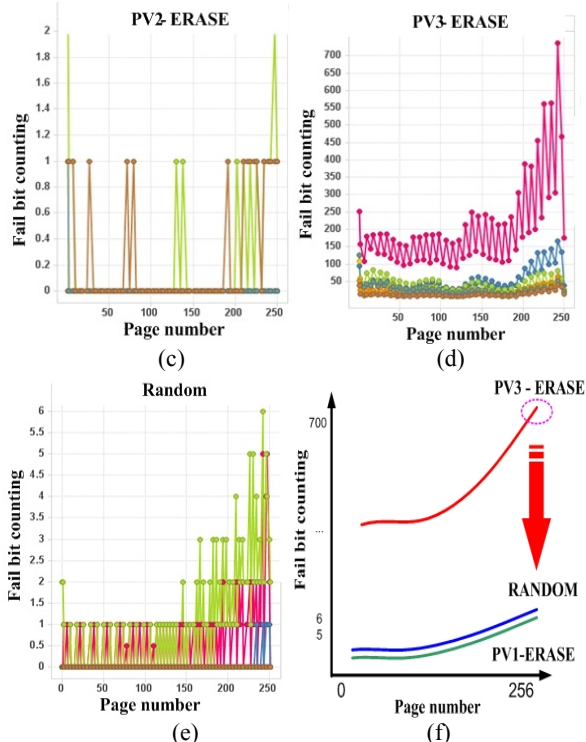
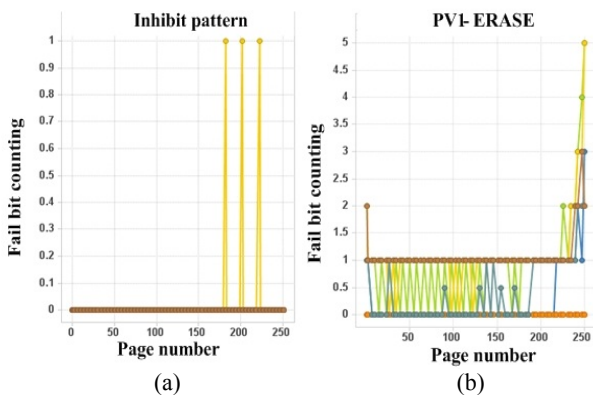


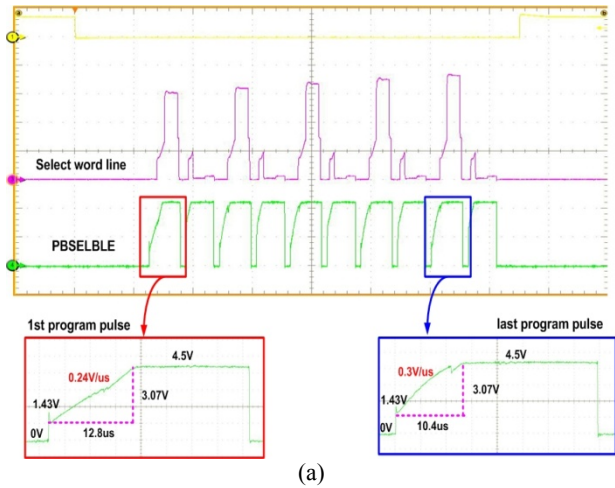
Fig. 12. Pattern dependency of (a) Inhibit, (b) PV1-ERASE, (c) PV2-ERASE, (d) PV3-ERASE, (e) Random and (f) Comparison of all cases.

bits to 6 bits. It's not different that best case of PV1-ERASE compares with the random pattern except for the inhibit pattern.

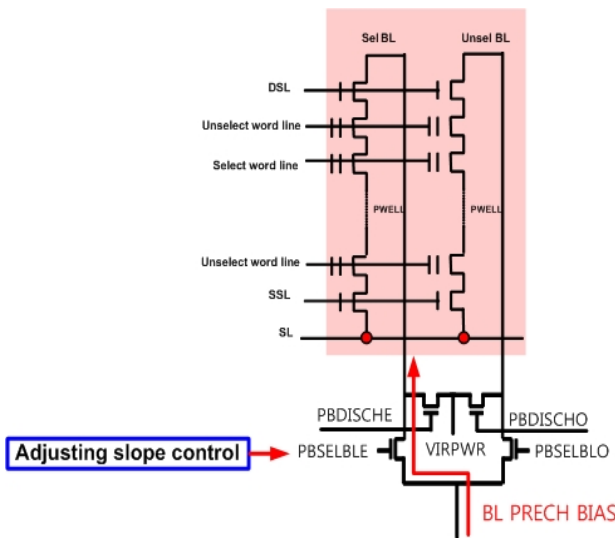
VI. PERFORMANCE ENHANCEMENT

1. Peak Current Compensation

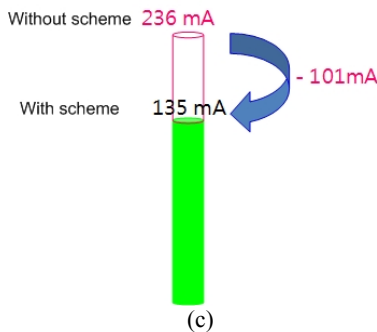
There exists the problem of large peak current consumption to design the large density and the high performance NAND Flash memory because of large bit line loading, large page buffer size, multi-stack and multi-channel. This peak current problem leads to serious power drop or abnormal function. This value must be satisfied with summing both the dedicated controller and multi-stack NAND Flash memory. In case that the many cells which are not programmed are existed around the beginning of program pulse, the slope will be lack of rising. In accordance with increasing program pulse, the cells are programmed gradually and the bit line has no lack of rising slope which is targeted. The value of peak current is enhanced about 43% from 236 mA to 135 mA, depicted in Fig. 13(a~c).



(a)



(b)



(c)

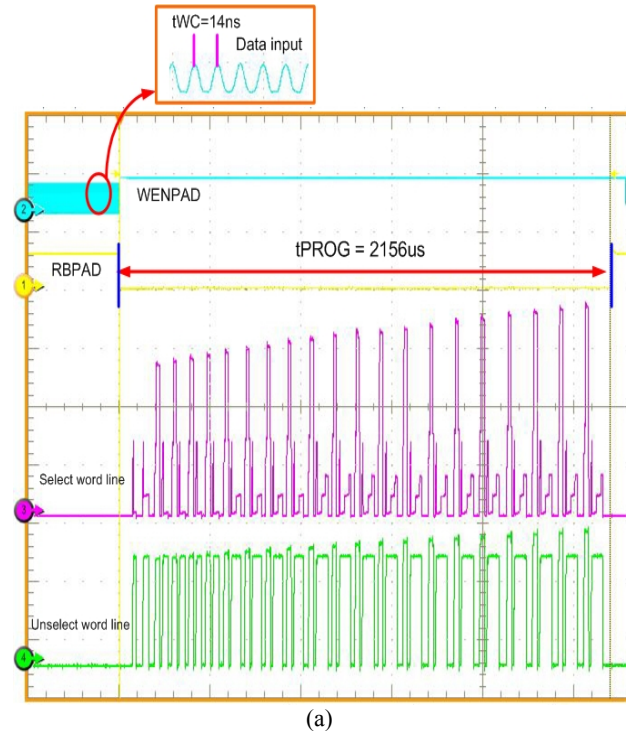
Fig. 13. (a) Gradual increase bit line pre-charge slope, (b) Bit line slope control behavior and (c) Peak current reduction amount.

2. Performance Enhancement

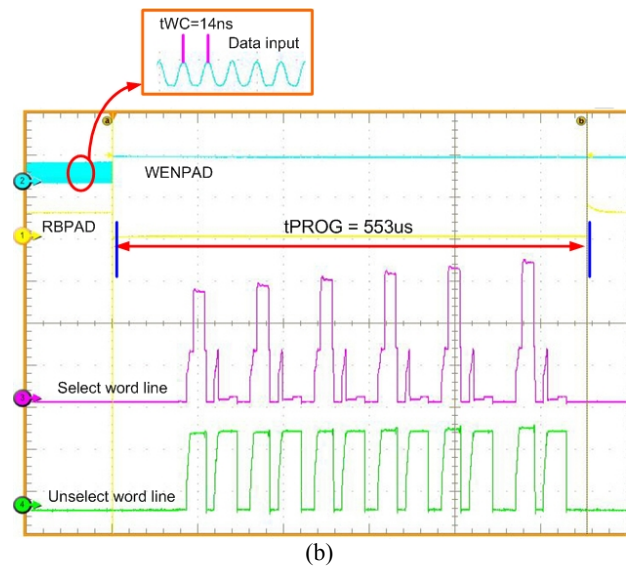
Both a NAND Flash memory and the dedicated NAND controller are packaged into one-chip. Therefore, performance degradation could be occurred essentially.

The architectural solution has implementations of t_{WC} , t_{RC} in 14ns. According to technology shrink drawback of interference. [2, 3] This NAND Flash memory has the average parameter of t_{PROG} is measured in 1361 μ s. The performance is calculated in 12.7 MB/s using multi plane and cache program operation in Fig. 14(a~c).

$$\text{Throughput(with cache)} = \frac{\text{Operated Inae number} \times \text{Page buffer size}}{t_{PROG}} \quad (2)$$



(a)



(b)

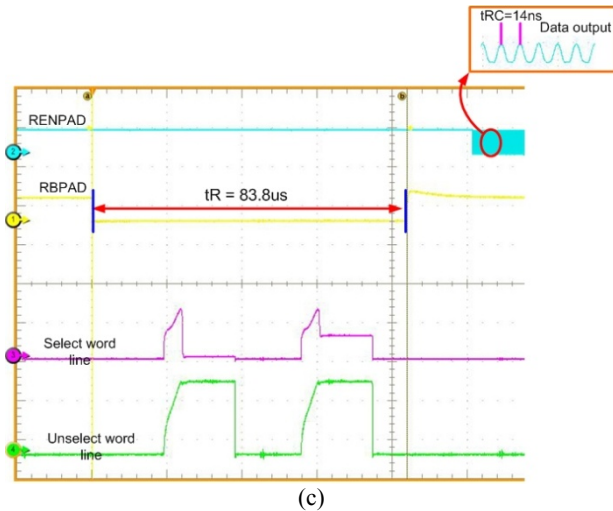


Fig. 14. (a) Program speed and tWC measurement at MSB page, (b) Program speed and tWC measurement at LSB page and (c) Read speed and tRC measurement at MSB page.

V. CONCLUSIONS

In this paper, it has been implemented by co-work designing both the NAND flash memory and the dedicated NAND controller for a high reliability and high speed IO. The Moving read using virtual negative read algorithm and randomization is proposed to make it a high reliability. As a result, fail bit ratio is significantly improved 70% and the randomized pattern data avoids the worst pattern and that fail bit count improves from 700 bits to 6 bits. Furthermore, the NAND chip size is reduced because of implementing those methods in the dedicated controller. However, there exist drawbacks of a large current and a communicated channel speed. It has been adapted with the shortest structure path and the smallest current consumption to overcome drawbacks providing the dual channel and multi-stack. The tWC and

Table 1. The 64Gb NAND Flash Memory key features in 26 nm technology

Technology	26 nm CMOS with 3 metals
Density	64G bits
Organization	1 Page size : 8K Bytes
	1 Block size : 256 pages
	1 Plane size : 2048 block
	1 Chip size : 2 plane
Power supply	2.7 V ~ 3.6 V
Program throughput	12.7 MB/s
Die size	179.32 mm ²

tRC of data input, output parameters are measured in 14 ns. The value of peak current is enhanced about 43% through adjusting slope control. The NAND Flash memory has the performance 12.7 MB/s. And this device is configured by two planes with row decoder at the both sides on each cell string. Each plane has 2048 blocks included within 256 page which is consist of 8K bytes page size. The 64 Gb MLC NAND Flash Memory key features in 26 nm technology can be seen in table1. and the chip architecture also is depicted in Fig. 15.

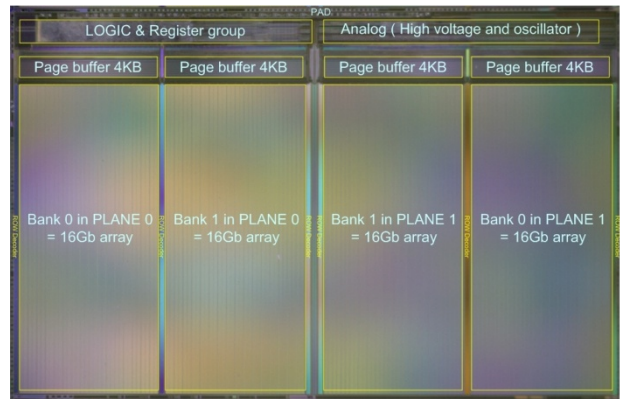


Fig. 15. The microscope photo of the NAND Flash memory chip architecture.

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